12 LVPECL/24 CMOS Output Clock Generator with Integrated 2.2 GHz VCO

Data Sheet

AD9520-2

FEATURES

- Low phase noise, phase-locked loop (PLL)
  - On-chip VCO tunes from 2.02 GHz to 2.335 GHz
  - Optional external 3.3 V/5 V VCO/VCXO to 2.4 GHz
  - 1 differential or 2 single-ended reference inputs
  - Accepts CMOS, LVDS, or LVPECL references to 250 MHz
  - Accepts 16.62 MHz to 33.3 MHz crystal for reference input
  - Optional reference clock doubler
  - Reference monitoring capability
  - Automatic/manual reference holdover and reference switchover modes, with revertive switching
  - Glitch-free switchover between references
  - Automatic recovery from holdover
  - Digital or analog lock detect, selectable
  - Optional zero delay operation
- Twelve 1.6 GHz LVPECL outputs divided into 4 groups
  - Each group of 3 outputs shares a 1-to-32 divider with phase delay
  - Additive output jitter as low as 225 fs rms
  - Channel-to-channel skew grouped outputs < 16 ps
  - Each LVPECL output can be configured as 2 CMOS outputs (for $f_{OUT} \leq 250$ MHz)
- Automatic synchronization of all outputs on power-up
- Manual output synchronization available
- SPI- and I^2C-compatible serial control port
- 64-lead LFCSP
- Nonvolatile EEPROM stores configuration settings

APPLICATIONS

- Low jitter, low phase noise clock distribution
- Clock generation and translation for SONET, 10Ge, 10GFC, Synchronous Ethernet, OTU2/3/4
- Forward error correction (G.710)
- Clocking high speed ADCs, DACs, DDSs, DDCs, DUCs, MxFEs
- High performance wireless transceivers
- ATE and high performance instrumentation
- Broadband infrastructures

GENERAL DESCRIPTION

The AD9520-2[1] provides a multioutput clock distribution function with subpicosecond jitter performance, along with an on-chip PLL and VCO. The on-chip VCO tunes from 2.02 GHz to 2.335 GHz. An external 3.3 V/5 V VCO/VCXO of up to 2.4 GHz can also be used.

FUNCTIONAL BLOCK DIAGRAM

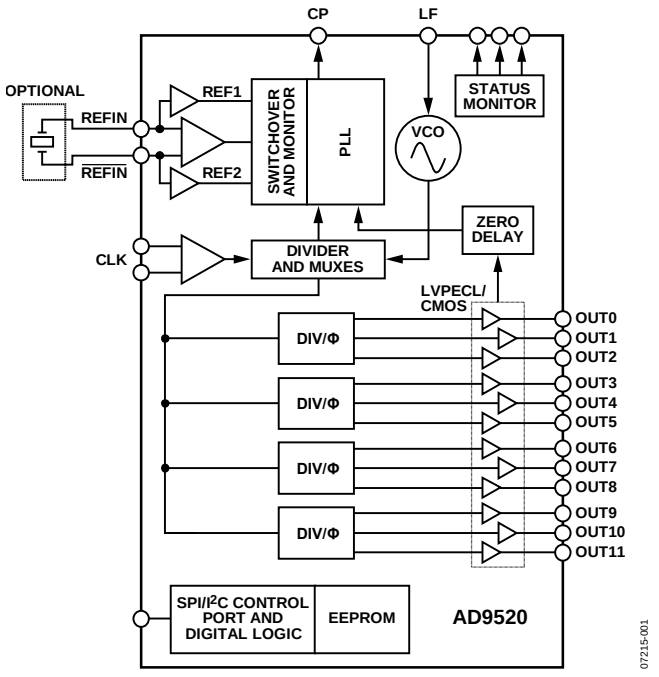


Figure 1.

The AD9520-2 serial interface supports both SPI and I^2C ports. An in-package EEPROM, which can be programmed through the serial interface, can store user-defined register settings for power-up and chip reset.

The AD9520-2 features 12 LVPECL outputs in four groups. Any of the 1.6 GHz LVPECL outputs can be reconfigured as two 250 MHz CMOS outputs. If an application requires LVDS drivers instead of LVPECL drivers, refer to the AD9522-2.

Each group of three outputs has a divider that allows both the divide ratio (from 1 to 32) and the phase offset or coarse time delay to be set.

The AD9520-2 is available in a 64-lead LFCSP and can be operated from a single 3.3 V supply. The external VCO can have an operating voltage of up to 5.5 V. A separate output driver power supply can be from 2.375 V to 3.465 V.

The AD9520-2 is specified for operation over the standard industrial range of −40°C to +85°C.

[1]AD9520 is used throughout this data sheet to refer to all the members of the AD9520 family. However, when AD9520-2 is used, it refers to that specific member of the AD9520 family.

Rev. B
Document Feedback

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REVISION HISTORY

10/2016—Rev. A to Rev. B

Changed AD9520 to AD9520-2 ..... Throughout
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Updated Outline Dimensions 80

8/13—Rev. 0 to Rev. A

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Change to Output Differential Voltage, V_{OD} Parameter Test Conditions/Comments; Added Source Current and Sink Current Parameters, Table 4 7
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Deleted Figure 13, Renumbered Sequentially; Change to f_{VCO} Value in Caption, Figure 13 and Figure 14 22
Reordered Figure 31 and Figure 32; Moved Figure 34 and Figure 35 to PLL External Loop Filter Section, Page 35; Added Figure 33, Renumbered Sequentially 25
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Changes to On-Chip VCO Section and PLL External Loop Filter Section; Added Figure 40; Moved Figure 41 and Figure 42 from Typical Performance Characteristics Section to PLL External Loop Filter Section; Changes to PLL Reference Inputs Section 35
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9/08—Revision 0: Initial Version

SPECIFICATIONS

Typical is given for $V_S = V_{S_DRV} = 3.3$ V ± 5%; $V_S \le V_{CP} \le 5.25$ V; $T_A = 25°C$; $R_{SET} = 4.12$ kΩ; $CP_{RSET} = 5.1$ kΩ, unless otherwise noted. Minimum and maximum values are given over full V_S and T_A (−40°C to +85°C) variation.

POWER SUPPLY REQUIREMENTS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER PINS					
VS	3.135	3.3	3.465	V	3.3 V ± 5%
VS_DRV	2.375		V_S	V	Nominally 2.5 V to 3.3 V ± 5%
VCP	V_S		5.25	V	Nominally 3.3 V to 5.0 V ± 5%
CURRENT SET RESISTORS					
RSET Pin Resistor		4.12		kΩ	Sets internal biasing currents; connect to ground
CPRSET Pin Resistor		5.1		kΩ	Sets internal CP current range, nominally 4.8 mA (CP_Isb = 600 µA); actual current can be calculated by CP_Isb = 3.06/CP_{RSET}; connect to ground
BYPASS PIN CAPACITOR		220		nF	Bypass for internal LDO regulator; necessary for LDO stability; connect to ground

PLL CHARACTERISTICS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VCO (ON CHIP)					
Frequency Range	2020		2335	MHz	
VCO Gain (K_{VCO})		38		MHz/V	See Figure 8
Tuning Voltage (V_T)	0.5		V_{CP} − 0.5	V	$V_T \le V_S$ when using internal VCO
Frequency Pushing (Open-Loop)		1		MHz/V	
Phase Noise at 1 kHz Offset		−52		dBc/Hz	f = 2175 MHz
Phase Noise at 100 kHz Offset		−108		dBc/Hz	f = 2175 MHz
Phase Noise at 1 MHz Offset		−128		dBc/Hz	f = 2175 MHz
REFERENCE INPUTS					
Differential Mode (REFIN, $\overline{\text{REFIN}}$)					Differential mode (can accommodate single-ended input by ac grounding undriven input)
Input Frequency	0		250	MHz	Frequencies below about 1 MHz should be dc-coupled; be careful to match V_{CM} (self-bias voltage)
Input Sensitivity		280		mV p-p	PLL figure of merit (FOM) increases with increasing slew rate (see Figure 12); the input sensitivity is sufficient for ac-coupled LVDS and LVPECL signals
Self-Bias Voltage, REFIN	1.35	1.60	1.75	V	Self-bias voltage of REFIN[1]
Self-Bias Voltage, $\overline{\text{REFIN}}$	1.30	1.50	1.60	V	Self-bias voltage of $\overline{\text{REFIN}}$[1]
Input Resistance, REFIN	4.0	4.8	5.9	kΩ	Self-biased[1]
Input Resistance, $\overline{\text{REFIN}}$	4.4	5.3	6.4	kΩ	Self-biased[1]
Dual Single-Ended Mode (REF1, REF2)					Two single-ended CMOS-compatible inputs
Input Frequency (AC-Coupled with DC Offset Off)	10		250	MHz	Slew rate must be > 50 V/µs
Input Frequency (AC-Coupled with DC Offset On)			250	MHz	Slew rate must be > 50 V/µs, and input amplitude sensitivity specification must be met; see the input sensitivity parameter
Input Frequency (DC-Coupled)	0		250	MHz	Slew rate > 50 V/µs; CMOS levels
Input Sensitivity (AC-Coupled with DC Offset Off)	0.55		3.28	V p-p	V_{IH} should not exceed V_S
Input Sensitivity (AC-Coupled with DC Offset On)	1.5		2.78	V p-p	V_{IH} should not exceed V_S
Input Logic High, DC Offset Off	2.0			V	
Input Logic Low, DC Offset Off			0.8	V	
Input Current	−100		+100	µA	
Input Capacitance		2		pF	Each pin, REFIN (REF1)/$\overline{\text{REFIN}}$ (REF2)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Pulse Width High/Low	1.8			ns	The amount of time that a square wave is high/low; determines the allowable input duty cycle
Crystal Oscillator					
Crystal Resonator Frequency Range	16.62		33.33	MHz	
Maximum Crystal Motional Resistance			30	Ω	
PHASE/FREQUENCY DETECTOR (PFD)					
PFD Input Frequency			100	MHz	Antibacklash pulse width = 1.3 ns
			45	MHz	Antibacklash pulse width = 2.9 ns
Reference Input Clock Doubler Frequency	0.004		50	MHz	
Antibacklash Pulse Width		1.3		ns	Register 0x017[1:0] = 01b
		2.9		ns	Register 0x017[1:0] = 00b; Register 0x017[1:0] = 11b
		6.0		ns	Register 0x017[1:0] = 10b
CHARGE PUMP (CP)					CP_V is the CP pin voltage; V_{CP} is the charge pump power supply voltage (VCP pin)
I_{CP} Sink/Source					Programmable
High Value		4.8		mA	With CP_{RSET} = 5.1 kΩ; higher I_{CP} is possible by changing CP_{RSET}
Low Value		0.60		mA	With CP_{RSET} = 5.1 kΩ; lower I_{CP} is possible by changing CP_{RSET}
Absolute Accuracy		2.5		%	$CP_V = V_{CP}/2$
CPRSET Range	2.7		10	kΩ	
I_{CP} High Impedance Mode Leakage		1		nA	
Sink-and-Source Current Matching		1		%	0.5 V < CP_V < V_{CP} − 0.5 V; CP_V is the CP pin voltage; V_{CP} is the charge pump power supply voltage (VCP pin)
I_{CP} vs. V_{CP}		1.5		%	0.5 V < CP_V < V_{CP} − 0.5 V
I_{CP} vs. Temperature		2		%	$CP_V = V_{CP}/2$
PRESCALER (PART OF N DIVIDER)					
Prescaler Input Frequency					
P = 1 FD			300	MHz	
P = 2 FD			600	MHz	
P = 3 FD			900	MHz	
P = 2 DM (2/3)			200	MHz	
P = 4 DM (4/5)			1000	MHz	
P = 8 DM (8/9)			2400	MHz	
P = 16 DM (16/17)			3000	MHz	
P = 32 DM (32/33)			3000	MHz	
Prescaler Output Frequency			300	MHz	A, B counter input frequency (prescaler input frequency divided by P)
PLL N DIVIDER DELAY					Register 0x019[2:0]; see Table 54
000		Off			
001		385		ps	
010		486		ps	
011		623		ps	
100		730		ps	
101		852		ps	
110		976		ps	
111		1101		ps	
PLL R DIVIDER DELAY					Register 0x019[5:3]; see Table 54
000		Off			
001		365		ps	
010		486		ps	
011		608		ps	
100		730		ps	
101		852		ps	
110		976		ps	
111		1101		ps	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PHASE OFFSET IN ZERO DELAY					REF refers to REFIN (REF1)/$\overline{\text{REFIN}}$ (REF2)
Phase Offset (REF-to-LVPECL Clock Output Pins) in Internal Zero Delay Mode	560	1060	1310	ps	When N delay and R delay are bypassed
Phase Offset (REF-to-LVPECL Clock Output Pins) in Internal Zero Delay Mode	−320	+50	+240	ps	When N delay setting = 110b, and R delay is bypassed
Phase Offset (REF-to-CLK Input Pins) in External Zero Delay Mode	140	630	870	ps	When N delay and R delay are bypassed
Phase Offset (REF-to-CLK Input Pins) in External Zero Delay Mode	−460	−20	+200	ps	When N delay setting = 011b, and R delay is bypassed
NOISE CHARACTERISTICS					
In-Band Phase Noise of the Charge Pump/ Phase Frequency Detector[2]					The PLL in-band phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log(N) (where N is the value of the N divider)
500 kHz PFD Frequency		−165		dBc/Hz	
1 MHz PFD Frequency		−162		dBc/Hz	
10 MHz PFD Frequency		−152		dBc/Hz	
50 MHz PFD Frequency		−144		dBc/Hz	
PLL Figure of Merit (FOM)		−222		dBc/Hz	Reference slew rate > 0.5 V/ns; FOM + 10 log(f_{PFD}) is an approximation of the PFD/CP in-band phase noise (in the flat region) inside the PLL loop bandwidth; when running closed-loop, the phase noise, as observed at the VCO output, is increased by 20 log(N); PLL figure of merit decreases with decreasing slew rate; see Figure 12
PLL DIGITAL LOCK DETECT WINDOW[3]					Signal available at the LD, STATUS, and REFMON pins when selected by appropriate register settings; the lock detect threshold varies linearly with the value of the CP_{RSET} resistor
Lock Threshold (Coincidence of Edges)					Selected by Register 0x017[1:0] and Register 0x018[4] (this is the threshold to go from unlock to lock)
Low Range (ABP 1.3 ns, 2.9 ns)		3.5		ns	Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 1b
High Range (ABP 1.3 ns, 2.9 ns)		7.5		ns	Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 0b
High Range (ABP 6.0 ns)		3.5		ns	Register 0x017[1:0] = 10b; Register 0x018[4] = 0b
Unlock Threshold (Hysteresis)[3]					Selected by Register 0x017[1:0] and Register 0x018[4] (this is the threshold to go from lock to unlock)
Low Range (ABP 1.3 ns, 2.9 ns)		7		ns	Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 1b
High Range (ABP 1.3 ns, 2.9 ns)		15		ns	Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 0b
High Range (ABP 6.0 ns)		11		ns	Register 0x017[1:0] = 10b; Register 0x018[4] = 0b

[1] The REFIN and $\overline{\text{REFIN}}$ self-bias points are offset slightly to avoid chatter on an open input condition.
[2] In-band means within the LBW of the PLL.
[3] For reliable operation of the digital lock detect, the period of the PFD frequency must be greater than the unlock-after-lock time.

CLOCK INPUTS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLOCK INPUTS (CLK, $\overline{CLK}$)					Differential input
Input Frequency	0[1]		2.4	GHz	High frequency distribution (VCO divider)
	0[1]		2.0	GHz	Distribution only (VCO divider bypassed); this is the frequency range supported by the channel divider for all divide ratios except divide-by-17 and divide-by-3
	0[1]		1.6	GHz	Distribution only (VCO divider bypassed); this is the frequency range supported by all channel divider ratios
Input Sensitivity, Differential		150		mV p-p	Measured at 2.4 GHz; jitter performance is improved with slew rates > 1 V/ns; the input sensitivity is sufficient for ac-coupled LVDS and LVPECL signals
Input Level, Differential			2	V p-p	Larger voltage swings can turn on the protection diodes and can degrade jitter performance
Input Common-Mode Voltage, V_{CM}	1.3	1.57	1.8	V	Self-biased; enables ac coupling
Input Common-Mode Range, V_{CMR}	1.3		1.8	V	With 200 mV p-p signal applied; dc-coupled
Input Sensitivity, Single-Ended		150		mV p-p	CLK ac-coupled; $\overline{CLK}$ ac-bypassed to RF ground
Input Resistance	3.9	4.7	5.7	kΩ	Self-biased
Input Capacitance		2		pF	

[1] Below about 1 MHz, the input should be dc-coupled. Care should be taken to match V_{CM}.

CLOCK OUTPUTS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL CLOCK OUTPUTS					Termination = 50 Ω to V_{S_DRV} − 2 V
OUT0, OUT1, OUT2, OUT3, OUT4, OUT5, OUT6, OUT7, OUT8, OUT9, OUT10, OUT11					Differential (OUT, $\overline{OUT}$)
Output Frequency, Maximum	2400			MHz	Using direct to output (see Figure 20); higher frequencies are possible, but the resulting amplitude does not meet the V_{OD} specification; the maximum output frequency is limited by either the maximum VCO frequency or the frequency at the CLK inputs, depending on the AD9520-2 configuration
Output High Voltage, V_{OH}	V_{S_DRV} − 1.07	V_{S_DRV} − 0.96	V_{S_DRV} − 0.84	V	
Output Low Voltage, V_{OL}	V_{S_DRV} − 1.95	V_{S_DRV} − 1.79	V_{S_DRV} −1.64	V	
Output Differential Voltage, V_{OD}	660	820	950	mV	V_{OH} − V_{OL} for each leg of a differential pair for default amplitude setting with the driver not toggling; the peak-to-peak amplitude measured using a differential probe across the differential pair with the driver toggling is roughly 2× these values (see Figure 20 for variation over frequency)
CMOS CLOCK OUTPUTS					
OUT0A, OUT0B, OUT1A, OUT1B, OUT2A, OUT2B, OUT3A, OUT3B, OUT4A, OUT4B, OUT5A, OUT5B, OUT6A, OUT6B, OUT7A, OUT7B, OUT8A, OUT8B, OUT9A, OUT9B, OUT10A, OUT10B, OUT11A, OUT11B					Single-ended; termination = 10 pF
Output Frequency			250	MHz	See Figure 21
Output Voltage High, V_{OH}	V_S − 0.1			V	1 mA load, V_{S_DRV} = 3.3 V/2.5 V
Output Voltage Low, V_{OL}			0.1	V	1 mA load, V_{S_DRV} = 3.3 V/2.5 V
Output Voltage High, V_{OH}	2.7			V	10 mA load, V_{S_DRV} = 3.3 V
Output Voltage Low, V_{OL}			0.5	V	10 mA load, V_{S_DRV} = 3.3 V
Output Voltage High, V_{OH}	1.8			V	10 mA load, V_{S_DRV} = 2.5 V
Output Voltage Low, V_{OL}			0.6	V	10 mA load, V_{S_DRV} = 2.5 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Source Current					Damage to the part can result if values are exceeded
Static			20	mA	
Dynamic			16	mA	
Sink Current					Damage to the part can result if values are exceeded
Static			8	mA	
Dynamic			16	mA	

TIMING CHARACTERISTICS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT RISE/FALL TIMES					Termination = 50 Ω to VS_DRV − 2 V
Output Rise Time, t_{RP}		130	170	ps	20% to 80%, measured differentially (rise/fall times are independent of V_S and are valid for V_{S_DRV} = 3.3 V and 2.5 V)
Output Fall Time, t_{FP}		130	170	ps	80% to 20%, measured differentially (rise/fall times are independent of V_S and are valid for V_{S_DRV} = 3.3 V and 2.5 V)
PROPAGATION DELAY, t_{PECL}, CLK-TO-LVPECL OUTPUT					
For All Divide Values	850	1050	1280	ps	High frequency clock distribution configuration
	800	970	1180	ps	Clock distribution configuration
Variation with Temperature		1.0		ps/°C	
OUTPUT SKEW, LVPECL OUTPUTS[1]					Termination = 50 Ω to V_{S_DRV} − 2 V
LVPECL Outputs Sharing the Same Divider		5	16	ps	V_{S_DRV} = 3.3 V
		5	20	ps	V_{S_DRV} = 2.5 V
LVPECL Outputs on Different Dividers		5	45	ps	V_{S_DRV} = 3.3 V
		5	60	ps	V_{S_DRV} = 2.5 V
All LVPECL Outputs Across Multiple Parts			190	ps	V_{S_DRV} = 3.3 V and 2.5 V
CMOS OUTPUT RISE/FALL TIMES					Termination = open
Output Rise Time, t_{RC}		750	960	ps	20% to 80%; C_{LOAD} = 10 pF; V_{S_DRV} = 3.3 V
Output Fall Time, t_{FC}		715	890	ps	80% to 20%; C_{LOAD} = 10 pF; V_{S_DRV} = 3.3 V
Output Rise Time, t_{RC}		965	1280	ps	20% to 80%; C_{LOAD} = 10 pF; V_{S_DRV} = 2.5 V
Output Fall Time, t_{FC}		890	1100	ps	80% to 20%; C_{LOAD} = 10 pF; V_{S_DRV} = 2.5 V
PROPAGATION DELAY, t_{CMOS}, CLK-TO-CMOS OUTPUT					Clock distribution configuration
For All Divide Values	2.1	2.75	3.55	ns	V_{S_DRV} = 3.3 V
		3.35		ns	V_{S_DRV} = 2.5 V
Variation with Temperature		2		ps/°C	V_{S_DRV} = 3.3 V and 2.5 V
OUTPUT SKEW, CMOS OUTPUTS[1]					
CMOS Outputs Sharing the Same Divider		7	85	ps	V_{S_DRV} = 3.3 V
		10	105	ps	V_{S_DRV} = 2.5 V
All CMOS Outputs on Different Dividers		10	240	ps	V_{S_DRV} = 3.3 V
		10	285	ps	V_{S_DRV} = 2.5 V
All CMOS Outputs Across Multiple Parts			600	ps	V_{S_DRV} = 3.3 V
			620	ps	V_{S_DRV} = 2.5 V
OUTPUT SKEW, LVPECL-TO-CMOS OUTPUTS[1]					All settings identical; different logic type
Outputs Sharing the Same Divider	1.18	1.76	2.48	ns	LVPECL to CMOS on same part
Outputs on Different Dividers	1.20	1.78	2.50	ns	LVPECL to CMOS on same part

[1] The output skew is the difference between any two similar delay paths while operating at the same voltage and temperature.

Timing Diagrams

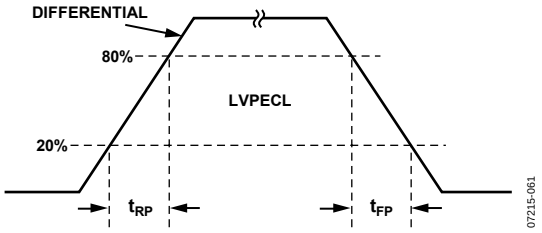


Figure 2. LVPECL Timing, Differential

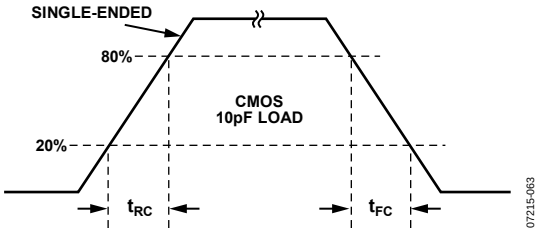


Figure 4. CMOS Timing, Single-Ended, 10 pF Load

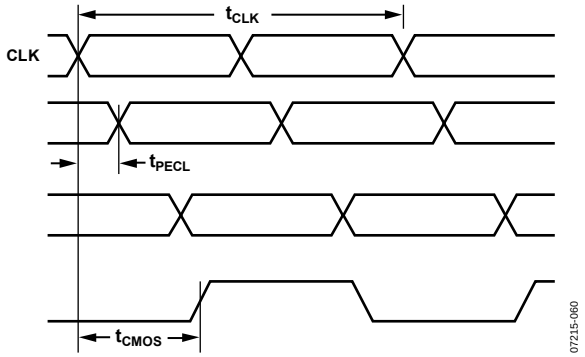


Figure 3. CLK/$\overline{CLK}$ to Clock Output Timing, DIV = 1

CLOCK OUTPUT ADDITIVE PHASE NOISE (DISTRIBUTION ONLY; VCO DIVIDER NOT USED)

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK-TO-LVPECL ADDITIVE PHASE NOISE					Distribution section only; does not include PLL and VCO
CLK = 1 GHz, Output = 1 GHz					Input slew rate > 1 V/ns
Divider = 1					
10 Hz Offset		−107		dBc/Hz	
100 Hz Offset		−117		dBc/Hz	
1 kHz Offset		−127		dBc/Hz	
10 kHz Offset		−135		dBc/Hz	
100 kHz Offset		−142		dBc/Hz	
1 MHz Offset		−145		dBc/Hz	
10 MHz Offset		−147		dBc/Hz	
100 MHz Offset		−150		dBc/Hz	
CLK = 1 GHz, Output = 200 MHz					Input slew rate > 1 V/ns
Divider = 5					
10 Hz Offset		−122		dBc/Hz	
100 Hz Offset		−132		dBc/Hz	
1 kHz Offset		−143		dBc/Hz	
10 kHz Offset		−150		dBc/Hz	
100 kHz Offset		−156		dBc/Hz	
1 MHz Offset		−157		dBc/Hz	
>10 MHz Offset		−157		dBc/Hz	
CLK-TO-CMOS ADDITIVE PHASE NOISE					Distribution section only; does not include PLL and VCO
CLK = 1 GHz, Output = 250 MHz					Input slew rate > 1 V/ns
Divider = 4					
10 Hz Offset		−107		dBc/Hz	
100 Hz Offset		−119		dBc/Hz	
1 kHz Offset		−125		dBc/Hz	
10 kHz Offset		−134		dBc/Hz	
100 kHz Offset		−144		dBc/Hz	
1 MHz Offset		−148		dBc/Hz	
>10 MHz Offset		−154		dBc/Hz	
CLK = 1 GHz, Output = 50 MHz					Input slew rate > 1 V/ns
Divider = 20					
10 Hz Offset		−126		dBc/Hz	
100 Hz Offset		−133		dBc/Hz	
1 kHz Offset		−140		dBc/Hz	
10 kHz Offset		−148		dBc/Hz	
100 kHz Offset		−157		dBc/Hz	
1 MHz Offset		−160		dBc/Hz	
>10 MHz Offset		−163		dBc/Hz	

CLOCK OUTPUT ABSOLUTE PHASE NOISE (INTERNAL VCO USED)

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL ABSOLUTE PHASE NOISE					Internal VCO; direct-to-LVPECL output and for loop bandwidths < 1 kHz
VCO = 2.335 GHz; Output = 2.335 GHz					
1 kHz Offset		−49		dBc/Hz	
10 kHz Offset		−80		dBc/Hz	
100 kHz Offset		−105		dBc/Hz	
1 MHz Offset		−125		dBc/Hz	
10 MHz Offset		−140		dBc/Hz	
40 MHz Offset		−146		dBc/Hz	
VCO = 2.175 GHz; Output = 2.175 GHz					
1 kHz Offset		−52		dBc/Hz	
10 kHz Offset		−83		dBc/Hz	
100 kHz Offset		−108		dBc/Hz	
1 MHz Offset		−128		dBc/Hz	
10 MHz Offset		−142		dBc/Hz	
40 MHz Offset		−147		dBc/Hz	
VCO = 2.05 GHz; Output = 2.05 GHz					
1 kHz Offset		−55		dBc/Hz	
10 kHz Offset		−84		dBc/Hz	
100 kHz Offset		−110		dBc/Hz	
1 MHz Offset		−130		dBc/Hz	
10 MHz Offset		−142		dBc/Hz	
40 MHz Offset		−147		dBc/Hz	

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK GENERATION USING INTERNAL VCO)

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup where the reference source is clean, so a wider PLL loop bandwidth is used; reference = 15.36 MHz; R divider = 1
VCO = 2.212 GHz; LVPECL = 245.76 MHz; PLL LBW = 66 kHz		145		fs rms	Integration BW = 200 kHz to 10 MHz
		321		fs rms	Integration BW = 12 kHz to 20 MHz
VCO = 2.212 GHz; LVPECL = 122.88 MHz; PLL LBW = 66 kHz		155		fs rms	Integration BW = 200 kHz to 10 MHz
		324		fs rms	Integration BW = 12 kHz to 20 MHz
VCO = 2.212 GHz; LVPECL = 61.44 MHz; PLL LBW = 66 kHz		169		fs rms	Integration BW = 200 kHz to 10 MHz
		336		fs rms	Integration BW = 12 kHz to 20 MHz

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK CLEANUP USING INTERNAL VCO)

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup where the reference source is jittery, so a narrower PLL loop bandwidth is used; reference = 19.44 MHz; R divider = 162
VCO = 2.177 GHz; LVPECL = 155.52 MHz; PLL LBW = 2.1 kHz		569		fs rms	Integration BW = 12 kHz to 20 MHz
VCO = 2.212 GHz; LVPECL = 122.88 MHz; PLL LBW = 2.2 kHz		599		fs rms	Integration BW = 12 kHz to 20 MHz

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK GENERATION USING EXTERNAL VCXO)

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup using an external 245.76 MHz VCXO (Toyocom TCO-2112); reference = 15.36 MHz; R divider = 1
LVPECL = 245.76 MHz; PLL LBW = 125 Hz		54		fs rms	Integration BW = 200 kHz to 5 MHz
		77		fs rms	Integration BW = 200 kHz to 10 MHz
		109		fs rms	Integration BW = 12 kHz to 20 MHz
LVPECL = 122.88 MHz; PLL LBW = 125 Hz		79		fs rms	Integration BW = 200 kHz to 5 MHz
		114		fs rms	Integration BW = 200 kHz to 10 MHz
		163		fs rms	Integration BW = 12 kHz to 20 MHz
LVPECL = 61.44 MHz; PLL LBW = 125 Hz		124		fs rms	Integration BW = 200 kHz to 5 MHz
		176		fs rms	Integration BW = 200 kHz to 10 MHz
		259		fs rms	Integration BW = 12 kHz to 20 MHz

CLOCK OUTPUT ADDITIVE TIME JITTER (VCO DIVIDER NOT USED)

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO; measured at rising edge of clock signal
CLK = 622.08 MHz Any LVPECL Output = 622.08 MHz Divide Ratio = 1		46		fs rms	Integration bandwidth = 12 kHz to 20 MHz
CLK = 622.08 MHz Any LVPECL Output = 155.52 MHz Divide Ratio = 4		64		fs rms	Integration bandwidth = 12 kHz to 20 MHz
CLK = 1000 MHz Any LVPECL Output = 100 MHz Divide Ratio = 10		223		fs rms	Calculated from SNR of ADC method Broadband jitter
CLK = 500 MHz Any LVPECL Output = 100 MHz Divide Ratio = 5		209		fs rms	Calculated from SNR of ADC method Broadband jitter
CMOS OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO
CLK = 200 MHz Any CMOS Output Pair = 100 MHz Divide Ratio = 2		325		fs rms	Calculated from SNR of ADC method Broadband jitter

CLOCK OUTPUT ADDITIVE TIME JITTER (VCO DIVIDER USED)

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO; uses rising edge of clock signal
CLK = 1.0 GHz; VCO DIV = 5; LVPECL = 100 MHz; Channel Divider = 2; Duty-Cycle Correction = Off		230		fs rms	Calculated from SNR of ADC method (broadband jitter)
CLK = 500 MHz; VCO DIV = 5; LVPECL = 100 MHz; Bypass Channel Divider; Duty-Cycle Correction = On		215		fs rms	Calculated from SNR of ADC method (broadband jitter)
CMOS OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL and VCO; uses rising edge of clock signal
CLK = 200 MHz; VCO DIV = 2; CMOS = 100 MHz; Bypass Channel Divider; Duty-Cycle Correction = Off		326		fs rms	Calculated from SNR of ADC method (broadband jitter)
CLK = 1600 MHz; VCO DIV = 2; CMOS = 100 MHz; Channel Divider = 8; Duty-Cycle Correction = Off		362		fs rms	Calculated from SNR of ADC method (broadband jitter)

SERIAL CONTROL PORT—SPI MODE

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{CS}$ (INPUT)					$\overline{CS}$ has an internal 30 kΩ pull-up resistor
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current			3	μA	
Input Logic 0 Current		−110		μA	The minus sign indicates that current is flowing out of the AD9520-2, which is due to the internal pull-up resistor
Input Capacitance		2		pF	
SCLK (INPUT IN SPI MODE)					SCLK has an internal 30 kΩ pull-down resistor in SPI mode, but not in I^2C mode
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		110		μA	
Input Logic 0 Current			1	μA	
Input Capacitance		2		pF	
SDIO (INPUT IN BIDIRECTIONAL MODE)					
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		1		μA	
Input Logic 0 Current		1		μA	
Input Capacitance		2		pF	
SDIO, SDO (OUTPUTS)					
Output Logic 1 Voltage	2.7			V	
Output Logic 0 Voltage			0.4	V	
TIMING					
Clock Rate (SCLK, $1/t_{SCLK}$)			25	MHz	
Pulse Width High, t_{HIGH}	16			ns	
Pulse Width Low, t_{LOW}	16			ns	
SDIO to SCLK Setup, t_{DS}	4			ns	
SCLK to SDIO Hold, t_{DH}	0			ns	
SCLK to Valid SDIO and SDO, t_{DV}			11	ns	
$\overline{CS}$ to SCLK Setup and Hold, t_S, t_C	2			ns	
$\overline{CS}$ Minimum Pulse Width High, t_{PWH}	3			ns	

SERIAL CONTROL PORT—I²C MODE

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SDA, SCL (WHEN INPUTTING DATA)					
Input Logic 1 Voltage	$0.7 \times V_S$			V	
Input Logic 0 Voltage			$0.3 \times V_S$	V	
Input Current with an Input Voltage Between $0.1 \times V_S$ and $0.9 \times V_S$	−10		+10	µA	
Hysteresis of Schmitt Trigger Inputs	$0.015 \times V_S$			V	
Pulse Width of Spikes That Must Be Suppressed by the Input Filter, t_{SPIKE}			50	ns	
SDA (WHEN OUTPUTTING DATA)					
Output Logic 0 Voltage at 3 mA Sink Current			0.4	V	
Output Fall Time from VIH_{MIN} to VIL_{MAX} with a Bus Capacitance from 10 pF to 400 pF	$20 + 0.1\ C_b$		250	ns	C_b = capacitance of one bus line in pF
TIMING					Note that all I²C timing values are referred to VIH_{MIN} ($0.3 \times VS$) and VIL_{MAX} levels ($0.7 \times V_S$)
Clock Rate (SCL, f_{I2C})			400	kHz	
Bus Free Time Between a Stop and Start Condition, t_{IDLE}	1.3			µs	
Setup Time for a Repeated Start Condition, $t_{SET;\ STR}$	0.6			µs	
Hold Time (Repeated) Start Condition, $t_{HLD;\ STR}$	0.6			µs	After this period, the first clock pulse is generated
Setup Time for Stop Condition, $t_{SET;\ STP}$	0.6			µs	
Low Period of the SCL Clock, t_{LOW}	1.3			µs	
High Period of the SCL Clock, t_{HIGH}	0.6			µs	
SCL, SDA Rise Time, t_{RISE}	$20 + 0.1\ C_b$		300	ns	
SCL, SDA Fall Time, t_{FALL}	$20 + 0.1\ C_b$		300	ns	
Data Setup Time, $t_{SET;\ DAT}$	120			ns	This is a minor deviation from the original I²C specification of 100 ns minimum
Data Hold Time, $t_{HLD;\ DAT}$	140		880	ns	This is a minor deviation from the original I²C specification of 0 ns minimum[1]
Capacitive Load for Each Bus Line, C_b			400	pF	

[1] According to the original I²C specification, an I²C master must also provide a minimum hold time of 300 ns for the SDA signal to bridge the undefined region of the SCL falling edge.

$\overline{PD}$, EEPROM, $\overline{RESET}$, AND $\overline{SYNC}$ PINS

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT CHARACTERISTICS					Each pin has a 30 kΩ internal pull-up resistor
Logic 1 Voltage	2.0			V	
Logic 0 Voltage			0.8	V	
Logic 1 Current			1	µA	
Logic 0 Current		−110		µA	The minus sign indicates that current is flowing out of the AD9520-2, which is due to the internal pull-up resistor
Capacitance		2		pF	
RESET TIMING					
Pulse Width Low	500			ns	
$\overline{RESET}$ Inactive to Start of Register Programming	100			ns	
$\overline{SYNC}$ TIMING					
Pulse Width Low	1.3			ns	High speed clock is CLK input signal

SERIAL PORT SETUP PINS—SP1, SP0

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SP1, SP0					These pins do not have internal pull-up/pull-down resistors
Logic Level 0			0.25 × V_S	V	V_S is the voltage on the VS pin
Logic Level ½	0.4 × V_S		0.65 × V_S	V	These pins can be floated to obtain Logic Level ½; if floating the pin, connect a capacitor to ground
Logic Level 1	0.8 × V_S			V	

LD, STATUS, AND REFMON PINS

Table 17.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CHARACTERISTICS					When selected as a digital output (CMOS); there are other modes in which these pins are not CMOS digital outputs; see Table 54,Register 0x017, Register 0x01A, and Register 0x01B
Output Voltage High, V_{OH}	2.7			V	
Output Voltage Low, V_{OL}			0.4	V	
MAXIMUM TOGGLE RATE		100		MHz	Applies when mux is set to any divider or counter output, or PFD up/down pulse; also applies in analog lock detect mode; usually debug mode only; beware that spurs can couple to output when any pin is toggling
ANALOG LOCK DETECT					
Capacitance		3		pF	On-chip capacitance; used to calculate RC time constant for analog lock detect readback; use a pull-up resistor
REF1, REF2, AND VCO FREQUENCY STATUS MONITOR					
Normal Range	1.02			MHz	Frequency above which the monitor indicates the presence of the reference
Extended Range	8			kHz	Frequency above which the monitor indicates the presence of the reference
LD PIN COMPARATOR					
Trip Point		1.6		V	
Hysteresis		260		mV	

POWER DISSIPATION

Table 18.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION, CHIP					Does not include power dissipated in external resistors; all LVPECL outputs terminated with 50 Ω to V_{CC} − 2 V; all CMOS outputs have 10 pF capacitive loading; V_{S_DRV} = 3.3 V
Power-On Default		1.32	1.5	W	No clock; no programming; default register values
PLL Locked; One LVPECL Output Enabled		0.55	0.64	W	f_{REF} = 25 MHz; f_{OUT} = 225 MHz; VCO = 2250 MHz; VCO divider = 2; one LVPECL output and output divider enabled; zero delay off; I_{CP} = 4.8 mA
PLL Locked; One CMOS Output Enabled		0.52	0.62	W	f_{REF} = 25 MHz; f_{OUT} = 62.5 MHz; VCO = 2250 MHz; VCO divider = 2; one CMOS output and output divider enabled; zero delay off; I_{CP} = 4.8 mA
Distribution Only Mode; VCO Divider On; One LVPECL Output Enabled		0.39	0.46	W	f_{CLK} = 2.4 GHz; f_{OUT} = 200 MHz; VCO divider = 2; one LVPECL output and output divider enabled; zero delay off
Distribution Only Mode; VCO Divider Off; One LVPECL Output Enabled		0.36	0.42	W	f_{CLK} = 2.4 GHz; f_{OUT} = 200 MHz; VCO divider bypassed; one LVPECL output and output divider enabled; zero delay off
Maximum Power, Full Operation		1.5	1.7	W	PLL on; internal VCO = 2250 MHz; VCO divider = 2; all channel dividers on; 12 LVPECL outputs at 125 MHz; zero delay on
$\overline{PD}$ Power-Down		60	80	mW	$\overline{PD}$ pin pulled low; does not include power dissipated in termination resistors
$\overline{PD}$ Power-Down, Maximum Sleep		24	43	mW	$\overline{PD}$ pin pulled low; PLL power-down, Register 0x010[1:0] = 01b; power-down SYNC, Register 0x230[2] = 1b; power-down distribution reference, Register 0x230[1] = 1b
VCP Supply		4	4.8	mW	PLL operating; typical closed-loop configuration
POWER DELTAS, INDIVIDUAL FUNCTIONS					Power delta when a function is enabled/disabled
VCO Divider On/Off		32	40	mW	VCO divider not used
REFIN (Differential) Off		25	30	mW	Delta between reference input off and differential reference input mode
REF1, REF2 (Single-Ended) On/Off		15	20	mW	Delta between reference inputs off and one singled-ended reference enabled; double this number if both REF1 and REF2 are powered up
VCO On/Off		67	104	mW	Internal VCO disabled; CLK input selected
PLL Dividers and Phase Detector On/Off		51	63	mW	PLL off to PLL on, normal operation; no reference enabled
LVPECL Channel		121	144	mW	No LVPECL output on to one LVPECL output on; channel divider is set to 1
LVPECL Driver		51	73	mW	Second LVPECL output turned on, same channel
CMOS Channel		145	180	mW	No CMOS output on to one CMOS output on; channel divider is set to 1; f_{OUT} = 62.5 MHz and 10 pF of capacitive loading
CMOS Driver On/Off		11	24	mW	Additional CMOS outputs within the same channel turned on
Channel Divider Enabled		40	57	mW	Delta between divider bypassed (divide-by-1) and divide-by-2 to divide-by-32
Zero Delay Block On/Off		30	34	mW	

ABSOLUTE MAXIMUM RATINGS

Table 19.

Parameter	Rating
VS to GND	−0.3 V to +3.6 V
VCP, CP to GND	−0.3 V to +5.8 V
VS_DRV to GND	−0.3 V to +3.6 V
REFIN, $\overline{\text{REFIN}}$ to GND	−0.3 V to V_S + 0.3 V
RSET, LF, BYPASS to GND	−0.3 V to V_S + 0.3 V
CPRSET to GND	−0.3 V to V_S + 0.3 V
CLK, $\overline{\text{CLK}}$ to GND	−0.3 V to V_S + 0.3 V
CLK to $\overline{\text{CLK}}$	−1.2 V to +1.2 V
SCLK/SCL, SDIO/SDA, SDO, $\overline{\text{CS}}$ to GND	−0.3 V to V_S + 0.3 V
OUT0, $\overline{\text{OUT0}}$, OUT1, $\overline{\text{OUT1}}$, OUT2, $\overline{\text{OUT2}}$, OUT3, $\overline{\text{OUT3}}$, OUT4, $\overline{\text{OUT4}}$, OUT5, $\overline{\text{OUT5}}$, OUT6, $\overline{\text{OUT6}}$, OUT7, $\overline{\text{OUT7}}$, OUT8, $\overline{\text{OUT8}}$, OUT9, $\overline{\text{OUT9}}$, OUT10, $\overline{\text{OUT10}}$, OUT11, $\overline{\text{OUT11}}$ to GND	−0.3 V to V_S + 0.3 V
$\overline{\text{SYNC}}$, $\overline{\text{RESET}}$, $\overline{\text{PD}}$ to GND	−0.3 V to V_S + 0.3 V
REFMON, STATUS, LD to GND	−0.3 V to V_S + 0.3 V
SP0, SP1, EEPROM to GND	−0.3 V to V_S + 0.3 V
Junction Temperature[1]	125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (10 sec)	300°C

[1] See Table 20 for θ_{JA}.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal impedance measurements were taken on a JEDEC JESD51-5 2S2P test board in still air, in accordance with JEDEC JESD51-2. See the Thermal Performance section for more details.

Table 20.

Package Type	θ_{JA}	Unit
64-Lead LFCSP (CP-64-4)	22	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

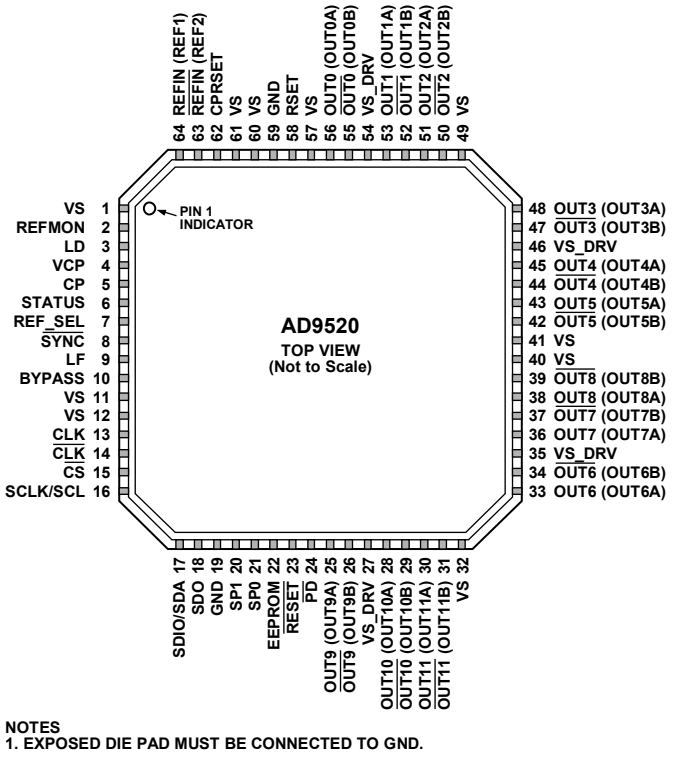


Figure 5. Pin Configuration

Table 21. Pin Function Descriptions

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
1, 11, 12, 32, 40, 41, 49, 57, 60, 61	I	Power	VS	3.3 V Power Pins.
2	O	3.3 V CMOS	REFMON	Reference Monitor (Output). This pin has multiple selectable outputs.
3	O	3.3 V CMOS	LD	Lock Detect (Output). This pin has multiple selectable outputs.
4	I	Power	VCP	Power Supply for Charge Pump (CP); $V_S \le V_{CP} \le 5.25$ V. VCP must still be connected to 3.3 V if the PLL is not used.
5	O	Loop filter	CP	Charge Pump (Output). This pin connects to an external loop filter; it can be left unconnected if the PLL is not used.
6	O	3.3 V CMOS	STATUS	Programmable Status Output.
7	I	3.3 V CMOS	REF_SEL	Reference Select. This pin selects REF1 (low) or REF2 (high) and has an internal 30 kΩ pull-down resistor.
8	I	3.3 V CMOS	$\overline{\text{SYNC}}$	Manual Synchronization and Manual Holdover. This pin initiates a manual synchronization and is used for manual holdover. Active low. This pin has an internal 30 kΩ pull-up resistor.
9	I	Loop filter	LF	Loop Filter (Input). This pin connects internally to the VCO control voltage node.
10	O	Loop filter	BYPASS	This pin is for bypassing the LDO to ground with a 220 nF capacitor. It can be left unconnected if the PLL is not used.
13	I	Differential clock input	CLK	Along with $\overline{\text{CLK}}$, this pin is the differential input for the clock distribution section.
14	I	Differential clock input	$\overline{\text{CLK}}$	Along with CLK, this pin is the differential input for the clock distribution section. If a single-ended input is connected to the CLK pin, connect a 0.1 µF bypass capacitor from this pin to ground.

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
15	I	3.3 V CMOS	$\overline{CS}$	Serial Control Port Chip Select; Active Low. This pin has an internal 30 kΩ pull-up resistor.
16	I	3.3 V CMOS	SCLK/SCL	Serial Control Port Clock Signal. This pin has an internal 30 kΩ pull-down resistor in SPI mode but is high impedance in I^2C mode.
17	I/O	3.3 V CMOS	SDIO/SDA	Serial Control Port Bidirectional Serial Data In/Out.
18	O	3.3 V CMOS	SDO	Serial Control Port Unidirectional Serial Data Out.
19, 59	I	GND	GND	Ground Pins.
20	I	Three-level logic	SP1	Select SPI or I^2C as the serial interface port and select the I^2C slave address in I^2C mode. Three-level logic. This pin is internally biased for the open logic level.
21	I	Three-level logic	SP0	Select SPI or I^2C as the serial interface port and select the I^2C slave address in I^2C mode. Three-level logic. This pin is internally biased for the open logic level.
22	I	3.3 V CMOS	EEPROM	Setting this pin high selects the register values stored in the internal EEPROM to be loaded at reset and/or power-up. Setting this pin low causes the AD9520-2 to load the hard-coded default register values at power-up/reset (unless Register 0xB02[1] is used. See the Soft Reset via the Serial Port section). This pin has an internal 30 kΩ pull-down resistor. Note that, to guarantee proper loading of the EEPROM during startup, a high-low-high pulse on the $\overline{RESET}$ pin should occur after the power supply has stabilized.
23	I	3.3 V CMOS	$\overline{RESET}$	Chip Reset, Active Low. This pin has an internal 30 kΩ pull-up resistor.
24	I	3.3 V CMOS	$\overline{PD}$	Chip Power-Down, Active Low. This pin has an internal 30 kΩ pull-up resistor.
25	O	LVPECL or CMOS	OUT9 (OUT9A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
26	O	LVPECL or CMOS	$\overline{OUT9}$ (OUT9B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
27, 35, 46, 54	I	Power	VS_DRV	Output Driver Power Supply Pins. As a group, these pins can be set to either 2.5 V or 3.3 V. All four pins must be set to the same voltage.
28	O	LVPECL or CMOS	OUT10 (OUT10A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
29	O	LVPECL or CMOS	$\overline{OUT10}$ (OUT10B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
30	O	LVPECL or CMOS	OUT11 (OUT11A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
31	O	LVPECL or CMOS	$\overline{OUT11}$ (OUT11B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
33	O	LVPECL or CMOS	OUT6 (OUT6A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
34	O	LVPECL or CMOS	$\overline{OUT6}$ (OUT6B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
36	O	LVPECL or CMOS	OUT7 (OUT7A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
37	O	LVPECL or CMOS	$\overline{OUT7}$ (OUT7B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
38	O	LVPECL or CMOS	OUT8 (OUT8A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
39	O	LVPECL or CMOS	$\overline{OUT8}$ (OUT8B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
42	O	LVPECL or CMOS	$\overline{OUT5}$ (OUT5B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
43	O	LVPECL or CMOS	OUT5 (OUT5A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
44	O	LVPECL or CMOS	$\overline{OUT4}$ (OUT4B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
45	O	LVPECL or CMOS	OUT4 (OUT4A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
47	O	LVPECL or CMOS	$\overline{\text{OUT3}}$ (OUT3B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
48	O	LVPECL or CMOS	OUT3 (OUT3A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
50	O	LVPECL or CMOS	$\overline{\text{OUT2}}$ (OUT2B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
51	O	LVPECL or CMOS	OUT2 (OUT2A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
52	O	LVPECL or CMOS	$\overline{\text{OUT1}}$ (OUT1B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
53	O	LVPECL or CMOS	OUT1 (OUT1A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
55	O	LVPECL or CMOS	$\overline{\text{OUT0}}$ (OUT0B)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
56	O	LVPECL or CMOS	OUT0 (OUT0A)	Clock Output. This pin can be configured as one side of a differential LVPECL output or as a single-ended CMOS output.
58	O	Current set resistor	RSET	Clock Distribution Current Set Resistor. Connect a 4.12 kΩ resistor from this pin to GND.
62	O	Current set resistor	CPRSET	Charge Pump Current Set Resistor. Connect a 5.1 kΩ resistor from this pin to GND. This resistor can be omitted if the PLL is not used.
63	I	Reference input	$\overline{\text{REFIN}}$ (REF2)	Along with REFIN, this is the differential input for the PLL reference. Alternatively, this pin is a single-ended input for REF2.
64	I	Reference input	REFIN (REF1)	Along with $\overline{\text{REFIN}}$, this is the differential input for the PLL reference. Alternatively, this pin is a single-ended input for REF1.
EPAD		GND	GND	The exposed die pad must be connected to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

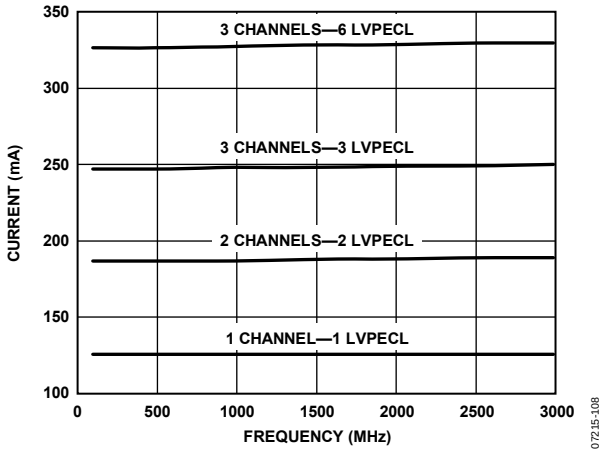


Figure 6. Total Current vs. Frequency, CLK-to-Output (PLL Off), LVPECL Outputs Terminated 50 Ω to V_{S_DRV} − 2 V

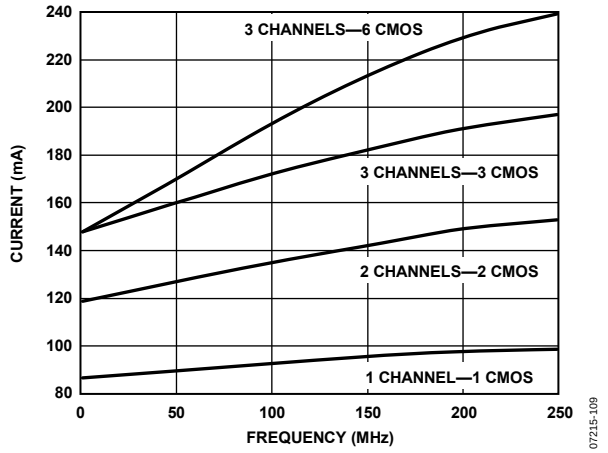


Figure 7. Total Current vs. Frequency, CLK-to-Output (PLL Off), CMOS Outputs with 10 pF Load

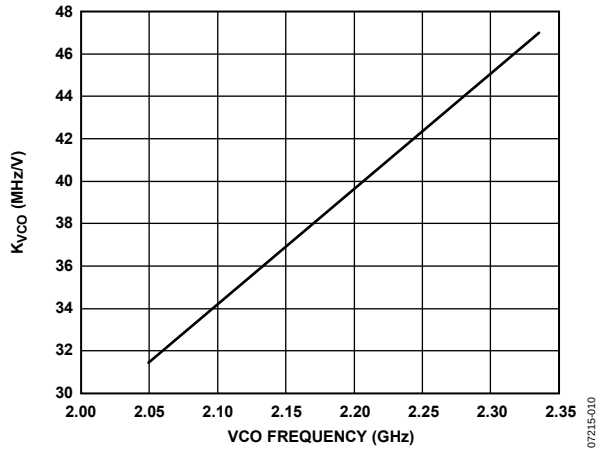


Figure 8. K_{VCO} vs. VCO Frequency

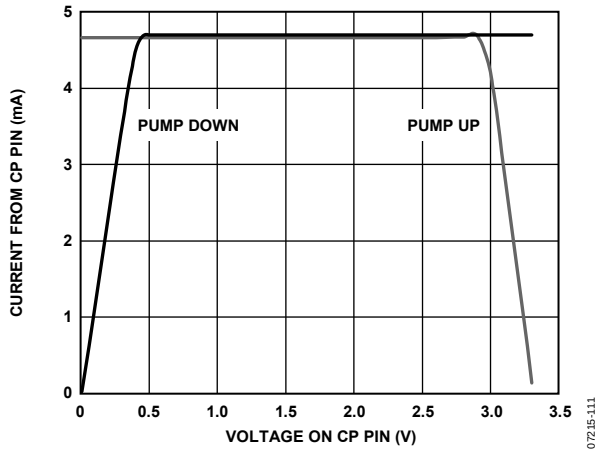


Figure 9. Charge Pump Characteristics at CP_V = 3.3 V

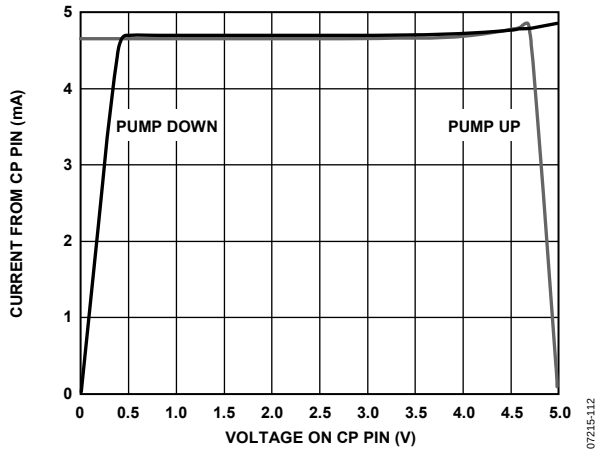


Figure 10. Charge Pump Characteristics at CP_V = 5.0 V

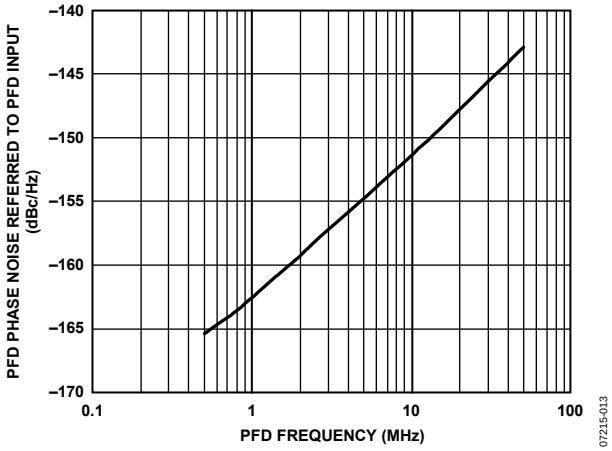


Figure 11. PFD Phase Noise Referred to PFD Input vs. PFD Frequency

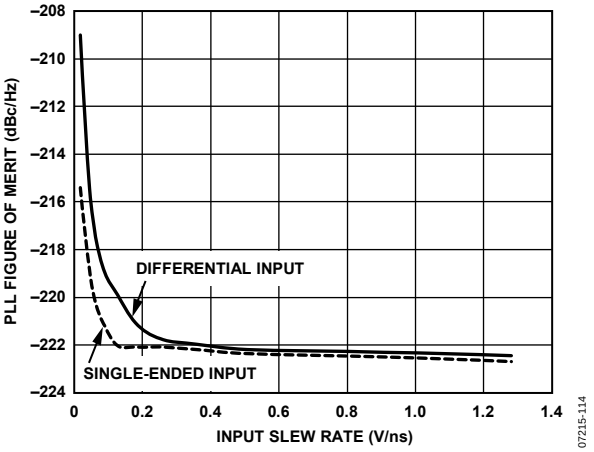


Figure 12. PLL Figure of Merit (FOM) vs. Slew Rate at REFIN/$\overline{REFIN}$

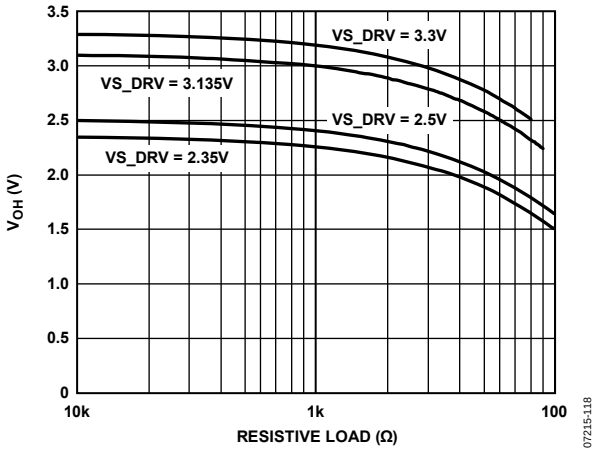


Figure 15. CMOS Output V_{OH} (Static) vs. R_{LOAD} (to Ground)

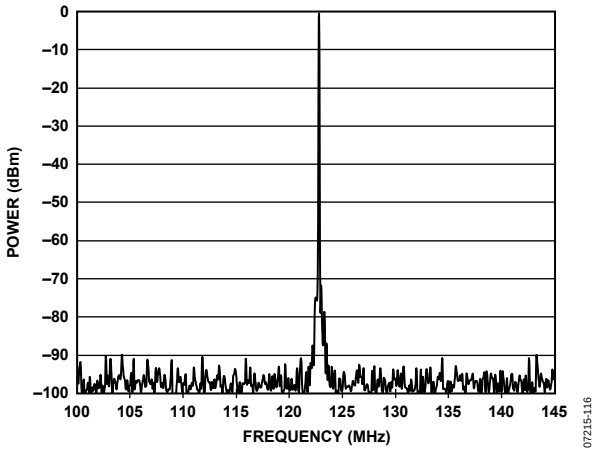


Figure 13. PFD/CP Spurs; 122.88 MHz; PFD = 15.36 MHz; LBW = 127 kHz; I_{CP} = 3.0 mA; f_{VCO} = 2211.84 MHz

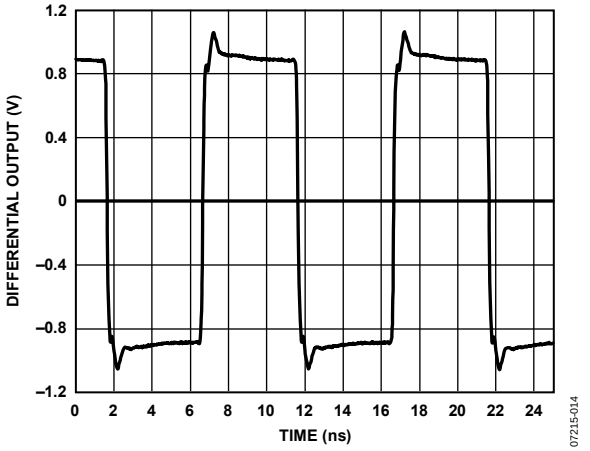


Figure 16. LVPECL Output (Differential) at 100 MHz

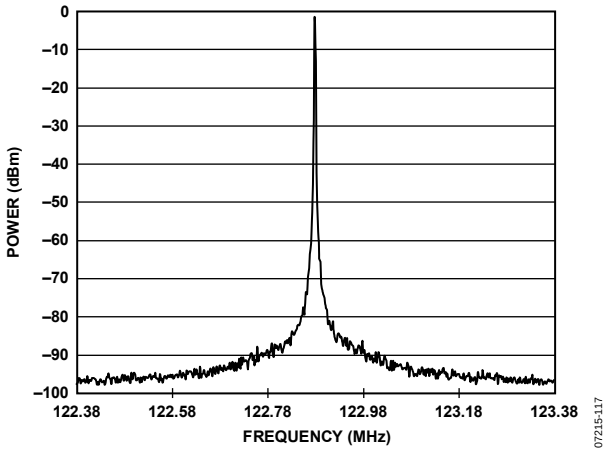


Figure 14. Output Spectrum, LVPECL; 122.88 MHz; PFD = 15.36 MHz; LBW = 127 kHz; I_{CP} = 3.0 mA; f_{VCO} = 2211.84 MHz

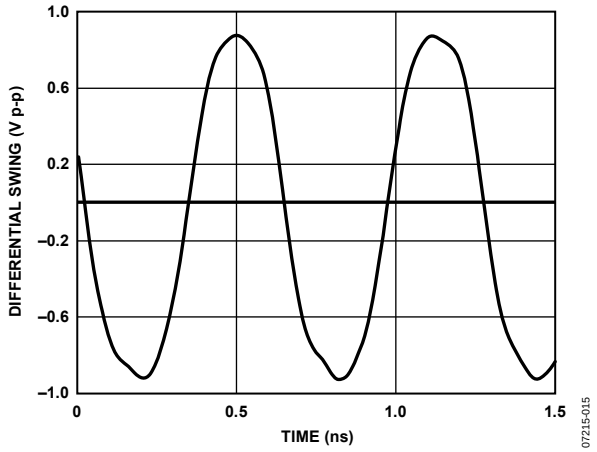


Figure 17. LVPECL Differential Voltage Swing at 1600 MHz

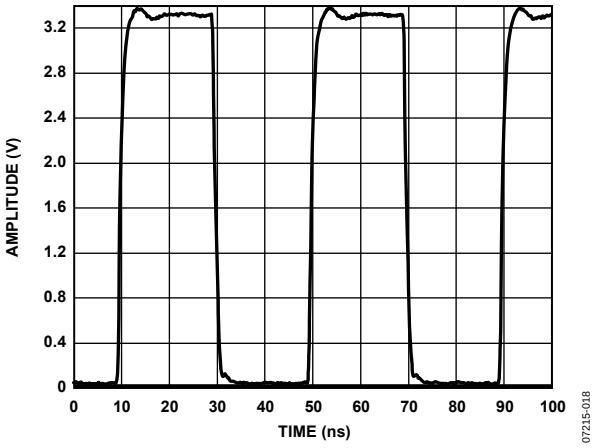


Figure 18. CMOS Output with 10 pF Load at 25 MHz

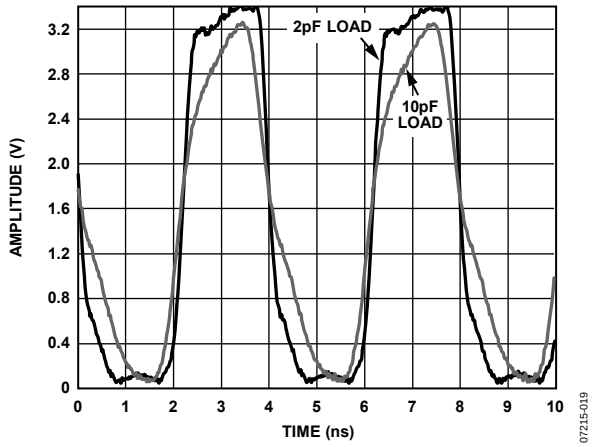


Figure 19. CMOS Output with 2 pF and 10 pF Load at 250 MHz

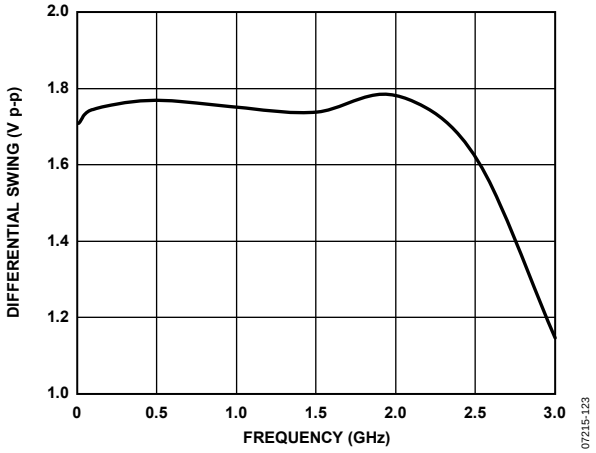


Figure 20. LVPECL Differential Voltage Swing vs. Frequency

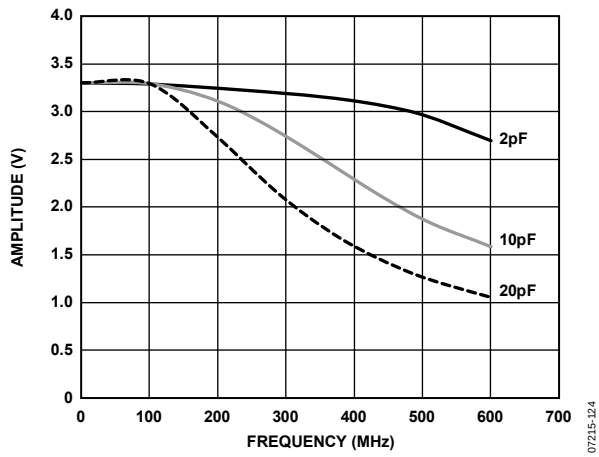


Figure 21. CMOS Output Swing vs. Frequency and Capacitive Load

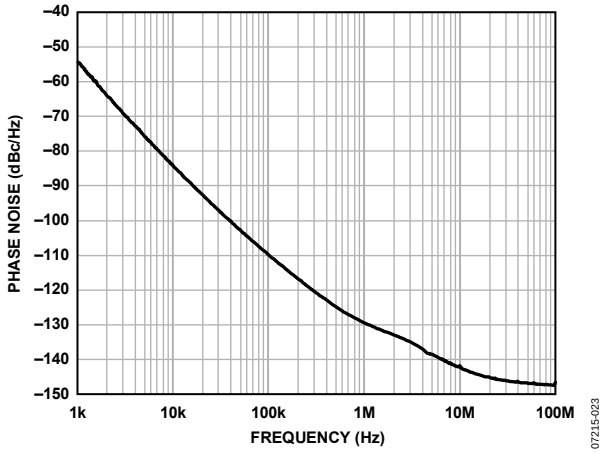


Figure 22. Internal VCO Phase Noise (Absolute), Direct-to-LVPECL at 2050 MHz

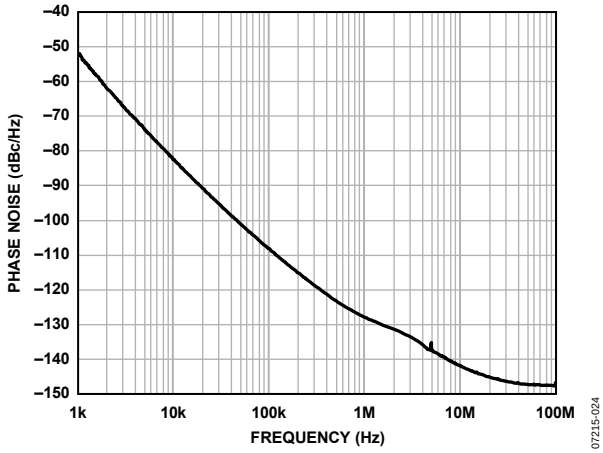


Figure 23. Internal VCO Phase Noise (Absolute), Direct-to-LVPECL at 2175 MHz

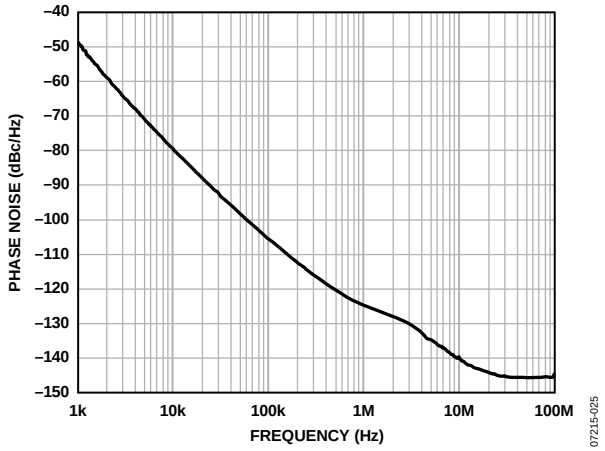


Figure 24. Internal VCO Phase Noise (Absolute), Direct-to-LVPECL at 2335 MHz

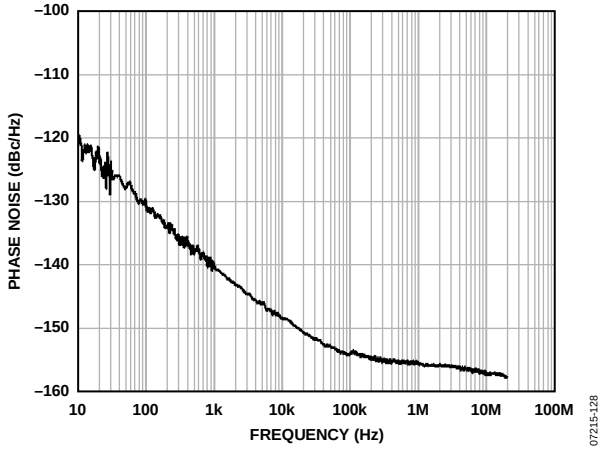


Figure 25. Additive (Residual) Phase Noise, CLK-to-LVPECL at 245.76 MHz, Divide-by-1

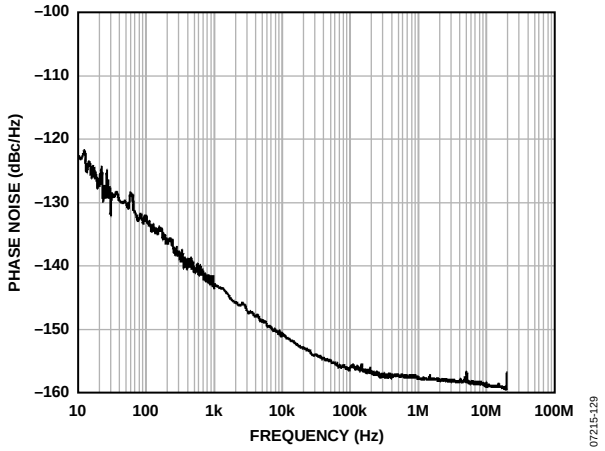


Figure 26. Additive (Residual) Phase Noise, CLK-to-LVPECL at 200 MHz, Divide-by-5

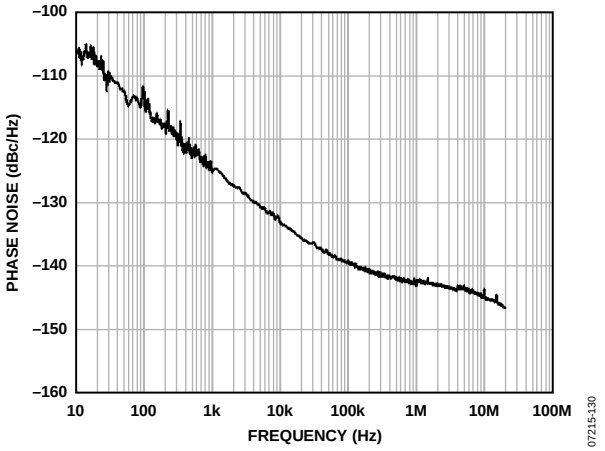


Figure 27. Additive (Residual) Phase Noise, CLK-to-LVPECL at 1600 MHz, Divide-by-1

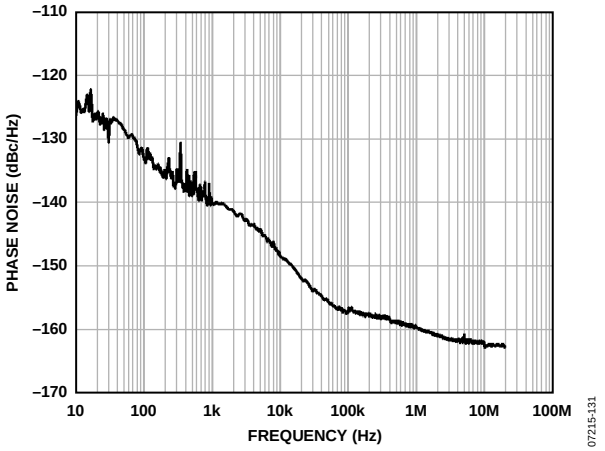


Figure 28. Additive (Residual) Phase Noise, CLK-to-CMOS at 50 MHz, Divide-by-20

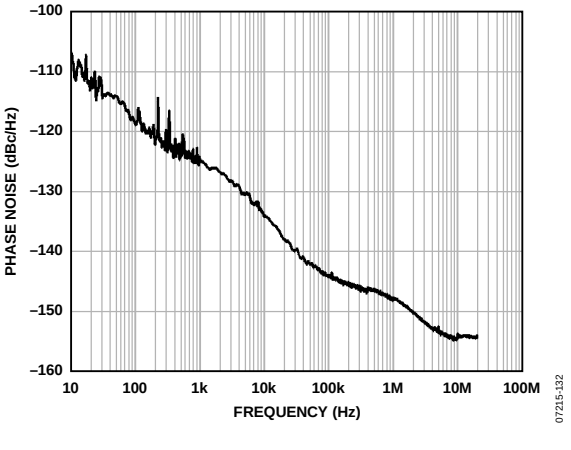
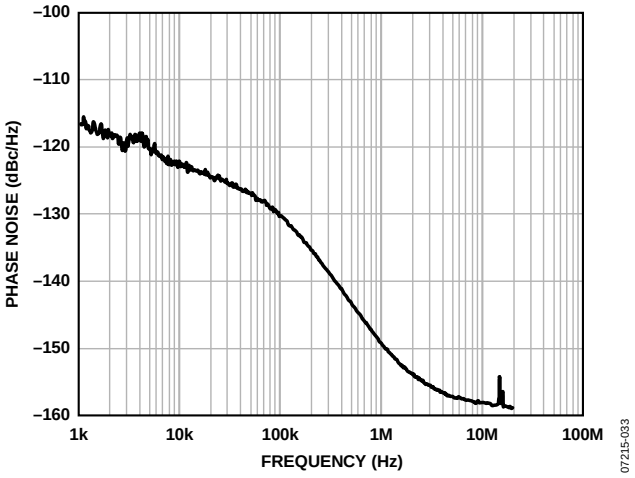
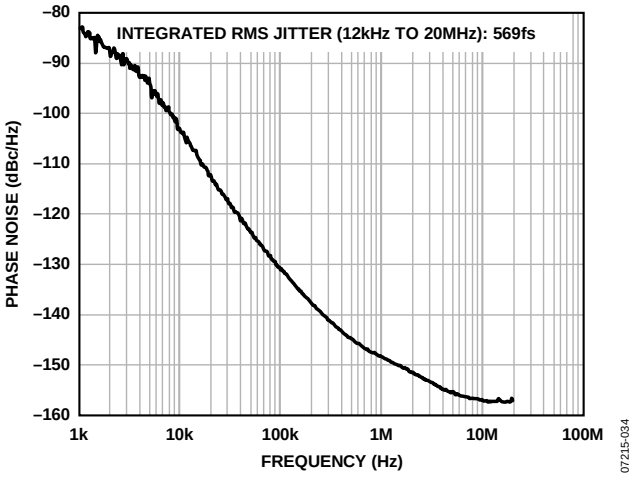


Figure 29. Additive (Residual) Phase Noise, CLK-to-CMOS at 250 MHz, Divide-by-4



NOTES
1. THE LOOP FILTER USED TO GENERATE THIS PLOT IS SHOWN IN FIGURE 41.

Figure 30. Phase Noise (Absolute) Clock Generation; Internal VCO at 2.212 GHz; PFD = 15.36 MHz; LBW = 66 kHz; LVPECL Output = 122.88 MHz



NOTES
1. THE LOOP FILTER USED TO GENERATE THIS PLOT IS SHOWN IN FIGURE 42.

Figure 32. Phase Noise (Absolute) Clock Cleanup; Internal VCO at 2.177 GHz; PFD = 120 kHz; LBW = 2.18 kHz; LVPECL Output = 155.52 MHz

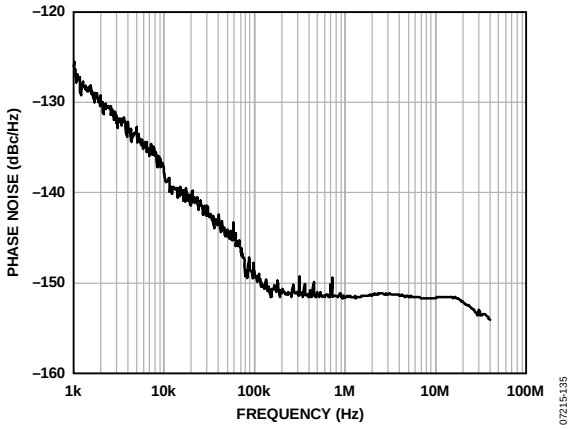


Figure 31. Phase Noise (Absolute), External VCXO (Toyocom TCO-2112) at 245.76 MHz; PFD = 15.36 MHz; LBW = 250 Hz; LVPECL Output = 245.76 MHz

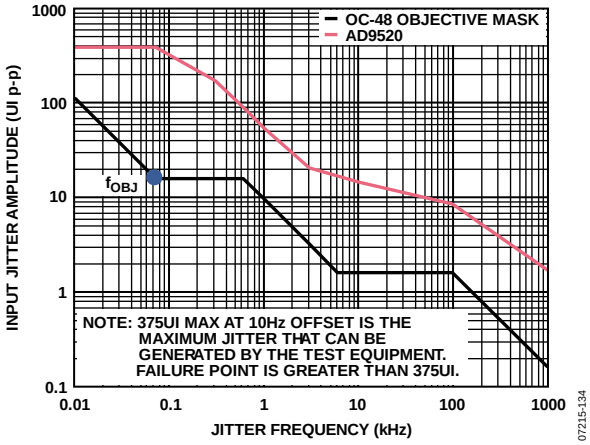


Figure 33. Telcordia GR-253 Jitter Tolerance Plot

TERMINOLOGY

Phase Jitter and Phase Noise
An ideal sine wave can be thought of as having a continuous and even progression of phase with time from 0° to 360° for each cycle. Actual signals, however, display a certain amount of variation from ideal phase progression over time. This phenomenon is called phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, which is characterized statistically as being Gaussian (normal) in distribution.

This phase jitter leads to a spreading out of the energy of the sine wave in the frequency domain, producing a continuous power spectrum. This power spectrum is usually reported as a series of values whose units are dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in decibels) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

It is meaningful to integrate the total power contained within some interval of offset frequencies (for example, 10 kHz to 10 MHz). This is called the integrated phase noise over that frequency offset interval and can be readily related to the time jitter due to the phase noise within that offset frequency interval.

Phase noise has a detrimental effect on the performance of ADCs, DACs, and RF mixers. It lowers the achievable dynamic range of the converters and mixers, although they are affected in somewhat different ways.

Time Jitter
Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings varies. In a square wave, the time jitter is a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Because these variations are random in nature, the time jitter is specified in seconds root mean square (rms) or 1 sigma of the Gaussian distribution.

Time jitter that occurs on a sampling clock for a DAC or an ADC decreases the signal-to-noise ratio (SNR) and dynamic range of the converter. A sampling clock with the lowest possible jitter provides the highest performance from a given converter.

Additive Phase Noise
Additive phase noise is the amount of phase noise that can be attributed to the device or subsystem being measured. The phase noise of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device impacts the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contributes its own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise. When there are multiple contributors to phase noise, the total is the square root of the sum of squares of the individual contributors.

Additive Time Jitter
Additive time jitter is the amount of time jitter that can be attributed to the device or subsystem being measured. The time jitter of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device impacts the total system time jitter when used in conjunction with the various oscillators and clock sources, each of which contributes its own time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.

DETAILED BLOCK DIAGRAM

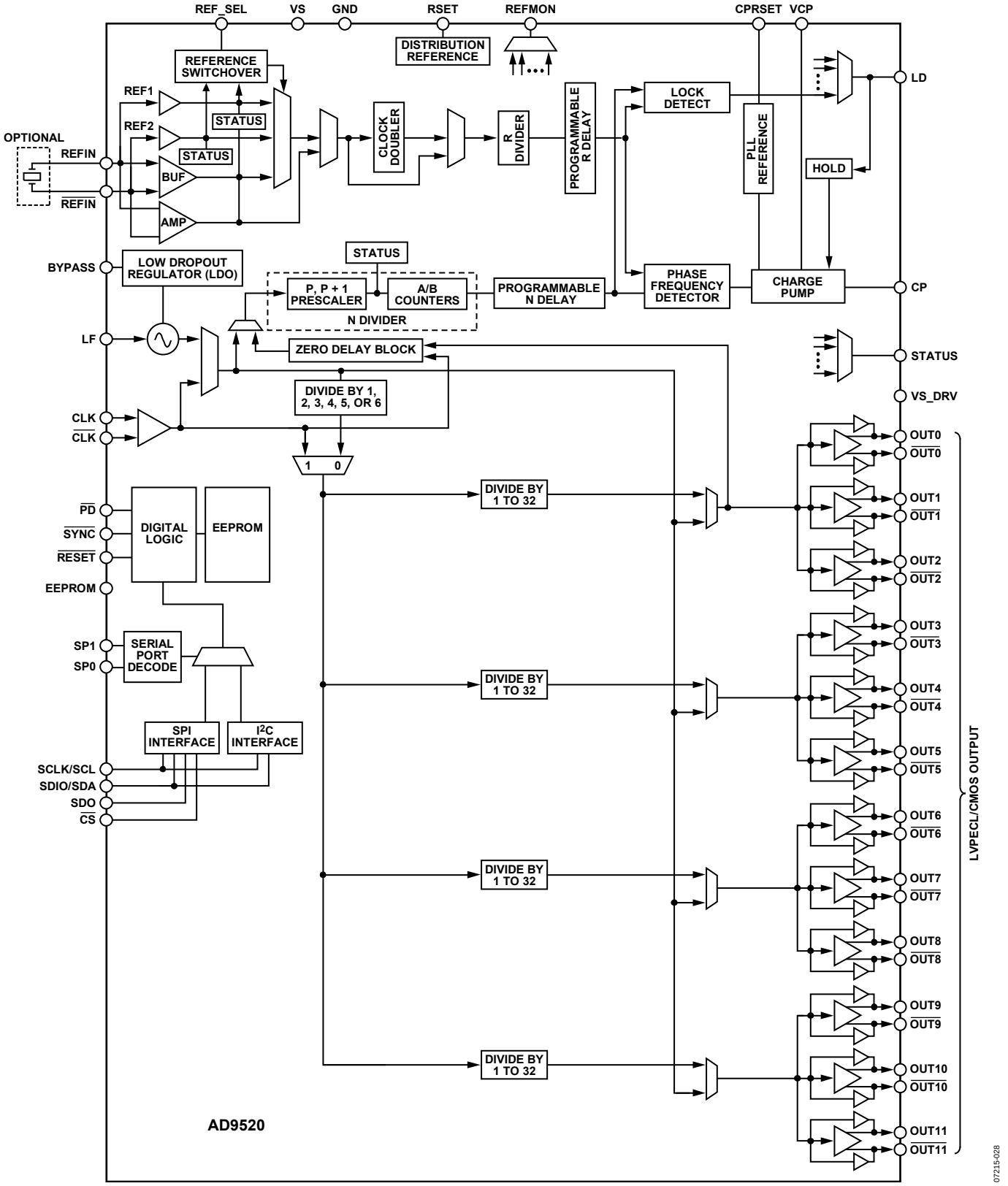


Figure 34.

THEORY OF OPERATION

OPERATIONAL CONFIGURATIONS

The AD9520-2 can be configured in several ways. These configurations must be set up by loading the control registers (see Table 50 to Table 61). Each section or function must be individually programmed by setting the appropriate bits in the corresponding control register or registers. After the desired configuration is programmed, the user can store these values in the on-board EEPROM to allow the part to power up in the desired configuration without user intervention.

Mode 0—Internal VCO and Clock Distribution

When the internal VCO and PLL are used, the VCO divider must also be used, in most cases, to ensure that the frequency presented to the channel dividers does not exceed its specified maximum frequency (see Table 3). The exceptions to this are the VCO direct mode and cases where the VCO frequency is ≤1600 MHz. The internal PLL uses an external loop filter to set the loop bandwidth. The external loop filter is also crucial to the loop stability.

When the internal VCO is used, the VCO must be calibrated (Register 0x018[0] = 1b) to ensure optimal performance.

For internal VCO and clock distribution applications, use the register settings shown in Table 22.

Table 22. Settings When Using Internal VCO

Register	Description
0x010[1:0] = 00b	PLL normal operation (PLL on)
0x010 to 0x01E	PLL settings; select and enable a reference input; set R, N (P, A, B), PFD polarity, and I_{CP} according to the intended loop configuration
0x1E1[1] = 1b	Select VCO as the source
0x01C[2:0]	Enable reference inputs
0x1E0[2:0]	Set VCO divider
0x1E1[0] = 0b	Use the VCO divider as the source for the distribution section
0x018[0] = 0b, 0x232[0] = 1b	Clear previous VCO calibration and issue IO_UPDATE (not necessary the first time after power-up, but must be done subsequently)
0x018[0] = 1b, 0x232[0] = 1b	Initiate VCO calibration, issue IO_UPDATE

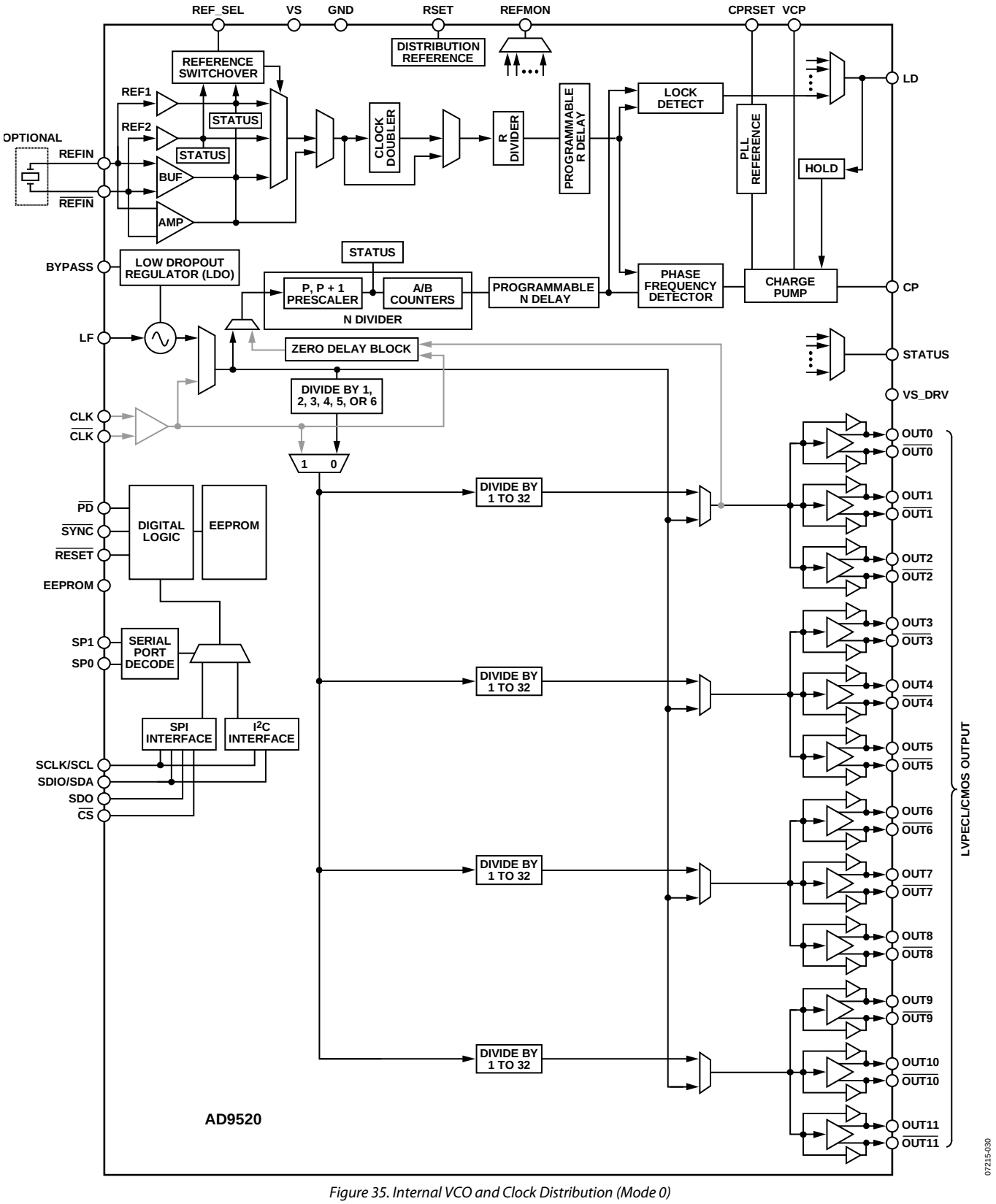


Figure 35. Internal VCO and Clock Distribution (Mode 0)

Mode 1—Clock Distribution or External VCO < 1600 MHz

When the external clock source to be distributed or the external VCO/VCXO is <1600 MHz, a configuration that bypasses the VCO divider can be used. This is the only difference from Mode 2. Bypassing the VCO divider limits the frequency of the clock source to <1600 MHz (due to the maximum input frequency allowed at the channel dividers).

Configuration and Register Settings

For clock distribution applications where the external clock is <1600 MHz, use the register settings shown in Table 23.

Table 23. Settings for Clock Distribution < 1600 MHz

Register	Description
0x010[1:0] = 01b	PLL asynchronous power-down (PLL off)
0x1E1[0] = 1b	Bypass the VCO divider as the source for the distribution section
0x1E1[1] = 0b	Select CLK as the source

When the internal PLL is used with an external VCO < 1600 MHz, the PLL must be turned on.

Table 24. Settings for Using Internal PLL with External VCO < 1600 MHz

Register	Description
0x1E1[0] = 1b	Bypass the VCO divider as the source for the distribution section
0x010[1:0] = 00b	PLL normal operation (PLL on) along with other appropriate PLL settings in Register 0x010 to Register 0x01E

An external VCO/VCXO requires an external loop filter that must be connected between the CP pin and the tuning pin of the VCO/VCXO. This loop filter determines the loop bandwidth and stability of the PLL. Make sure to select the proper PFD polarity for the VCO/VCXO being used.

Table 25. Setting the PFD Polarity

Register	Description
0x010[7] = 0b	PFD polarity positive (higher control voltage produces higher frequency)
0x010[7] = 1b	PFD polarity negative (higher control voltage produces lower frequency)

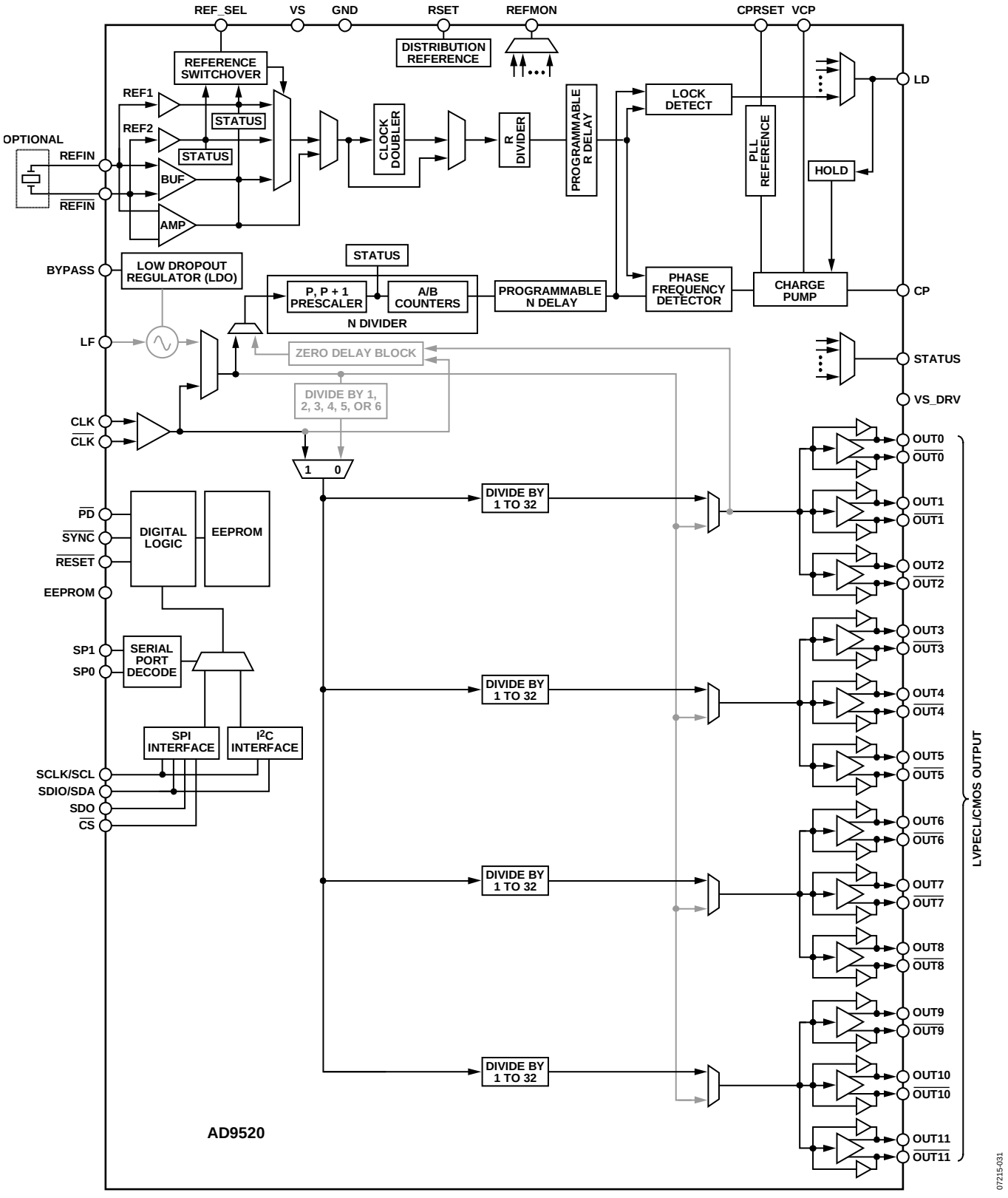


Figure 36. Clock Distribution or External VCO < 1600 MHz (Mode 1)

Mode 2—High Frequency Clock Distribution; CLK or External VCO > 1600 MHz

The AD9520-2 power-up default configuration has the PLL powered off and the routing of the input set so that the CLK/$\overline{\text{CLK}}$ input is connected to the distribution section through the VCO divider (divide-by-1/divide-by-2/divide-by-3/divide-by-4/divide-by-5/divide-by-6). This is a distribution-only mode that allows for an external input up to 2400 MHz (see Table 3). The maximum frequency that can be applied to the channel dividers is 1600 MHz; therefore, higher input frequencies must be divided down before reaching the channel dividers.

When the PLL is enabled, this routing also allows the use of the PLL with an external VCO or VCXO with a frequency of less than 2400 MHz. In this configuration, the internal VCO is not used and is powered off. The external VCO/VCXO feeds directly into the prescaler.

The register settings shown in Table 26 are the default values of these registers at power-up or after a reset operation.

Table 26. Default Register Settings for Clock Distribution Mode

Register	Description
0x010[1:0] = 01b	PLL asynchronous power-down (PLL off)
0x1E0[2:0] = 000b	Set VCO divider = 2
0x1E1[0] = 0b	Use the VCO divider
0x1E1[1] = 0b	Select CLK as the source

When the internal PLL is used with an external VCO, the PLL must be turned on.

Table 27. Settings When Using an External VCO

Register	Description
0x010[1:0] = 00b	PLL normal operation (PLL on)
0x010 to 0x01E	PLL settings; select and enable a reference input; set R, N (P, A, B), PFD polarity, and I_{CP} according to the intended loop configuration
0x1E1[1] = 0b	Select CLK as the source

An external VCO requires an external loop filter that must be connected between CP and the tuning pin of the VCO. This loop filter determines the loop bandwidth and stability of the PLL. Make sure to select the proper PFD polarity for the VCO being used.

Table 28. Setting the PFD Polarity

Register	Description
0x010[7] = 0b	PFD polarity positive (higher control voltage produces higher frequency)
0x010[7] = 1b	PFD polarity negative (higher control voltage produces lower frequency)

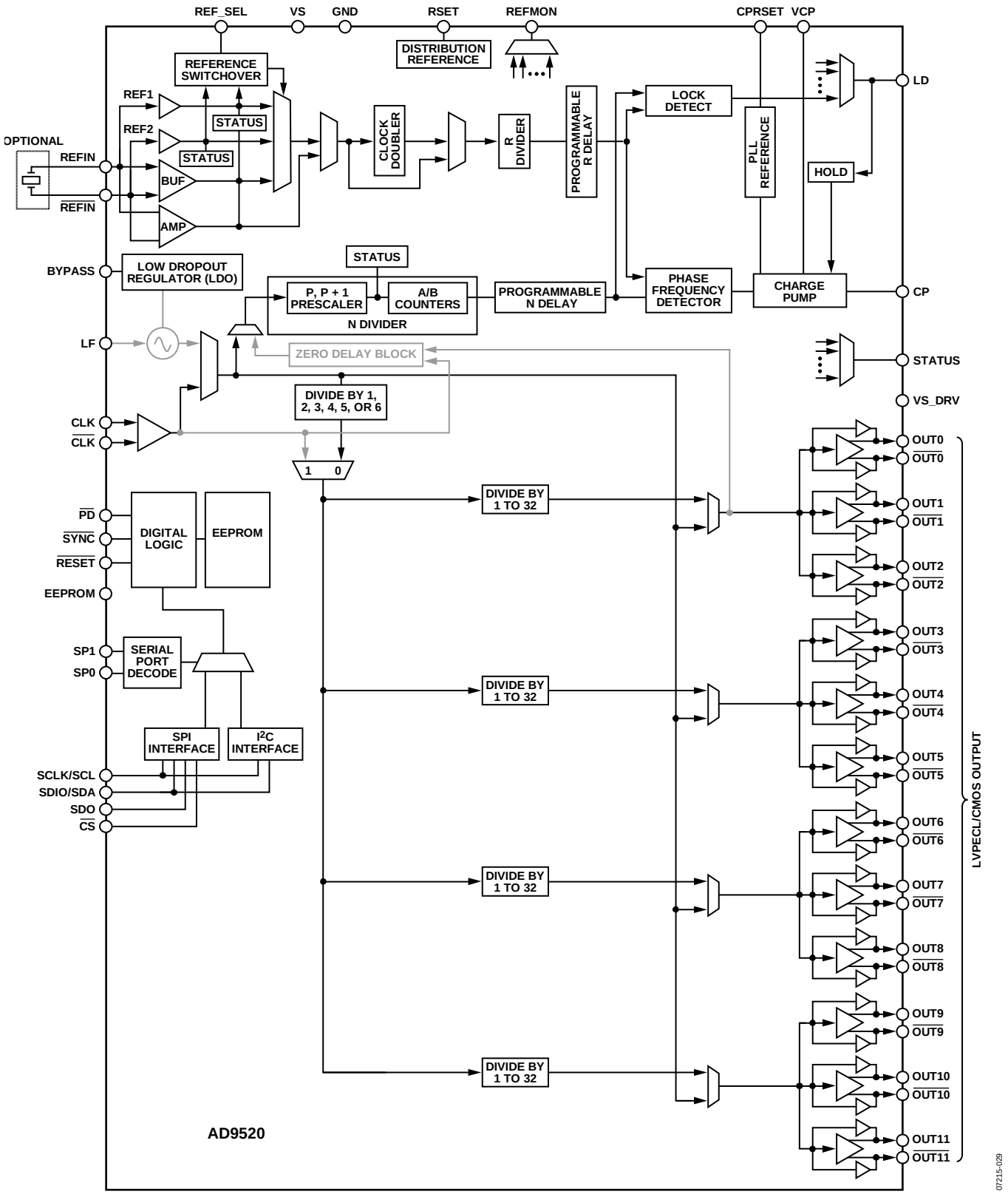


Figure 37. High Frequency Clock Distribution or External VCO > 1600 MHz (Mode 2)

Phase-Locked Loop (PLL)

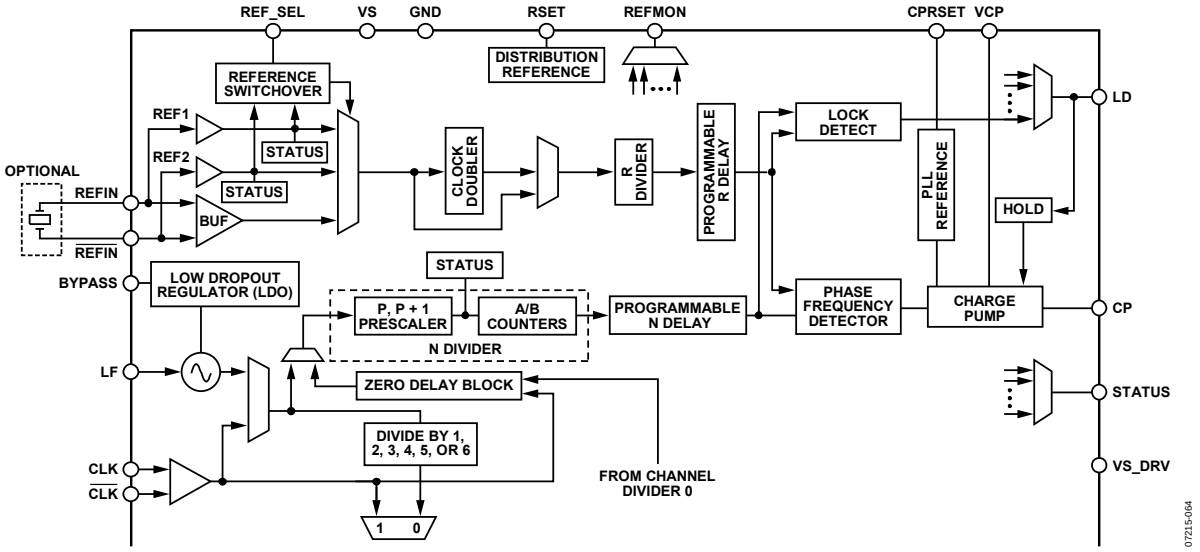


Figure 38. PLL Functional Block Diagram

The AD9520-2 includes an on-chip PLL with an on-chip VCO. The PLL blocks can be used either with the on-chip VCO to create a complete phase-locked loop or with an external VCO or VCXO. The PLL requires an external loop filter, which usually consists of a small number of capacitors and resistors. The configuration and components of the loop filter help to establish the loop bandwidth and stability of the operating PLL.

The AD9520-2 PLL is useful for generating clock frequencies from a supplied reference frequency. This includes conversion of reference frequencies to much higher frequencies for subsequent division and distribution. In addition, the PLL can be used to clean up jitter and phase noise on a noisy reference. The exact choice of PLL parameters and loop dynamics is application specific. The flexibility and depth of the AD9520-2 PLL allow the part to be tailored to function in many different applications and signal environments.

Configuration of the PLL

The AD9520-2 allows flexible configuration of the PLL, which accommodates various reference frequencies, PFD comparison frequencies, VCO frequencies, internal or external VCO/VCXO, and loop dynamics. This is accomplished by the various settings for the R divider, N divider, PFD polarity (applicable only to the external VCO/VCXO), antibacklash pulse width, charge pump current, selection of internal VCO or external VCO/ VCXO, and the loop bandwidth. These are managed through programmable register settings (see Table 50 and Table 54) and by the design of the external loop filter. Successful PLL operation and satisfactory PLL loop performance are highly dependent upon proper configuration of the PLL settings, and the design of the external loop filter is crucial to the proper operation of the PLL.

ADIsimCLK™ is a free program that can help with the design and exploration of the capabilities and features of the AD9520-2, including the design of the PLL loop filter.

Phase Frequency Detector (PFD)

The PFD takes inputs from the R divider and the N divider and produces an output proportional to the phase and frequency difference between them. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. The antibacklash pulse width is set by Register 0x017[1:0].

An important limit to keep in mind is the maximum frequency allowed into the PFD. The maximum input frequency into the PFD is a function of the antibacklash pulse setting, as specified in the phase/frequency detector (PFD) parameter in Table 2.

Charge Pump (CP)

The charge pump is controlled by the PFD. The PFD monitors the phase and frequency relationship between its two inputs and tells the CP to pump up or pump down to charge or discharge the integrating node (part of the loop filter). The integrated and filtered CP current is transformed into a voltage that drives the tuning node of the internal VCO through the LF pin (or the tuning pin of an external VCO) to move the VCO frequency up or down. The CP can be set (Register 0x010[3:2]) for high impedance (allows holdover operation), for normal operation (attempts to lock the PLL loop), or for pump-up or pump-down (test modes). The CP current is programmable in eight steps from (nominally) 0.6 mA to 4.8 mA. The CP current LSB is set by the CPRSET resistor, which is nominally 5.1 kΩ. The exact value of the CP current can be calculated with the following equation:

$$I_{CP}\ (A) = \frac{3.06}{CP_{RSET}\ (\Omega)}$$

On-Chip VCO

The AD9520-2 includes an on-chip VCO covering the frequency range shown in Table 2. The calibration procedure ensures that the VCO operating voltage is centered for the desired VCO frequency. The VCO must be calibrated when the VCO loop is first set up, as well as any time the nominal VCO frequency changes. However, once the VCO is calibrated, the VCO has sufficient operating range to stay locked over temperature and voltage extremes without needing additional calibration. See the VCO Calibration section for additional information.

The on-chip VCO is powered by an on-chip, low dropout (LDO), linear voltage regulator. The LDO provides some isolation of the VCO from variations in the power supply voltage level. The BYPASS pin should be connected to ground by a 220 nF capacitor to ensure stability. This LDO employs the same technology that is used in the anyCAP® line of regulators from Analog Devices, Inc., making it insensitive to the type of capacitor used. Driving an external load from the BYPASS pin is not supported.

PLL External Loop Filter

When using the internal VCO, reference the external loop filter to the BYPASS pin for optimal noise and spurious performance. Figure 39 shows an example of an external loop filter for the PLL. This third-order design usually offers the best performance. A loop filter must be calculated for each desired PLL configuration. The component values depend upon the VCO frequency, the K_{VCO}, the PFD frequency, the CP current, the desired loop bandwidth, and the desired phase margin. The loop filter affects the phase noise, loop settling time, and loop stability. A knowledge of PLL theory is necessary for understanding loop filter design. Available tools, such as ADIsimCLK, can help with the calculation of a loop filter according to the application requirements.

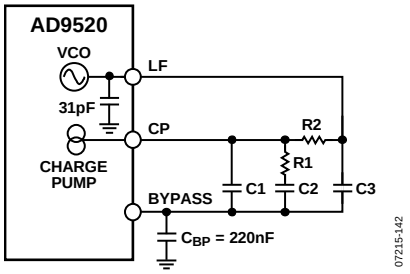


Figure 39. Example of External Loop Filter for a PLL Using the Internal VCO

When using an external VCO, ensure that the external loop filter is referenced to ground. See Figure 40 for an example of an external loop filter for a PLL using an external VCO.

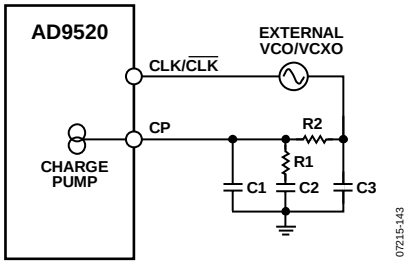


Figure 40. Example of External Loop Filter for a PLL Using an External VCO

Figure 41 and Figure 42 show the typical PLL loop filters that are used to generate the plots in Figure 30 and Figure 32, respectively.

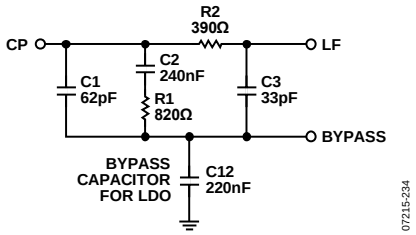


Figure 41. Typical PLL Loop Filter Used for Clock Generation

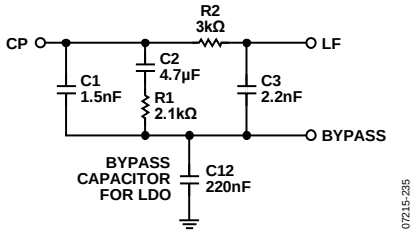


Figure 42. Typical PLL Loop Filter Used for Clock Cleanup

PLL Reference Inputs

The AD9520-2 features a flexible PLL reference input circuit that allows a fully differential input, two separate single-ended inputs, or a 16.67 MHz to 33.33 MHz crystal oscillator with an on-chip maintaining amplifier. An optional reference clock doubler can be used to double the PLL reference frequency. The input frequency range for the reference inputs is specified in Table 2. Both the differential and the single-ended inputs are self-biased, allowing for easy ac coupling of input signals.

Either a differential or a single-ended reference must be specifically enabled. All PLL reference inputs are off by default.

The differential input and the single-ended inputs share two pins, REFIN and $\overline{\text{REFIN}}$ (REF1 and REF2, respectively). The desired reference input type is selected and controlled by Register 0x01C (see Table 50 and Table 54).

When the differential reference input is selected, the self-bias level of the two sides is offset slightly (~100 mV, see Table 2) to prevent chattering of the input buffer when the reference is slow or missing. This increases the voltage swing that is required of the driver and overcomes the offset. The differential reference input can be driven by either ac-coupled LVDS or ac-coupled LVPECL signals.

The single-ended inputs can be driven by either a dc-coupled CMOS level signal or an ac-coupled sine wave or square wave. To avoid input buffer chatter when a single-ended, ac-coupled input signal stops toggling, the user can set Register 0x018[7] to 1b. This shifts the dc offset bias point down 140 mV. To increase isolation and reduce power, each single-ended input can be independently powered down.

The differential reference input receiver is powered down when the differential reference input is not selected or when the PLL is powered down. The single-ended buffers power down when the PLL is powered down or when their respective individual power-down registers are set. When the differential mode is selected, the single-ended inputs are powered down.

In differential mode, the reference input pins are internally self-biased so that they can be ac-coupled via capacitors. It is possible to dc couple to these inputs. If the differential REFIN is driven by a single-ended signal, the unused side ($\overline{\text{REFIN}}$) should be decoupled via a suitable capacitor to a quiet ground. Figure 43 shows the equivalent circuit of REFIN.

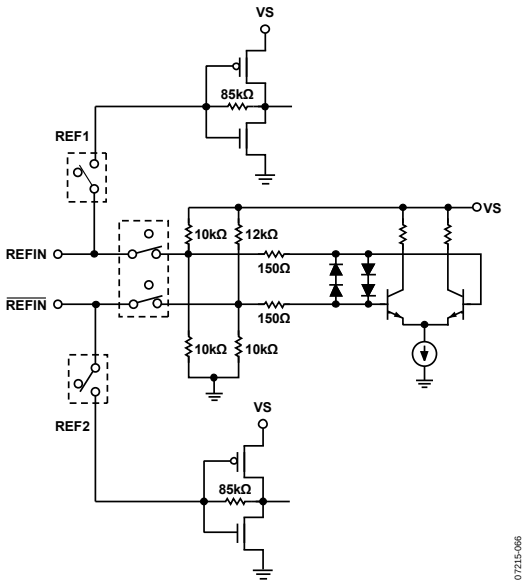


Figure 43. REFIN Equivalent Circuit for Non-XTAL Mode

Crystal mode is nearly identical to differential mode. The user enables a maintaining amplifier by setting the enable XTAL OSC bit and putting a series resonant, AT fundamental cut crystal across the REFIN and $\overline{\text{REFIN}}$ pins.

Reference Switchover

The AD9520-2 supports dual single-ended CMOS inputs, as well as a single differential reference input. In the dual single-ended reference mode, the AD9520-2 supports automatic revertive and manual PLL reference clock switching between REF1 (on Pin REFIN) and REF2 (on Pin $\overline{\text{REFIN}}$). This feature supports networking and other applications that require smooth switching of redundant references. When used in conjunction with the automatic holdover function, the AD9520-2 can achieve a worst-case reference input switchover with an output frequency disturbance as low as 10 ppm.

The AD9520-2 features a dc offset option in single-ended mode. This option is designed to eliminate the risk of the reference inputs chattering when they are ac-coupled and the reference clock disappears. When using the reference switchover, the single-ended reference inputs should be dc-coupled CMOS levels (with the AD9520-2 dc offset feature disabled). Alternatively, the inputs can be ac-coupled and dc offset feature enabled. Keep in mind, however, that the minimum input amplitude for the reference inputs is greater when the dc offset is turned on.

Reference switchover can be performed manually or automatically. Manual switchover is performed either through Register 0x01C or by using the REF_SEL pin. Manual switchover requires the presence of a clock on the reference input that is being switched to; otherwise, the deglitching feature must be disabled in Bit 7 of Register 0x01C. The reference switching logic fails if this condition is not met, and the PLL does not reacquire.

Automatic revertive switchover relies on the REFMON pin to indicate when REF1 disappears. By programming Register 0x01B = 0xF7 and Register 0x01C = 0x26, the REFMON pin is programmed to be high when REF1 is invalid, which commands the switch to REF2. When REF1 is valid again, the REFMON pin goes low, and the part again locks to REF1. The STATUS pin can also be used for this function, and REF2 can be used as the preferred reference.

A switchover deglitch feature ensures that the PLL does not receive rising edges that are far out of alignment with the newly selected reference. For the switchover deglitch feature to work correctly, the presence of a clock is required on the reference input that is being switched to. The deglitching feature can also be disabled (Register 0x01C[7]).

Automatic nonrevertive switching is not supported.

Reference Divider R

The reference inputs are routed to the reference divider, R. R is a 14-bit counter that can be set to any value from 0 to 16,383 by writing to Register 0x011 and Register 0x012 (both R = 0 and R = 1 give divide-by-1.) The output of the R divider goes to one of the PFD inputs to be compared with the VCO frequency divided by the N divider. The frequency applied to the PFD must not exceed the maximum allowable frequency, which depends on the antibacklash pulse setting (see Table 2).

The R divider has its own reset. The R divider can be reset using the shared reset bit of the R, A, and B counters. It can also be reset by a $\overline{\text{SYNC}}$ operation.

VCO/VCXO Feedback Divider N—P, A, and B

The N divider is a combination of a prescaler, P, and two counters, A and B. The total divider value is

$$N = (P \times B) + A$$

where P can be 2, 4, 8, 16, or 32.

Prescaler

The prescaler of the AD9520-2 allows for two modes of operation: a fixed divide (FD) mode of 1, 2, or 3, and a dual modulus (DM) mode where the prescaler divides by P and (P + 1) {2 and 3, 4 and 5, 8 and 9, 16 and 17, or 32 and 33}. The prescaler modes of operation are given in Table 54, Register 0x016[2:0]. Not all modes are available at all frequencies (see Table 2).

When operating the AD9520-2 in dual modulus mode, P/(P + 1), the equation used to relate the input reference frequency to the VCO output frequency is

$$f_{VCO} = (f_{REF}/R) \times (P \times B + A) = f_{REF} \times N/R$$

However, when operating the prescaler in FD Mode 1, FD Mode 2, or FD Mode 3, the A counter is not used (A = 0; the divide is a fixed divide of P = 2, 4, 8, 16, or 32) and the equation simplifies to

$$f_{VCO} = (f_{REF}/R) \times (P \times B) = f_{REF} \times N/R$$

By using combinations of DM and FD modes, the AD9520-2 can achieve values of N from 1 to 262,175.

Table 29 shows how a 10 MHz reference input can be locked to any integer multiple of N.

Note that the same value of N can be derived in different ways, as illustrated by the case of N = 12. The user can choose a fixed divide mode of P = 2 with B = 6; use the dual modulus mode of 2/3 with A = 0, B = 6; or use the dual modulus mode of 4/5 with A = 0, B = 3.

A and B Counters

The B counter must be ≥3 or bypassed, and unlike the R counter, A = 0 is actually zero.

When the prescaler is in dual modulus mode, the A counter must be equal to or less than the B counter.

The maximum input frequency to the A/B counter is reflected in the maximum prescaler output frequency (~300 MHz) that is specified in Table 2. This is the prescaler input frequency (VCO or CLK) divided by P. For example, a dual modulus mode of P = 8/9 is not allowed if the VCO frequency is greater than 2400 MHz because the frequency going to the A/B counter is too high.

When the AD9520-2 B counter is bypassed (B = 1), the A counter should be set to zero, and the overall resulting divide is equal to the prescaler setting, P. The possible divide ratios in this mode are 1, 2, 3, 4, 8, 16, and 32. This mode is useful only when an external VCO/VCXO is used because the frequency range of the internal VCO requires an overall feedback divider greater than 32.

Although manual reset is not normally required, the A/B counters have their own reset bit. Alternatively, the A and B counters can be reset using the shared reset bit of the R, A, and B counters. Note that these reset bits are not self-clearing.

R, A, and B Counters—$\overline{\text{SYNC}}$ Pin Reset

The R, A, and B counters can be reset simultaneously through the $\overline{\text{SYNC}}$ pin. This function is controlled by Register 0x019[7:6] (see Table 54). The $\overline{\text{SYNC}}$ pin reset is disabled by default.

R and N Divider Delays

Both the R and N dividers feature a programmable delay cell. These delays can be enabled to allow adjustment of the phase relationship between the PLL reference clock and the VCO or CLK. Each delay is controlled by three bits. The total delay range is about 1 ns. See Register 0x019 in Table 2 and Table 54.

Table 29. How a 10 MHz Reference Input Can Be Locked to Any Integer Multiple of N

f_{REF} (MHz)	R	P	A	B	N	f_{VCO} (MHz)	Mode	Description
10	1	1	X[1]	1	1	10	FD	P = 1, B = 1 (A and B counters are bypassed).
10	1	2	X[1]	1	2	20	FD	P = 2, B = 1 (A and B counters are bypassed).
10	1	1	X[1]	3	3	30	FD	A counter is bypassed.
10	1	1	X[1]	4	4	40	FD	A counter is bypassed.
10	1	1	X[1]	5	5	50	FD	A counter is bypassed.
10	1	2	X[1]	3	6	60	FD	A counter is bypassed.
10	1	2	0	3	6	60	DM	
10	1	2	1	3	7	70	DM	Maximum frequency into prescaler in P = 2/3 mode is 200 MHz. If N = 7 or N = 11 is desired for prescaler input frequency of 200 MHz to 300 MHz, use P = 1, and N = 7 or 11, respectively.
10	1	2	2	3	8	80	DM	
10	1	2	1	4	9	90	DM	
10	1	8	6	18	150	1500	DM	
10	1	8	7	18	151	1510	DM	
10	1	16	7	9	151	1510	DM	
10	10	32	6	47	1510	1510	DM	
10	1	8	0	25	200	2000	DM	
10	1	16	0	15	240	2400	DM	
10	10	32	0	75	2400	2400	DM	

[1] X = don't care.

Digital Lock Detect (DLD)

By selecting the proper output through the mux on each pin, the DLD function is available at the LD, STATUS, and REFMON pins. The digital lock detect circuit indicates a lock when the time difference of the rising edges at the PFD inputs is less than a specified value (the lock threshold). The loss of a lock is indicated when the time difference exceeds a specified value (the unlock threshold). Note that the unlock threshold is wider than the lock threshold, which allows some phase error in excess of the lock window to occur without chattering on the lock indicator.

The lock detect window timing depends on the value of the CP_{RSET} resistor, as well as three settings: the digital lock detect window bit (Register 0x018[4]), the antibacklash pulse width bit (Register 0x017[1:0], see Table 2), and the lock detect counter (Register 0x018[6:5]). The lock and unlock detection values listed in Table 2 are for the nominal value of CP_{RSET} = 5.11 kΩ. Doubling the CP_{RSET} value to 10 kΩ doubles the values in Table 2.

A lock is not indicated until there is a programmable number of consecutive PFD cycles with a time difference that is less than the lock detect threshold. The lock detect circuit continues to indicate a lock until a time difference that is greater than the unlock threshold occurs on a single subsequent cycle. For the lock detect to work properly, the period of the PFD frequency must be greater than the unlock threshold. The number of consecutive PFD cycles required for lock is programmable (Register 0x018[6:5]).

Note that, in certain low (<500 Hz) loop bandwidth, high phase margin cases, the DLD may chatter during acquisition, which can cause the AD9520-2 to automatically enter and exit holdover. To avoid this problem, it is recommended that the user provide for a capacitor to ground on the LD pin such that current source digital lock detect (CSDLD) mode can be used.

Analog Lock Detect (ALD)

The AD9520-2 provides an ALD function that can be selected for use at the LD pin. There are two operating modes for ALD:

- N-channel open-drain lock detect. This signal requires a pull-up resistor to the positive supply, VS. The output is normally high with short, low going pulses. Lock is indicated by the minimum duty cycle of the low going pulses.
- P-channel open-drain lock detect. This signal requires a pull-down resistor to GND. The output is normally low with short, high going pulses. Lock is indicated by the minimum duty cycle of the high going pulses.

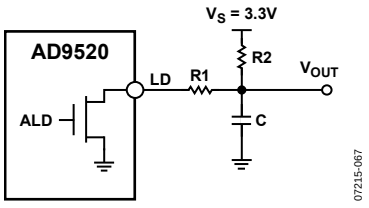


Figure 44. Example of Analog Lock Detect Filter Using N-Channel Open-Drain Driver

The analog lock detect function requires an RC filter to provide a logic level indicating lock/unlock. The ADIsimCLK tool can be used to help the user select the right passive component values for ALD to ensure its correct operation.

Current Source Digital Lock Detect (CSDLD)

During the PLL locking sequence, it is normal for the DLD signal to toggle a number of times before remaining steady when the PLL is completely locked and stable. There may be applications where it is desirable to have DLD asserted only after the PLL is solidly locked. This is possible by using the current source digital lock detect function.

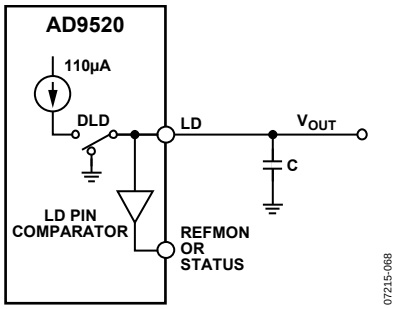


Figure 45. Current Source Digital Lock Detect

The current source lock detect provides a current of 110 µA when DLD is true and shorts to ground when DLD is false. If a capacitor is connected to the LD pin, it charges at a rate determined by the current source during the DLD true time but is discharged nearly instantly when DLD is false. By monitoring the voltage at the LD pin (top of the capacitor), LD = high happens only after the DLD is true for a sufficiently long time. Any momentary DLD false resets the charging. By selecting a properly sized capacitor, it is possible to delay a lock detect indication until the PLL is stably locked and the lock detect does not chatter.

To use current source digital lock detect, do the following:

- Place a capacitor to ground on the LD pin.
- Set Register 0x01A[5:0] = 0x04.
- Enable the LD pin comparator (Register 0x01D[3] = 1b).

The LD pin comparator senses the voltage on the LD pin, and the comparator output can be made available at the REFMON pin control (Register 0x01B[4:0]) or the STATUS pin control (Register 0x017[7:2]). The internal LD pin comparator trip point and hysteresis are given in Table 17. The voltage on the capacitor can also be sensed by an external comparator that is connected to the LD pin. In this case, enabling the on-board LD pin comparator is not necessary.

The user can asynchronously enable individual clock outputs only when CSDLD is high. To enable this feature, set the appropriate bits in the enable output on the CSDLD registers (Register 0x0FC and Register 0x0FD).

External VCXO/VCO Clock Input (CLK/$\overline{CLK}$)

This differential input is used to drive the AD9520-2 clock distribution section. This input can receive up to 2.4 GHz. The pins are internally self-biased, and the input signal should be ac-coupled via capacitors.

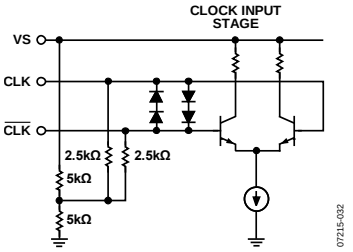


Figure 46. CLK Equivalent Input Circuit

The CLK/$\overline{CLK}$ input can be used either as a distribution only input (with the PLL off) or as a feedback input for an external VCO/VCXO using the internal PLL when the internal VCO is not used. These inputs are also used as a feedback path for the external zero delay mode.

Holdover Mode

The AD9520-2 PLL has a holdover function. Holdover mode allows the VCO to maintain a relatively constant frequency even though there is no reference clock. This function is useful when the PLL reference clock is lost. Holdover is implemented by placing the charge pump in a high impedance state. Without this function, the charge pump is placed into a constant pump-up or pump-down state, resulting in a massive VCO frequency shift. Because the charge pump is placed in a high impedance state, any leakage that occurs at the charge pump output or the VCO tuning node causes a drift of the VCO frequency. This drift can be mitigated by using a loop filter that contains a large capacitive component because this drift is limited by the current leakage induced slew rate (I_{LEAK}/C) of the VCO control voltage.

Both a manual holdover mode, using the $\overline{SYNC}$ pin, and an automatic holdover mode are provided. To use either function, the holdover function must be enabled (Register 0x01D[0]).

Manual/External Holdover Mode

A manual holdover mode can be enabled that allows the user to place the charge pump into a high impedance state when the $\overline{SYNC}$ pin is asserted low. This operation is edge sensitive, not level sensitive. The charge pump enters a high impedance state immediately. To take the charge pump out of a high impedance state, take the $\overline{SYNC}$ pin high. The charge pump then leaves the high impedance state synchronously with the next PFD rising edge from the reference clock. This prevents extraneous charge pump events from occurring during the time between $\overline{SYNC}$ going high and the next PFD event. This also means that the charge pump stays in a high impedance state if no reference clock is present.

The B counter (in the N divider) is reset synchronously with the charge pump, leaving the high impedance state on the reference path PFD event. This helps align the edges out of the R and N dividers for faster settling of the PLL. Because the prescaler is not reset, this feature works best when the B and R numbers are close, resulting in a smaller phase difference for the loop to settle out.

When using this mode, set the channel dividers to ignore the $\overline{SYNC}$ pin (at least after an initial $\overline{SYNC}$ event). If the dividers are not set to ignore the $\overline{SYNC}$ pin, the distribution outputs turn off when $\overline{SYNC}$ is taken low to put the part into holdover mode. The channel divider ignore SYNC function is programmed in Bit 6 of Register 0x191, Register 0x194, Register 0x197, and Register 0x19A for Channel Divider 0, Channel Divider 1, Channel Divider 2, and Channel Divider 3, respectively.

Automatic/Internal Holdover Mode

When enabled, this function automatically places the charge pump into a high impedance state when the loop loses lock. The assumption is that the only reason the loop loses lock is due to the PLL losing the reference clock; therefore, the holdover function puts the charge pump into a high impedance state to maintain the VCO frequency as close as possible to the original frequency before the reference clock disappeared.

The holdover function senses the logic level of the LD pin as a condition to enter holdover. The signal at LD can be from the DLD, ALD, or current source LD mode. The LD comparator can be disabled (Register 0x01D[3]), which causes the holdover function to always sense LD as being high. If DLD is used, it is possible for the DLD signal to chatter while the PLL is reacquiring lock. The holdover function may retrigger, thereby preventing the holdover mode from terminating. Use of the current source lock detect mode is recommended to avoid this situation (see the Current Source Digital Lock Detect (CSDLD) section).

When in holdover mode, the charge pump stays in a high impedance state as long as there is no reference clock present.

As in the external holdover mode, the B counter (in the N divider) is reset synchronously with the charge pump leaving the high impedance state on the reference path PFD event. This helps align the edges out of the R and N dividers for faster settling of the PLL and reduces frequency errors during settling. Because the prescaler is not reset, this feature works best when the B and R numbers are close because this results in a smaller phase difference for the loop to settle out.

After leaving holdover, the loop then reacquires lock, and the LD pin must go high (if Register 0x01D[3] = 1b) before it can reenter holdover (CP high impedance).

The holdover function always responds to the state of the currently selected reference (Register 0x01C). If the loop loses lock during a reference switchover (see the Reference Switchover section), holdover is triggered briefly until the next reference clock edge at the PFD.

A flowchart of the automatic/internal holdover function operation is shown in Figure 47.

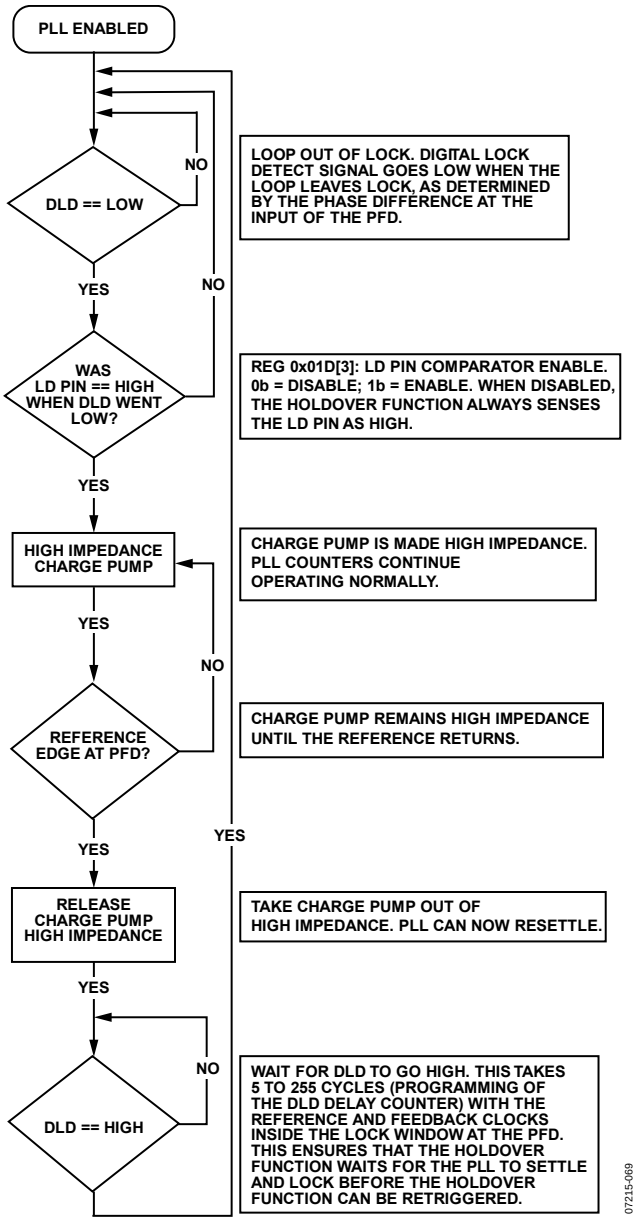


Figure 47. Flowchart of Automatic/Internal Holdover Mode

The following registers affect the automatic/internal holdover function:

- Register 0x018[6:5]—lock detect counter. This changes how many consecutive PFD cycles with edges inside the lock detect window are required for the DLD indicator to indicate lock. This impacts the time required before the LD pin can begin to charge as well as the delay from the end of a holdover event until the holdover function can be reengaged.
- Register 0x018[3]—disable digital lock detect. This bit must be set to 0b to enable the DLD circuit. Automatic/internal holdover does not operate correctly without the DLD function enabled.
- Register 0x01A[5:0]—lock detect pin control. Set these bits to 000100b to program the current source lock detect mode if using the LD pin comparator. Load the LD pin with a capacitor of an appropriate value.
- Register 0x01D[3]—LD pin comparator enable. 1b = enable; 0b = disable. When disabled, the holdover function always senses the LD pin as high.
- Register 0x01D[1]—external holdover control.
- Register 0x01D[0]—holdover enable. If holdover is disabled, both external- and automatic/ internal holdover are disabled.

In the following example, automatic holdover is configured with

- Automatic reference switchover, prefer REF1.
- Digital lock detect: five PFD cycles, high range window.
- Automatic holdover using the LD pin comparator.

The following registers are set (in addition to the normal PLL registers):

- Register 0x018[6:5] = 00b; lock detect counter = five cycles.
- Register 0x018[4] = 0b; digital lock detect window = high range.
- Register 0x018[3] = 1b; disable DLD normal operation.
- Register 0x01A[5:0] = 000100b; program LD pin control to current source lock detect mode.
- Register 0x01C[4] = 1b; enable automatic switchover.
- Register 0x01C[3] = 0b; prefer REF1.
- Register 0x01C[2:1] = 11b; enable REF1 and REF2 input buffers.
- Register 0x01D[3] = 1b; enable LD pin comparator.
- Register 0x01D[1] = 0b; disable external holdover mode and use automatic/internal holdover mode.
- Register 0x01D[0] = 1b; enable holdover.

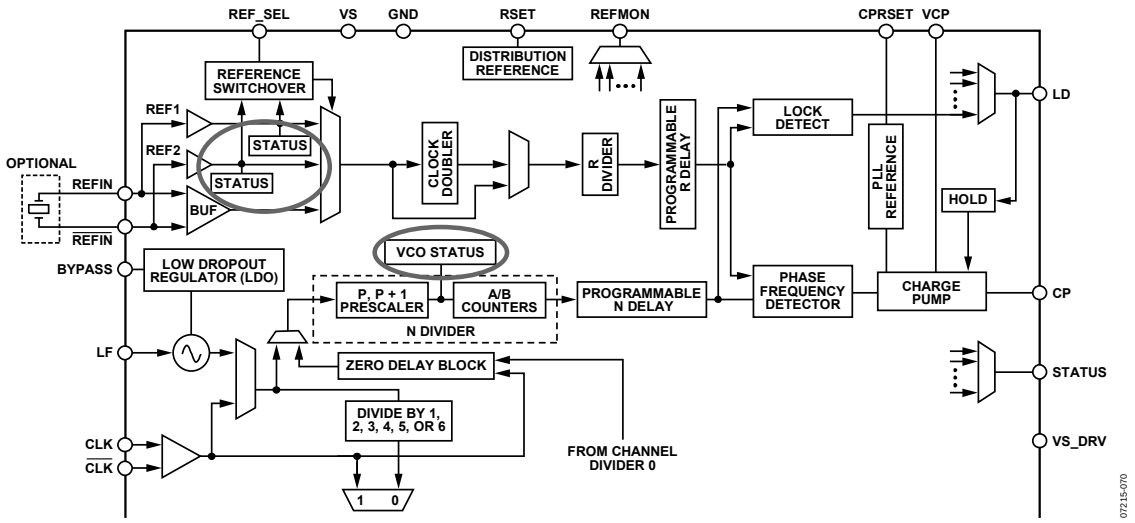


Figure 48. Reference and VCO/CLK Frequency Status Monitors

Frequency Status Monitors

The AD9520-2 contains three frequency status monitors that are used to indicate if the PLL reference (or references in the case of single-ended mode) and the VCO/CLK input have fallen below a threshold frequency. Note that the VCO frequency monitor becomes a CLK input frequency monitor if the CLK input is selected instead of the internal VCO. Figure 48 shows the location of the frequency status monitors in the PLL.

The PLL reference monitors have two threshold frequencies: normal and extended (see Table 17). The reference frequency monitor thresholds are set in Register 0x01A[6].

VCO Calibration

The AD9520-2 on-chip VCO must be calibrated to ensure proper operation over process and temperature. The VCO calibration is controlled by a calibration controller running off a divided REFIN clock. The calibration requires that the PLL be set up properly to lock the PLL loop and that the REFIN clock be present. The REFIN clock must come from a stable source external to the AD9520-2.

VCO calibration can be performed two ways: automatically at power-up and manually. Automatic VCO calibration occurs when the EEPROM is set to automatically load the preprogrammed values in the EEPROM and then automatically calibrate the VCO. For the automatic calibration to complete, a valid reference must be provided at power-up. If no valid reference is provided, the user must calibrate the VCO manually.

During the first initialization after a power-up or a reset of the AD9520-2, a manual VCO calibration sequence is initiated by setting Register 0x018[0] = 1b. This can be done as part of the initial setup before executing an update all registers operation (IO_UPDATE, Register 0x232[0] = 1b).

Subsequent to the initial setup, a VCO calibration sequence is initiated by resetting Register 0x018[0] = 0b, executing an IO_UPDATE, setting Register 0x018[0] = 1b, and executing another IO_UPDATE. A readback bit (Register 0x01F[6]) indicates when VCO calibration is finished by returning a logic true (that is, 1b).

The sequence of operations for the VCO calibration follows:

1. Program the PLL registers to the proper values for the PLL loop. Note that the VCO divider (Register 0x1E0[2:0]) must not be set to static during VCO calibration.
2. Ensure that the input reference signal is present.
3. For initial setting of the registers after a power-up or reset, initiate a VCO calibration by setting Register 0x018[0] = 1b.
4. Subsequently, whenever a calibration is desired, set Register 0x018[0] = 0b, update registers; and then set Register 0x018[0] = 1b, update registers.
5. A SYNC operation is initiated internally, causing the outputs to go to a static state determined by normal SYNC function operation.
6. VCO is calibrated to the desired setting for the requested VCO frequency.
7. Internally, the SYNC signal is released, allowing outputs to continue clocking.
8. The PLL loop is closed.
9. The PLL locks.

A SYNC is executed during the VCO calibration; therefore, the outputs of the AD9520-2 are held static during the calibration, which prevents unwanted frequencies from being produced. However, at the end of a VCO calibration, the outputs may resume clocking before the PLL loop is completely settled.

The VCO calibration clock divider is set as shown in Table 54 (Register 0x018[2:1]). The calibration divider divides the PFD frequency (reference frequency divided by R) down to the calibration clock. The calibration occurs at the PFD frequency divided by the calibration divider setting. Lower VCO calibration clock frequencies result in longer times for a calibration to be done.

The VCO calibration clock frequency is given by

$$f_{CAL_CLOCK} = f_{REFIN}/(R \times cal_div)$$

where:
f_{REFIN} is the frequency of the REFIN signal.
R is the value of the R counter.
cal_div is the division set for the VCO calibration divider (Register 0x018[2:1]).

Choose a calibration divider such that the calibration frequency is less than 6.25 MHz. Table 30 shows the appropriate value for the calibration divider.

Table 30. VCO Calibration Divider Values for Different Phase Detector Frequencies

PFD Rate (MHz)	Recommended VCO Calibration Divider
<12	Any
12 to 25	4, 8, 16
25 to 50	8, 16
50 to 100	16

The VCO calibration takes 4400 calibration clock cycles. Therefore, the VCO calibration time in PLL reference clock cycles is given by

Time to Calibrate VCO =

4400 × *R* × *cal_div PLL Reference Clock Cycles*

Table 31. Example Time to Complete a VCO Calibration with Different f_{REFIN} Frequencies

f_{REFIN} (MHz)	R Divider	PFD	Time to Calibrate VCO
100	1	100 MHz	88 µs
10	10	1 MHz	8.8 ms
10	100	100 kHz	88 ms

A VCO calibration must be manually initiated, which allows for flexibility in deciding what order to program registers and when to initiate a calibration, instead of having it occur every time the values of certain PLL registers change. For example, this allows for the VCO frequency to be changed by small amounts without having an automatic calibration occur each time; this should be done with caution and only when the user knows the VCO control voltage will not exceed the nominal best performance limits. For example, a few 100 kHz steps are fine, but a few MHz may not be.

In addition, because the calibration procedure results in rapid changes in the VCO frequency, the distribution section is automatically placed in SYNC until the calibration is finished. Therefore, this temporary loss of outputs must be expected.

A VCO calibration should be initiated in the following conditions:

- After changing any of the PLL R, P, B, and A divider settings or after a change in the PLL reference clock frequency. This, in effect, means any time a PLL register or reference clock is changed such that a different VCO frequency results.
- When system calibration is desired. The VCO is designed to operate properly over extremes of temperature even when it is first calibrated at the opposite extreme. However, a VCO calibration can be initiated at any time, if desired.

ZERO DELAY OPERATION

Zero delay operation aligns the phase of the output clocks with the phase of the external PLL reference input. There are two zero delay modes on the AD9520-2: internal and external.

Internal Zero Delay Mode

The internal zero delay function of the AD9520-2 is achieved by feeding the output of Channel Divider 0 back to the PLL N divider. In Figure 49, the change in signal routing for internal zero delay mode is shown in blue.

Set Register 0x01E[2:1] = 01b to select internal zero delay mode. In the default internal zero delay mode, the output of Channel Divider 0 is routed back to the PLL (N divider) through MUX3 and MUX1 (feedback path shown in blue in Figure 49). The PLL synchronizes the phase/edge of the output of Channel Divider 0 with the phase/edge of the reference input. External zero delay mode must be used if Channel Divider 1, Channel Divider 2, or Channel Divider 3 is to be used for zero delay feedback. This is accomplished by changing the value in Register 0x01E[4:3].

Because the channel dividers are synchronized to each other, the outputs of the channel divider are synchronous with the reference input. Both the R delay and the N delay inside the PLL can be programmed to compensate for the propagation delay from the output drivers and PLL components to minimize the phase offset between the clock output and the reference input to achieve zero delay.

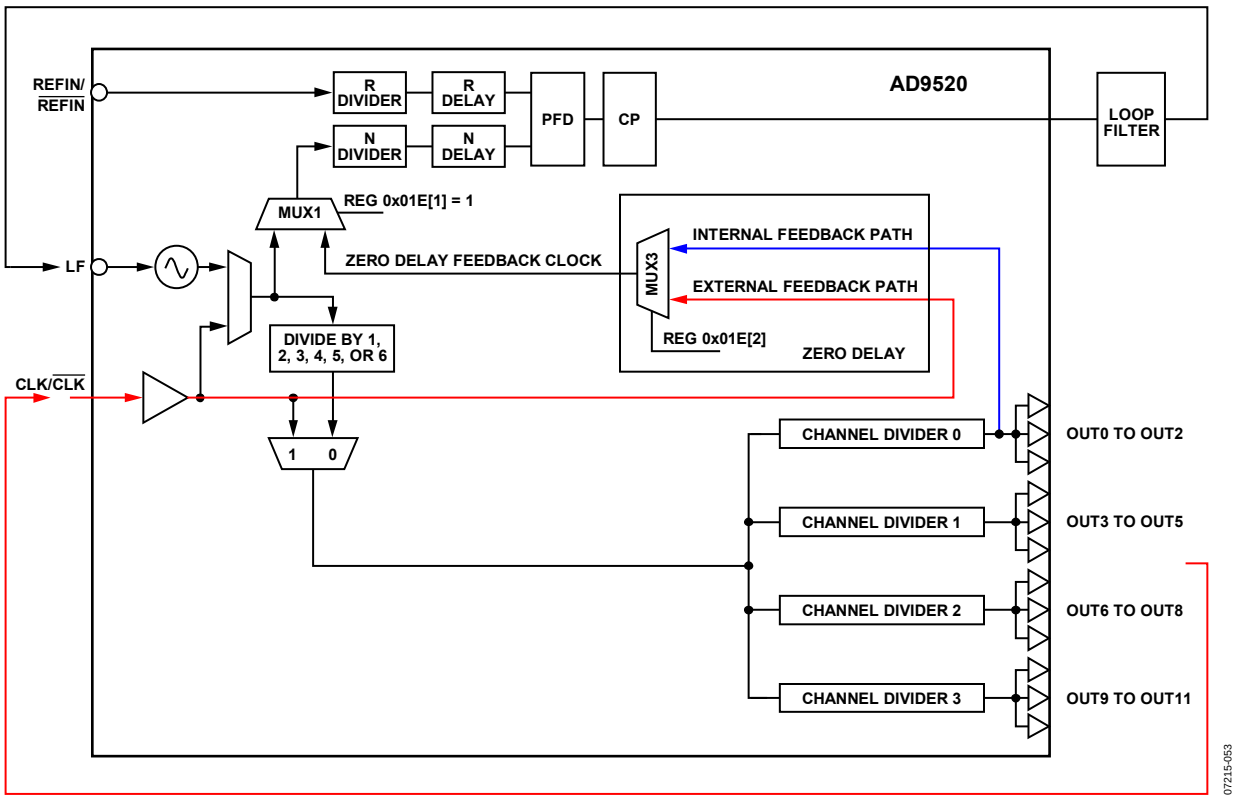


Figure 49. Zero Delay Function

External Zero Delay Mode

The external zero delay function of the AD9520-2 is achieved by feeding one clock output back to the CLK input and ultimately back to the PLL N divider. In Figure 49, the change in signal routing for external zero delay mode is shown in red.

Set Register 0x01E[2:1] = 11b to select external zero delay mode. In external zero delay mode, one of the twelve output clocks (OUT0 to OUT11) can be routed back to the PLL (N divider) through the CLK/$\overline{\text{CLK}}$ pins and through MUX3 and MUX1. This feedback path is shown in red in Figure 49.

For VCO calibration to work correctly, the user must specify which channel divider is used for external zero delay mode. Channel Divider 0 is the default. Change the value in Register 0x01E[4:3] to select Channel Divider 1, Channel Divider 2, or Channel Divider 3 for zero delay feedback.

The PLL synchronizes the phase/edge of the feedback output clock with the phase/edge of the reference input. Because the channel dividers are synchronized to each other, the clock outputs are synchronous with the reference input. Both the R delay and the N delay inside the PLL can be programmed to compensate for the propagation delay from the PLL components to minimize the phase offset between the feedback clock and the reference input.

CLOCK DISTRIBUTION

A clock channel consists of three LVPECL clock outputs or six CMOS clock outputs that share a common divider. A clock output consists of the drivers that connect to the output pins. The clock outputs have either LVPECL or CMOS at the pins.

The AD9520-2 has four clock channels. Each channel has its own programmable divider that divides the clock frequency applied to its input. The channel dividers can divide by any integer from 1 to 32.

The AD9520-2 features a VCO divider that divides the VCO output by 1, 2, 3, 4, 5, or 6 before going to the individual channel dividers.

The VCO divider has two purposes. The first is to limit the maximum input frequency of the channel dividers to 1.6 GHz. The other is to allow the AD9520-2 to generate even lower frequencies than would be possible with only a simple post divider. External clock signals connected to the CLK input can also use the VCO divider.

The channel dividers allow for a selection of various duty cycles, depending on the currently set division. That is, for any specific division, D, the output of the divider can be set to high for N + 1 input clock cycles and low for M + 1 input clock cycles (where D = N + M + 2). For example, a divide-by-5 can be high for one divider input cycle and low for four cycles, or a divide-by-5 can be high for three divider input cycles and low for two cycles. Other combinations are also possible.

The channel dividers include a duty-cycle correction function that can be disabled. In contrast to the selectable duty cycle just described, this function can correct a non-50% duty cycle caused by an odd division. However, this requires that the division be set by M = N + 1.

In addition, the channel dividers allow a coarse phase offset or delay to be set. Depending on the division selected, the output can be delayed by up to 15 input clock cycles. For example, if the frequency at the input of the channel divider is 1 GHz, the channel divider output can be delayed by up to 15 ns. The divider outputs can also be set to start high or to start low.

Operation Modes

There are three clock distribution operating modes, and these are shown in Figure 50. One of these modes uses the internal VCO, whereas the other two modes bypass the internal VCO and use the signal provided on the CLK/$\overline{\text{CLK}}$ pins.

In Mode 0 (internal VCO mode), there are two signal paths available. In the first path, the VCO signal is sent to the VCO divider and then to the individual channel dividers. In the second path, the user bypasses the VCO and channel dividers and sends the VCO signal directly to the drivers.

When CLK is selected as the source, it is not necessary to use the VCO divider if the CLK frequency is less than the maximum channel divider input frequency (1600 MHz); otherwise, the VCO divider must be used to reduce the frequency going to the channel dividers.

Table 32 shows how the VCO, CLK, and VCO divider are selected. Register 0x1E1[1:0] selects the channel divider source and determines whether the VCO divider is used. It is not possible to select the VCO without using the VCO divider.

Table 32. Operation Modes

	Register 0x1E1			
Mode	Bit 1	Bit 0	Channel Divider Source	VCO Divider
2	0	0	CLK	Used
1	0	1	CLK	Not used
0	1	0	VCO	Used
	1	1	Not allowed	Not allowed

CLK or VCO Direct-to-LVPECL Outputs

It is possible to connect either the internal VCO or the CLK (whichever is selected as the input to the VCO divider) directly to the LVPECL outputs. This configuration can pass frequencies up to the maximum frequency of the VCO directly to the LVPECL outputs. However, the LVPECL outputs may not be able to meet the V_{OD} specification in Table 4 at the highest frequencies.

Either the internal VCO or the CLK can be selected as the source for the direct-to-output signal routing. To connect the LVPECL outputs directly to the internal VCO or CLK, the VCO divider must be selected as the source to the distribution section, even if no channel uses it.

Table 33. Routing VCO Divider Input Directly to the Outputs

Register Setting	Selection
0x1E1[1:0] = 00b	CLK is the source; VCO divider selected
0x1E1[1:0] = 10b	VCO is the source; VCO divider selected
0x192[1] = 1b	Direct-to-output OUT0, OUT1, OUT2
0x195[1] = 1b	Direct-to-output OUT3, OUT4, OUT5
0x198[1] = 1b	Direct-to-output OUT6, OUT7, OUT8
0x19B[1] = 1b	Direct-to-output OUT9, OUT10, OUT11

Clock Frequency Division

The total frequency division is a combination of the VCO divider (when used) and the channel divider. When the VCO divider is used, the total division from the VCO or CLK to the output is the product of the VCO divider (1, 2, 3, 4, 5, and 6) and the division of the channel divider. Table 34 shows how the frequency division for a channel is set.

Table 34. Frequency Division

CLK or VCO Selected	VCO Divider Setting[1]	Channel Divider Setting	Direct-to-Output Setting	Resulting Frequency Division
CLK or VCO input	1 to 6	Don't care	Enable	1
CLK or VCO input	1 to 6	2 to 32	Disable	(1 to 6) × (2 to 32)
CLK or VCO input	2 to 6	Bypass	Disable	(2 to 6) × (1)
CLK or VCO input	1	Bypass	Disable	Output static (illegal state)
CLK (internal VCO off)	VCO divider bypassed	Bypass	Don't care	1
CLK (internal VCO off)	VCO divider bypassed	2 to 32	Don't care	2 to 32

[1] The bypass VCO divider (Register 0x1E1[0] = 1b) is not the same as VCO divider = 1 (divide-by-1).

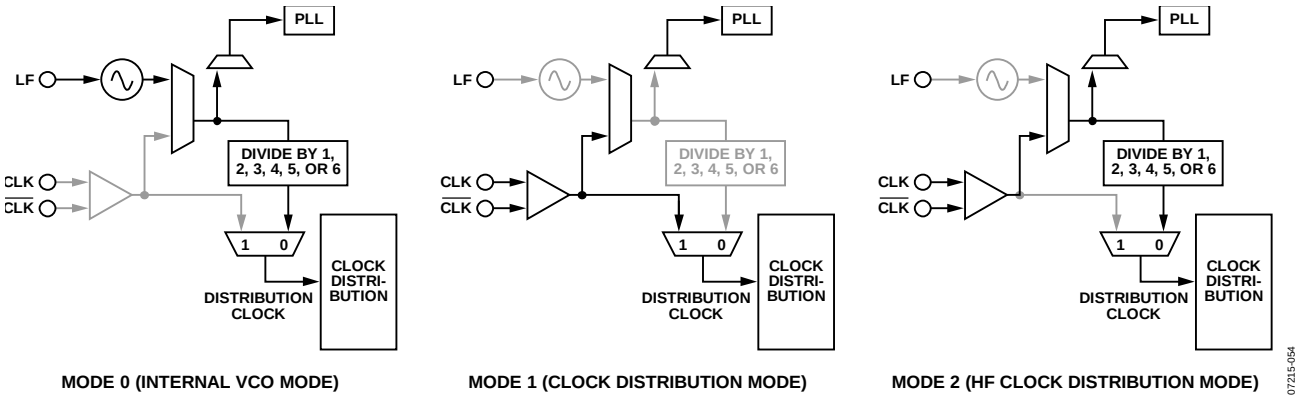


Figure 50. Simplified Diagram of the Three Clock Distribution Operation Modes

The channel dividers feeding the output drivers contain one 2-to-32 frequency divider. This divider provides for division-by-1 to division-by-32. Division-by-1 is accomplished by bypassing the divider. The dividers also provide for a programmable duty cycle, with optional duty-cycle correction when the divide ratio is odd. A phase offset or delay in increments of the input clock cycle is selectable. The channel dividers operate with a signal of up to 1600 MHz at their inputs across all channel divider ratios. The features and settings of the dividers are selected by programming the appropriate setup and control registers (see Table 50 through Table 61).

VCO Divider

The VCO divider provides frequency division between the internal VCO or the external CLK input and the clock distribution channel dividers. The VCO divider can be set to divide by 1, 2, 3, 4, 5, or 6 (see Register 0x1E0[2:0]). However, when the VCO divider is set to 1, none of the channel output dividers can be bypassed.

The VCO divider can also be set to static, which is useful for applications where the only desired output frequency is the VCO frequency. Making the VCO divider static increases the wide band spurious-free dynamic range (SFDR). If the VCO divider is static during VCO calibration, there is no output signal.

Therefore, it is important to calibrate the VCO with the VCO divider set to a nonstatic value during VCO calibration, and then set the VCO divider to static when VCO calibration is complete.

The recommended alternative to achieving the same SFDR performance is to set the VCO divider to 1 and enable VCO direct mode. This allows the user to program the EEPROM with the desired values and does not require further action after the VCO calibration is complete.

Channel Dividers

A channel divider drives each group of three LVPECL outputs. There are four channel dividers (0, 1, 2, and 3) driving 12 LVPECL outputs (OUT0 to OUT11). Table 35 lists the bit locations used for setting the division and other functions of these dividers. The division is set by the M and N values. The divider can be bypassed (equivalent to divide-by-1, divider circuit is powered down) by setting the bypass bit. The duty-cycle correction can be enabled or disabled according to the setting of the disable Divider x DCC bits.

Table 35. Setting D_X for the Output Dividers

Divider	Low Cycles, M Value Bits	High Cycles, N Value Bits	Bypass Bits	Disable Divider x DCC Bits
0	0x190[7:4]	0x190[3:0]	0x191[7]	0x192[0]
1	0x193[7:4]	0x193[3:0]	0x194[7]	0x195[0]
2	0x196[7:4]	0x196[3:0]	0x197[7]	0x198[0]
3	0x199[7:4]	0x199[3:0]	0x19A[7]	0x19B[0]

Channel Divider Maximum Frequency

The maximum frequency at which all features of the channel divider are guaranteed to work is 1.6 GHz, this is the number that appears elsewhere in the datasheet. The maximum frequency at which all features of the channel divider are guaranteed to work is 1.6 GHz; this is the number that appears elsewhere in the data sheet. However, if the divide-by-3 and divide-by-17 settings are avoided, the maximum channel divider input frequency is 2 GHz.

Channel Frequency Division (0, 1, 2, or 3)

For each channel (where the channel number (x) is 0, 1, 2, or 3), the frequency division, D_X, is set by the values of M and N (four bits each, representing Decimal 0 to Decimal 15), where

Number of Low Cycles = *M* + 1
Number of High Cycles = *N* + 1

The high and low cycles are the cycles of the clock signal that are currently routed to the input of the channel dividers (VCO divider out or CLK).

When a divider is bypassed, $D_X = 1$.

Otherwise, $D_X = (N + 1) + (M + 1) = N + M + 2$. This allows each channel divider to divide by any integer from 2 to 32.

Duty Cycle and Duty-Cycle Correction

The duty cycle of the clock signal at the output of a channel is a result of some or all of the following conditions:

- M and N values for the channel
- DCC enabled/disabled
- VCO divider enabled/bypassed
- CLK input duty cycle (note that the internal VCO has a 50% duty cycle)

The DCC function is enabled, by default, for each channel divider. However, the DCC function can be disabled individually for each channel divider by setting the disable Divider x DCC bit for that channel.

Certain M and N values for a channel divider result in a non-50% duty cycle. A non-50% duty cycle can also result in an even division, if $M \neq N$. The duty-cycle correction function automatically corrects non-50% duty cycles at the channel divider output to 50% duty cycle.

Duty-cycle correction requires the following channel divider conditions:

- An even division must be set as M = N.
- An odd division must be set as M = N + 1.

When not bypassed or corrected by the DCC function, the duty cycle of each channel divider output is the numerical value of (N + 1)/(N + M + 2), expressed as a percent.

Table 36 to Table 39 show the output duty cycle for various configurations of the channel divider and VCO divider.

Table 36. Channel Divider Output Duty Cycle with VCO Divider ≠ 1; Input Duty Cycle Is 50%

	D_X	Output Duty Cycle	
VCO Divider	**N + M + 2**	**Disable Divider x DCC = 1b**	**Disable Divider x DCC = 0b**
Even	Channel divider bypassed	50%	50%
Odd = 3	Channel divider bypassed	33.3%	50%
Odd = 5	Channel divider bypassed	40%	50%
Even, odd	Even	(N + 1)/(N + M + 2)	50%, requires M = N
Even, odd	Odd	(N + 1)/(N + M + 2)	50%, requires M = N + 1

Table 37. Channel Divider Output Duty Cycle with VCO Divider ≠ 1; Input Duty Cycle Is X%

	D_X	Output Duty Cycle	
VCO Divider	**N + M + 2**	**Disable Divider x DCC = 1b**	**Disable Divider x DCC = 0b**
Even	Channel divider bypassed	50%	50%
Odd = 3	Channel divider bypassed	33.3%	(1 + X%)/3
Odd = 5	Channel divider bypassed	40%	(2 + X%)/5
Even	Even	(N + 1)/(N + M + 2)	50%, requires M = N
Even	Odd	(N + 1)/(N + M + 2)	50%, requires M = N + 1
Odd = 3	Even	(N + 1)/(N + M + 2)	50%, requires M = N
Odd = 3	Odd	(N + 1)/(N + M + 2)	(3N + 4 + X%)/(6N + 9), requires M = N + 1
Odd = 5	Even	(N + 1)/(N + M + 2)	50%, requires M = N
Odd = 5	Odd	(N + 1)/(N + M + 2)	(5N + 7 + X%)/(10N + 15), requires M = N + 1

Table 38. Channel Divider Output Duty Cycle When the VCO Divider Is Enabled and Set to 1

Input Clock Duty Cycle	D_X	Output Duty Cycle	
	N + M + 2	**Disable Divider x DCC = 1b**	**Disable Divider x DCC = 0b**
Any	Even	(N + 1)/(M + N + 2)	50%, requires M = N
50%	Odd	(N + 1)/(M + N + 2)	50%, requires M = N + 1
X%	Odd	(N + 1)/(M + N + 2)	(N + 1 + X%)/(2 × N + 3), requires M = N + 1

The channel divider must be enabled when the VCO divider = 1.

Table 39. Channel Divider Output Duty Cycle When the VCO Divider Is Bypassed

Input Clock Duty Cycle	D_X	Output Duty Cycle	
	N + M + 2	**Disable Divider x DCC = 1b**	**Disable Divider x DCC = 0b**
Any	Channel divider bypassed	Same as input duty cycle	Same as input duty cycle
Any	Even	(N + 1)/(M + N + 2)	50%, requires M = N
50%	Odd	(N + 1)/(M + N + 2)	50%, requires M = N + 1
X%	Odd	(N + 1)/(M + N + 2)	(N + 1 + X%)/(2 × N + 3), requires M = N + 1

The internal VCO has a duty cycle of 50%. Therefore, when the VCO is connected directly to the output, the duty cycle is 50%. If the CLK input is routed directly to the output, the duty cycle of the output is the same as the CLK input.

Phase Offset or Coarse Time Delay

Each channel divider allows for a phase offset or a coarse time delay to be programmed by setting register bits (see Table 40). These settings determine the number of cycles (successive rising edges) of the channel divider input frequency by which to offset, or delay, the rising edge of the output of the divider. This delay is with respect to a nondelayed output (that is, with a phase offset of zero). The amount of the delay is set by five bits loaded into the phase offset (PO) register plus the start high (SH) bit for each channel divider.

When the start high bit is set, the delay is also affected by the number of low cycles (M) programmed for the divider.

The SYNC function must be used to make phase offsets effective (see the Synchronizing the Outputs—SYNC Function section).

Table 40. Setting Phase Offset and Division

Divider	Start High (SH) Bits	Phase Offset (PO) Bits	Low Cycles, M Value Bits	High Cycles, N Value Bits
0	0x191[4]	0x191[3:0]	0x190[7:4]	0x190[3:0]
1	0x194[4]	0x194[3:0]	0x193[7:4]	0x193[3:0]
2	0x197[4]	0x197[3:0]	0x196[7:4]	0x196[3:0]
3	0x19A[4]	0x19A[3:0]	0x199[7:4]	0x199[3:0]

Note that the value stored in the register equals the number of cycles minus one. For example, Register 0x190[7:4] = 0001b equals two low cycles (M = 2) for Divider 0.

Let
Δ_t = delay (in seconds).
Δ_c = delay (in cycles of clock signal at input to D_X).
T_X = period of the clock signal at the input of the divider, D_X (in seconds).
Φ =
16 × SH[4] + 8 × PO[3] + 4 × PO[2] + 2 × PO[1] + 1 × PO[0].

The channel divide-by is set as N = high cycles and M = low cycles.

Case 1

For $\Phi \leq 15$,
$\Delta_t = \Phi \times T_X$
$\Delta_c = \Delta_t / T_X = \Phi$

Case 2

For $\Phi \geq 16$,
$\Delta_t = (\Phi - 16 + M + 1) \times T_X$
$\Delta_c = \Delta_t / T_X$

By giving each divider a different phase offset, output-to-output delays can be set in increments of the channel divider input clock cycle. Figure 51 shows the results of setting such a coarse offset between outputs.

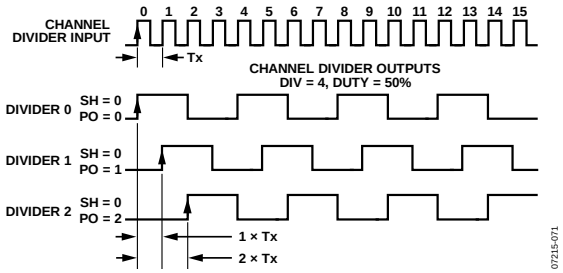


Figure 51. Effect of Coarse Phase Offset (or Delay)

Synchronizing the Outputs—SYNC Function

The AD9520-2 clock outputs can be synchronized to each other. Outputs can be individually excluded from synchronization. Synchronization consists of setting the nonexcluded outputs to a preset set of static conditions. These conditions include the divider ratio and phase offsets for a given channel divider. This allows the user to specify different divide ratios and phase offsets for each of the four channel dividers. Releasing the $\overline{\text{SYNC}}$ pin allows the outputs to continue clocking with the preset conditions applied.

Synchronization of the outputs is executed in the following ways:

- The $\overline{\text{SYNC}}$ pin is forced low and then released (manual sync).
- By setting and then resetting any one of the following three bits: the soft SYNC bit (Register 0x230[0]), the soft reset bit (Register 0x000[5] [mirrored]), and the power-down distribution reference bit (Register 0x230[1]).
- Synchronization of the outputs can be executed as part of the chip power-up sequence.
- The $\overline{\text{RESET}}$ pin is forced low and then released (chip reset).
- The $\overline{\text{PD}}$ pin is forced low, then released (chip power-down).
- When a VCO calibration is completed, an internal SYNC signal is automatically asserted at the beginning and released upon the completion of a VCO calibration.

The most common way to execute the SYNC function is to use the $\overline{\text{SYNC}}$ pin to perform a manual synchronization of the outputs. This requires a low going signal on the $\overline{\text{SYNC}}$ pin, which is held low and then released when synchronization is desired.

The timing of the SYNC operation is shown in Figure 52 (using the VCO divider) and in Figure 53 (the VCO divider is not used). There is an uncertainty of up to one cycle of the clock at the input to the channel divider due to the asynchronous nature of the SYNC signal with respect to the clock edges inside the AD9520-2.

The pipeline delay from the $\overline{\text{SYNC}}$ rising edge to the beginning of the synchronized output clocking is between 14 cycles and 15 cycles of clock at the channel divider input, plus either one cycle of the VCO divider input (see Figure 52), or one cycle of the channel divider input (see Figure 53), depending on whether the VCO divider is used. Cycles are counted from the rising edge of the signal. In addition, there is an additional 1.2 ns (typical) delay from the SYNC signal to the internal synchronization logic, as well as the propagation delay of the output driver. The driver propagation delay is approximately 100 ps for the LVPECL driver and approximately 1.5 ns for the CMOS driver.

Another common way to execute the SYNC function is by setting and resetting the soft SYNC bit at Register 0x230[0]. Both setting and resetting of the soft SYNC bit require an update all registers (Register 0x232[0] = 1b) operation to take effect.

A SYNC operation brings all outputs that have not been excluded (by the ignore SYNC bit) to a preset condition before allowing the outputs to begin clocking in synchronicity. The preset condition takes into account the settings in each of the channel's start high bit and its phase offset. These settings govern both the static state of each output when the SYNC operation is happening and the state and relative phase of the outputs when they begin clocking again upon completion of the SYNC operation. Between outputs and after synchronization, this allows for the setting of phase offsets.

The AD9520-2 differential LVPECL outputs are four groups of three, sharing a channel divider per triplet. In the case of CMOS, each LVPECL differential pair can be configured as two single-ended CMOS outputs. The synchronization conditions apply to all of the drivers that belong to that channel divider.

Each channel (a divider and its outputs) can be excluded from any SYNC operation by setting the ignore SYNC bit of the channel. Channels that are set to ignore SYNC (excluded channels) do not set their outputs static during a SYNC operation, and their outputs are not synchronized with those of the included channels.

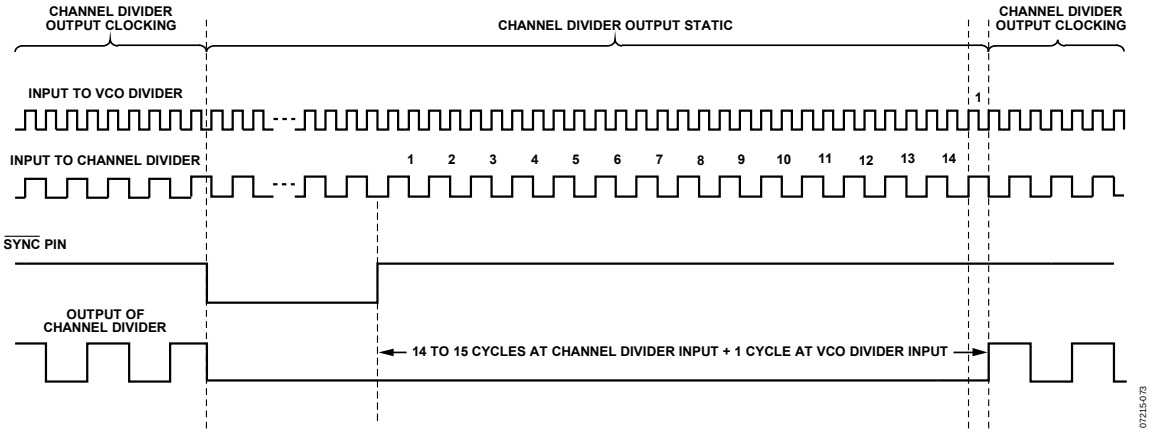


Figure 52. SYNC Timing Pipeline Delay When the VCO Divider Is Used—CLK or VCO Is Input

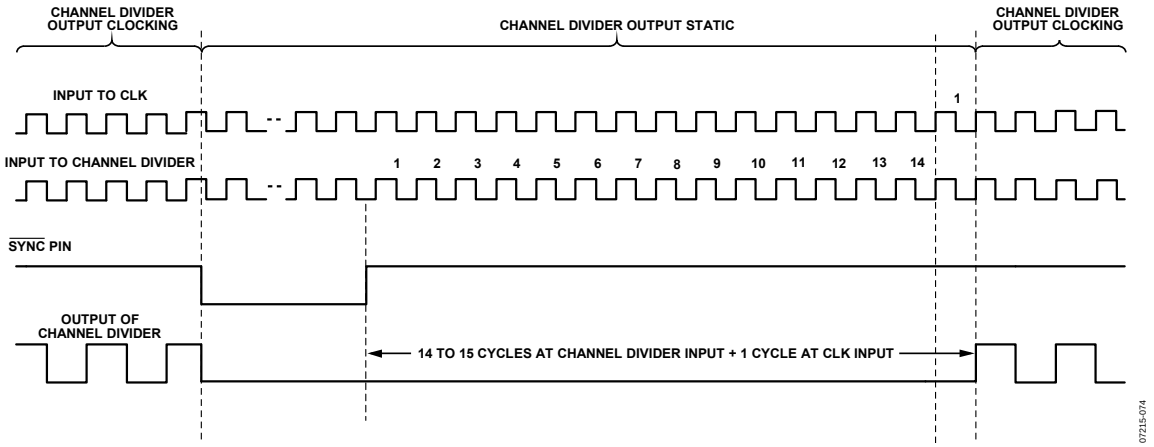


Figure 53. SYNC Timing Pipeline Delay When the VCO Divider Is Not Used—CLK Input Only

LVPECL Output Drivers

The LVPECL differential voltage (V_{OD}) is selectable (from ~400 mV to 960 mV, see Bit 1 and Bit 2 in Register 0x0F0 to Register 0x0FB). The LVPECL outputs have dedicated pins for power supply (VS_DRV), allowing a separate power supply to be used. V_{S_DRV} can be set to either 2.5 V or 3.3 V.

The LVPECL output polarity can be set as noninverting or inverting, which allows for the adjustment of the relative polarity of outputs within an application without requiring a board layout change. Each LVPECL output can be powered down or powered up as needed. Because of the architecture of the LVPECL output stages, there is the possibility of electrical overstress and breakdown under certain power-down conditions.

For this reason, the LVPECL outputs have two power-down modes: total power-down and safe power-down.

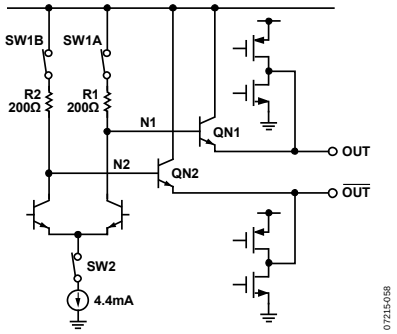


Figure 54. LVPECL Output Simplified Equivalent Circuit

In total power-down mode, all output drivers are shut off simultaneously. This mode must not be used if there is an external voltage bias network (such as Thevenin equivalent termination) on the output pins that causes a dc voltage to appear at the powered down outputs. However, total power-down mode is allowed when the LVPECL drivers are terminated using only pull-down resistors. The total power-down mode is activated by setting Register 0x230[1].

The primary power-down mode is the safe power-down mode. This mode continues to protect the output devices while powered down. There are three ways to activate safe power-down mode: individually set the power-down bit for each driver, power down an individual output channel (all of the drivers associated with that channel are powered down automatically), and activate sleep mode.

CMOS Output Drivers

The user can also individually configure each LVPECL output as a pair of CMOS outputs, which provides up to 24 CMOS outputs. When an output is configured as CMOS, CMOS Output A and CMOS Output B are automatically turned on. For any given differential pair, either CMOS Output A or CMOS Output B can be turned on or off independently.

The user can also select the relative polarity of the CMOS outputs for any combination of inverting and noninverting (refer to Register 0x0F0 to Register 0x0FB).

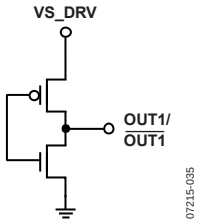


Figure 55. CMOS Equivalent Output Circuit

Each CMOS output can be powered down, as needed, to save power. The CMOS output power-down is individually controlled by the enable CMOS output bits, Bits[6:5] in Register 0x0F0 to Register 0x0FB. The CMOS driver is in tristate when it is powered down.

Note that activating a CMOS driver in the same output channel group as the LVPECL drivers may cause the LVPECL driver performance to degrade. In applications where jitter performance is critical, the user should test the desired configuration using an evaluation board, and special steps may need to be taken to ensure the desired performance.

RESET MODES

The AD9520-2 has a power-on reset (POR) and several other ways to apply a reset condition to the chip.

Power-On Reset

During chip power-up, a power-on reset pulse is issued when V_S reaches ~2.6 V (<2.8 V) and restores the chip either to the setting that is stored in the EEPROM (with the EEPROM pin = 1b) or to the on-chip setting (with the EEPROM pin = 0b). At power-on, the AD9520-2 also executes a SYNC operation approximately 50 ms after the supply reaches ~ 2.4 V, which brings the outputs into phase alignment according to the default settings. It takes ~70 ms for the outputs to begin toggling after the power-on reset pulse signal is internally generated.

Hardware Reset via the $\overline{\text{RESET}}$ Pin

$\overline{\text{RESET}}$, a hard reset (an asynchronous hard reset is executed by briefly pulling $\overline{\text{RESET}}$ low), restores the chip either to the setting stored in the EEPROM (the EEPROM pin = 1b) or to the on-chip setting (the EEPROM pin = 0b). A hard reset also executes a SYNC operation, bringing the outputs into phase alignment according to the default settings. When the EEPROM is inactive (the EEPROM pin = 0b), it takes ~2 µs for the outputs to begin toggling after $\overline{\text{RESET}}$ is issued. When the EEPROM is active (the EEPROM pin = 1b), it takes ~20 ms for the outputs to toggle after $\overline{\text{RESET}}$ is brought high.

Soft Reset via the Serial Port

The serial port control register allows for a soft reset by setting Bit 2 and Bit 5 in Register 0x000. The function of this register is determined by the state of the EEPROM pin.

When Bit 2 and Bit 5 are set and the EEPROM pin is high, the chip is restored to the settings saved in the EEPROM. When Bit 2 and Bit 5 are set and the EEPROM pin is low, the chip is restored to the on-chip defaults.

Except for the self-clearing bits, Bit 2 and Bit 5, Register 0x000 retains its previous value prior to reset. During the internal reset, the outputs hold static. However, the self-clearing operation does not complete until an additional serial port SCLK cycle occurs, and the AD9520-2 is held in reset until that happens.

Soft Reset to Settings in EEPROM when EEPROM Pin = 0b via the Serial Port

If the EEPROM pin is low, the serial port control register allows the chip to be reset to settings in EEPROM via Register 0xB02[1]. (Bit 1 is self-clearing.) This bit does not have any effect when the EEPROM pin is high. It takes ~20 ms for the outputs to begin toggling after the SOFT_EEPROM register is cleared.

POWER-DOWN MODES

Chip Power-Down via $\overline{\text{PD}}$

The AD9520-2 can be put into a power-down condition by pulling the $\overline{\text{PD}}$ pin low. Power-down turns off most of the functions and currents inside the AD9520-2. The chip remains in this power-down state until $\overline{\text{PD}}$ is brought back to logic high. When taken out of power-down mode, the AD9520-2 returns to the settings programmed into its registers prior to the power-down, unless the registers are changed by new programming while the $\overline{\text{PD}}$ pin is held low.

Powering down the chip shuts down the currents on the chip, except for the bias current necessary to maintain the LVPECL outputs in a safe shutdown mode. The LVPECL bias currents are needed to protect the LVPECL output circuitry from damage that can be caused by certain termination and load configurations when tristated. Because this is not a complete power-down, it can be called sleep mode. The AD9520-2 contains special circuitry to prevent runt pulses on the outputs when the chip is entering or exiting sleep mode.

When the AD9520-2 is in a $\overline{\text{PD}}$ power-down, the chip is in the following state:

- The PLL is off (asynchronous power-down).
- The VCO is off.
- The CLK input buffer is off, but the CLK input dc bias circuit is on.
- In differential mode, the reference input buffer is off, but the dc bias circuit is still on.
- In singled-ended mode, the reference input buffer is off, and the dc bias circuit is off.
- All dividers are off.
- All CMOS outputs are tristated.
- All LVPECL outputs are in safe off mode.
- The serial control port is active, and the chip responds to commands.

PLL Power-Down

The PLL section of the AD9520-2 can be selectively powered down. There are two PLL power-down modes set by Register 0x010[1:0]: asynchronous and synchronous.

In asynchronous power-down mode, the device powers down as soon as the registers are updated. In synchronous power-down mode, the PLL power-down is gated by the charge pump to prevent unwanted frequency jumps. The device goes into power-down on the occurrence of the next charge pump event after the registers are updated.

Distribution Power-Down

The distribution section can be powered down by writing Register 0x230[1] = 1b, which turns off the bias to the distribution section. If the LVPECL power-down mode is in normal operation (Register 0x230[1] = 0b), it is possible for a low impedance load on that LVPECL output to draw significant current during this power-down. If the LVPECL power-down mode is set to 1b, the LVPECL output is not protected from reverse bias and can be damaged under certain termination conditions.

Individual Clock Output Power-Down

Any of the clock distribution outputs can be powered down into safe power-down mode by individually writing to the appropriate registers. The register map details the individual power-down settings for each output. These settings are found in Bit 0 of Register 0x0F0 to Register 0x0FB.

Individual Clock Channel Power-Down

Any of the clock distribution channels can be powered down individually by writing to the appropriate registers. Powering down a clock channel is similar to powering down an individual driver, but it saves more power because the dividers are also powered down. Powering down a clock channel also automatically powers down the drivers connected to it. The register map details the individual power-down settings for each output channel. These settings are found in Bit 2 of Register 0x192, Register 0x195, Register 0x198, and Register 0x19B.

SERIAL CONTROL PORT

The AD9520-2 serial control port is a flexible, synchronous serial communications port that allows an easy interface with many industry-standard microcontrollers and microprocessors. The AD9520-2 serial control port is compatible with most synchronous transfer formats, including Philips I²C, Motorola® SPI®, and Intel® SSR protocols. The AD9520-2 I²C implementation deviates from the classic I²C specification on two specifications, and these deviations are documented in Table 14 of this data sheet. The serial control port allows read/write access to all registers that configure the AD9520-2.

SPI/I²C PORT SELECTION

The AD9520-2 has two serial interfaces, SPI and I²C. Users can select either SPI or I²C depending on the states of the three- level (high, open, low) logic input pins, SP1 and SP0. When both SP1 and SP0 are high, the SPI interface is active. Otherwise, I²C is active with eight different I²C slave address (seven bits wide) settings (see Table 41). The four MSBs of the slave address are hardware coded as 1011b; the three LSBs are programmed by SP1 and SP0.

Table 41. Serial Port Mode Selection

SP1	SP0	Address
Low	Low	I²C, 1011000b
Low	Open	I²C, 1011001b
Low	High	I²C, 1011010b
Open	Low	I²C, 1011011b
Open	Open	I²C, 1011100b
Open	High	I²C, 1011101b
High	Low	I²C, 1011110b
High	Open	I²C, 1011111b
High	High	SPI

I²C SERIAL PORT OPERATION

The AD9520-2 I²C port is based on the I²C fast mode standard. The AD9520-2 supports both I²C protocols: standard mode (100 kHz) and fast mode (400 kHz).

The AD9520-2 I²C port has a 2-wire interface consisting of a serial data line (SDA) and a serial clock line (SCL). In an I²C bus system, the AD9520-2 is connected to the serial bus (data bus SDA and clock bus SCL) as a slave device, meaning that no clock is generated by the AD9520-2. The AD9520-2 uses direct 16-bit (two bytes) memory addressing instead of traditional 8-bit (one byte) memory addressing.

I²C Bus Characteristics

Table 42. I²C Bus Definitions

Abbreviation	Definition
S	Start
Sr	Repeated start
P	Stop
A	Acknowledge
$\overline{A}$	No acknowledge
W	Write
R	Read

One pulse on the SCL clock line is generated for each data bit transferred.

The data on the SDA line must not change during the high period of the clock. The state of the data line can change only when the clock on the SCL line is low.

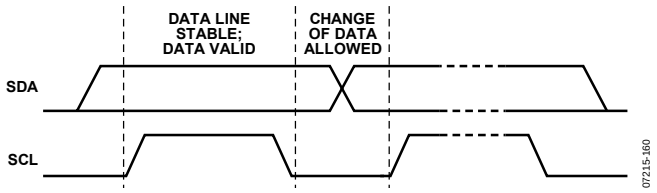


Figure 56. Valid Bit Transfer

A start condition is a transition from high to low on the SDA line while SCL is high. The start condition is always generated by the master to initialize the data transfer.

A stop condition is a transition from low to high on the SDA line while SCL is high. The stop condition is always generated by the master to end the data transfer.

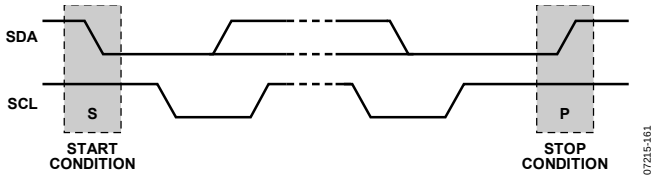


Figure 57. Start and Stop Conditions

A byte on the SDA line is always eight bits long. An acknowledge bit must follow every byte. Bytes are sent MSB first.

The acknowledge bit is the ninth bit attached to any 8-bit data byte. An acknowledge bit is always generated by the receiving device (receiver) to inform the transmitter that the byte has been received. It is accomplished by pulling the SDA line low during the ninth clock pulse after each 8-bit data byte.

The no acknowledge bit is the ninth bit attached to any 8-bit data byte. A no acknowledge bit is always generated by the receiving device (receiver) to inform the transmitter that the byte has not been received. It is accomplished by leaving the SDA line high during the ninth clock pulse after each 8-bit data byte.

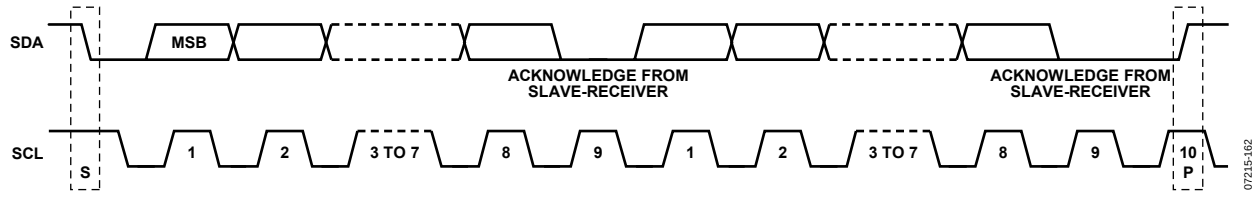


Figure 58. Acknowledge Bit

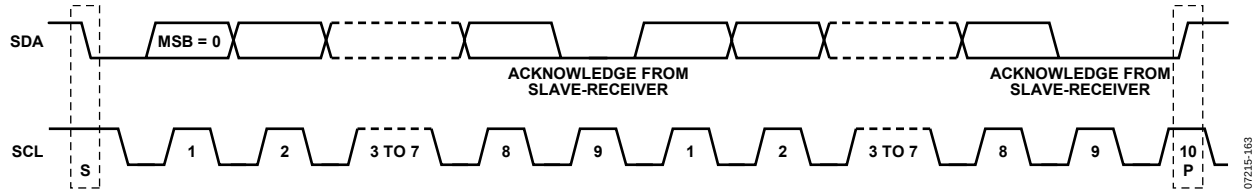


Figure 59. Data Transfer Process (Master Write Mode, 2-Byte Transfer Used for Illustration)

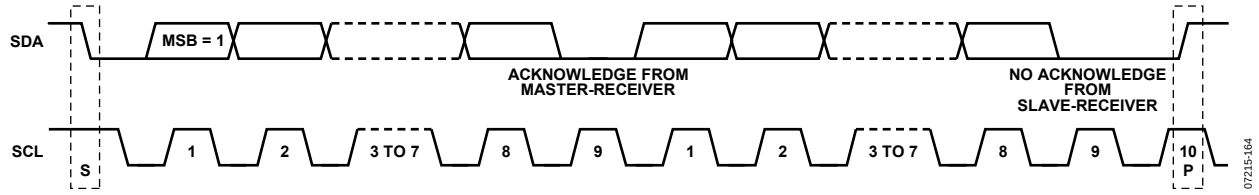


Figure 60. Data Transfer Process (Master Read Mode, 2-Byte Transfer Used for Illustration)

Data Transfer Process

The master initiates data transfer by asserting a start condition. This indicates that a data stream follows. All I²C slave devices connected to the serial bus respond to the start condition.

The master then sends an 8-bit address byte over the SDA line, consisting of a 7-bit slave address (MSB first) plus an R/W bit. This bit determines the direction of the data transfer, that is, whether data is written to or read from the slave device (0b = write, 1b = read).

The peripheral whose address corresponds to the transmitted address responds by sending an acknowledge bit. All other devices on the bus remain idle while the selected device waits for data to be read from or written to it. If the R/W bit is 0b, the master (transmitter) writes to the slave device (receiver). If the R/W bit is 1b, the master (receiver) reads from the slave device (transmitter).

The format for these commands is described in the Data Transfer Format section.

Data is then sent over the serial bus in the format of nine clock pulses, one data byte (8-bit) from either master (write mode) or slave (read mode), followed by an acknowledge bit from the receiving device. The number of bytes that can be transmitted per transfer is unrestricted. In write mode, the first two data bytes immediately after the slave address byte are the internal memory (control registers) address bytes with the high address byte first. This addressing scheme gives a memory address up to $2^{16} - 1 = 65,535$. The data bytes after these two memory address bytes are register data written into the control registers. In read mode, the data bytes after the slave address byte are register data read from the control registers.

When all data bytes are read or written, stop conditions are established. In write mode, the master (transmitter) asserts a stop condition to end data transfer during the (10th) clock pulse following the acknowledge bit for the last data byte from the slave device (receiver). In read mode, the master device (receiver) receives the last data byte from the slave device (transmitter) but does not pull it low during the ninth clock pulse. This is known as a no acknowledge bit. By receiving the no acknowledge bit, the slave device knows that the data transfer is finished and releases the SDA line. The master then takes the data line low during the low period before the 10th clock pulse and high during the 10th clock pulse to assert a stop condition.

A repeated start (Sr) condition can be used in place of a stop condition. Furthermore, a start or stop condition can occur at any time, and partially transferred bytes are discarded.

Data Transfer Format

Send byte format—the send byte protocol is used to set up the register address for subsequent commands.

S	Slave Address	W	A	RAM Address High Byte	A	RAM Address Low Byte	A	P

Write byte format—the write byte protocol is used to write a register address to the RAM starting from the specified RAM address.

S	Slave Address	W	A	RAM Address High Byte	A	RAM Address Low Byte	A	RAM Data 0	A	RAM Data 1	A	RAM Data 2	A	P

Receive byte format—the receive byte protocol is used to read the data byte(s) from RAM starting from the current address.

S	Slave Address	R	A	RAM Data 0	A	RAM Data 1	A	RAM Data 2	$\overline{A}$	P

Read byte format—the combined format of the send byte and the receive byte.

S	Slave Address	W	A	RAM Address High Byte	A	RAM Address Low Byte	A	Sr	Slave Address	R	A	RAM Data 0	A	RAM Data 1	A	RAM Data 2	$\overline{A}$	P

I²C Serial Port Timing

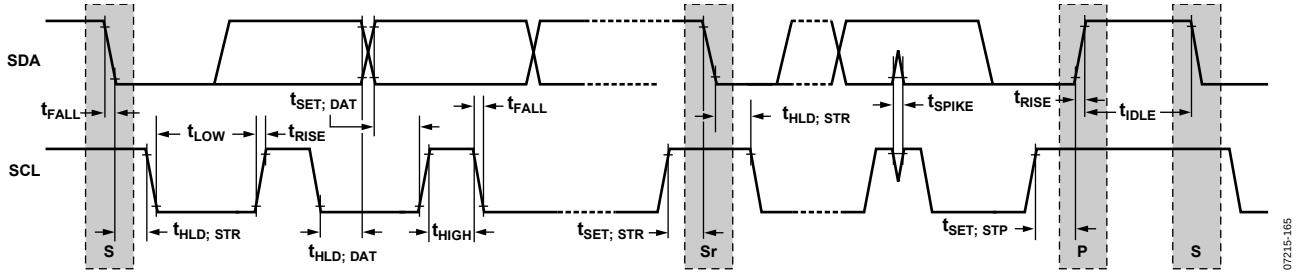


Figure 61. I²C Serial Port Timing

Table 43. I²C Timing Definitions

Parameter	Description
f_{I2C}	I²C clock frequency
t_{IDLE}	Bus idle time between stop and start conditions
$t_{HLD;\ STR}$	Hold time for repeated start condition
$t_{SET;\ STR}$	Setup time for repeated start condition
$t_{SET;\ STP}$	Setup time for stop condition
$t_{HLD;\ DAT}$	Hold time for data
$t_{SET;\ DAT}$	Setup time for data
t_{LOW}	Duration of SCL clock low
t_{HIGH}	Duration of SCL clock high
t_{RISE}	SCL/SDA rise time
t_{FALL}	SCL/SDA fall time
t_{SPIKE}	Voltage spike pulse width that must be suppressed by the input filter

SPI SERIAL PORT OPERATION

Pin Descriptions

SCLK (serial clock) is the serial shift clock. This pin is an input. SCLK is used to synchronize serial control port reads and writes. Write data bits are registered on the rising edge of this clock, and the read data bits transition on the falling edge of SCLK. This pin is internally pulled down by a 30 kΩ resistor to ground.

SDIO (serial data input/output) is a dual-purpose pin and acts either as an input only (unidirectional mode) or as both an input and an output (bidirectional mode). The AD9520-2 defaults to the bidirectional I/O mode (Register 0x000[7] = 0b).

SDO (serial data out) is used only in the unidirectional I/O mode (Register 0x000[7]) as a separate output pin for reading back data.

$\overline{CS}$ (chip select bar) is an active low control that gates the read and write cycles. When $\overline{CS}$ is high, SDO and SDIO are in a high impedance state. This pin is internally pulled up by a 30 kΩ resistor to V_S.

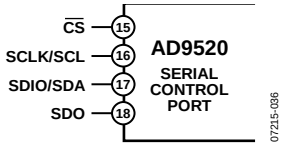


Figure 62. Serial Control Port

SPI Mode Operation

In SPI mode, single or multiple byte transfers are supported, as well as MSB first or LSB first transfer formats. The AD9520-2 serial control port can be configured for a single bidirectional I/O pin (SDIO only) or for two unidirectional I/O pins (SDIO/SDO). By default, the AD9520-2 is in bidirectional mode. Short instruction mode (8-bit instructions) is not supported. Only long (16-bit) instruction mode is supported. It is possible that the serial activity on the SDIO/SDO pins may induce jitter on the PLL while data is being transmitted.

A write or a read operation to the AD9520-2 is initiated by pulling $\overline{CS}$ low.

The $\overline{CS}$ stalled high mode is supported in data transfers where three or fewer bytes of data (plus instruction data) are transferred (see Table 44). In this mode, the $\overline{CS}$ pin can temporarily return high on any byte boundary, allowing time for the system controller to process the next byte. $\overline{CS}$ can go high on byte boundaries only and can go high during either part (instruction or data) of the transfer.

During this period, the serial control port state machine enters a wait state until all data is sent. If the system controller decides to abort the transfer before all of the data is sent, the state machine must be reset by either completing the remaining transfers or by returning $\overline{CS}$ low for at least one complete SCLK cycle (but fewer than eight SCLK cycles). Raising the $\overline{CS}$ pin on a nonbyte boundary terminates the serial transfer and flushes the buffer.

In the streaming mode (see Table 44), any number of data bytes can be transferred in a continuous stream. The register address is automatically incremented or decremented (see the SPI MSB/LSB First Transfers section). $\overline{CS}$ must be raised at the end of the last byte to be transferred, thereby ending streaming mode.

Communication Cycle—Instruction Plus Data

There are two parts to a communication cycle with the AD9520-2. The first part writes a 16-bit instruction word into the AD9520-2, coincident with the first 16 SCLK rising edges. The instruction word provides the AD9520-2 serial control port with information regarding the data transfer, which is the second part of the communication cycle. The instruction word defines whether the upcoming data transfer is a read or a write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer.

Write

If the instruction word is for a write operation, the second part is the transfer of data into the serial control port buffer of the AD9520-2. Data bits are registered on the rising edge of SCLK.

The length of the transfer (one, two, or three bytes, or streaming mode) is indicated by two bits (W1:W0) in the instruction byte. When the transfer is one, two, or three bytes, but not streaming, $\overline{CS}$ can be raised after each sequence of eight bits to stall the bus (except after the last byte, where it ends the cycle). When the bus is stalled, the serial transfer resumes when $\overline{CS}$ is lowered. Raising the $\overline{CS}$ pin on a nonbyte boundary resets the serial control port. During a write, streaming mode does not skip over reserved or blank registers, and the user can write 0x00 to the reserved register addresses.

Because data is written into a serial control port buffer area, not directly into the actual control registers of the AD9520-2, an additional operation is needed to transfer the serial control port buffer contents to the actual control registers of the AD9520-2, thereby causing them to become active. The update registers operation consists of setting Register 0x232[0] = 1b (this bit is self-clearing). Any number of bytes of data can be changed before executing an update registers. The update registers simultaneously actuates all register changes that have been written to the buffer since any previous update.

Read

The AD9520-2 supports only the long instruction mode. If the instruction word is for a read operation, the next N × 8 SCLK cycles clock out the data from the address specified in the instruction word, where N is 1 to 3 as determined by Bits[W1:W0]. If N = 4, the read operation is in streaming mode, continuing until $\overline{CS}$ is raised. Streaming mode does not skip over reserved or blank registers. The readback data is valid on the falling edge of SCLK.

The default mode of the AD9520-2 serial control port is the bidirectional mode. In bidirectional mode, both the sent data and the readback data appear on the SDIO pin. It is also possible to set the AD9520-2 to unidirectional mode (Register 0x000[7] = 1b and Register 0x000[0] = 1b). In unidirectional mode, the readback data appears on the SDO pin.

A readback request reads the data in the serial control port buffer area or the data in the active registers (see Figure 63). Readback of the buffer or active registers is controlled by Register 0x004[0].

The AD9520 uses Register 0x000 to Register 0xB03.

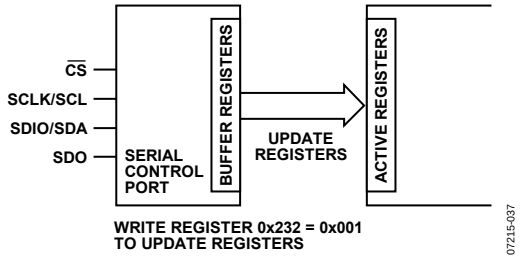


Figure 63. Relationship Between Serial Control Port Buffer Registers and Active Registers of the AD9520-2

SPI INSTRUCTION WORD (16 BITS)

The MSB of the instruction word is R/$\overline{W}$, which indicates whether the instruction is a read or a write. The next two bits (W1:W0) indicate the length of the transfer in bytes. The final 13 bits are the address (A12:A0) at which to begin the read or write operation.

For a write, the instruction word is followed by the number of bytes of data indicated by Bits[W1:W0], see Table 44.

Table 44. Byte Transfer Count

W1	W0	Bytes to Transfer
0	0	1
0	1	2
1	0	3
1	1	Streaming mode

Bits[A12:A0] select the address within the register map that is written to or read from during the data transfer portion of the communications cycle. For multibyte transfers, this address is the starting byte address. In MSB first mode, subsequent bytes decrement the address.

SPI MSB/LSB FIRST TRANSFERS

The AD9520-2 instruction word and byte data can be MSB first or LSB first. Any data written to Register 0x000 must be mirrored; the upper four bits (Bits[7:4]) must mirror the lower four bits (Bits[3:0]). This makes it irrelevant whether LSB first or MSB first is in effect. As an example of this mirroring, see the default setting for Register 0x000, which mirrors Bit 4 and Bit 3. This sets the long instruction mode, which is the default and the only mode that is supported.

The default for the AD9520-2 is MSB first.

When LSB first is set by Register 0x000[1] and Register 0x000[6], it takes effect immediately because it affects only the operation of the serial control port and does not require that an update be executed.

When MSB first mode is active, the instruction and data bytes must be written from MSB to LSB. Multibyte data transfers in MSB first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes must follow in order from the high address to the low address. In MSB first mode, the serial control port internal address generator decrements for each data byte of the multibyte transfer cycle.

When LSB first is active, the instruction and data bytes must be written from LSB to MSB. Multibyte data transfers in LSB first format start with an instruction byte that includes the register address of the least significant data byte followed by multiple data bytes. In a multibyte transfer cycle, the internal byte address generator of the serial port increments for each byte.

The AD9520-2 serial control port register address decrements from the register address just written toward Register 0x000 for multibyte I/O operations if the MSB first mode is active (default). If the LSB first mode is active, the register address of the serial control port increments from the address just written toward Register 0x232 for multibyte I/O operations.

Streaming mode always terminates when it reaches Register 0x232. Note that unused addresses are not skipped during multibyte I/O operations.

Table 45. Streaming Mode (No Addresses Are Skipped)

Write Mode	Address Direction	Stop Sequence
LSB first	Increment	Register 0x230, Register 0x231, Register 0x232, stop
MSB first	Decrement	Register 0x001, Register 0x000, Register 0x232, stop

Table 46. Serial Control Port, 16-Bit Instruction Word, MSB First

MSB															LSB
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
R/$\overline{W}$	W1	W0	A12 = 0	A11 = 0	A10 = 0	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

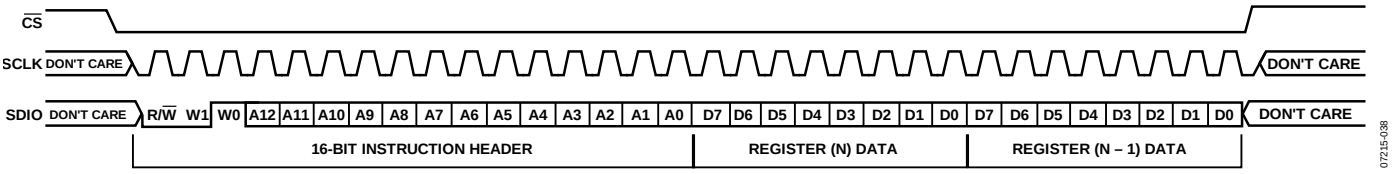


Figure 64. Serial Control Port Write—MSB First, 16-Bit Instruction, Two Bytes of Data

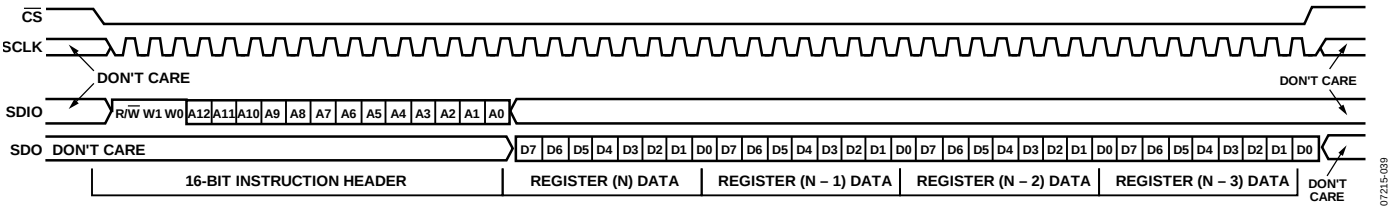


Figure 65. Serial Control Port Read—MSB First, 16-Bit Instruction, Four Bytes of Data

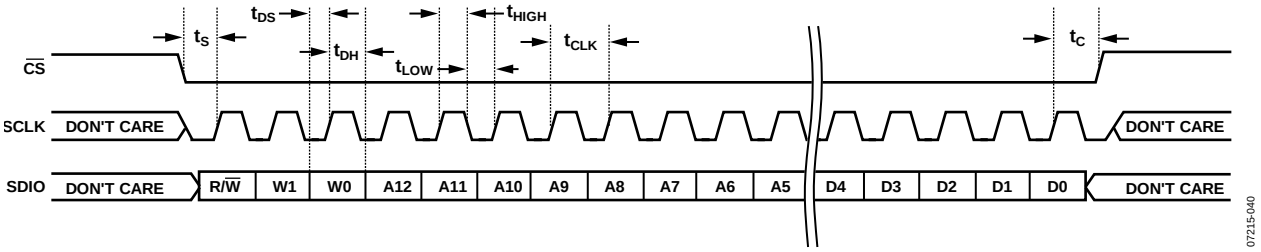


Figure 66. Serial Control Port Write—MSB First, 16-Bit Instruction, Timing Measurements

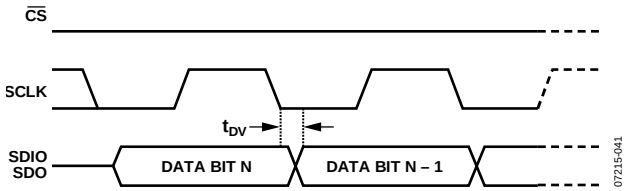


Figure 67. Timing Diagram for Serial Control Port Register Read

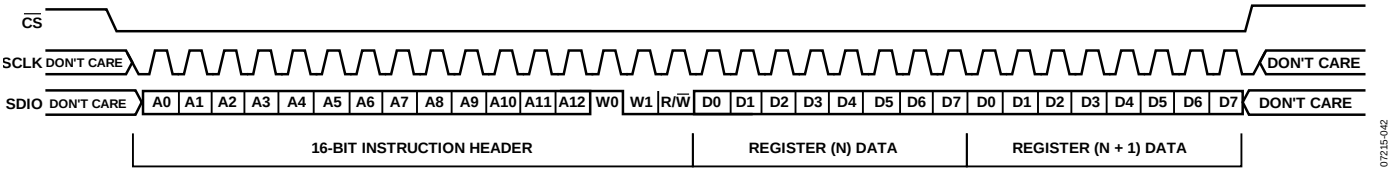


Figure 68. Serial Control Port Write—LSB First, 16-Bit Instruction, Two Bytes of Data

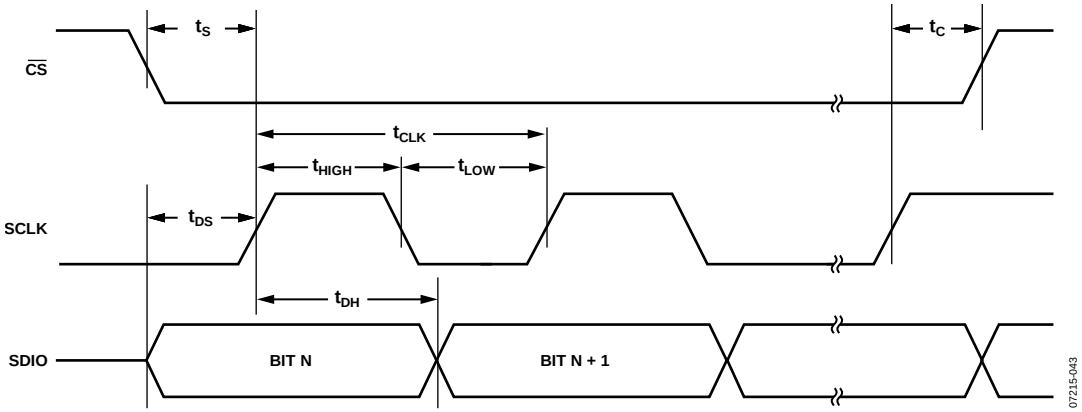


Figure 69. Serial Control Port Timing—Write

Table 47. Serial Control Port Timing

Parameter	Description
t_{DS}	Setup time between data and rising edge of SCLK
t_{DH}	Hold time between data and rising edge of SCLK
t_{CLK}	Period of the clock
t_S	Setup time between the $\overline{CS}$ falling edge and the SCLK rising edge (start of communication cycle)
t_C	Setup time between the SCLK rising edge and the $\overline{CS}$ rising edge (end of communication cycle)
t_{HIGH}	Minimum period that SCLK should be in a logic high state
t_{LOW}	Minimum period that SCLK should be in a logic low state
t_{DV}	SCLK to valid SDIO and SDO (see Figure 67)

EEPROM OPERATIONS

The AD9520-2 contains an internal EEPROM (nonvolatile memory). The EEPROM can be programmed by users to create and store a user-defined register setting file when the power is off. This setting file can be used for power-up and chip reset as a default setting. The EEPROM size is 512 bytes.

Note that, to guarantee proper loading of the EEPROM during startup, a high-low-high pulse on the $\overline{\text{RESET}}$ pin should occur after the power supply has stabilized.

During the data transfer process, the write and read registers via the serial port are generally not available except for one readback register, STATUS_EEPROM.

To determine the data transfer state through the serial port in SPI mode, users can read the value of STATUS_EEPROM (1b = in process; 0b = completed).

In I^2C mode, the user can address the AD9520-2 slave port with the external I^2C master (send an address byte to the AD9520-2). If the AD9520-2 responds with a no acknowledge bit, the data transfer process does not take place. If the AD9520-2 responds with an acknowledge bit, the data transfer process is completed. The user can monitor the STATUS_EEPROM register or program the STATUS pin to monitor the status of the data transfer.

WRITING TO THE EEPROM

The EEPROM cannot be programmed directly through the serial port interface. To program the EEPROM and store a register setting file, do the following:

1. Program the AD9520-2 registers to the desired circuit state. If the user wants the PLL to lock automatically after power-up, the VCO calibration now bit (Register 0x018[0]) must be set to 1b. This allows VCO calibration to start automatically after register loading. Note that a valid input reference signal must be present during VCO calibration.
2. Program the EEPROM buffer registers, if necessary (see the Programming the EEPROM Buffer Segment section). This step is necessary only if the user wants to use the EEPROM to control the default setting of some (but not all) of the AD9520-2 registers or to control the register setting update sequence during power-up or chip reset.
3. Set the enable EEPROM write bit (Register 0xB02[0]) to 1b to enable the EEPROM.
4. Set the REG2EEPROM bit (Register 0xB03[0]) to 1b.
5. Set the IO_UPDATE bit (Register 0x232[0]) to 1b, which starts the process of writing data into the EEPROM to create the EEPROM setting file. This enables the AD9520-2 EEPROM controller to transfer the current register values, as well as the memory address and instruction bytes from the EEPROM buffer segment, into the EEPROM. After the write process is completed, the internal controller sets Register 0xB03[0] (REG2EEPROM) back to 0b.

   The STATUS_EEPROM bit in the readback register (Register 0xB00[0]) is used to indicate the data transfer status between the EEPROM and the control registers (0b = complete/inactive; 1b = in process/active). At the start of the data transfer, STATUS_EEPROM is set to 1b by the EEPROM controller and cleared to 0b at the end of the data transfer. The STATUS_EEPROM bit can be accessed through the STATUS pin when the STATUS pin is programmed to monitor the STATUS_EEPROM bit. Alternatively, the user can monitor the STATUS_EEPROM bit directly by reading the register.
6. When the data transfer process is done (Register 0xB00[0] = 0b), set the enable EEPROM write bit (Register 0xB02[0]) to 0b to disable writing to the EEPROM.

To verify that the data transfer has completed correctly, ensure that Register 0xB01[0] = 0b. A value of 1b in this register indicates a data transfer error. When an EEPROM save/load transfer is complete, wait a minimum of 10 µs before starting the next EEPROM save/load transfer.

READING FROM THE EEPROM

The following reset-related events can start the process of restoring the settings stored in EEPROM to control registers.

When the EEPROM pin is set high, do any of the following:

- Power-up the AD9520-2.
- Perform a hardware chip reset by pulling the $\overline{\text{RESET}}$ pin low and then releasing $\overline{\text{RESET}}$.
- Set the self-clearing soft reset bit (Register 0x000[5]) to 1b.

When the EEPROM pin is set low, set the self-clearing SOFT_EEPROM bit (Register 0xB02[1]) to 1b. The AD9520-2 then starts to read the EEPROM and loads the values into the active registers.

If the EEPROM pin is low during reset or power-up, the EEPROM is not active, and the AD9520-2 default values are loaded instead.

Note that, when using the EEPROM to automatically load the AD9520-2 register values and lock the PLL, the VCO calibration now bit (Register 0x018[0]) must be set to 1b when the register values are written to the EEPROM. This allows VCO calibration to start automatically after register loading. A valid input reference signal must be present during VCO calibration.

To verify that the data transfer has completed correctly, verify that Register 0xB01[0] = 0b. A value of 1b in this register indicates a data transfer error. When an EEPROM save/load transfer is complete, wait a minimum of 10 µs before starting the next EEPROM save/load transfer.

PROGRAMMING THE EEPROM BUFFER SEGMENT

The EEPROM buffer segment is a register space on the AD9520-2. The user can specify which groups of registers are stored to the EEPROM during EEPROM programming. Note that programming this register space is optional. The default power-up values for the EEPROM buffer segment allow storage of all the AD9520-2 register values from Register 0x000 to Register 0x231 to the EEPROM.

As an example, a user might want to load only the output driver settings from the EEPROM without disturbing the PLL register settings currently stored in the AD9520-2. The user can alter the EEPROM buffer segment to include only the registers that apply to the output drivers and exclude the registers that apply to the PLL configuration.

There are two parts to the EEPROM buffer segment: register section definition groups and operational codes. Table 48 shows an example of the EEPROM buffer segment.

Register Section Definition Group

Note that the AD9520-2 register map is noncontiguous, and the EEPROM is only 512 bytes long. The register section definition group tells the EEPROM controller how the AD9520-2 register map is segmented. Each register section definition group contains the starting address and number of bytes to be written to EEPROM.

The register section definition group defines a continuous register section for the EEPROM profile. It consists of three bytes. The first byte defines how many continuous register bytes are in this group. If the user writes 0x000 to the first byte, it means that there is only one byte in this group. If the user writes 0x001, it means that there are two bytes in this group. The maximum number of registers in one group is 128. The next two bytes are the low byte and high byte, respectively, of the 16-bit memory address of the first register in this group.

Operational Codes

There are three operational codes: IO_UPDATE, end-of-data, and pseudo-end-of-data. It is important that the EEPROM buffer segment always have either an end-of-data or a pseudo-end-of-data operational code and that an IO_UPDATE operational code appear at least once before the end-of-data operational code.

IO_UPDATE (Operational Code 0x80)

The EEPROM controller uses this operational code to generate an IO_UPDATE signal to update the active control register bank from the buffer register bank during the download process.

At a minimum, there should be at least one IO_UPDATE operational code after the end of the final register section definition group. This code is needed so that at least one IO_UPDATE occurs after all of the AD9520-2 registers are loaded when the EEPROM is read. If this operational code is absent during a write to the EEPROM, the register values loaded from the EEPROM are not transferred to the active register space, and these values do not take effect after they are loaded from the EEPROM to the AD9520-2.

End-of-Data (Operational Code 0xFF)

The EEPROM controller uses this operational code to terminate the data transfer process between EEPROM and the control register during the upload and download process. The last item appearing in the EEPROM buffer segment should be either this operational code or the pseudo-end-of-data operational code.

Pseudo-End-of-Data (Operational Code 0xFE)

The AD9520-2 EEPROM buffer segment has 23 bytes that can contain up to seven register section definition groups. If the user wants to define more than seven register section definition groups, the pseudo-end-of-data operational code can be used. During the upload process, when the EEPROM controller receives the pseudo-end-of-data operational code, it halts the data transfer process, clears the REG2EEPROM bit, and enables the AD9520-2 serial port. The user can then program the EEPROM buffer segment again and reinitiate the data transfer process by setting the REG2EEPROM bit (Register 0xB03[0]) to 1b and the IO_UPDATE bit (Register 0x232[0]) to 1b. The internal I^2C master then begins writing to the EEPROM starting from the EEPROM address held from the last writing.

This sequence provides the user with more discrete instructions that can be written to the EEPROM than would otherwise be possible due to the limited size of the EEPROM buffer segment. It also allows for the same register to be written multiple times with a different value each time.

Table 48. Example of the EEPROM Buffer Segment

Reg Addr (Hex)	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Start EEPROM Buffer Segment								
0xA00	0	Number of bytes [6:0] of the first group of registers						
0xA01	Address [15:8] of the first group of registers							
0xA02	Address [7:0] of the first group of registers							
0xA03	0	Number of bytes [6:0] of the second group of registers						
0xA04	Address [15:8] of the second group of registers							
0xA05	Address [7:0] of the second group of registers							
0xA06	0	Number of bytes [6:0] of the third group of registers						
0xA07	Address [15:8] of the third group of registers							
0xA08	Address [7:0] of the third group of registers							
0xA09	IO_UPDATE operational code (0x80)							
0xA0A	End-of-data operational code (0xFF)							

THERMAL PERFORMANCE

Table 49. Thermal Parameters for 64-Lead LFCSP

Symbol	Thermal Characteristic Using a JEDEC JESD51-7 Plus JEDEC JESD51-5 2S2P Test Board	Value (°C/W)
θ_{JA}	Junction-to-ambient thermal resistance, 0.0 m/sec airflow per JEDEC JESD51-2 (still air)	22.0
θ_{JMA}	Junction-to-ambient thermal resistance, 1.0 m/sec airflow per JEDEC JESD51-6 (moving air)	19.2
θ_{JMA}	Junction-to-ambient thermal resistance, 2.0 m/sec airflow per JEDEC JESD51-6 (moving air)	17.2
Ψ_{JB}	Junction-to-board characterization parameter, 1.0 m/sec airflow per JEDEC JESD51-6 (moving air) and JEDEC JESD51-8	11.6
θ_{JC}	Junction-to-case thermal resistance (die-to-heat sink) per MIL-Std 883, Method 1012.1	1.3
Ψ_{JT}	Junction-to-top-of-package characterization parameter, 0 m/sec airflow per JEDEC JESD51-2 (still air)	0.1

The AD9520-2 is specified for a case temperature (T_{CASE}). To ensure that T_{CASE} is not exceeded, an airflow source can be used.

Use the following equation to determine the junction temperature on the application PCB:

$$T_J = T_{CASE} + (\Psi_{JT} \times PD)$$

where:
T_J is the junction temperature (°C).
T_{CASE} is the case temperature (°C) measured by the user at the top center of the package.
Ψ_{JT} is the value from Table 49.
PD is the power dissipation (see the total power dissipation in Table 18.)

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first-order approximation of T_J by the equation

$$T_J = T_A + (\theta_{JA} \times PD)$$

where T_A is the ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

Values of Ψ_{JB} are provided for package comparison and PCB design considerations.

REGISTER MAP

Register addresses that are not listed in Table 50 are not used, and writing to those registers has no effect. Writing to register addresses that are marked as unused also has no effect.

Table 50. Register Map Overview

Addr (Hex)	Parameter	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)
Serial Port Configuration										
0x000	Serial port config (SPI mode)	SDO active	LSB first/ addr incr	Soft reset (self-clear)	Unused	Unused	Soft reset (self-clear)	LSB first/addr incr	SDO active	0x00
	Serial port config (I^2C mode)	Unused		Soft reset (self-clear)	Unused	Unused	Soft reset (self-clear)	Unused		0x00
0x001	Unused	Unused								N/A
0x002	Reserved	Reserved								N/A
0x003	Part ID	Part ID (read only)								0x20
0x004	Readback control	Unused							Read back active regs	0x00
EEPROM ID										
0x005	EEPROM customer version ID	EEPROM customer version ID (LSB)								0x00
0x006		EEPROM customer version ID (MSB)								0x00
0x007 to 0x00F	Unused	Unused								0x00
PLL										
0x010	PFD charge pump	PFD polarity	Charge pump current			Charge pump mode		PLL power-down		0x7D
0x011	R counter	14-bit R counter, Bits[7:0] (LSB)								0x01
0x012		Unused		14-bit R counter, Bits[13:8] (MSB)						0x00
0x013	A counter	Unused		6-bit A counter						0x00
0x014	B counter	13-bit B counter, Bits[7:0] (LSB)								0x03
0x015		Unused			13-bit B counter, Bits[12:8] (MSB)					0x00
0x016	PLL_CTRL_1	Set CP pin to $V_{CP}/2$	Reset R counter	Reset A and B counters	Reset all counters	B counter bypass	Prescaler P			0x06
0x017	PLL_CTRL_2	STATUS pin control						Antibacklash pulse width		0x00
0x018	PLL_CTRL_3	Enable CMOS reference input dc offset	Lock detect counter		Digital lock detect window	Disable digital lock detect	VCO calibration divider		VCO calibration now	0x06
0x019	PLL_CTRL_4	R, A, and B counters $\overline{\text{SYNC}}$ pin reset		R path delay			N path delay			0x00
0x01A	PLL_CTRL_5	Enable STATUS pin divider	Ref freq monitor threshold	LD pin control						0x00
0x01B	PLL_CTRL_6	Enable VCO frequency monitor	Enable $\overline{\text{REF2}}$ ($\overline{\text{REFIN}}$) frequency monitor	Enable REF1 (REFIN) frequency monitor	REFMON pin control					0x00
0x01C	PLL_CTRL_7	Disable switchover deglitch	Select REF2	Use REF_SEL pin	Enable automatic reference switchover	Stay on REF2	Enable REF2	Enable REF1	Enable differential reference	0x00
0x01D	PLL_CTRL_8	Enable STATUS_EEPROM at STATUS pin	Enable XTAL OSC	Enable clock doubler	Disable PLL status register	Enable LD pin comparator	Unused	Enable external holdover	Enable holdover	0x80
0x01E	PLL_CTRL_9	Unused			External zero delay feedback channel divider select		Enable external zero delay	Enable zero delay	Unused	0x00
0x01F	PLL_Readback (read only)	Unused	VCO cal finished	Holdover active	REF2 selected	VCO freq > threshold	REF2 freq > threshold	REF1 freq > threshold	Digital lock detect	N/A

Addr (Hex)	Parameter	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)
Output Driver Control										
0x0F0	OUT0 control	OUT0 format	OUT0 CMOS configuration		OUT0 polarity		OUT0 LVPECL differential voltage		OUT0 LVPECL power-down	0x64
0x0F1	OUT1 control	OUT1 format	OUT1 CMOS configuration		OUT1 polarity		OUT1 LVPECL differential voltage		OUT1 LVPECL power-down	0x64
0x0F2	OUT2 control	OUT2 format	OUT2 CMOS configuration		OUT2 polarity		OUT2 LVPECL differential voltage		OUT2 LVPECL power-down	0x64
0x0F3	OUT3 control	OUT3 format	OUT3 CMOS configuration		OUT3 polarity		OUT3 LVPECL differential voltage		OUT3 LVPECL power-down	0x64
0x0F4	OUT4 control	OUT4 format	OUT4 CMOS configuration		OUT4 polarity		OUT4 LVPECL differential voltage		OUT4 LVPECL power-down	0x64
0x0F5	OUT5 control	OUT5 format	OUT5 CMOS configuration		OUT5 polarity		OUT5 LVPECL differential voltage		OUT5 LVPECL power-down	0x64
0x0F6	OUT6 control	OUT6 format	OUT6 CMOS configuration		OUT6 polarity		OUT6 LVPECL differential voltage		OUT6 LVPECL power-down	0x64
0x0F7	OUT7 control	OUT7 format	OUT7 CMOS configuration		OUT7 polarity		OUT7 LVPECL differential voltage		OUT7 LVPECL power-down	0x64
0x0F8	OUT8 control	OUT8 format	OUT8 CMOS configuration		OUT8 polarity		OUT8 LVPECL differential voltage		OUT8 LVPECL power-down	0x64
0x0F9	OUT9 control	OUT9 format	OUT9 CMOS configuration		OUT9 polarity		OUT9 LVPECL differential voltage		OUT9 LVPECL power-down	0x64
0x0FA	OUT10 control	OUT10 format	OUT10 CMOS configuration		OUT10 polarity		OUT10 LVPECL differential voltage		OUT10 LVPECL power-down	0x64
0x0FB	OUT11 control	OUT11 format	OUT11 CMOS configuration		OUT11 polarity		OUT11 LVPECL differential voltage		OUT11 LVPECL power-down	0x64
0x0FC	Enable output on CSDLD	CSDLD en OUT7	CSDLD en OUT6	CSDLD en OUT5	CSDLD en OUT4	CSDLD en OUT3	CSDLD en OUT2	CSDLD en OUT1	CSDLD en OUT0	0x00
0x0FD		Unused	Unused	Unused	Unused	CSDLD en OUT11	CSDLD en OUT10	CSDLD en OUT9	CSDLD en OUT8	0x00
0x0FE to 0x18F	Unused	Unused								0x00
LVPECL Channel Dividers										
0x190	Divider 0 (PECL)	Divider 0 low cycles				Divider 0 high cycles				0x77
0x191		Divider 0 bypass	Divider 0 ignore SYNC	Divider 0 force high	Divider 0 start high	Divider 0 phase offset				0x00
0x192		Unused				Unused	Channel 0 power-down	Channel 0 direct-to-output	Disable Divider 0 DCC	0x00
0x193	Divider 1 (PECL)	Divider 1 low cycles				Divider 1 high cycles				0x33
0x194		Divider 1 bypass	Divider 1 ignore SYNC	Divider 1 force high	Divider 1 start high	Divider 1 phase offset				0x00
0x195		Unused				Unused	Channel 1 power-down	Channel 1 direct-to-output	Disable Divider 1 DCC	0x00
0x196	Divider 2 (PECL)	Divider 2 low cycles				Divider 2 high cycles				0x11
0x197		Divider 2 bypass	Divider 2 ignore SYNC	Divider 2 force high	Divider 2 start high	Divider 2 phase offset				0x00
0x198		Unused				Unused	Channel 2 power-down	Channel 2 direct-to-output	Disable Divider 2 DCC	0x00
0x199	Divider 3 (PECL)	Divider 3 low cycles				Divider 3 high cycles				0x00
0x19A		Divider 3 bypass	Divider 3 ignore SYNC	Divider 3 force high	Divider 3 start high	Divider 3 phase offset				0x00
0x19B		Unused				Unused	Channel 3 power-down	Channel 3 direct-to-output	Disable Divider 3 DCC	0x00
0x19C to 0x1DF	Unused	Unused								0x00

Addr (Hex)	Parameter	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)
VCO Divider and CLK Input										
0x1E0	VCO divider	Unused				Unused	VCO divider			0x00
0x1E1	Input CLKs	Unused	Unused (default = 01b)		Power down clock input section	Power down VCO clock interface	Power down VCO and CLK	Select VCO or CLK	Bypass VCO divider	0x20
0x1E2 to 0x22A	Unused	Unused								0x00
System										
0x230	Power-down and SYNC	Unused				Disable power on SYNC	Power down SYNC	Power down distribution reference	Soft SYNC	0x00
0x231	Unused	Unused				Unused				0x00
Update All Registers										
0x232	IO_UPDATE	Unused							IO_UPDATE (self-clearing)	0x00
0x233 to 0x9FF	Unused	Unused								0x00
EEPROM Buffer Segment										
0xA00	Serial port configuration	Data transfer: one byte								0x00
0xA01		Starting address: Address 0x000								0x00
0xA02										0x00
0xA03	EEPROM customer version ID	Data transfer: three bytes								0x02
0xA04		Starting address: Address 0x004								0x00
0xA05										0x04
0xA06	PLL settings	Data transfer: 16 bytes								0x0E
0xA07		Starting address: Address 0x010								0x00
0xA08										0x10
0xA09	Output driver control	Data transfer: 16 bytes								0x0E
0xA0A		Starting address: Address 0x0F0								0x00
0xA0B										0xF0
0xA0C	LVPECL channel dividers	Data transfer: 12 bytes								0x0B
0xA0D		Starting address: Address 0x190								0x01
0xA0E										0x90
0xA0F	VCO divider and CLK input	Data transfer: two bytes								0x01
0xA10		Starting address: Address 0x1E0								0x01
0xA11										0xE0
0xA12	Power-down and SYNC	Data transfer: two bytes								0x01
0xA13		Starting address: Address 0x230								0x02
0xA14										0x30
0xA15	I/O update	Action: IO_UPDATE								0x80
0xA16	End of data	Action: end of data								0xFF
0xA17 to 0xAFF	Unused	Unused (available for additional EEPROM instructions)								0x00
EEPROM Control										
0xB00	EEPROM status (read only)	Unused						Unused	STATUS_ EEPROM	0x00
0xB01	EEPROM error checking (read only)	Unused						Unused	EEPROM data error	0x00
0xB02	EEPROM Control 1	Unused						SOFT_EEPROM (self-clearing)	Enable EEPROM write	0x00
0xB03	EEPROM Control 2	Unused						Unused	REG2EEPROM (self-clearing)	0x00

REGISTER MAP DESCRIPTIONS

Table 51 to Table 61 provide a detailed description of each of the control register functions.

Table 51. SPI Mode Serial Port Configuration

Reg. Addr. (Hex)	Bits	Name	Description
0x000	7	SDO active	Selects unidirectional or bidirectional data transfer mode. 0: SDIO pin is used for write and read; SDO pin is high impedance (default). 1: SDO pin is used for read; SDIO pin is used for write; unidirectional mode.
	6	LSB first/addr incr	SPI MSB or LSB data orientation. (This bit is ignored in I²C mode.) 0: data-oriented MSB first; the addressing decrements (default). 1: data-oriented LSB first; the addressing increments.
	5	Soft reset	Soft reset. 1 (self-clearing): if the EEPROM pin is high, soft reset loads the register values from the EEPROM. If the EEPROM pin is low, soft reset loads the register values to the on-chip defaults.
	4	Unused	Unused.
	[3:0]	Mirror[7:4]	Bits[3:0] should always mirror Bits[7:4] so that it does not matter whether the part is in MSB or LSB first mode (see Register 0x000[6]). Set the bits as follows: Bit 0 = Bit 7. Bit 1 = Bit 6. Bit 2 = Bit 5. Bit 3 = Bit 4.
0x003	[7:0]	Part ID (read only)	Uniquely identifies the dash version (AD9520-0 to AD9520-5) of the AD9520, as follows: AD9520-0: 0x20. AD9520-1: 0x60. AD9520-2: 0xA0. AD9520-3: 0x61. AD9520-4: 0xE1. AD9520-5: 0xE0.
0x004	[7:1]	Unused	Unused.
	0	Read back active registers	Selects register bank used for a readback. 0: reads back buffer registers (default). 1: reads back active registers.

Table 52. I²C Mode Serial Port Configuration

Reg. Addr. (Hex)	Bits	Name	Description
0x000	[7:6]	Unused	Unused.
	5	Soft reset	Soft reset. 1 (self-clearing): if the EEPROM pin is high, soft reset loads the register values from the EEPROM. If the EEPROM pin is low, soft reset loads the register values to the on chip defaults.
	4	Unused	Unused.
	[3:0]	Mirror[7:4]	Bits[3:0] should always mirror Bits[7:4] so that it does not matter whether the part is in MSB or LSB first mode. See Table 51, Register 0x000, Bits[3:0].
0x003	[7:0]	Part ID (read only)	Uniquely identifies the dash version (AD9520-0 to AD9520-5) of the AD9520. See Table 51, Register 0x003.
0x004	[7:1]	Unused	Unused.
	0	Read back active registers	Selects register bank used for a readback. 0: reads back buffer registers (default). 1: reads back active registers.

Table 53. EEPROM Customer Version ID

Reg. Addr. (Hex)	Bits	Name	Description
0x005	[7:0]	EEPROM customer version ID (LSB)	16-bit EEPROM ID[7:0]. This register, along with Register 0x006, allows the user to store a unique ID to identify which version of the AD9520-2 register settings is stored in the EEPROM. It does not affect AD9520-2 operation in any way (default: 0x00).
0x006	[7:0]	EEPROM customer version ID (MSB)	16-bit EEPROM ID[15:8]. This register, along with Register 0x005, allows the user to store a unique ID to identify which version of the AD9520-2 register settings is stored in the EEPROM. It does not affect AD9520-2 operation in any way (default: 0x00).

Table 54. PLL

Reg. Addr. (Hex)	Bits	Name	Description
0x010	7	PFD polarity	Sets the PFD polarity. Negative polarity is for use (if needed) with external VCO/VCXO only. The on-chip VCO requires positive polarity; Bit 7 = 0b. 0: positive (higher control voltage produces higher frequency) (default). 1: negative (higher control voltage produces lower frequency).
	[6:4]	CP current	Charge pump current (with CP_{RSET} = 5.1 kΩ).
			Bit 6 / Bit 5 / Bit 4 / I_{CP} (mA)
			0 / 0 / 0 / 0.6
			0 / 0 / 1 / 1.2
			0 / 1 / 0 / 1.8
			0 / 1 / 1 / 2.4
			1 / 0 / 0 / 3.0
			1 / 0 / 1 / 3.6
			1 / 1 / 0 / 4.2
			1 / 1 / 1 / 4.8 (default)
	[3:2]	CP mode	Charge pump operating mode.
			Bit 3 / Bit 2 / Charge Pump Mode
			0 / 0 / High impedance state.
			0 / 1 / Forces source current (pump up).
			1 / 0 / Forces sink current (pump down).
			1 / 1 / Normal operation (default).
	[1:0]	PLL power-down	PLL operating mode.
			Bit 1 / Bit 0 / Mode
			0 / 0 / Normal operation; this mode must be selected to use the PLL.
			0 / 1 / Asynchronous power-down (default).
			1 / 0 / Unused.
			1 / 1 / Synchronous power-down.
0x011	[7:0]	14-bit R counter, Bits[7:0] (LSB)	Reference divider LSBs—lower eight bits. The reference divider (also called the R divider or R counter) is 14 bits long. The lower eight bits are in this register (default: 0x01).
0x012	[7:6]	Unused	Unused.
	[5:0]	14-bit R counter, Bits[13:8] (MSB)	Reference divider MSBs—upper six bits. The reference divider (also called the R divider or R counter) is 14 bits long. The upper six bits are in this register (default: 0x00).
0x013	[7:6]	Unused	Unused.
	[5:0]	6-bit A counter	A counter (part of N divider). The N divider is also called the feedback divider (default: 0x00).
0x014	[7:0]	13-bit B counter, Bits[7:0] (LSB)	B counter (part of N divider)—lower eight bits. The N divider is also called the feedback divider (default: 0x03).
0x015	[7:5]	Unused	Unused.
	[4:0]	13-bit B counter, Bits[12:8] (MSB)	B counter (part of N divider)—upper five bits. The N divider is also called the feedback divider (default: 0x00).
0x016	7	Set CP pin to $V_{CP}/2$	Sets the CP pin to one-half of the VCP supply voltage. 0: CP normal operation (default). 1: CP pin set to $V_{CP}/2$.
	6	Reset R counter	Resets R counter (R divider). 0: normal (default). 1: holds R counter in reset.
	5	Reset A and B counters	Resets A and B counters (part of N divider). 0: normal (default). 1: holds A and B counters in reset.
	4	Reset all counters	Resets R, A, and B counters. 0: normal (default). 1: holds R, A, and B counters in reset.
	3	B counter bypass	B counter bypass. This is valid only when operating the prescaler in FD mode. 0: normal (default). 1: B counter is set to divide-by-1. This allows the prescaler setting to determine the divide for the N divider.

Reg. Addr. (Hex)	Bits	Name	Description
	[2:0]	Prescaler P	Prescaler: DM = dual modulus; FD = fixed divide. Prescaler P is part of the feedback divider. See the VCO/VCXO Feedback Divider N—P, A, and B section of the datasheet for details.

Bit 2	Bit 1	Bit 0	Mode	Prescaler
0	0	0	FD	Divide-by-1.
0	0	1	FD	Divide-by-2.
0	1	0	DM	Divide-by-2 and divide-by-3 when A ≠ 0; divide-by-2 when A = 0.
0	1	1	DM	Divide-by-4 and divide-by-5 when A ≠ 0; divide-by-4 when A = 0.
1	0	0	DM	Divide-by-8 and divide-by-9 when A ≠ 0; divide-by-8 when A = 0.
1	0	1	DM	Divide-by-16 and divide-by-17 when A ≠ 0; divide-by-16 when A = 0.
1	1	0	DM	Divide-by-32 and divide-by-33 when A ≠ 0; divide-by-32 when A = 0 (default).
1	1	1	FD	Divide-by-3.

Reg. Addr. (Hex)	Bits	Name	Description
0x017	[7:2]	STATUS pin control	Selects the signal that appears at the STATUS pin. Register 0x01D[7] must be 0b to reprogram the STATUS pin.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Level or Dynamic Signal	Signal at STATUS Pin
0	0	0	0	0	0	LVL	Ground (dc) (default).
0	0	0	0	0	1	DYN	N divider output (after the delay).
0	0	0	0	1	0	DYN	R divider output (after the delay).
0	0	0	0	1	1	DYN	A divider output.
0	0	0	1	0	0	DYN	Prescaler output.
0	0	0	1	0	1	DYN	PFD up pulse.
0	0	0	1	1	0	DYN	PFD down pulse.
0	X	X	X	X	X	LVL	Ground (dc). Used for all settings of these bits that are not otherwise specified in this table.
							The selections that follow are also used for REFMON and LD pin control.
1	0	0	0	0	0	LVL	Ground (dc).
1	0	0	0	0	1	DYN	REF1 clock (differential reference when in differential mode).
1	0	0	0	1	0	DYN	REF2 clock (N/A in differential mode).
1	0	0	0	1	1	DYN	Selected reference to PLL (differential reference when in differential mode).
1	0	0	1	0	0	DYN	Unselected reference to PLL (not available in differential mode).
1	0	0	1	0	1	LVL	Status of selected reference (status of differential reference); active high.
1	0	0	1	1	0	LVL	Status of unselected reference (not available in differential mode); active high.
1	0	0	1	1	1	LVL	Status of REF1 frequency; active high.
1	0	1	0	0	0	LVL	Status of REF2 frequency; active high.
1	0	1	0	0	1	LVL	(Status of REF1 frequency) AND (status of REF2 frequency).
1	0	1	0	1	0	LVL	(DLD) AND (status of selected reference) AND (status of VCO).
1	0	1	0	1	1	LVL	Status of VCO frequency; active high.
1	0	1	1	0	0	LVL	Selected reference (low = REF1, high = REF2).
1	0	1	1	0	1	LVL	DLD; active high.
1	0	1	1	1	0	LVL	Holdover active; active high.
1	0	1	1	1	1	LVL	N/A. Do not use.
1	1	0	0	0	0	LVL	V_S (PLL power supply).
1	1	0	0	0	1	DYN	$\overline{\text{REF1 clock}}$ (differential reference when in differential mode).
1	1	0	0	1	0	DYN	$\overline{\text{REF2 clock}}$ (not available in differential mode).
1	1	0	0	1	1	DYN	$\overline{\text{Selected reference to PLL}}$ (differential reference when in differential mode).
1	1	0	1	0	0	DYN	$\overline{\text{Unselected reference to PLL}}$ (not available when in differential mode).
1	1	0	1	0	1	LVL	Status of selected reference (status of differential reference); active low.
1	1	0	1	1	0	LVL	Status of unselected reference (not available in differential mode); active low.
1	1	0	1	1	1	LVL	Status of REF1 frequency; active low.
1	1	1	0	0	0	LVL	Status of REF2 frequency; active low.
1	1	1	0	0	1	LVL	$\overline{\text{(Status of REF1 frequency) AND (status of REF2 frequency)}}$.
1	1	1	0	1	0	LVL	$\overline{\text{(DLD) AND (status of selected reference) AND (status of VCO)}}$.
1	1	1	0	1	1	LVL	Status of VCO frequency; active low.
1	1	1	1	0	0	LVL	Selected reference (low = REF2, high = REF1).
1	1	1	1	0	1	LVL	DLD; active low.
1	1	1	1	1	0	LVL	Holdover active; active low.
1	1	1	1	1	1	LVL	N/A. Do not use.

Reg. Addr. (Hex)	Bits	Name	Description		
	[1:0]	Antibacklash pulse width	**Bit 1**	**Bit 0**	**Antibacklash Pulse Width (ns)**
			0	0	2.9 (default)
			0	1	1.3
			1	0	6.0
			1	1	2.9
0x018	7	Enable CMOS reference input dc offset	Enables dc offset in single-ended CMOS input mode to prevent chattering when ac-coupled and input is lost. 0: disables dc offset (default). 1: enables dc offset.		
	[6:5]	Lock detect counter	Required consecutive number of PFD cycles with edges inside lock detect window before the DLD indicates a locked condition.		
			Bit 6	**Bit 5**	**PFD Cycles to Determine Lock**
			0	0	5 (default)
			0	1	16
			1	0	64
			1	1	255
	4	Digital lock detect window	If the time difference of the rising edges at the inputs to the PFD is less than the lock detect window time, the digital lock detect flag is set. The flag remains set until the time difference is greater than the loss-of-lock threshold. 0: high range (default). The default setting is 3.5 ns. 1: low range.		
	3	Disable digital lock detect	Digital lock detect operation. 0: normal lock detect operation (default). 1: disables lock detect.		
	[2:1]	VCO calibration divider	Divider used to generate the VCO calibration clock from the PLL reference clock (see the VCO Calibration section for the recommended setting of the VCO calibration divider based on the PFD rate).		
			Bit 2	**Bit 1**	**VCO Calibration Clock Divider**
			0	0	2. This setting is fine for PFD frequencies < 12.5 MHz. The PFD frequency is f_{REF}/R.
			0	1	4. This setting is fine for PFD frequencies < 12.5 MHz. The PFD frequency is f_{REF}/R.
			1	0	8. This setting is fine for PFD frequencies < 50 MHz.
			1	1	16. (default). This setting is fine for any PFD frequency, but it also results in the longest VCO calibration time.
	0	VCO calibration now	Initiates VCO calibration. This bit must be toggled from 0b to 1b in the active registers. The sequence to initiate a calibration is as follows: program to 0b, followed by an IO_UPDATE (Register 0x232[0]); then program to 1b, followed by another IO_UPDATE (Register 0x232[0]). This sequence gives complete control over when the VCO calibration occurs relative to the programming of other registers that can impact the calibration (default = 0b). Note that the VCO divider (Register 0x1E0[2:0]) must not be static during VCO calibration.		
0x019	[7:6]	R, A, B counters $\overline{\text{SYNC}}$ pin reset	**Bit 7**	**Bit 6**	**Action**
			0	0	Does nothing on $\overline{\text{SYNC}}$ (default).
			0	1	Asynchronous reset.
			1	0	Synchronous reset.
			1	1	Does nothing on $\overline{\text{SYNC}}$.
	[5:3]	R path delay	R path delay, see Table 2 (default: 0x0).		
	[2:0]	N path delay	N path delay, see Table 2 (default: 0x0).		
0x01A	7	Enable STATUS pin divider	Enables a divide-by-4 on the STATUS pin. This makes it easier to look at low duty-cycle signals out of the R and N dividers. 0: divide-by-4 disabled on STATUS pin (default). 1: divide-by-4 enabled on STATUS pin.		
	6	Ref freq monitor threshold	Sets the reference (REF1/REF2) frequency monitor's detection threshold frequency. This does not affect the VCO frequency monitor's detection threshold (see Table 17: REF1, REF2, and VCO frequency status monitor parameter). 0: frequency valid if frequency is above 1.02 MHz (default). 1: frequency valid if frequency is above 6 kHz.		

Reg. Addr. (Hex)	Bits	Name	Description							
	[5:0]	LD pin control	Selects the signal that is connected to the LD pin.							
			Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Level or Dynamic Signal	Signal at LD Pin
			0	0	0	0	0	0	LVL	Digital lock detect (high = lock; low = unlock, default).
			0	0	0	0	0	1	DYN	P-channel, open-drain lock detect (analog lock detect).
			0	0	0	0	1	0	DYN	N-channel, open-drain lock detect (analog lock detect).
			0	0	0	0	1	1	HIZ	Tristate (high-Z) LD pin.
			0	0	0	1	0	0	CUR	Current source lock detect (110 µA when DLD is true).
			0	X	X	X	X	X	LVL	Ground (dc). Used for all settings of these bits that are not otherwise specified in this table.
										The selections that follow are also used for REFMON and STATUS pin control.
			1	0	0	0	0	0	LVL	Ground (dc).
			1	0	0	0	0	1	DYN	REF1 clock (differential reference when in differential mode).
			1	0	0	0	1	0	DYN	REF2 clock (N/A in differential mode).
			1	0	0	0	1	1	DYN	Selected reference to PLL (differential reference when in differential mode).
			1	0	0	1	0	0	DYN	Unselected reference to PLL (not available in differential mode).
			1	0	0	1	0	1	LVL	Status of selected reference (status of differential reference); active high.
			1	0	0	1	1	0	LVL	Status of unselected reference (not available in differential mode); active high.
			1	0	0	1	1	1	LVL	Status of REF1 frequency; active high.
			1	0	1	0	0	0	LVL	Status of REF2 frequency; active high.
			1	0	1	0	0	1	LVL	(Status of REF1 frequency) AND (status of REF2 frequency).
			1	0	1	0	1	0	LVL	(DLD) AND (status of selected reference) AND (status of VCO).
			1	0	1	0	1	1	LVL	Status of VCO frequency; active high.
			1	0	1	1	0	0	LVL	Selected reference (low = REF1, high = REF2).
			1	0	1	1	0	1	LVL	DLD; active high.
			1	0	1	1	1	0	LVL	Holdover active; active high.
			1	0	1	1	1	1	LVL	N/A. Do not use.
			1	1	0	0	0	0	LVL	V_S (PLL power supply).
			1	1	0	0	0	1	DYN	$\overline{\text{REF1 clock}}$ (differential reference when in differential mode).
			1	1	0	0	1	0	DYN	$\overline{\text{REF2 clock}}$ (not available in differential mode).
			1	1	0	0	1	1	DYN	$\overline{\text{Selected reference to PLL}}$ (differential reference when in differential mode).
			1	1	0	1	0	0	DYN	$\overline{\text{Unselected reference to PLL}}$ (not available when in differential mode).
			1	1	0	1	0	1	LVL	Status of selected reference (status of differential reference); active low.
			1	1	0	1	1	0	LVL	Status of unselected reference (not available in differential mode); active low.
			1	1	0	1	1	1	LVL	Status of REF1 frequency; active low.
			1	1	1	0	0	0	LVL	Status of REF2 frequency; active low.
			1	1	1	0	0	1	LVL	$\overline{\text{(Status of REF1 frequency) AND (status of REF2 frequency).}}$
			1	1	1	0	1	0	LVL	$\overline{\text{(DLD) AND (status of selected reference) AND (status of VCO).}}$
			1	1	1	0	1	1	LVL	Status of VCO frequency; active low.
			1	1	1	1	0	0	LVL	Selected reference (low = REF2, high = REF1).
			1	1	1	1	0	1	LVL	DLD; active low.
			1	1	1	1	1	0	LVL	Holdover active; active low.
			1	1	1	1	1	1	LVL	N/A. Do not use.
0x01B	7	Enable VCO frequency monitor	Enables or disables the VCO frequency monitor. 0: disables the VCO frequency monitor (default). 1: enables the VCO frequency monitor.							
	6	$\overline{\text{Enable}}$ REF2 (REFIN) frequency monitor	Enables or disables the REF2 frequency monitor. 0: disables the REF2 frequency monitor (default). 1: enables the REF2 frequency monitor.							
	5	Enable REF1 (REFIN) frequency monitor	REF1 (REFIN) frequency monitor enabled; this is for both REF1 (single-ended) and REFIN (differential) inputs (as selected by differential reference mode). 0: disables the REF1 (REFIN) frequency monitor (default). 1: enables the REF1 (REFIN) frequency monitor.							

Reg. Addr. (Hex)	Bits	Name	Description						
	[4:0]	REFMON pin control	Selects the signal that is connected to the REFMON pin.						
			Bit 4	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Level or Dynamic Signal**	**Signal at REFMON Pin**
			0	0	0	0	0	LVL	Ground, dc (default).
			0	0	0	0	1	DYN	REF1 clock (differential reference when in differential mode).
			0	0	0	1	0	DYN	REF2 clock (N/A in differential mode).
			0	0	0	1	1	DYN	Selected reference to PLL (differential reference when in differential mode).
			0	0	1	0	0	DYN	Unselected reference to PLL (not available in differential mode).
			0	0	1	0	1	LVL	Status of selected reference (status of differential reference); active high.
			0	0	1	1	0	LVL	Status of unselected reference (not available in differential mode); active high.
			0	0	1	1	1	LVL	Status of REF1 frequency; active high.
			0	1	0	0	0	LVL	Status of REF2 frequency; active high.
			0	1	0	0	1	LVL	(Status REF1 frequency) AND (status REF2 frequency).
			0	1	0	1	0	LVL	(DLD) AND (status of selected reference) AND (status of VCO).
			0	1	0	1	1	LVL	Status of VCO frequency (active high).
			0	1	1	0	0	LVL	Selected reference (low = REF1, high = REF2).
			0	1	1	0	1	LVL	DLD; active high.
			0	1	1	1	0	LVL	Holdover active; active high.
			0	1	1	1	1	LVL	N/A. Do not use.
			1	0	0	0	0	LVL	V_S (PLL power supply).
			1	0	0	0	1	DYN	$\overline{\text{REF1 clock}}$ (differential reference when in differential mode).
			1	0	0	1	0	DYN	$\overline{\text{REF2 clock}}$ (not available in differential mode).
			1	0	0	1	1	DYN	$\overline{\text{Selected reference to PLL}}$ (differential reference when in differential mode).
			1	0	1	0	0	DYN	$\overline{\text{Unselected reference to PLL}}$ (not available when in differential mode).
			1	0	1	0	1	LVL	Status of selected reference (status of differential reference); active low.
			1	0	1	1	0	LVL	Status of unselected reference (not available in differential mode); active low.
			1	0	1	1	1	LVL	Status of REF1 frequency; active low.
			1	1	0	0	0	LVL	Status of REF2 frequency; active low.
			1	1	0	0	1	LVL	$\overline{\text{(Status of REF1 frequency) AND (status of REF2 frequency).}}$
			1	1	0	1	0	LVL	$\overline{\text{(DLD) AND (status of selected reference) AND (status of VCO).}}$
			1	1	0	1	1	LVL	Status of VCO frequency; active low.
			1	1	1	0	0	LVL	Selected reference (low = REF2, high = REF1).
			1	1	1	0	1	LVL	DLD; active low.
			1	1	1	1	0	LVL	Holdover active; active low.
			1	1	1	1	1	LVL	N/A. Do not use.
0x01C	7	Disable switchover deglitch	Disables or enables the switchover deglitch circuit. 0: enables the switchover deglitch circuit (default). 1: disables the switchover deglitch circuit.						
	6	Select REF2	If Register 0x01C[5] = 0b, selects the reference for PLL when in manual; register selected reference control. 0: selects REF1 (default). 1: selects REF2.						
	5	Use REF_SEL pin	If Register 0x01C[4] = 0b (manual), sets the method of PLL reference selection. 0: uses Register 0x01C[6] (default). 1: uses REF_SEL pin.						
	4	Enable automatic reference switchover	Automatic or manual reference switchover. Single-ended reference mode must be selected by Register 0x01C[0] = 0b. 0: manual reference switchover (default). 1: automatic reference switchover. Setting this bit also powers on REF1 and REF2 and overrides the settings in Register 0x01C[2:1].						
	3	Stay on REF2	Stays on REF2 after switchover. 0: returns to REF1 automatically when REF1 status is good again (default). 1: stays on REF2 after switchover. Does not automatically return to REF1.						
	2	Enable REF2	This bit turns the REF2 power on. This bit is overridden when automatic reference switchover is enabled. 0: REF2 power off (default). 1: REF2 power on.						
	1	Enable REF1	This bit turns the REF1 power on. This bit is overridden when automatic reference switchover is enabled. 0: REF1 power off (default). 1: REF1 power on.						
	0	Enable differential ref	Selects the PLL reference mode, differential or single-ended. Register 0x01C[2:1] should be cleared when this bit is set. 0: single-ended reference mode (default); 1: differential reference mode.						

Reg. Addr. (Hex)	Bits	Name	Description
0x01D	7	Enable STATUS_EEPROM at STATUS pin	Enables the STATUS_EEPROM signal at the STATUS pin. 0: the STATUS pin is controlled by the Register 0x017[7:2] selection. 1: selects the STATUS_EEPROM signal at the STATUS pin. This bit overrides the Register 0x017[7:2] selection (default).
	6	Enable XTAL OSC	Enables the maintaining amplifier needed by a crystal oscillator at the PLL reference input. 0: crystal oscillator maintaining amplifier disabled (default). 1: crystal oscillator maintaining amplifier enabled.
	5	Enable clock doubler	Enables PLL reference input clock doubler. 0: doubler disabled (default). 1: doubler enabled.
	4	Disable PLL status register	Disables the PLL status register readback. 0: PLL status register enabled (default). 1: PLL status register disabled. If this bit is set, Register 0x01F is not automatically updated.
	3	Enable LD pin comparator	Enables the LD pin voltage comparator. Used with the LD pin current source lock detect mode. When the AD9520-2 is in internal (automatic) holdover mode, this bit enables the use of the voltage on the LD pin to determine if the PLL was previously in a locked state (see Figure 47). Otherwise, this can be used with the REFMON and STATUS pins to monitor the voltage on the LD pin. 0: disables LD pin comparator and ignores the LD pin voltage; the automatic/internal holdover controller treats this pin as true (high, default). 1: enables the LD pin comparator (uses the LD pin voltage to determine if the PLL was previously locked).
	2	Unused	Unused.
	1	Enable external holdover	Enables the external hold control through the $\overline{\text{SYNC}}$ pin. (This bit disables the internal holdover mode.) 0: automatic holdover mode; holdover controlled by the automatic holdover circuit (default). 1: external holdover mode; holdover controlled by the $\overline{\text{SYNC}}$ pin.
	0	Enable holdover	Enables the internally controlled holdover function. 0: holdover disabled (default). 1: holdover enabled.
0x01E	[7:5]	Unused	Unused.
	[4:3]	External zero delay feedback channel divider select	**Bit 4** / **Bit 3** / **Selection of Channel Divider for Use in the External Zero-Delay Path** 0 / 0 / Selects Channel Divider 0 (default). 0 / 1 / Selects Channel Divider 1. 1 / 0 / Selects Channel Divider 2. 1 / 1 / Selects Channel Divider 3.
	2	Enable external zero delay	Selects which zero delay mode to use. 0: enables internal zero delay mode if Register 0x01E[1] = 1 (default). 1: enables external zero delay mode if Register 0x01E[1] = 1.
	1	Enable zero delay	Enables zero delay function. 0: disables zero delay function (default). 1: enables zero delay function.
	0	Unused	Unused.
0x01F	7	Unused	Unused.
	6	VCO calibration finished (read only)	Readback register. Indicates the status of the VCO calibration. 0: VCO calibration not finished. 1: VCO calibration finished.
	5	Holdover active (read only)	Readback register. Indicates if the part is in the holdover state (see Figure 47). Note that this is not the same as holdover enabled. 0: not in holdover state. 1: holdover state active.
	4	REF2 selected (read only)	Readback register. Indicates which PLL reference is selected as the input to the PLL. 0: REF1 selected (or differential reference if in differential mode). 1: REF2 selected.
	3	VCO frequency > threshold (read only)	Readback register. Indicates if the VCO frequency is greater than the threshold (see Table 17: REF1, REF2, and VCO frequency status monitor parameter). 0: VCO frequency is less than the threshold. 1: VCO frequency is greater than the threshold.
	2	REF2 frequency > threshold (read only)	Readback register. Indicates if the frequency of the signal at REF2 is greater than the threshold frequency set by Register 0x01A[6]. 0: REF2 frequency is less than the threshold frequency. 1: REF2 frequency is greater than the threshold frequency.
	1	REF1 frequency > threshold (read only)	Readback register. Indicates if the frequency of the signal at REF1 is greater than the threshold frequency set by Register 0x01A[6]. 0: REF1 frequency is less than the threshold frequency. 1: REF1 frequency is greater than the threshold frequency.
	0	Digital lock detect (read only)	Readback register. Digital lock detect. 0: PLL is not locked. 1: PLL is locked.

Table 55. Output Driver Control

Reg. Addr. (Hex)	Bits	Name	Description
0x0F0	7	OUT0 format	Selects the output type for OUT0. 0: LVPECL (default). 1: CMOS.
	[6:5]	OUT0 CMOS configuration	Sets the CMOS output configuration for OUT0 when Register 0x0F0[7] = 1.

Bits[6:5]	OUT0A	OUT0B
00	Tristate	Tristate
01	On	Tristate
10	Tristate	On
11 (default)	On	On

| | | Sets the output polarity for OUT0. |

Bit 7	Bit 4	Bit 3	Output Type	OUT0A	OUT0B
0 (default)	X	0 (default)	LVPECL	Noninverting	Inverting
0	X	1	LVPECL	Inverting	Noninverting
1	0 (default)	0	CMOS	Noninverting	Noninverting
1	0	1	CMOS	Inverting	Inverting
1	1	0	CMOS	Noninverting	Inverting
1	1	1	CMOS	Inverting	Noninverting

| | | OUT0 LVPECL differential voltage | Sets the LVPECL output differential voltage (V_{OD}). |

Bit 2	Bit 1	V_{OD} (mV)
0	0	400
0	1	600
1 (default)	0 (default)	780
1	1	960

	0	OUT0 LVPECL power-down	LVPECL power-down. 0: normal operation (default). 1: safe power-down.
0x0F1	[7:0]	OUT1 control	This register controls OUT1, and the bit assignments for this register are identical to Register 0x0F0.
0x0F2	[7:0]	OUT2 control	This register controls OUT2, and the bit assignments for this register are identical to Register 0x0F0.
0x0F3	[7:0]	OUT3 control	This register controls OUT3, and the bit assignments for this register are identical to Register 0x0F0.
0x0F4	[7:0]	OUT4 control	This register controls OUT4, and the bit assignments for this register are identical to Register 0x0F0.
0x0F5	[7:0]	OUT5 control	This register controls OUT5, and the bit assignments for this register are identical to Register 0x0F0.
0x0F6	[7:0]	OUT6 control	This register controls OUT6, and the bit assignments for this register are identical to Register 0x0F0.
0x0F7	[7:0]	OUT7 control	This register controls OUT7, and the bit assignments for this register are identical to Register 0x0F0.
0x0F8	[7:0]	OUT8 control	This register controls OUT8, and the bit assignments for this register are identical to Register 0x0F0.
0x0F9	[7:0]	OUT9 control	This register controls OUT9, and the bit assignments for this register are identical to Register 0x0F0.
0x0FA	[7:0]	OUT10 control	This register controls OUT10, and the bit assignments for this register are identical to Register 0x0F0.
0x0FB	[7:0]	OUT11 control	This register controls OUT11, and the bit assignments for this register are identical to Register 0x0F0.
0x0FC	7	CSDLD en OUT7	OUT7 is enabled only if the CSDLD signal is high.

Bit 7	CSDLD Signal	OUT7 Enable Status
0	0	Not affected by CSDLD signal (default).
1	0	Asynchronous power-down.
1	1	Asynchronously enables OUT7 if not powered down by other settings. For this feature, use current source digital lock detect and set the enable LD pin comparator bit (Register 0x01D[3]).

	6	CSDLD en OUT6	OUT6 is enabled only if CSDLD is high. Setting is identical to Register 0x0FC[7].
	5	CSDLD en OUT5	OUT5 is enabled only if CSDLD is high. Setting is identical to Register 0x0FC[7].
	4	CSDLD en OUT4	OUT4 is enabled only if CSDLD is high. Setting is identical to Register 0x0FC[7].
	3	CSDLD en OUT3	OUT3 is enabled only if CSDLD is high. Setting is identical to Register 0x0FC[7].
	2	CSDLD en OUT2	OUT2 is enabled only if CSDLD is high. Setting is identical to Register 0x0FC[7].
	1	CSDLD en OUT1	OUT1 is enabled only if CSDLD is high. Setting is identical to Register 0x0FC[7].
	0	CSDLD en OUT0	OUT0 is enabled only if CSDLD is high. Setting is identical to Register 0x0FC[7].
0x0FD	[7:4]	Unused	Unused.
	3	CSDLD en OUT11	OUT11 is enabled only if CSDLD is high. Setting is identical to Register 0x0FC[7].
	2	CSDLD en OUT10	OUT10 is enabled only if CSDLD is high. Setting is identical to Register 0x0FC[7].
	1	CSDLD en OUT9	OUT9 is enabled only if CSDLD is high. Setting is identical to Register 0x0FC[7].
	0	CSDLD en OUT8	OUT8 is enabled only if CSDLD is high. Setting is identical to Register 0x0FC[7].

Table 56. LVPECL Channel Dividers

Reg. Addr. (Hex)	Bits	Name	Description
0x190	[7:4]	Divider 0 low cycles	Number of clock cycles (minus 1) of the divider input during which the divider output stays low. A value of 0x7 means that the divider is low for eight input clock cycles (default: 0x7).
	[3:0]	Divider 0 high cycles	Number of clock cycles (minus 1) of the divider input during which the divider output stays high. A value of 0x7 means that the divider is high for eight input clock cycles (default: 0x7).
0x191	7	Divider 0 bypass	Bypasses and powers down the divider; routes input to divider output. 0: uses divider (default). 1: bypasses divider.
	6	Divider 0 ignore SYNC	Ignores SYNC. 0: obeys chip-level SYNC signal (default). 1: ignores chip-level SYNC signal.
	5	Divider 0 force high	Forces divider output to a specific state. This requires that ignore SYNC also be set. Note that this bit has no effect if the channel divider is bypassed, but the driver polarity can still be reversed. 0: divider output is forced to low (default). 1: divider output is forced to the setting stored in Bit 4 of this register.
	4	Divider 0 start high	Selects clock output to start high or start low. 0: starts low (default). 1: starts high.
	[3:0]	Divider 0 phase offset	Phase offset (default: 0x0).
0x192	[7:3]	Unused	Unused.
	2	Channel 0 power-down	Channel 0 powers down. 0: normal operation (default). 1: powered down. (Setting this bit puts OUT0/$\overline{\text{OUT0}}$, OUT1/$\overline{\text{OUT1}}$, and OUT2/$\overline{\text{OUT2}}$ into safe power-down mode.)
	1	Channel 0 direct-to-output	Connects OUT0, OUT1, and OUT2 to Divider 0 or directly to VCO or CLK. 0: OUT0, OUT1, and OUT2 are connected to Divider 0 (default). 1: If Register 0x1E1[1:0] = 10b, the VCO is routed directly to OUT0, OUT1, and OUT2. If Register 0x1E1[1:0] = 00b, the CLK is routed directly to OUT0, OUT1, and OUT2. If Register 0x1E1[1:0] = 01b, there is no effect.
	0	Disable Divider 0 DCC	Duty-cycle correction function. 0: enables duty-cycle correction (default). 1: disables duty-cycle correction.
0x193	[7:4]	Divider 1 low cycles	Number of clock cycles (minus 1) of the divider input during which the divider output stays low. A value of 0x3 means that the divider is low for four input clock cycles (default: 0x3).
	[3:0]	Divider 1 high cycles	Number of clock cycles (minus 1) of the divider input during which the divider output stays high. A value of 0x3 means that the divider is high for four input clock cycles (default: 0x3).
0x194	7	Divider 1 bypass	Bypasses and powers down the divider; routes input to divider output. 0: uses divider (default). 1: bypasses divider.
	6	Divider 1 ignore SYNC	Ignores SYNC. 0: obeys chip-level SYNC signal (default). 1: ignores chip-level SYNC signal.
	5	Divider 1 force high	Forces divider output to a specific state. This requires that ignore SYNC also be set. Note that this bit has no effect if the channel divider is bypassed, but the driver polarity can still be reversed. 0: divider output is forced to low (default). 1: divider output is forced to the setting stored in Bit 4 of this register.
	4	Divider 1 start high	Selects clock output to start high or start low. 0: starts low (default). 1: starts high.
	[3:0]	Divider 1 phase offset	Phase offset (default: 0x0).

Reg. Addr. (Hex)	Bits	Name	Description
0x195	[7:3]	Unused	Unused.
	2	Channel 1 power-down	Channel 1 powers down. 0: normal operation (default). 1: powered down. (Setting this bit puts OUT3/$\overline{\text{OUT3}}$, OUT4/$\overline{\text{OUT4}}$, and OUT5/$\overline{\text{OUT5}}$ into safe power-down mode.)
	1	Channel 1 direct-to-output	Connects OUT3, OUT4, and OUT5 to Divider 1 or directly to VCO or CLK. 0: OUT3, OUT4, and OUT5 are connected to Divider 1 (default). 1: If Register 0x1E1[1:0] = 10b, the VCO is routed directly to OUT3, OUT4, and OUT5. If Register 0x1E1[1:0] = 00b, the CLK is routed directly to OUT3, OUT4, and OUT5. If Register 0x1E1[1:0] = 01b, there is no effect.
	0	Disable Divider 1 DCC	Duty-cycle correction function. 0: enables duty-cycle correction (default). 1: disables duty-cycle correction.
0x196	[7:4]	Divider 2 low cycles	Number of clock cycles (minus 1) of the divider input during which the divider output stays low. A value of 0x1 means that the divider is low for two input clock cycles (default: 0x1).
	[3:0]	Divider 2 high cycles	Number of clock cycles (minus 1) of the divider input during which the divider output stays high. A value of 0x1 means that the divider is high for two input clock cycles (default: 0x1).
0x197	7	Divider 2 bypass	Bypasses and powers down the divider; routes input to divider output. 0: uses divider (default). 1: bypasses divider.
	6	Divider 2 ignore SYNC	Ignores SYNC. 0: obeys chip-level SYNC signal (default). 1: ignores chip-level SYNC signal.
	5	Divider 2 force high	Forces divider output to a specific state. This requires that ignore SYNC also be set. Note that this bit has no effect if the channel divider is bypassed, but the driver polarity can still be reversed. 0: divider output is forced to low (default). 1: divider output is forced to the setting stored in Bit 4 of this register.
	4	Divider 2 start high	Selects clock output to start high or start low. 0: starts low (default). 1: starts high.
	[3:0]	Divider 2 phase offset	Phase offset (default: 0x0).
0x198	[7:3]	Unused	Unused.
	2	Channel 2 power-down	Channel 2 powers down. 0: normal operation (default). 1: powered down. (Setting this bit puts OUT6/$\overline{\text{OUT6}}$, OUT7/$\overline{\text{OUT7}}$, and OUT8/$\overline{\text{OUT8}}$ into safe power-down mode.)
	1	Channel 2 direct-to-output	Connects OUT6, OUT7, and OUT8 to Divider 2 or directly to VCO or CLK. 0: OUT6, OUT7, and OUT8 are connected to Divider 2 (default). 1: If Register 0x1E1[1:0] = 10b, the VCO is routed directly to OUT6, OUT7, and OUT8. If Register 0x1E1[1:0] = 00b, the CLK is routed directly to OUT6, OUT7, and OUT8. If Register 0x1E1[1:0] = 01b, there is no effect.
	0	Disable Divider 2 DCC	Duty-cycle correction function. 0: enables duty-cycle correction (default). 1: disables duty-cycle correction.
0x199	[7:4]	Divider 3 low cycles	Number of clock cycles (minus 1) of the divider input during which the divider output stays low. A value of 0x0 means that the divider is low for one input clock cycle (default: 0x0).
	[3:0]	Divider 3 high cycles	Number of clock cycles (minus 1) of the divider input during which the divider output stays high. A value of 0x0 means that the divider is high for one input clock cycle (default: 0x0).

Reg. Addr. (Hex)	Bits	Name	Description
0x19A	7	Divider 3 bypass	Bypasses and powers down the divider; routes input to divider output. 0: uses divider (default). 1: bypasses divider.
	6	Divider 3 ignore SYNC	Ignores SYNC. 0: obeys chip-level SYNC signal (default). 1: ignores chip-level SYNC signal.
	5	Divider 3 force high	Forces divider output to a specific state. This requires that ignore SYNC also be set. Note that this bit has no effect if the channel divider is bypassed, but the driver polarity can still be reversed. 0: divider output is forced to low (default). 1: divider output is forced to the setting stored in Bit 4 of this register.
	4	Divider 3 start high	Selects clock output to start high or start low. 0: starts low (default). 1: starts high.
	[3:0]	Divider 3 phase offset	Phase offset (default: 0x0).
0x19B	[7:3]	Unused	Unused.
	2	Channel 3 power-down	Channel 3 powers down. 0: normal operation (default). 1: powered down. (Setting this bit puts OUT9/$\overline{\text{OUT9}}$, OUT10/$\overline{\text{OUT10}}$, and OUT11/$\overline{\text{OUT11}}$ into safe power-down mode.)
	1	Channel 3 direct-to-output	Connects OUT9, OUT10, and OUT11 to Divider 3 or directly to VCO or CLK. 0: OUT9, OUT10, and OUT11 are connected to Divider 3 (default). 1: If Register 0x1E1[1:0] = 10b, the VCO is routed directly to OUT9, OUT10, and OUT11. If Register 0x1E1[1:0] = 00b, the CLK is routed directly to OUT9, OUT10, and OUT11. If Register 0x1E1[1:0] = 01b, there is no effect.
	0	Disable Divider 3 DCC	Duty-cycle correction function. 0: enables duty-cycle correction (default). 1: disables duty-cycle correction.

Table 57. VCO Divider and CLK Input

Reg. Addr. (Hex)	Bits	Name	Description			
0x1E0	[2:0]	VCO divider	**Bit 2**	**Bit 1**	**Bit 0**	**Divide**
			0	0	0	2 (default)
			0	0	1	3
			0	1	0	4
			0	1	1	5
			1	0	0	6
			1	0	1	Output static
			1	1	0	1 (bypass)
			1	1	1	Output static
0x1E1	[7:5]	Unused	Unused.			
	4	Power down clock input section	Powers down the clock input section (including CLK buffer, VCO divider, and CLK tree). 0: normal operation (default). 1: power-down.			
	3	Power down VCO clock interface	Powers down the interface block between VCO and clock distribution. 0: normal operation (default). 1: power-down.			
	2	Power down VCO and CLK	Powers down both the VCO and the CLK input. 0: normal operation (default). 1: power-down.			
	1	Select VCO or CLK	Selects either the VCO or the CLK as the input to VCO divider. 0: selects external CLK as input to VCO divider (default). 1: selects VCO as input to VCO divider; VCO divider cannot be bypassed when this bit is set. This bit must be set to use the PLL with the internal VCO.			
	0	Bypass VCO divider	Bypasses or uses the VCO divider. 0: uses VCO divider (default). 1: bypasses VCO divider; VCO cannot be selected as input when this bit is set.			

Table 58. System

Reg. Addr. (Hex)	Bits	Name	Description
0x230	[7:4]	Unused	Unused.
	3	Disable power on SYNC	Powers on SYNC mode. Used to disable the antiruntpulse circuitry. 0: enables the antiruntpulse circuitry (default). 1: disables the antiruntpulse circuitry.
	2	Power down SYNC	Powers down the SYNC function. 0: normal operation of the SYNC function (default). 1: powers down SYNC circuitry.
	1	Power down distribution reference	Powers down the reference for the distribution section. 0: normal operation of the reference for the distribution section (default). 1: powers down the reference for the distribution section.
	0	Soft SYNC	The soft SYNC bit works in the same way as the $\overline{\text{SYNC}}$ pin, except that the polarity of the bit is reversed. That is, a high level forces selected channels into a predetermined static state, and a 1b-to-0b transition triggers a SYNC. 0: same as $\overline{\text{SYNC}}$ pin high. 1: same as $\overline{\text{SYNC}}$ pin low.

Table 59. Update All Registers

Reg. Addr. (Hex)	Bits	Name	Description
0x232	[7:1]	Unused	Unused.
	0	IO_UPDATE	This bit must be set to 1b to transfer the contents of the buffer registers into the active registers. This transfer occurs on the next SCLK rising edge. This bit is self-clearing; that is, it does not have to be set back to 0b. 1 (self-clearing): updates all active registers to the contents of the buffer registers.

Table 60. EEPROM Buffer Segment

Reg. Addr. (Hex)	Bits	Name	Description
0xA00 to 0xAFF		EEPROM buffer segment	The EEPROM buffer segment section stores the starting address and number of bytes that are to be stored and then read back to and from the EEPROM. Because the AD9520-2 register space is noncontiguous, the EEPROM controller uses the starting address and number of bytes in the AD9520-2 register space to store and retrieve from the EEPROM. There are two types of entries in the EEPROM buffer segment: data transfers and operational codes. For a data transfer, Bit 7 of the command byte is set to 0b. The remaining seven bits are the size of the transfer, minus 1 (that is, 0x01 indicates a 2-byte transfer). The starting address (MSB first) of the transfer is contained in the two bytes of the EEPROM buffer segment that immediately follow the data transfer command. For an operational code, Bit 7 of the command byte is set to 1b and is a special instruction for the EEPROM controller. There are two operational codes: IO_UPDATE and end of data. The IO_UPDATE operational code instructs the EEPROM controller to transfer the AD9520-2 register values into the active register space (and is functionally equivalent to writing 0x01 to Register 0x232). The end-of-data operational code informs the EEPROM controller that the end of data has been reached and to terminate the transfer. The last byte of the EEPROM buffer segment must contain an end-of-data operational code. Using the on-chip default setting of the EEPROM buffer segment registers, the EEPROM controller transfers all register values to/from the EEPROM, and an IO_UPDATE is issued after transfer. Therefore, the user does not normally need to alter the EEPROM buffer segment. See the Programming the EEPROM Buffer Segment section for more information.

Table 61. EEPROM Control

Reg. Addr. (Hex)	Bits	Name	Description
0xB00	[7:1]	Unused	Unused.
	0	STATUS_EEPROM (read only)	This read-only register indicates the status of the data transfer between the EEPROM and the buffer register bank during the writing and reading of the EEPROM. This signal is also available at the STATUS pin when Register 0x01D[7] is set. 0: data transfer is complete. 1: data transfer is not complete.
0xB01	[7:1]	Unused	Unused.
	0	EEPROM data error (read only)	This read-only register indicates an error during the data transfer between the EEPROM and the buffer. 0: no error. Data is correct. 1: incorrect data detected.
0xB02	[7:2]	Unused	Unused.
	1	SOFT_EEPROM	When the EEPROM pin is tied low, setting SOFT_EEPROM resets the AD9520-2 using the settings saved in the EEPROM. 1: soft reset with EEPROM settings (self-clearing).
	0	Enable EEPROM write	Enables the user to write to the EEPROM. 0: EEPROM write protection is enabled. User cannot write to the EEPROM (default). 1: EEPROM write protection is disabled. User can write to the EEPROM. Once an EEPROM save/load transfer is complete, the user must wait a minimum of 10 µs before starting the next EEPROM save/load transfer.
0xB03	[7:1]	Unused	Unused.
	0	REG2EEPROM	Transfers data from the buffer register to the EEPROM (self-clearing). 1: setting this bit initiates the data transfer from the buffer register to the EEPROM (writing process); it is reset by the I^2C master after the data transfer is complete. Once an EEPROM save/load transfer is complete, the user must wait a minimum of 10 µs before starting the next EEPROM save/load transfer.

APPLICATIONS INFORMATION

FREQUENCY PLANNING USING THE AD9520-2

The AD9520-2 is a highly flexible PLL. When choosing the PLL settings and version of the AD9520-2, keep in mind the following guidelines.

The AD9520-2 has four frequency dividers: the reference (or R) divider, the feedback (or N) divider, the VCO divider, and the channel divider. When trying to achieve a particularly difficult frequency divide ratio requiring a large amount of frequency division, some of the frequency division can be done by either the VCO divider or the channel divider, thus allowing a higher phase detector frequency and more flexibility in choosing the loop bandwidth.

Within the AD9520-2 family, lower VCO frequencies generally result in slightly better jitter. The difference in integrated jitter (from 12 kHz to 20 MHz offset) for the same output frequency is usually less than 150 fs over the entire VCO frequency range (1.4 GHz to 2.95 GHz) of the AD9520-2 family. If the desired frequency plan can be achieved with a version of the AD9520-2 that has a lower VCO frequency, choosing the lower frequency part results in the best phase noise and the lowest jitter. However, choosing a higher VCO frequency can result in more flexibility in frequency planning.

When determining a starting point, choosing a nominal charge pump current in the middle of the allowable range allows the designer to increase or decrease the charge pump current and, thus, allows fine-tuning of the PLL loop bandwidth in either direction.

Analog Devices has an AD9520 configuration tool that can determine the best PLL configuration, based on the user's input and output frequencies. It can also design the loop filter based on user requirements.

In addition to the configuration tool, ADIsimCLK is a powerful PLL modeling tool and a very accurate tool for determining the optimal loop filter for a given application.

USING THE AD9520-2 OUTPUTS FOR ADC CLOCK APPLICATIONS

Any high speed ADC is extremely sensitive to the quality of the AD9520-2 sampling clock. An ADC can be thought of as a sampling mixer; and any noise, distortion, or time jitter on the clock is combined with the desired signal at the analog-to-digital output. Clock integrity requirements scale with the analog input frequency and resolution, with higher analog input frequency applications at ≥ 14-bit resolution being the most stringent. The theoretical SNR of an ADC is limited by the ADC resolution and the jitter on the sampling clock.

Considering an ideal ADC of infinite resolution, where the step size and quantization error can be ignored, the available SNR can be expressed, approximately, by the following equation:

$$SNR(\text{dB}) = 20\log\left(\frac{1}{2\pi f_A t_J}\right)$$

where:
f_A is the highest analog frequency being digitized.
t_J is the rms jitter on the sampling clock.

Figure 70 shows the required sampling clock jitter as a function of the analog frequency and effective number of bits (ENOB).

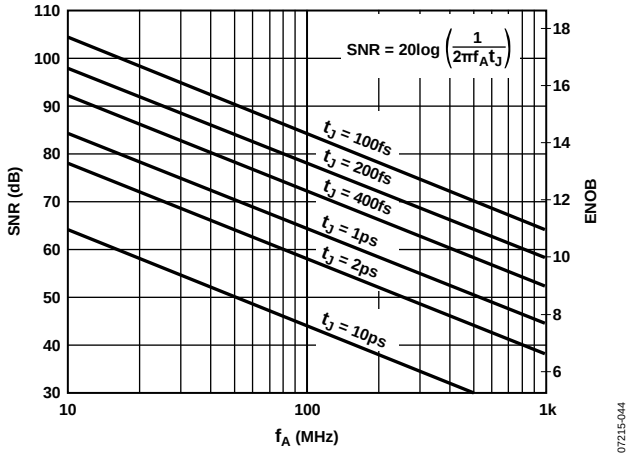


Figure 70. SNR and ENOB vs. Analog Input Frequency

For more information, see the AN-756 Application Note, *Sampled Systems and the Effects of Clock Phase Noise and Jitter*; and the AN-501 Application Note, *Aperture Uncertainty and ADC System Performance.*

Many high performance ADCs feature differential clock inputs to simplify the task of providing the required low jitter clock on a noisy PCB. Distributing a single-ended clock on a noisy PCB can result in coupled noise on the sampling clock. Differential distribution has inherent common-mode rejection that can provide superior clock performance in a noisy environment. The differential LVPECL outputs of the AD9520-2 enable clock solutions that maximize converter SNR performance.

The input requirements of the ADC (differential or single-ended, logic level termination) should be considered when selecting the best clocking/converter solution.

LVPECL CLOCK DISTRIBUTION

The LVPECL outputs of the AD9520-2 provide the lowest jitter clock signals available from the AD9520-2. The LVPECL outputs (because they are open emitter) require a dc termination to bias the output transistors. The simplified equivalent circuit in Figure 54 shows the LVPECL output stage.

In most applications, an LVPECL far-end Thevenin termination (see Figure 71) or Y-termination (see Figure 72) is recommended. In both cases, V_S of the receiving buffer should match V_{S_DRV}. If it does not, ac coupling is recommended (see Figure 73).

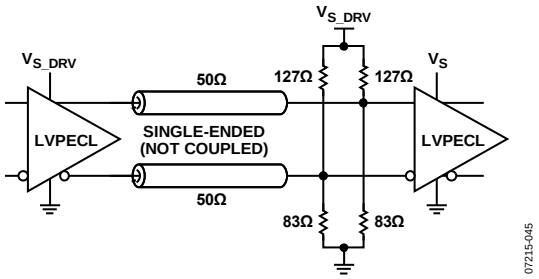


Figure 71. DC-Coupled 3.3 V LVPECL Far-End Thevenin Termination

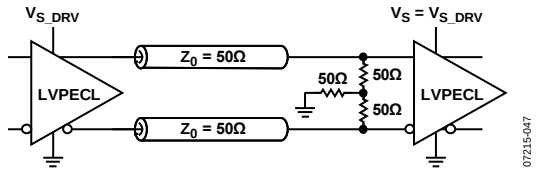


Figure 72. DC-Coupled 3.3 V LVPECL Y-Termination

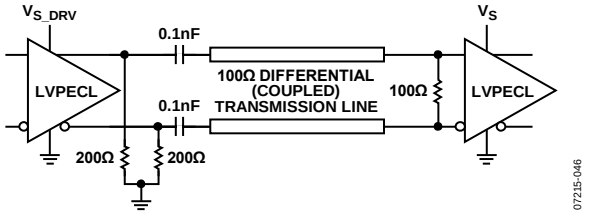


Figure 73. AC-Coupled LVPECL with Parallel Transmission Line

LVPECL Y-Termination

LVPECL Y-termination is an elegant termination scheme that uses the fewest components and offers both odd- and even-mode impedance matching. Even-mode impedance matching is an important consideration for closely coupled transmission lines at high frequencies. Its main drawback is that it offers limited flexibility for varying the drive strength of the emitter-follower LVPECL driver. This can be an important consideration when driving long trace lengths but is usually not an issue. In the case where VS_DRV = 2.5 V, the 50 Ω termination resistor connected to ground in Figure 72 should be changed to 19 Ω.

Far-End Thevenin Termination

Far-end Thevenin termination uses a resistor network to provide 50 Ω termination to a dc voltage that is below V_{OL} of the LVPECL driver. In this case, V_{S_DRV} on the AD9520-2 should equal V_S of the receiving buffer. Although the resistor combination shown results in a dc bias point of V_{S_DRV} − 2 V, the actual common-mode voltage is V_{S_DRV} − 1.3 V because there is additional current flowing from the AD9520-2 LVPECL driver through the pull-down resistor.

The circuit is identical for the case where V_{S_DRV} = 2.5 V, except that the pull-down resistor is 62.5 Ω and the pull-up resistor is 250 Ω.

CMOS CLOCK DISTRIBUTION

The output drivers of the AD9520-2 can be configured as CMOS drivers. When selected as a CMOS driver, each output becomes a pair of CMOS outputs, each of which can be individually turned on or off and set as inverting or noninverting. These outputs are 3.3 V or 2.5 V CMOS compatible. However, every output driver (including the LVPECL drivers) must be run at either 2.5 V or 3.3 V. The user cannot mix and match 2.5 V and 3.3 V outputs.

When using single-ended CMOS clocking, consider the following guidelines:

- Using the CMOS drivers in the same output channel group as the LVPECL drivers may result in performance degradation of the LVPECL drivers. Where possible, program the two CMOS drivers that form the same output of a differential pair to be out of phase such that one driver is high while the other is low. It is recommended that the evaluation board be used to verify the performance of the AD9520-2 in demanding applications where both CMOS and LVPECL drivers are in the same group, and the very best jitter performance is required.
- If possible, design point-to-point connections such that each driver has only one receiver. Connecting outputs in this manner allows for simple termination schemes and minimizes ringing due to possible mismatched impedances on the output trace. Series termination at the source is generally required to provide transmission line matching and/or to reduce current transients at the driver.
- The value of the resistor is dependent on the board design and timing requirements (typically 10 Ω to 100 Ω is used). CMOS outputs are also limited in terms of the capacitive load or trace length that they can drive. Typically, trace lengths of less than 3 inches are recommended to preserve signal rise/fall times and signal integrity.

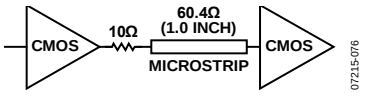


Figure 74. Series Termination of CMOS Output

Termination at the far end of the PCB trace is a second option. The CMOS outputs of the AD9520-2 do not supply enough current to provide a full voltage swing with a low impedance resistive, far-end termination, as shown in Figure 75. The far-end termination network should match the PCB trace impedance and provide the desired switching point. The reduced signal swing may still meet receiver input requirements in some applications. This can be useful when driving long trace lengths on less critical nets.

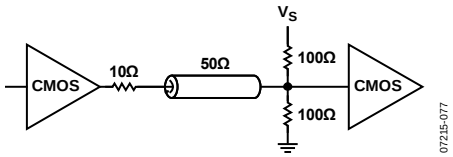
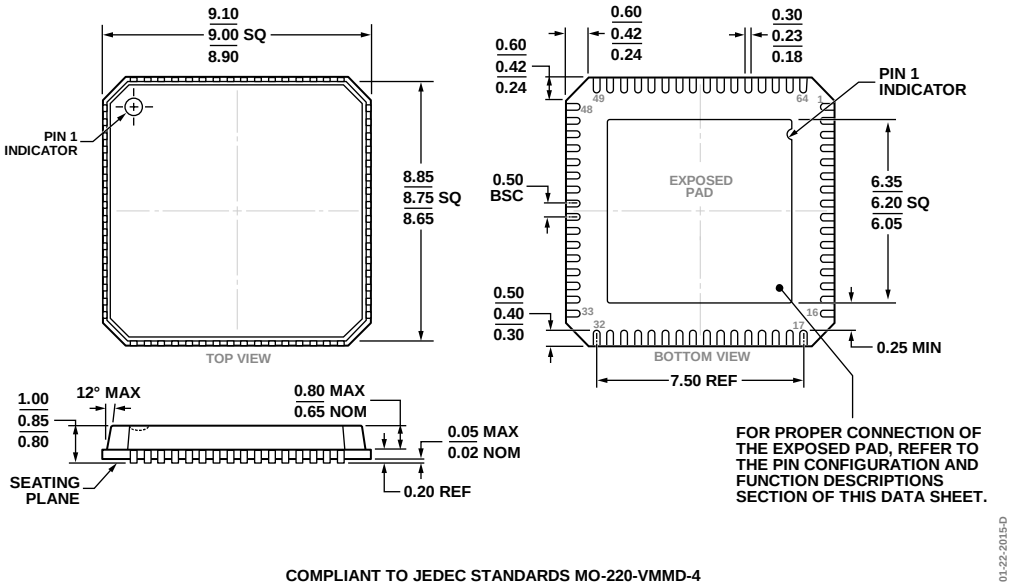


Figure 75. CMOS Output with Far-End Termination

Because of the limitations of single-ended CMOS clocking, consider using differential outputs when driving high speed signals over long traces. The AD9520-2 offers LVPECL outputs that are better suited for driving long traces where the inherent noise immunity of differential signaling provides superior performance for clocking converters.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4

Figure 76. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
CP-64-4
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9520-2BCPZ	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-64-4
AD9520-2BCPZ-REEL7	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-64-4
AD9520-2/PCBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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