1.2 GHz Clock Fanout Buffer with Output Dividers and Delay

Enhanced Product

AD9508-EP

FEATURES

- 1.2 GHz differential clock inputs/outputs
- 10-bit programmable dividers, 1 to 1024, all integers
- Up to 4 differential outputs or 8 CMOS outputs
- Pin strapping mode for hardwired programming at power-up
- <115 fs rms broadband random jitter (see Figure 25)
- Additive output jitter: 41 fs rms typical (12 kHz to 20 MHz)
- Excellent output-to-output isolation
- Automatic synchronization of all outputs
- Single 2.5 V power supply
- Internal low dropout (LDO) voltage regulator for enhanced power supply immunity
- Phase offset select for output-to-output coarse delay adjust
- 3 programmable output logic levels: LVDS, HSTL, and CMOS
- Serial control port (SPI/I²C) or pin programmable mode
- Space-saving 24-lead LFCSP

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Extended temperature range: −55°C to +105°C
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- Low jitter, low phase noise clock distribution
- Clocking high speed ADCs, DACs, DDSs, DDCs, DUCs, MxFEs
- High performance wireless transceivers
- High performance instrumentation
- Broadband infrastructure

GENERAL DESCRIPTION

The AD9508-EP provides clock fanout capability in a design that emphasizes low jitter to maximize system performance. The AD9508-EP benefits applications such as clocking data converters with demanding phase noise and low jitter requirements.

The AD9508-EP has four independent differential clock outputs, each with various types of logic levels available. Available logic types are LVDS (1.2 GHz), HSTL (1.2 GHz), and 1.8 V CMOS (250 MHz). In 1.8 V CMOS output mode, the differential output becomes two CMOS single-ended signals. The CMOS outputs are 1.8 V logic levels.

Each output has a programmable divider that can be bypassed or set to divide by any integer up to 1024. In addition, the AD9508-EP supports coarse output phase adjustment between the outputs.

The device can also be pin programmed for various fixed configurations at power-up without the need for SPI or I²C programming.

The AD9508-EP is available in a 24-lead LFCSP and operates from a single 2.5 V power supply. The temperature range is −55°C to +105°C.

Additional application and technical information can be found in the AD9508 data sheet.

FUNCTIONAL BLOCK DIAGRAM

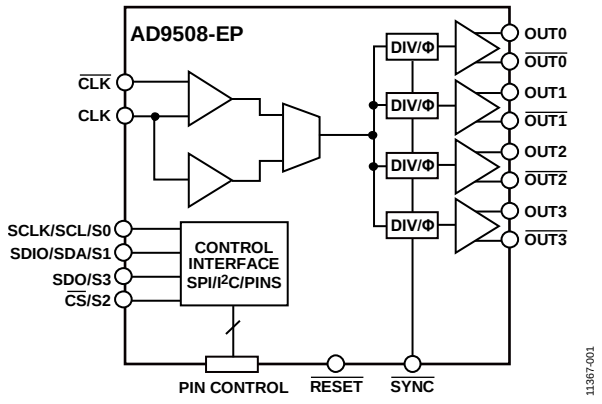


Figure 1.

Rev. D

Document Feedback

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REVISION HISTORY

9/2018—Rev. C to Rev. D

Changed CP-24-14 to CP-24-15 ... Throughout
Updated Outline Dimensions ... 19
Changes to Ordering Guide ... 19

7/2017—Rev. B to Rev. C

Changed CP-24-7 to CP-24-14 ... Throughout
Updated Outline Dimensions ... 19
Changes to Ordering Guide ... 19

10/2014—Rev. A to Rev. B

Changed Input Resistance (Differential) to Input Resistance (Single-Ended), Table 2 ... 3

10/2013—Rev. 0 to Rev. A

Changes to Ordering Guide ... 19

7/2013—Revision 0: Initial Version

SPECIFICATIONS

Typical values are given for V_S = 2.5 V and T_A = 25°C; minimum and maximum values are given over the full supply voltage range (V_{DD} = 2.5 V ± 5%) and temperature range (T_A = −55°C to +105°C); input slew rate > 1 V/ns, unless otherwise noted.

POWER SUPPLY CURRENT AND TEMPERATURE CONDITIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE	2.375	2.5	2.625	V	
CURRENT CONSUMPTION					
LVDS Configuration		132	148	mA	Input clock at 1200 MHz, differential mode; all LVDS output drivers at 1200 MHz
		96	108	mA	Input clock at 800 MHz, differential mode; all LVDS output drivers at 200 MHz
HSTL Configuration		156	175	mA	Input clock at 1200 MHz, differential mode; all HSTL output drivers at 1200 MHz
		121	136	mA	Input clock at 491.52 MHz, differential mode; all HSTL output drivers at 491.52 MHz
		86	96	mA	Input clock at 122.88 MHz, differential mode; all HSTL output drivers at 122.88 MHz
CMOS Configuration		142	159	mA	Input clock at 1200 MHz, differential mode; all CMOS output drivers at 200 MHz, C_{LOAD} = 10 pF
		118	132	mA	Input clock at 800 MHz, differential mode; all CMOS output drivers at 200 MHz, C_{LOAD} = 10 pF
		76	85	mA	Input clock at 100 MHz, differential mode; all CMOS output drivers at 100 MHz, C_{LOAD} = 10 pF
Full Power-Down		4.6	8	mA	
TEMPERATURE					
Ambient Temperature Range, T_A	−55	+25	+105	°C	
Junction Temperature, T_J			135	°C	Junction temperatures above 115°C can degrade performance, but no damage should occur unless the absolute temperature is exceeded

CLOCK INPUT AND OUTPUT DC SPECIFICATIONS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CLOCK INPUTS (DIFFERENTIAL MODE)						
Input Frequency		0		1200	MHz	Differential input
Input Sensitivity		360		2200	mV p-p	As measured with a differential probe; jitter performance improves with higher slew rates (greater voltage swing)
Input Common-Mode Voltage	V_{ICM}	0.95	1.05	1.15	V	Input pins are internally self biased, which enables ac coupling
Input Voltage Offset			30		mV	
DC-Coupled Input Common-Mode Range	V_{CMR}	0.58		1.67	V	Allowable common-mode voltage range when dc-coupled
Pulse Width Low		417			ps	
Pulse Width High		417			ps	
Input Resistance (Single-Ended)		5.0	7	9	kΩ	
Input Capacitance	C_{IN}		2		pF	
Input Bias Current (Each Pin)		100		400	µA	Full input swing

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CMOS CLOCK MODE (SINGLE-ENDED)						
Input Frequency				250	MHz	
Input Voltage High	V_{IH}	V_{DD} − 0.4			V	
Input Voltage Low	V_{IL}			0.4	V	
Input Current High	I_{INH}		1		µA	
Input Current Low	I_{INL}		−142		µA	
Input Capacitance	C_{IN}		2		pF	
LVDS CLOCK OUTPUTS						Termination = 100 Ω differential (OUTx, $\overline{OUTx}$)
Output Frequency				1200	MHz	
Differential Output Voltage	V_{OD}	247	375	454	mV	$V_{OH} - V_{OL}$ measurement across a differential pair at the default amplitude setting with output driver not toggling; see Figure 6 for variation over frequency
Delta V_{OD}	ΔV_{OD}			50	mV	Absolute value of the difference between V_{OD} when the normal output is high vs. when the complementary output is high
Offset Voltage	V_{OS}	1.125	1.18	1.375	V	$(V_{OH} + V_{OL})/2$ across a differential pair
Delta V_{OS}	ΔV_{OS}			50	mV	Absolute value of the difference between V_{OS} when the normal output is high vs. when the complementary output is high
Short-Circuit Current	I_SA, I_SB		13.6	24	mA	Each pin (output shorted to GND)
LVDS Duty Cycle		45		55	%	Up to 750 MHz input
		39		61	%	750 MHz to 1200 MHz input
HSTL CLOCK OUTPUTS						Termination = 100 Ω differential; default amplitude setting
Output Frequency				1200	MHz	
Differential Output Voltage	V_O	859	925	978	mV	$V_{OH} - V_{OL}$ with output driver static
Common-Mode Output Voltage	V_{OCM}	905	940	971	mV	$(V_{OH} + V_{OL})/2$ with output driver static
HSTL Duty Cycle		45		55	%	Up to 750 MHz input
		40		60	%	750 MHz to 1200 MHz input
CMOS CLOCK OUTPUTS						Single-ended; termination = open; OUTx and $\overline{OUTx}$ in phase
Output Frequency				250	MHz	10 pF load per output; see Figure 14 for output swing vs. frequency
Output Voltage						
1 mA Load						
High	V_{OH}	1.7			V	
Low	V_{OL}			0.1	V	
10 mA Load						
High	V_{OH}	1.2			V	
Low	V_{OL}			0.6	V	
10 mA Load (2 × CMOS Mode)						
High	V_{OH}	1.45			V	
Low	V_{OL}			0.35	V	
CMOS Duty Cycle		45		55	%	Up to 250 MHz

OUTPUT DRIVER TIMING CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS OUTPUTS						Termination = 100 Ω differential, 1 × LVDS
Output Rise/Fall Time	t_R, t_F		152	192	ps	20% to 80% measured differentially
Propagation Delay, Clock to LVDS Output	t_{PD}	1.52	2.01	2.49	ns	
Temperature Coefficient			2.8		ps/°C	
Output Skew, All LVDS Outputs[1]						
On the Same Part				48	ps	
Across Multiple Parts				781	ps	Assumes same temperature and supply; takes into account worst-case propagation delay delta due to worst-case process variation
HSTL OUTPUTS						Termination = 100 Ω differential, 1 × HSTL
Output Rise/Fall Time	t_R, t_F		118	154	ps	20% to 80% measured differentially
Propagation Delay, Clock to HSTL Output	t_{PD}	1.55	2.05	2.56	ns	
Temperature Coefficient			2.9		ps/°C	
Output Skew, All HSTL Outputs[1]						
On the Same Part				59	ps	
Across Multiple Parts				825	ps	Assumes same temperature and supply; takes into account worst-case propagation delay delta due to worst-case process variation
CMOS OUTPUTS						
Output Rise/Fall Time	t_R, t_F		1.18	1.47	ns	20% to 80%; C_{LOAD} = 10 pF
Propagation Delay, Clock to CMOS Output	t_{PD}	1.98	2.56	3.14	ns	10 pF load
Temperature Coefficient			3.3		ps/°C	
Output Skew, All CMOS Outputs[1]						
On the Same Part				112	ps	
Across Multiple Parts				965	ps	Assumes same temperature and supply; takes into account worst-case propagation delay delta due to worst-case process variation
OUTPUT LOGIC SKEW[1]						CMOS load = 10 pF and LVDS load = 100 Ω
LVDS Outputs and HSTL Outputs			77	119	ps	Outputs on the same device; assumes worst-case output combination
LVDS Outputs and CMOS Outputs			497	708	ps	Outputs on the same device; assumes worst-case output combination
HSTL Outputs and CMOS Outputs			424	628	ps	Outputs on the same device; assumes worst-case output combination

[1] Output skew is the difference between any two similar delay paths while operating at the same voltage and temperature.

LOGIC INPUTS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS ($\overline{\text{RESET}}$, $\overline{\text{SYNC}}$, IN_SEL)						
Input Voltage High	V_{IH}	1.7			V	2.5 V supply voltage operation
Input Voltage Low	V_{IL}			0.7	V	2.5 V supply voltage operation
Input Current	I_{INH}, I_{INL}	−300		+100	µA	
Input Capacitance	C_{IN}		2		pF	

SERIAL PORT SPECIFICATIONS—SPI MODE

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{CS}$					$\overline{CS}$ has an internal 35 kΩ pull-up resistor
Input Voltage					
Logic 1	VDD – 0.4			V	
Logic 0			0.4	V	
Input Current					
Logic 1		–4		µA	
Logic 0		–85		µA	
Input Capacitance		2		pF	
SCLK					SCLK has an internal 35 kΩ pull-down resistor
Input Voltage					
Logic 1	VDD – 0.4			V	
Logic 0			0.4	V	
Input Current					
Logic 1		70		µA	
Logic 0		13		µA	
Input Capacitance		2		pF	
SDIO (INPUT)					
Input Voltage					
Logic 1	VDD – 0.4			V	
Logic 0			0.4	V	
Input Current					
Logic 1		–1		µA	
Logic 0		–1		µA	
Input Capacitance		2		pF	
SDIO (OUTPUT)					
Output Voltage					1 mA load current
Logic 1	VDD – 0.4			V	
Logic 0			0.4	V	
SDO					
Output Voltage					1 mA load current
Logic 1	VDD – 0.4			V	
Logic 0			0.4	V	
TIMING					
SCLK					
Clock Rate, $1/t_{CLK}$			30	MHz	
Pulse Width High, t_{HIGH}	4.6			ns	
Pulse Width Low, t_{LOW}	3.5			ns	
SDIO to SCLK Setup, t_{DS}	2.9			ns	
SCLK to SDIO Hold, t_{DH}	0			ns	
SCLK to Valid SDIO and SDO, t_{DV}			15	ns	
$\overline{CS}$ to SCLK Setup (t_S)	3.4			ns	
$\overline{CS}$ to SCLK Hold (t_C)	0			ns	
$\overline{CS}$ Minimum Pulse Width High	3.4			ns	

SERIAL PORT SPECIFICATIONS—I²C MODE

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SDA, SCL (INPUTS)					SDA and SCL have internal 80 kΩ pull-up resistors
Input Voltage					
Logic 1	VDD − 0.4			V	
Logic 0			0.4	V	
Input Current	−40		0	μA	V_{IN} = 10% to 90%
Hysteresis of Schmitt Trigger Inputs	150			mV	
SDA (OUTPUT)					
Output Logic 0 Voltage			0.4	V	I_O = 3 mA
Output Fall Time from $V_{IH\ (MIN)}$ to $V_{IL\ (MAX)}$			250	ns	10 pF ≤ C_b ≤ 400 pF
TIMING					
SCL Clock Rate			400	kHz	
Bus-Free Time Between a Stop and Start Condition, t_{BUF}	1.3			μs	
Repeated Start Condition Setup Time, $t_{SU;\ STA}$			0.6	μs	
Repeated Start Condition Hold Time, $t_{HD;\ STA}$	0.6			μs	After this period, the first clock pulse is generated
Stop Condition Setup Time, $t_{SU;\ STO}$	0.6			μs	
Low Period of the SCL Clock, t_{LOW}	1.3			μs	
High Period of the SCL Clock, t_{HIGH}	0.6			μs	
Data Setup Time, $t_{SU;\ DAT}$	100			ns	
Data Hold Time, $t_{HD;\ DAT}$	0		0.9	μs	

EXTERNAL RESISTOR VALUES FOR PIN STRAPPING MODE

Table 7.

Parameter	Resistor Polarity	Min	Typ	Max	Unit	Test Conditions/Comments
EXTERNAL RESISTORS						Using 10% tolerance resistor
Voltage Level 0	Pull down to ground		820		Ω	
Voltage Level 1	Pull down to ground		1.8		kΩ	
Voltage Level 2	Pull down to ground		3.9		kΩ	
Voltage Level 3	Pull down to ground		8.2		kΩ	
Voltage Level 4	Pull up to VDD		820		Ω	
Voltage Level 5	Pull up to VDD		1.8		kΩ	
Voltage Level 6	Pull up to VDD		3.9		kΩ	
Voltage Level 7	Pull up to VDD		8.2		kΩ	

CLOCK OUTPUT ADDITIVE PHASE NOISE

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADDITIVE PHASE NOISE, CLOCK TO HSTL OR LVDS					
CLK = 1200 MHz, OUTx = 1200 MHz					Input slew rate > 1 V/ns
Divide Ratio = 1					
10 Hz Offset		−90		dBc/Hz	
100 Hz Offset		−101		dBc/Hz	
1 kHz Offset		−110		dBc/Hz	
10 kHz Offset		−117		dBc/Hz	
100 kHz Offset		−135		dBc/Hz	
1 MHz Offset		−144		dBc/Hz	
10 MHz Offset		−149		dBc/Hz	
100 MHz Offset		−150		dBc/Hz	
ADDITIVE PHASE NOISE, CLOCK TO HSTL, LVDS, OR CMOS					
CLK = 625 MHz, OUTx = 125 MHz					Input slew rate > 1 V/ns
Divide Ratio = 5					
10 Hz Offset		−114		dBc/Hz	
100 Hz Offset		−125		dBc/Hz	
1 kHz Offset		−133		dBc/Hz	
10 kHz Offset		−141		dBc/Hz	
100 kHz Offset		−159		dBc/Hz	
1 MHz Offset		−162		dBc/Hz	
10 MHz Offset		−163		dBc/Hz	
20 MHz Offset		−163		dBc/Hz	
ADDITIVE PHASE NOISE, CLOCK TO HSTL OR LVDS					
CLK = 491.52 MHz, OUTx = 491.52 MHz					Input slew rate > 1 V/ns
Divide Ratio = 1					
10 Hz Offset		−100		dBc/Hz	
100 Hz Offset		−111		dBc/Hz	
1 kHz Offset		−120		dBc/Hz	
10 kHz Offset		−127		dBc/Hz	
100 kHz Offset		−146		dBc/Hz	
1 MHz Offset		−153		dBc/Hz	
10 MHz Offset		−153		dBc/Hz	
20 MHz Offset		−153		dBc/Hz	

CLOCK OUTPUT ADDITIVE TIME JITTER

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS OUTPUT ADDITIVE TIME JITTER					
CLK = 622.08 MHz, Outputs = 622.08 MHz		41		fs rms	BW = 12 kHz to 20 MHz
		70		fs rms	BW = 20 kHz to 80 MHz
		69		fs rms	BW = 50 kHz to 80 MHz
CLK = 622.08 MHz, Outputs = 155.52 MHz		93		fs rms	BW = 12 kHz to 20 MHz
		144		fs rms	BW = 20 kHz to 80 MHz
		142		fs rms	BW = 50 kHz to 80 MHz
CLK = 125 MHz, Outputs = 125 MHz		105		fs rms	BW = 12 kHz to 20 MHz
		209		fs rms	BW = 20 kHz to 80 MHz
		206		fs rms	BW = 50 kHz to 80 MHz
CLK = 400 MHz, Outputs = 50 MHz		184		fs rms	BW = 12 kHz to 20 MHz
HSTL OUTPUT ADDITIVE TIME JITTER					
CLK = 622.08 MHz, Outputs = 622.08 MHz		41		fs rms	BW = 12 kHz to 20 MHz
		56		fs rms	BW = 100 Hz to 20 MHz
		72		fs rms	BW = 20 kHz to 80 MHz
		70		fs rms	BW = 50 kHz to 80 MHz
CLK = 622.08 MHz, Outputs = 155.52 MHz		76		fs rms	BW = 12 kHz to 20 MHz
		87		fs rms	BW = 100 Hz to 20 MHz
		158		fs rms	BW = 20 kHz to 80 MHz
		156		fs rms	BW = 50 kHz to 80 MHz
CMOS OUTPUT ADDITIVE TIME JITTER					
CLK = 100 MHz, Outputs = 100 MHz		91		fs rms	BW = 12 kHz to 20 MHz

ABSOLUTE MAXIMUM RATINGS

Table 10.

Parameter	Rating
Supply Voltage (VDD)	3.6 V
Maximum Digital Input Voltage	−0.5 V to VDD + 0.5 V
CLK and $\overline{\text{CLK}}$	−0.5 V to VDD + 0.5 V
Maximum Digital Output Voltage	−0.5 V to VDD + 0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +105°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

The following equation determines the junction temperature on the application PCB:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:
T_J is the junction temperature (°C).
T_{CASE} is the case temperature (°C) measured by the customer at the top center of the package.
Ψ_{JT} is the value indicated in Table 11.
P_D is the power dissipation.

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first-order approximation of T_J by the following equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where T_A is the ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

Values of θ_{JB} are provided for package comparison and PCB design considerations.

THERMAL CHARACTERISTICS

Thermal characteristics are established using JEDEC JESD51-7 and JEDEC JESD51-5 2S2P test boards.

Table 11. Thermal Characteristics, 24-Lead LFCSP

Symbol	Thermal Characteristic[1]	Value[2]	Unit
θ_{JA}	Junction-to-ambient thermal resistance per JEDEC JESD51-2 (still air)	43.5	°C/W
θ_{JMA}	Junction-to-ambient thermal resistance, 1.0 m/sec airflow per JEDEC JESD51-6 (moving air)	40	°C/W
θ_{JMA}	Junction-to-ambient thermal resistance, 2.5 m/sec airflow per JEDEC JESD51-6 (moving air)	38.5	°C/W
θ_{JB}	Junction-to-board thermal resistance per JEDEC JESD51-8 (still air)	16.2	°C/W
θ_{JC}	Junction-to-case thermal resistance (die-to-heat sink) per MIL-STD-883, Method 1012.1	7.1	°C/W
Ψ_{JT}	Junction-to-top-of-package characterization parameter per JEDEC JESD51-2 (still air)	0.33	°C/W

[1] The exposed pad on the bottom of the package must be soldered to ground (VSS) to achieve the specified thermal performance.
[2] Results are from simulations. The PCB is a JEDEC multilayer type. Thermal performance for actual applications requires careful inspection of the conditions in the application to determine whether they are similar to those assumed in these calculations.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

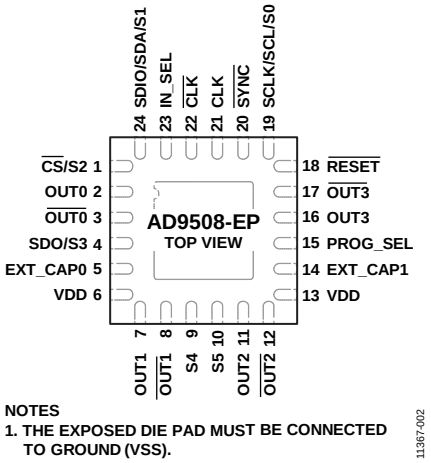


Figure 2. Pin Configuration

Table 12. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{CS}$/S2	Chip Select ($\overline{CS}$)/Pin Programming (S2). This dual-purpose pin is controlled by the PROG_SEL pin. In SPI mode, $\overline{CS}$ is an active low CMOS input. When programming the device in SPI mode, $\overline{CS}$ must be held low. In systems with two or more AD9508-EP devices, $\overline{CS}$ enables individual programming of each device. In pin programming mode, S2 is hardwired with a resistor to either VDD or ground. The resistor value and resistor biasing determine the channel divider value for the outputs on Pin 11 and Pin 12.
2	OUT0	LVDS/HSTL Differential Output or Single-Ended CMOS Output.
3	$\overline{OUT0}$	Complementary LVDS/HSTL Differential Output or Single-Ended CMOS Output.
4	SDO/S3	SPI Serial Data Output (SDO)/Pin Programming (S3). This dual-purpose pin is controlled by the PROG_SEL pin. In SPI mode, SDO can be configured as an output to read back the internal register settings. In pin programming mode, S3 is hardwired with a resistor to either VDD or ground. The resistor value and resistor biasing determine the channel divider value for the outputs on Pin 16 and Pin 17.
5	EXT_CAP0	Node for External Decoupling Capacitor for LDO Regulator. Tie this pin with a 0.47 µF capacitor to ground.
6	VDD	Power Supply (2.5 V Operation).
7	OUT1	LVDS/HSTL Differential Output or Single-Ended CMOS Output.
8	$\overline{OUT1}$	Complementary LVDS/HSTL Differential Output or Single-Ended CMOS Output.
9	S4	The S4 pin is used in pin programming mode only. (The PROG_SEL pin determines which programming mode is used.) S4 is hardwired with a resistor to either VDD or ground. The resistor value and resistor biasing determine the output logic levels used for the outputs on Pin 2, Pin 3, Pin 7, and Pin 8.
10	S5	The S5 pin is used in pin programming mode only. (The PROG_SEL pin determines which programming mode is used.) S5 is hardwired with a resistor to either VDD or ground. The resistor value and resistor biasing determine the output logic levels used for the outputs on Pin 11, Pin 12, Pin 16, and Pin 17.
11	OUT2	LVDS/HSTL Differential Output or Single-Ended CMOS Output.
12	$\overline{OUT2}$	Complementary LVDS/HSTL Differential Output or Single-Ended CMOS Output.
13	VDD	Power Supply (2.5 V Operation).
14	EXT_CAP1	Node for External Decoupling Capacitor for LDO Regulator. Tie this pin with a 0.47 µF capacitor to ground.
15	PROG_SEL	Three-State CMOS Input. Pin 15 selects the device programming interface used by the AD9508-EP: SPI, I^2C, or pin programming.
16	OUT3	LVDS/HSTL Differential Output or Single-Ended CMOS Output.
17	$\overline{OUT3}$	Complementary LVDS/HSTL Differential Output or Single-Ended CMOS Output.
18	$\overline{RESET}$	Device Reset (CMOS Input, Active Low). When this pin is asserted, the internal register settings revert to their default state after the $\overline{RESET}$ pin is released. $\overline{RESET}$ also powers down the device when an active low signal is applied to the pin. The $\overline{RESET}$ pin has an internal 24 kΩ pull-up resistor.

Pin No.	Mnemonic	Description
19	SCLK/SCL/S0	SPI Serial Clock (SCLK)/I²C Serial Clock (SCL)/Pin Programming (S0). This multipurpose pin is controlled by the PROG_SEL pin. In SPI mode, SCLK is the serial clock. In I²C mode, SCL is the serial clock. In pin programming mode, S0 is hardwired with a resistor to either VDD or ground. The resistor value and resistor biasing determine the channel divider value for the outputs on Pin 2 and Pin 3.
20	$\overline{\text{SYNC}}$	Clock Synchronization (Active Low). When this pin is asserted, the output drivers are held static and then synchronized on a low-to-high transition of this pin. The $\overline{\text{SYNC}}$ pin has an internal 24 kΩ pull-up resistor.
21	CLK	Differential Clock Input or Single-Ended CMOS Input. This pin serves as a differential clock input or as a single-ended CMOS input, depending on the logic state of the IN_SEL pin.
22	$\overline{\text{CLK}}$	Complementary Differential Clock Input.
23	IN_SEL	Input Select (CMOS Input). A logic high on this pin configures the CLK and $\overline{\text{CLK}}$ inputs for a differential input signal. A logic low configures the CLK input for single-ended CMOS; ac-couple the unused $\overline{\text{CLK}}$ pin to ground with a 0.1 µF capacitor.
24	SDIO/SDA/S1	SPI Serial Data Input and Output (SDIO)/I²C Serial Data (SDA)/Pin Programming (S1). This multipurpose pin is controlled by the PROG_SEL pin. In SPI mode, SDIO is the serial input/output pin. In 4-wire SPI mode, data writes occur on this pin; in 3-wire SPI mode, both data reads and writes occur on this pin. This pin has no internal pull-up/pull-down resistor. In I²C mode, SDA is the serial data pin. In pin programming mode, S1 is hardwired with a resistor to either VDD or ground. The resistor value and resistor biasing determine the channel divider values for the outputs on Pin 7 and Pin 8.
	EP	Exposed Pad. The exposed die pad must be connected to ground (VSS).

TYPICAL PERFORMANCE CHARACTERISTICS

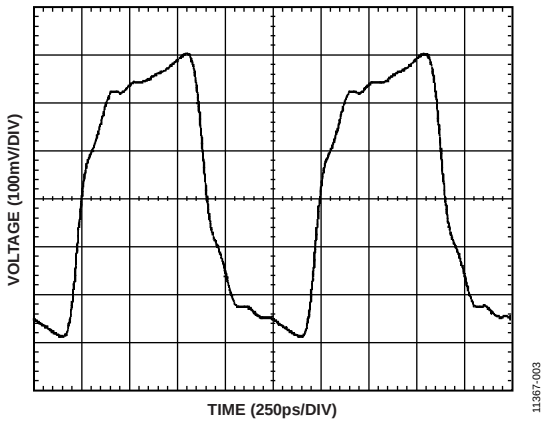


Figure 3. LVDS Differential Output Waveform at 800 MHz

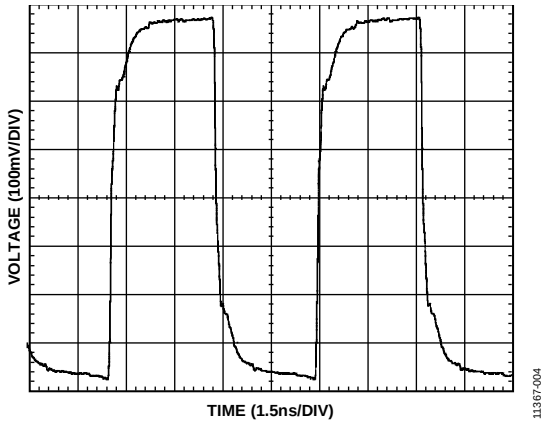


Figure 4. LVDS Differential Output Waveform at 156.25 MHz

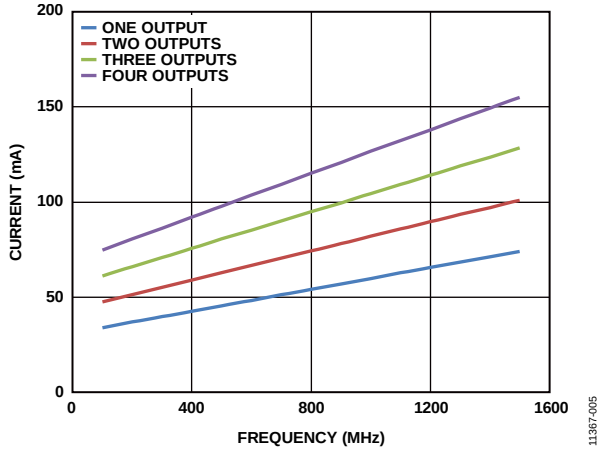


Figure 5. Power Supply Current vs. Frequency and Number of Outputs Used, LVDS Mode

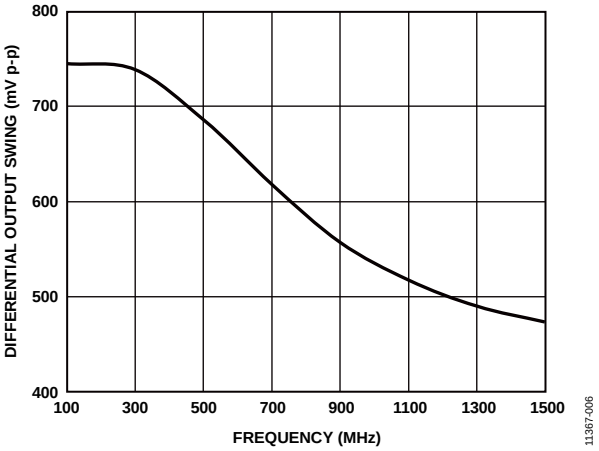


Figure 6. LVDS Differential Output Swing vs. Frequency

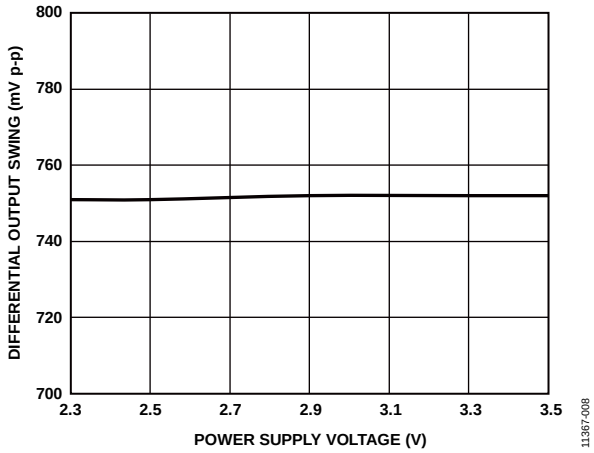


Figure 7. LVDS Differential Output Swing vs. Power Supply Voltage

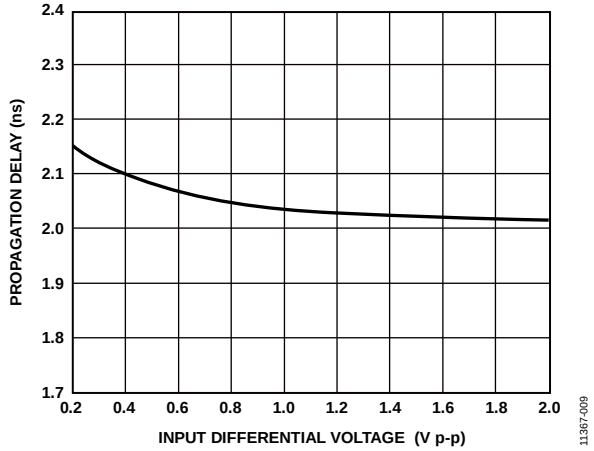


Figure 8. LVDS Propagation Delay vs. Input Differential Voltage

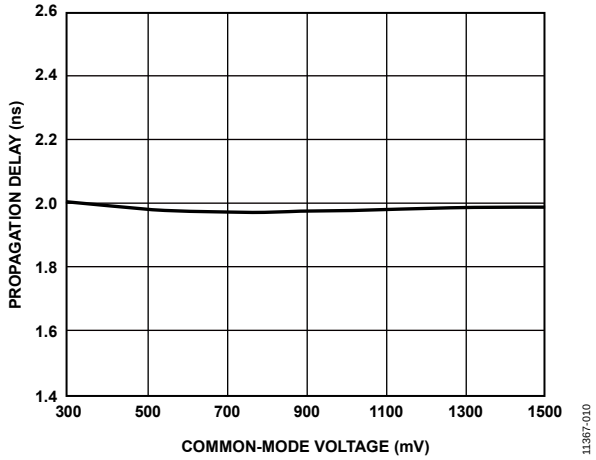


Figure 9. LVDS Propagation Delay vs. Input Common-Mode Voltage

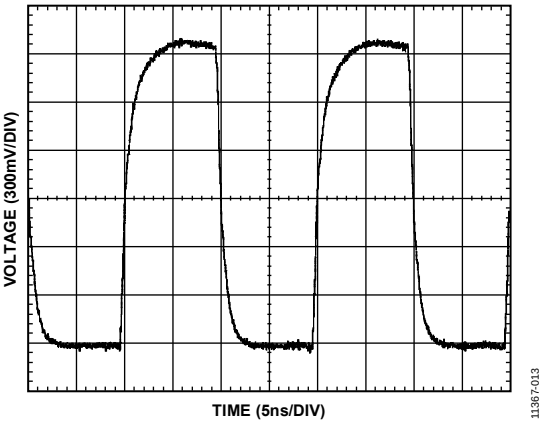


Figure 12. CMOS Output Waveform at 50 MHz with 10 pF Load

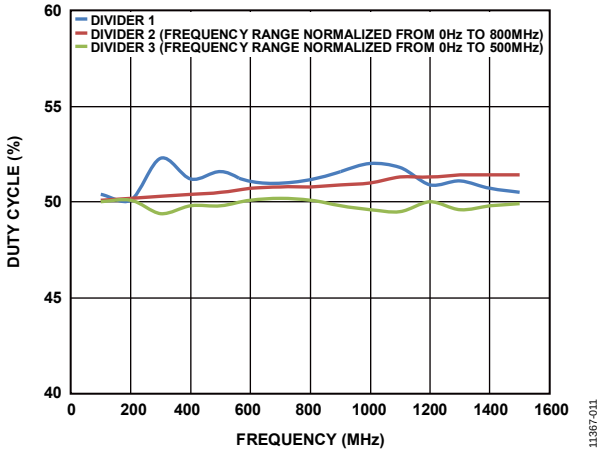


Figure 10. LVDS Output Duty Cycle vs. Output Frequency

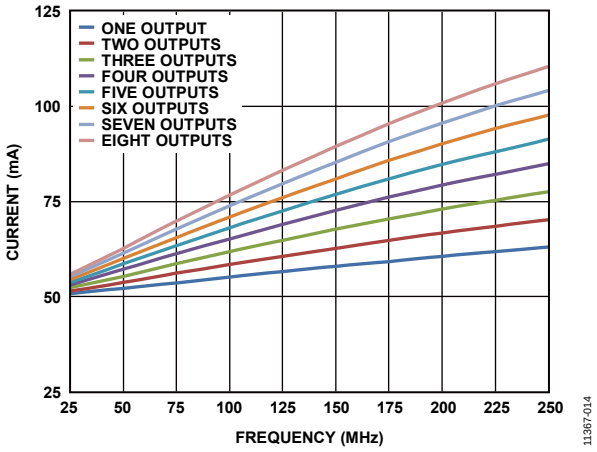


Figure 13. Power Supply Current vs. Frequency and Number of Outputs Used, CMOS Mode

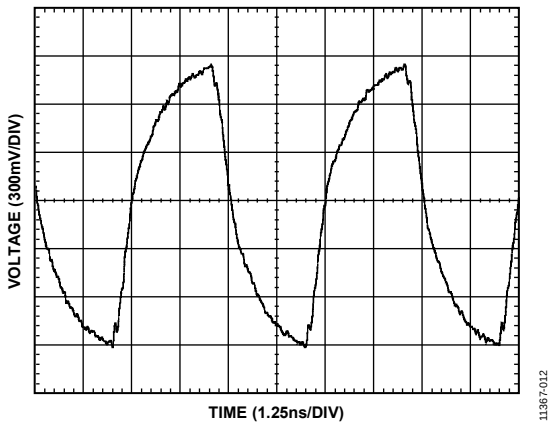


Figure 11. CMOS Output Waveform at 200 MHz with 10 pF Load

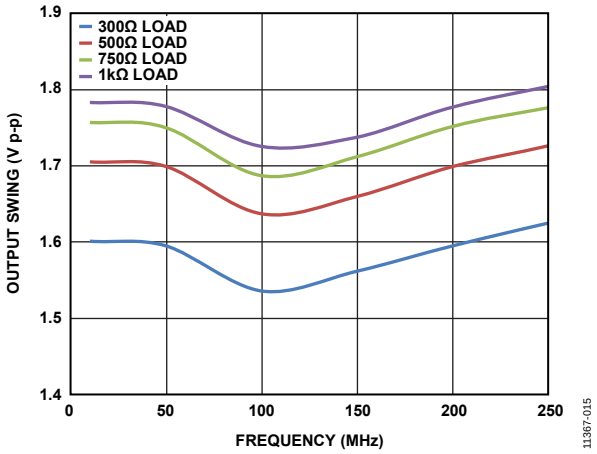


Figure 14. CMOS Output Swing vs. Frequency and Resistive Load

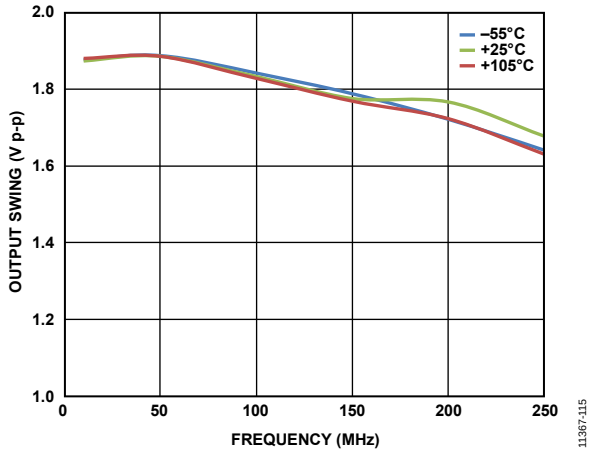


Figure 15. CMOS Output Swing vs. Frequency and Temperature (10 pF Load)

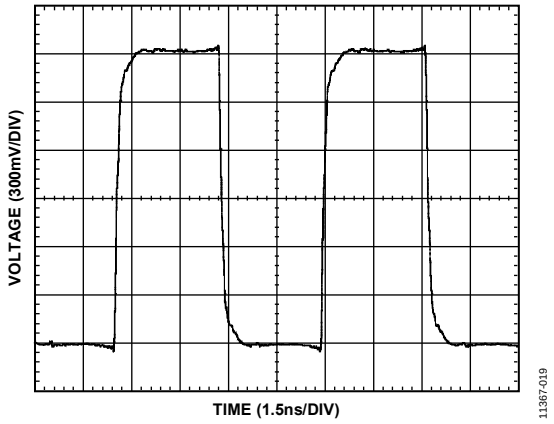


Figure 18. HSTL Differential Output Waveform at 156.25 MHz

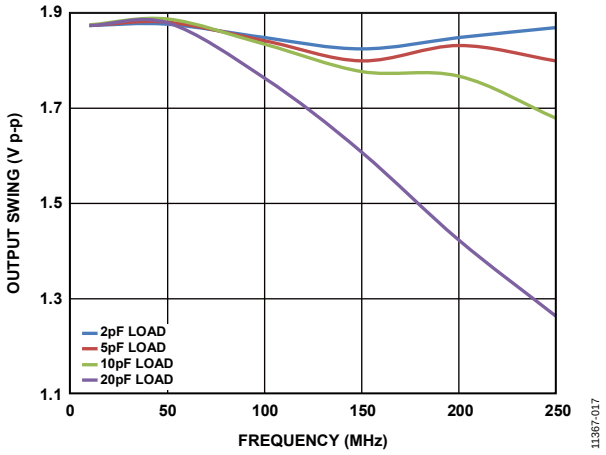


Figure 16. CMOS Output Swing vs. Frequency and Capacitive Load

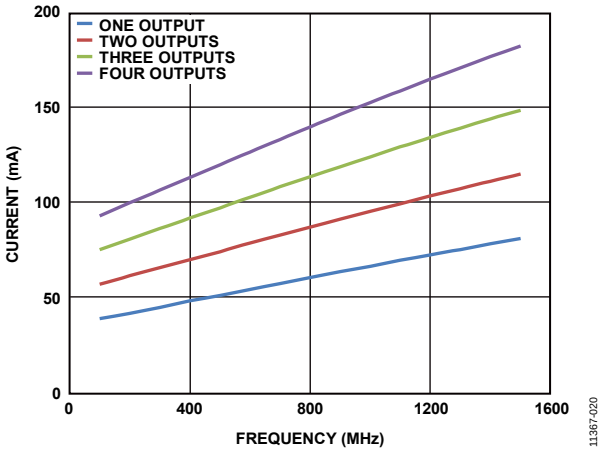


Figure 19. Power Supply Current vs. Frequency and Number of Outputs Used, HSTL Mode

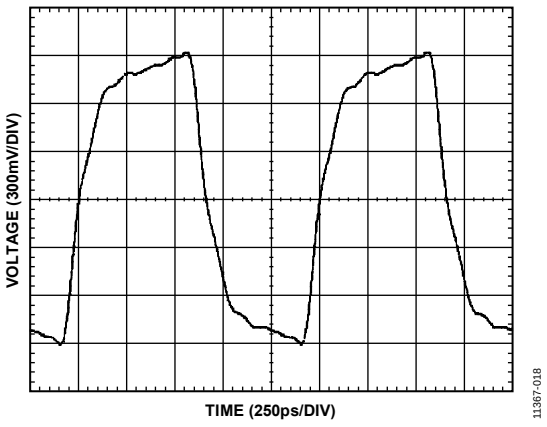


Figure 17. HSTL Differential Output Waveform at 800 MHz

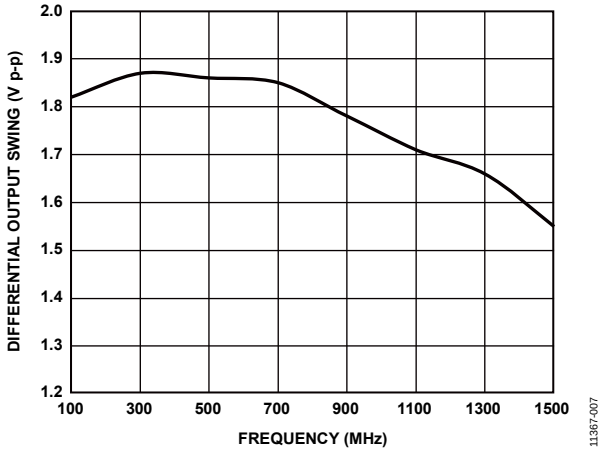


Figure 20. HSTL Differential Output Swing vs. Frequency

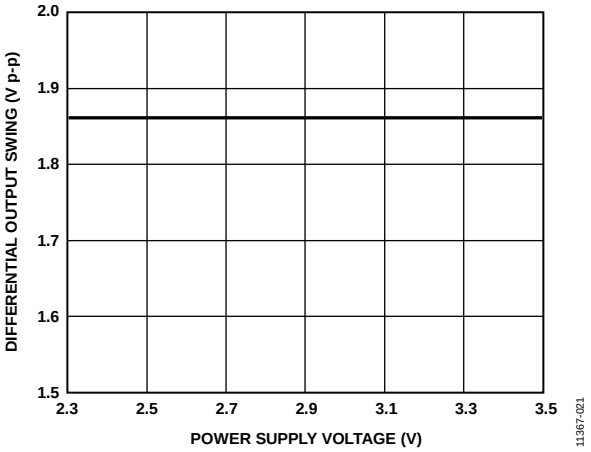


Figure 21. HSTL Differential Output Swing vs. Power Supply Voltage

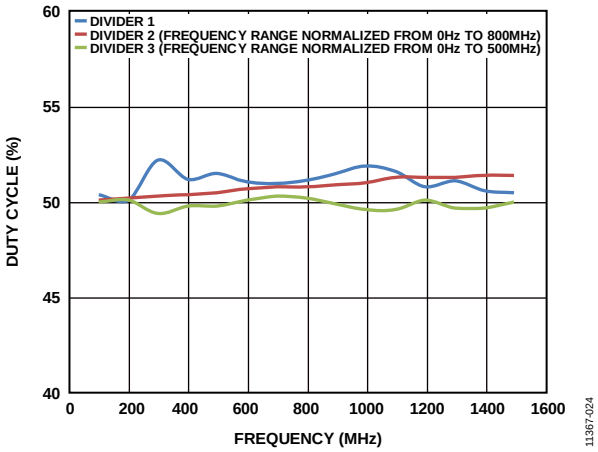


Figure 24. HSTL Output Duty Cycle vs. Output Frequency

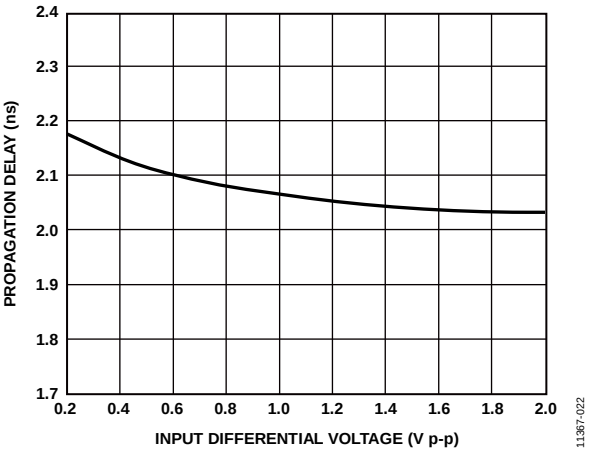


Figure 22. HSTL Propagation Delay vs. Input Differential Voltage

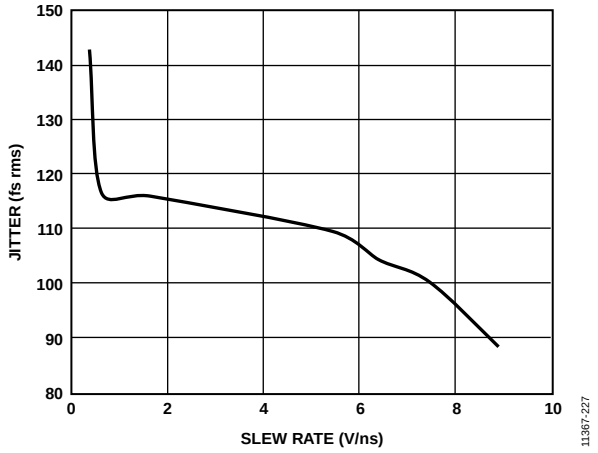


Figure 25. Additive Broadband Jitter vs. Input Slew Rate, LVDS and HSTL Modes (Calculated from SNR of ADC Method)

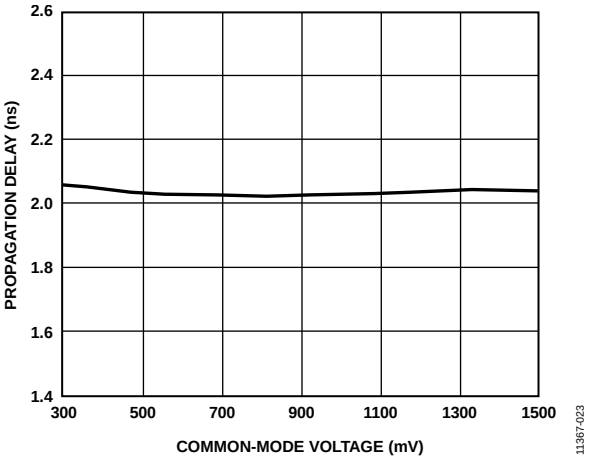


Figure 23. HSTL Propagation Delay vs. Input Common-Mode Voltage

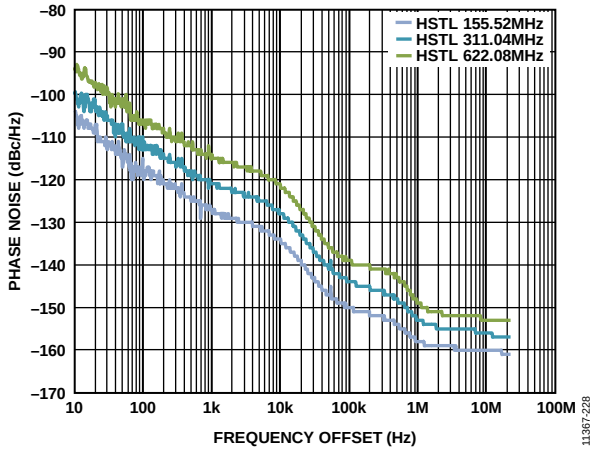


Figure 26. Absolute Phase Noise in HSTL Mode with Clock Input at 622.08 MHz and Outputs = 622.08 MHz, 311.04 MHz, and 155.52 MHz

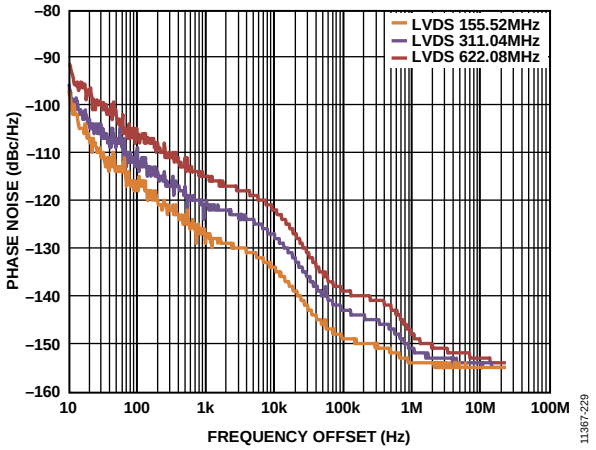


Figure 27. Absolute Phase Noise in LVDS Mode with Clock Input at 622.08 MHz and Outputs = 622.08 MHz, 311.04 MHz, and 155.52 MHz

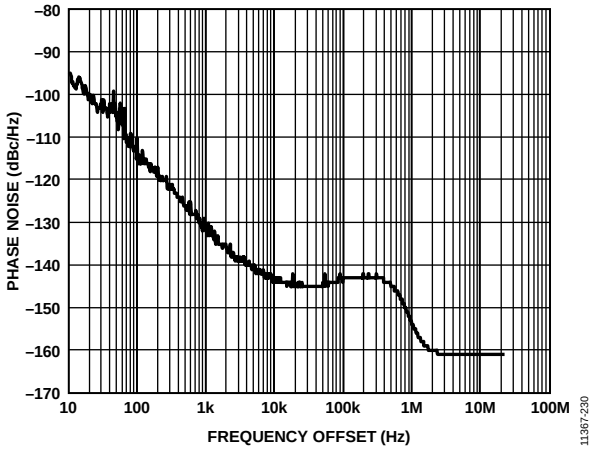


Figure 28. Absolute Phase Noise of Clock Source at 622.08 MHz

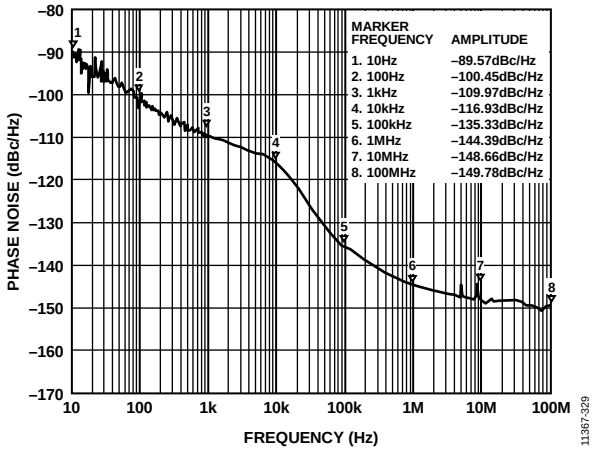


Figure 29. Additive Phase Noise with Clock Input = 1200 MHz and HSTL Outputs = 1200 MHz

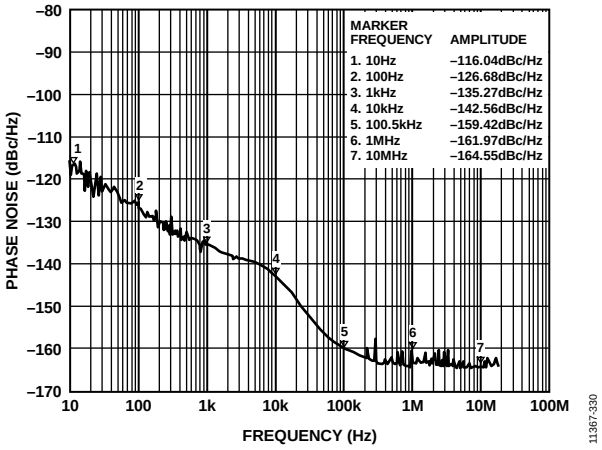


Figure 30. Additive Phase Noise with Clock Input = 1200 MHz and HSTL Outputs = 100 MHz

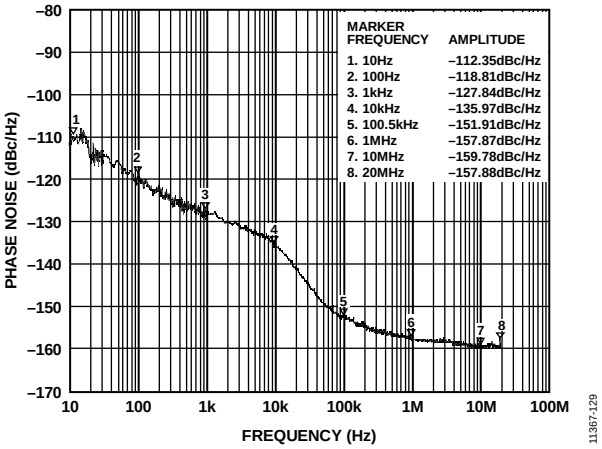


Figure 31. Additive Phase Noise with Clock Input = 622.08 MHz and HSTL Outputs = 155.52 MHz

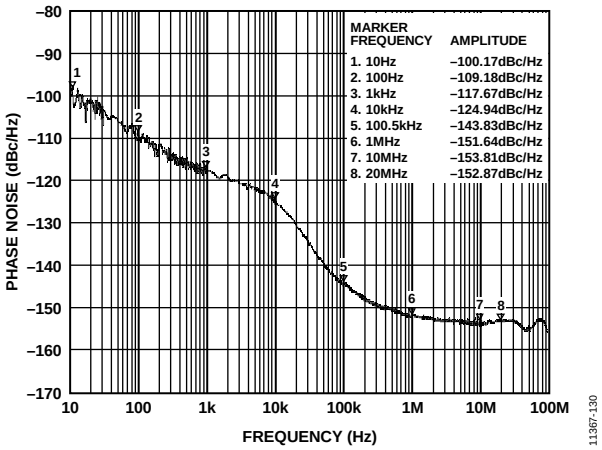


Figure 32. Additive Phase Noise with Clock Input = 622.08 MHz and LVDS Outputs = 622.08 MHz

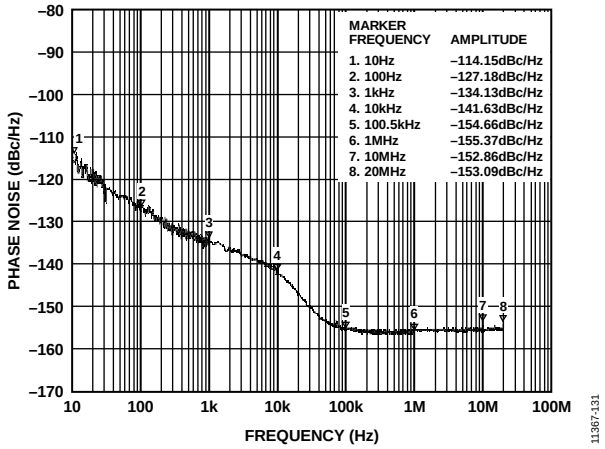


Figure 33. Additive Phase Noise with Clock Input = 100 MHz and CMOS Outputs = 100 MHz

OUTLINE DIMENSIONS

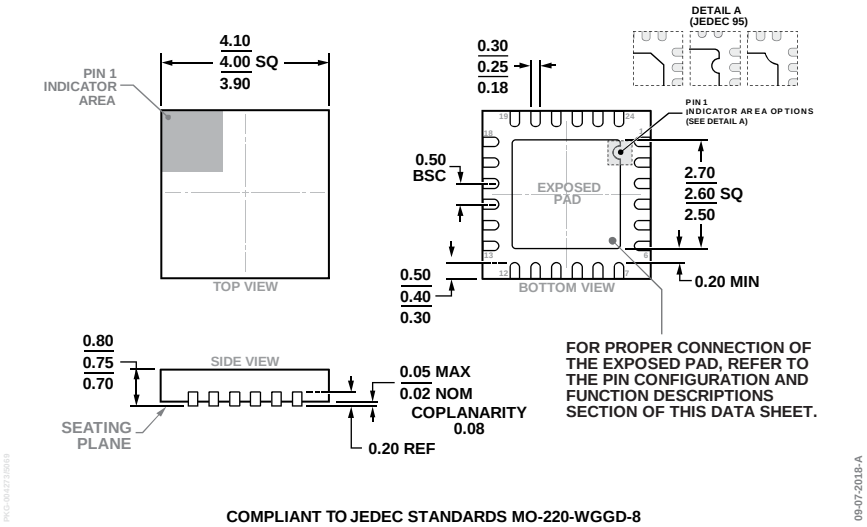


Figure 34. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-15)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9508SCPZ-EP	−55°C to +105°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-15
AD9508SCPZ-EP-R7	−55°C to +105°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-15
AD9508/PCBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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D11367-0-9/18(D)