12-Bit, 6 GSPS, JESD204B/C Dual Analog-to-Digital Converter

Preliminary Technical Data

AD9207

FEATURES

- Buffered input with −3 dB bandwidth ≥ 7.5 GHz
  - Full-scale of 1.4 V p-p with R_{IN} = 100 Ω
  - Overload protection clamp
  - Supports dc-coupled with common-mode feedback
- AC performance at f_{IN} < 2.6 GHz
  - HD2 < −63 dBc and HD3 < −67 dBc
  - Small signal (−12 dBFS) noise spectral density (NSD) = −153 dBFS/Hz
- Low code error rate (CER) < 2×-10^{-15}
- Flexible ADC clocking options
  - On-chip PLL or external RF clock
- Versatile digital features
- Configurable digital down conversion (DDC)
  - 2 coarse complex DDCs per ADC
  - 4 fine complex DDCs per ADC
- Programmable 192 tap FIR filter
- Integer/fractional sample delay for digital predistortion (DPD) or IQ mismatch
- Automatic gain control (AGC) support with dedicated AGC support pins
  - Fast detect with low latency for fast AGC control
  - Signal monitor for slow AGC control
- Auxiliary features
- Fast frequency hopping
- ADC clock driver with selectable divide ratios
- On-chip temperature sensor
- Programmable GPIO pins
- JESD204B/C (Subclass 1) interface, 8 lanes
  - JESD204B compatible with the maximum 15.5 Gbps lane rate
  - JESD204C compatible with the maximum 24.75 Gbps lane rate
  - Sample/bit repeat mode for receive lane rate matching
  - Supports real or complex digital data (12-bit, 16-bit, or 24-bit)
  - Multichip synchronization
- Power consumption~ 4 W to 5.5 W
- 15 mm × 15 mm BGA with 0.8 mm pitch

APPLICATIONS

- Diversity multiband and multimode digital receivers
- Microwave point-to-point, E-Band, and 5G mm wave
- Broadband communications systems
- Phased array radar and electronic warfare
- Electronic test and measurement systems

GENERAL DESCRIPTION

The AD9207 is a dual, 12-bit, 6 GSPS analog-to-digital converter (ADC). The ADC input features an on-chip wideband buffer with overload protection. This device is designed to support communications applications capable of direct sampling wideband signals up to 7.5 GHz. An optional low phase noise phase-locked loop (PLL) clock synthesizer is available to generate the ADC sampling clock, simplifying printed circuit board (PCB) distribution of a high frequency clock signal. Alternatively, the CLKIN of the device can be driven directly with the ADC sampling clock (or a higher version up to 12 GHz when the internal clock divider is enabled). An optional CLKOUT buffer is available to transmit the ADC sampling clock to other devices.

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FUNCTIONAL BLOCK DIAGRAM

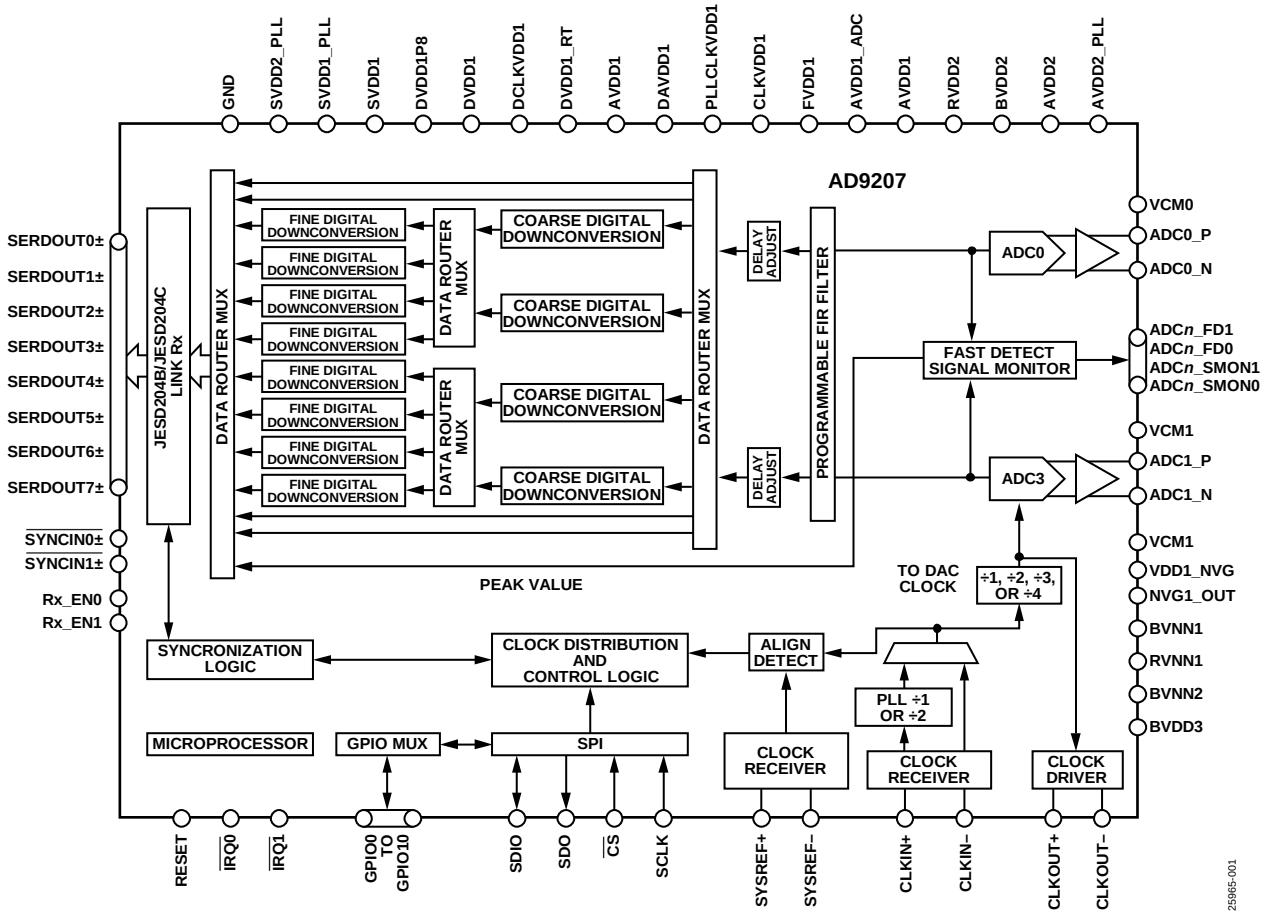

Figure 1.

ABSOLUTE MAXIMUM RATINGS

Table 1.

Parameter	Rating
ISET, DACxP, DACxN, TDP, TDN	−0.3 V to AVDD2 + 0.3 V
VCO_COARSE, VCO_FINE, VCO_VCM, VCO_VREG	−0.3 V to AVDD2_PLL + 0.3 V
ADC0P, ADC0N, ADC1P, ADC1N	−0.3 V to BVDD2 + 0.3 V
VCM0, VCM1	−0.3 V to RVDD2 + 0.3 V
CLKINP, CLKINN	−0.2 V to PLLCLKVDD1 + 0.2 V
ADCDRVN, ADCDRVP	−0.2 V to CLKVDD1 + 0.2 V
SERDINx±, SERDOUTx±	−0.2 V to SVDD1 + 0.2 V
SYSREFP, SYSREFN, and $\overline{\text{SYNCxIN±}}$	−0.2 V to +2.5 V
$\overline{\text{SYNCxOUT±}}$, $\overline{\text{SYNCxIN±}}$, $\overline{\text{RESET}}$, TXENx, RXENx, $\overline{\text{IRQx}}$, $\overline{\text{CS}}$, SCLK, SDIO, SDO, TMU_REFN, TMU_REFP, ADCx_SMON0, ADCx_SMON1, ADCx_FD0, ADCx_FD1, GPIOx	−0.3 V to DVDD1P8 + 0.3 V
AVDD2, AVDD2_PLL, BVDD2, RVDD2, SVDD2_PLL, DVDD1P8	−0.3 V to +2.2 V
PLLCLKVDD1, AVDD1, AVDD1_ADC, CLKVDD1, FVDD1, DAVDD1, DVDD1_RT, DCLKVDD1, SVDD1, SVDD1_PLL	−0.2 V to +1.2 V
VNN1	−1.1 V to +0.2 V
Temperature	
Maximum Junction (T_J)[1]	120°C
Storage Range	−40°C to +150°C

[1] Do not exceed this temperature for any duration of time when the device is powered.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

REFLOW PROFILE

The AD9207 reflow profile is in accordance with the JEDEC JESD 20 criteria for Pb-free devices. The maximum reflow temperature is 260°C.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. The use of appropriate thermal management techniques is recommended to ensure that the maximum T_J does not exceed the limits shown in Table 1.

θ_{JA} is the natural convection, junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC_TOP} is the junction-to-case thermal resistance.

θ_{JB} is the junction-to-board thermal resistance.

Table 2. Thermal Resistance[1]

Package Type	Airflow Velocity (m/sec)	θ_{JA}	θ_{JC_TOP}	θ_{JB}	Unit
BP-324-3	0.0	11.7	0.40	2.3	°C/W

[1] Thermal resistance values specified are simulated based on JEDEC specifications in compliance with JESD51-12 with the device power equal to 9 W.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

OUTLINE DIMENSIONS

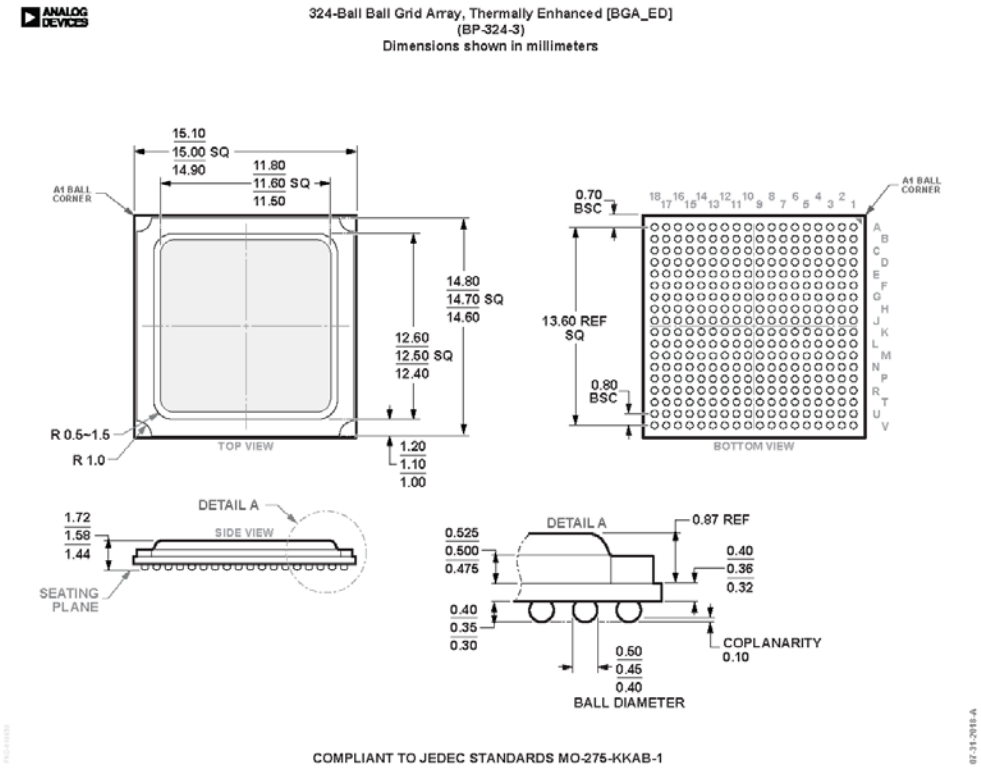

Figure 2. 324-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]
(BP-324-3)
Dimensions shown in millimeters

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