Dual, 14-Bit, 1230 MSPS, TxDAC+ Digital-to-Analog Converter

Data Sheet

AD9121

FEATURES

- Flexible LVDS interface allows word or byte load
- Single-carrier W-CDMA ACLR = 82 dBc at 122.88 MHz IF
- Analog output: adjustable 8.7 mA to 31.7 mA, R_L = 25 Ω to 50 Ω
- Integrated 2×/4×/8× interpolator/complex modulator allows carrier placement anywhere in the DAC bandwidth
- Gain, dc offset, and phase adjustment for sideband suppression
- Multiple chip synchronization interfaces
- High performance, low noise PLL clock multiplier
- Digital inverse sinc filter
- Low power: 1.5 W at 1.2 GSPS, 800 mW at 500 MSPS, full operating conditions
- 72-lead, exposed paddle LFCSP

APPLICATIONS

- Wireless infrastructure
- W-CDMA, CDMA2000, TD-SCDMA, WiMAX, GSM, LTE
- Digital high or low IF synthesis
- Transmit diversity
- Wideband communications: LMDS/MMDS, point-to-point

GENERAL DESCRIPTION

The AD9121 is a dual, 14-bit, high dynamic range digital-to-analog converter (DAC) that provides a sample rate of 1230 MSPS, permitting multicarrier generation up to the Nyquist frequency.

The AD9121 TxDAC+® includes features optimized for direct conversion transmit applications, including complex digital modulation, and gain and offset compensation. The DAC outputs are optimized to interface seamlessly with analog quadrature modulators, such as the ADL537x F-MOD series from Analog Devices, Inc. A 4-wire serial port interface provides for programming/readback of many internal parameters. Full-scale output current can be programmed over a range of 8.7 mA to 31.7 mA. The AD9121 comes in a 72-lead LFCSP.

PRODUCT HIGHLIGHTS

1. Ultralow noise and intermodulation distortion (IMD) enable high quality synthesis of wideband signals from baseband to high intermediate frequencies (IF).
2. Proprietary DAC output switching technique enhances dynamic performance.
3. Current outputs are easily configured for various single-ended or differential circuit topologies.
4. Flexible LVDS digital interface allows the standard 28-wire bus to be reduced to one-half of the width.

COMPANION PRODUCTS

- **IQ Modulators:** ADL5370, ADL537x family
- **IQ Modulators with PLL and VCO:** ADRF6701, ADRF670x family
- **Clock Drivers:** AD9516, AD951x family
- **Voltage Regulator Design Tool:** ADIsimPower

TYPICAL SIGNAL CHAIN

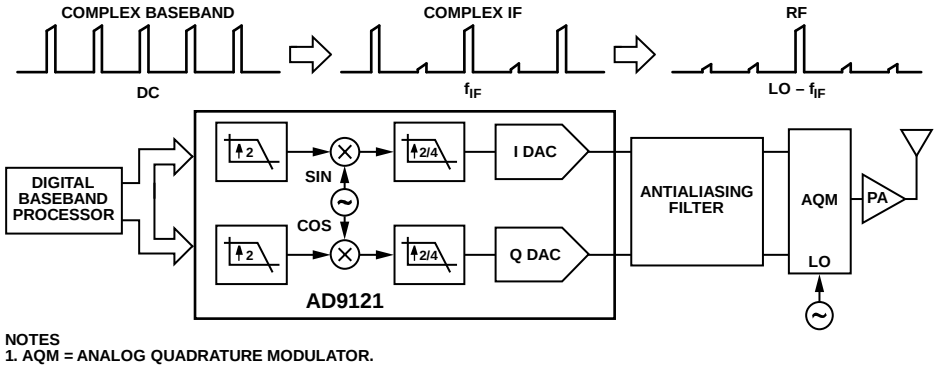


Figure 1.

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

©2012 Analog Devices, Inc. All rights reserved.

Technical Support www.analog.com

TABLE OF CONTENTS

Features 1
Applications 1
General Description 1
Product Highlights 1
Companion Products 1
Typical Signal Chain 1
Revision History 3
Functional Block Diagram 4
Specifications 5
DC Specifications 5
Digital Specifications 6
Digital Input Data Timing Specifications 6
AC Specifications 7
Absolute Maximum Ratings 8
Thermal Resistance 8
ESD Caution 8
Pin Configuration and Function Descriptions 9
Typical Performance Characteristics 11
Terminology 17
Theory of Operation 18
Serial Port Operation 18
Data Format 18
Serial Port Pin Descriptions 18
Serial Port Options 19
Device Configuration Register Map and Descriptions 20
LVDS Input Data Ports 31
Word Interface Mode 31
Byte Interface Mode 31
Interface Timing 31
Recommended Frame Input Bias Circuitry 32
FIFO Operation 32
Digital Datapath 36
Premodulation 36
Interpolation Filters 36
NCO Modulation 39
Datapath Configuration 39
Determining Interpolation Filter Modes 40
Datapath Configuration Examples 41
Data Rates vs. Interpolation Modes 42
Coarse Modulation Mixing Sequences 42
Quadrature Phase Correction 43
DC Offset Correction 43
Inverse Sinc Filter 43
DAC Input Clock Configurations 44
Driving the DACCLK and REFCLK Inputs 44
Direct Clocking 44
Clock Multiplication 44
PLL Settings 45
Configuring the VCO Tuning Band 45
Analog Outputs 46
Transmit DAC Operation 46
Auxiliary DAC Operation 47
Interfacing to Modulators 48
Baseband Filter Implementation 48
Driving the ADL5375-15 48
Reducing LO Leakage and Unwanted Sidebands 49
Device Power Management 50
Power Dissipation 50
Temperature Sensor 51
Multichip Synchronization 52
Synchronization with Clock Multiplication 52
Synchronization with Direct Clocking 53
Data Rate Mode Synchronization 53
FIFO Rate Mode Synchronization 54
Additional Synchronization Features 55
Interrupt Request Operation 56
Interrupt Service Routine 56
Interface Timing Validation 57
SED Operation 57
SED Example 58
Example Start-Up Routine 59
Device Configuration 59
Derived PLL Settings 59
Derived NCO Settings 59
Start-Up Sequence 59
Outline Dimensions 60
Ordering Guide 60

REVISION HISTORY

10/12—Rev. 0 to Rev. B

Updated Outline Dimensions.....60

FUNCTIONAL BLOCK DIAGRAM

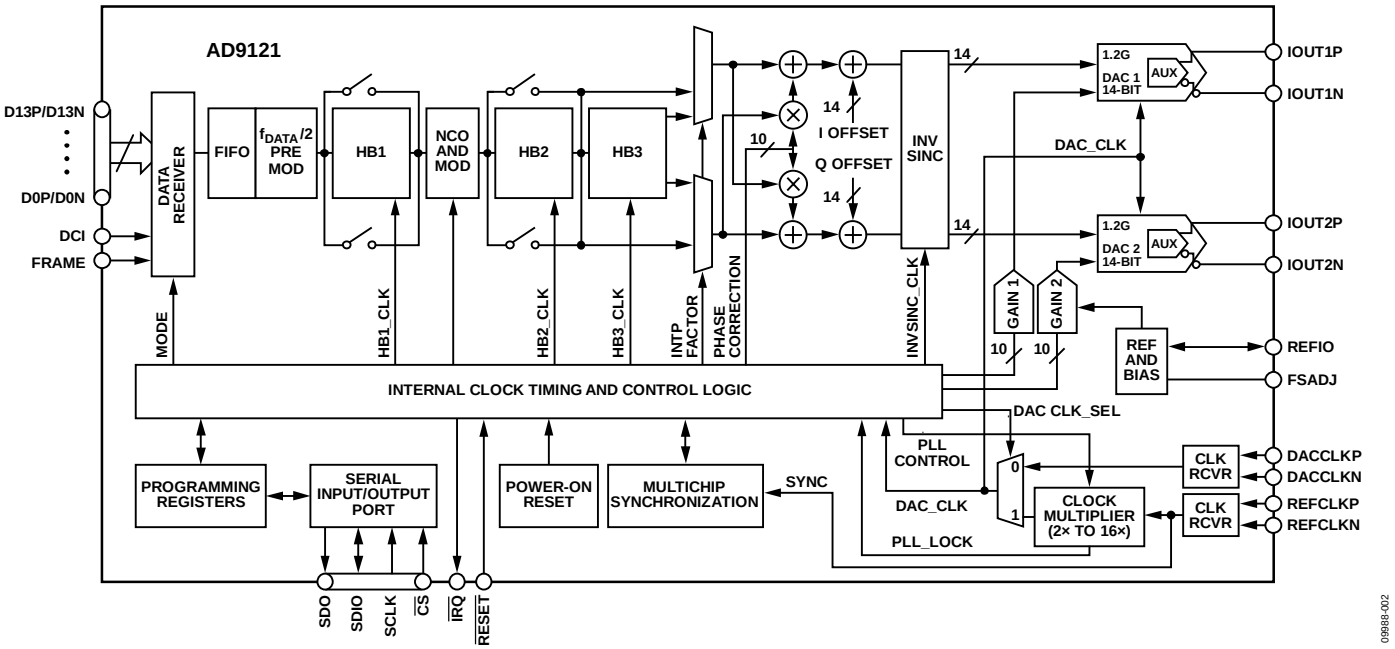


Figure 2.

SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{FS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION		14		Bits
ACCURACY				
Differential Nonlinearity (DNL)		±0.5		LSB
Integral Nonlinearity (INL)		±1.0		LSB
MAIN DAC OUTPUTS				
Offset Error	−0.001	0	+0.001	% FSR
Gain Error (with Internal Reference)	−3.6	±2	+3.6	% FSR
Full-Scale Output Current[1]	8.66	19.6	31.66	mA
Output Compliance Range	−1.0		+1.0	V
Power Supply Rejection Ratio, AVDD33	−0.3		+0.3	% FSR/V
Output Resistance		10		MΩ
Gain DAC Monotonicity		Guaranteed		
Settling Time to Within ±0.5 LSB		20		ns
MAIN DAC TEMPERATURE DRIFT				
Offset		0.04		ppm/°C
Gain		100		ppm/°C
Reference Voltage		30		ppm/°C
REFERENCE				
Internal Reference Voltage		1.2		V
Output Resistance		5		kΩ
ANALOG SUPPLY VOLTAGES				
AVDD33	3.13	3.3	3.47	V
CVDD18	1.71	1.8	1.89	V
DIGITAL SUPPLY VOLTAGES				
DVDD18	1.71	1.8	1.89	V
IOVDD	1.71	1.8/3.3	3.47	V
POWER CONSUMPTION				
2× Mode, f_{DAC} = 491.22 MSPS, IF = 10 MHz, PLL Off		834		mW
2× Mode, f_{DAC} = 491.22 MSPS, IF = 10 MHz, PLL On		913		mW
8× Mode, f_{DAC} = 800 MSPS, IF = 10 MHz, PLL Off		1135	1241	mW
AVDD33		55	57	mA
CVDD18		85	90	mA
DVDD18		444	495	mA
Power-Down Mode (Register 0x01 = 0xF0)		6.5	18.8	mW
POWER-UP TIME		260		ms
OPERATING RANGE	−40	+25	+85	°C

[1] Based on a 10 kΩ external resistor between FSADJ and AVSS.

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, IOVDD = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{FS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL					
Input V_{IN} Logic High	IOVDD = 1.8 V	1.2			V
	IOVDD = 2.5 V	1.6			V
	IOVDD = 3.3 V	2.0			V
Input V_{IN} Logic Low	IOVDD = 1.8 V			0.6	V
	IOVDD = 2.5 V, 3.3 V			0.8	V
CMOS OUTPUT LOGIC LEVEL					
Output V_{OUT} Logic High	IOVDD = 1.8 V	1.4			V
	IOVDD = 2.5 V	1.8			V
	IOVDD = 3.3 V	2.4			V
Output V_{OUT} Logic Low	IOVDD = 1.8 V, 2.5 V, 3.3 V			0.4	V
LVDS RECEIVER INPUTS[1]	Applies to data, DCI, and FRAME inputs				
Input Voltage Range, V_{IA} or V_{IB}		825		1675	mV
Input Differential Threshold, V_{IDTH}		−100		+100	mV
Input Differential Hysteresis, V_{IDTHH} to V_{IDTHL}			20		mV
Receiver Differential Input Impedance, R_{IN}		80		120	Ω
LVDS Input Rate	See Table 5				
DAC CLOCK INPUT (DACCLKP, DACCLKN)					
Differential Peak-to-Peak Voltage		100	500	2000	mV
Common-Mode Voltage	Self-biased input, ac-coupled		1.25		V
Maximum Clock Rate		1230			MHz
REFCLK INPUT (REFCLKP, REFCLKN)					
Differential Peak-to-Peak Voltage		100	500	2000	mV
Common-Mode Voltage			1.25		V
REFCLK Frequency (PLL Mode)	1 GHz ≤ f_{VCO} ≤ 2.1 GHz	15.625		600	MHz
REFCLK Frequency (SYNC Mode)	See the Multichip Synchronization section for conditions	0		600	MHz
SERIAL PORT INTERFACE					
Maximum Clock Rate (SCLK)		40			MHz
Minimum Pulse Width High (t_{PWH})				12.5	ns
Minimum Pulse Width Low (t_{PWL})				12.5	ns
Setup Time, SDIO to SCLK (t_{DS})		1.9			ns
Hold Time, SDIO to SCLK (t_{DH})		0.2			ns
Data Valid, SDO to SCLK (t_{DV})		2.3			ns
Setup Time, $\overline{CS}$ to SCLK (t_{DCSB})			1.4		ns

[1] LVDS receiver is compliant with the IEEE 1596 reduced range link, unless otherwise noted.

DIGITAL INPUT DATA TIMING SPECIFICATIONS

Table 3.

Parameter	Value	Unit
LATENCY (DACCLK CYCLES)		
1× Interpolation (With or Without Modulation)	64	Cycles
2× Interpolation (With or Without Modulation)	135	Cycles
4× Interpolation (With or Without Modulation)	292	Cycles
8× Interpolation (With or Without Modulation)	608	Cycles
Inverse Sinc	20	Cycles
Fine Modulation	8	Cycles

AC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{FS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)				
f_{DAC} = 100 MSPS, f_{OUT} = 20 MHz		78		dBc
f_{DAC} = 200 MSPS, f_{OUT} = 50 MHz		80		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 70 MHz		69		dBc
f_{DAC} = 800 MSPS, f_{OUT} = 70 MHz		72		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)				
f_{DAC} = 200 MSPS, f_{OUT} = 50 MHz		84		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 60 MHz		86		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 80 MHz		84		dBc
f_{DAC} = 800 MSPS, f_{OUT} = 100 MHz		81		dBc
NOISE SPECTRAL DENSITY (NSD), EIGHT-TONE, 500 kHz TONE SPACING				
f_{DAC} = 200 MSPS, f_{OUT} = 80 MHz		−162		dBm/Hz
f_{DAC} = 400 MSPS, f_{OUT} = 80 MHz		−163		dBm/Hz
f_{DAC} = 800 MSPS, f_{OUT} = 80 MHz		−164		dBm/Hz
W-CDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE-CARRIER				
f_{DAC} = 491.52 MSPS, f_{OUT} = 10 MHz		84		dBc
f_{DAC} = 491.52 MSPS, f_{OUT} = 122.88 MHz		82		dBc
f_{DAC} = 983.04 MSPS, f_{OUT} = 122.88 MHz		83		dBc
W-CDMA SECOND ACLR, SINGLE-CARRIER				
f_{DAC} = 491.52 MSPS, f_{OUT} = 10 MHz		88		dBc
f_{DAC} = 491.52 MSPS, f_{OUT} = 122.88 MHz		86		dBc
f_{DAC} = 983.04 MSPS, f_{OUT} = 122.88 MHz		88		dBc

Table 5. Maximum Rate (MSPS) with DVDD and CVDD Supply Regulation

		$f_{INTERFACE}$ (MSPS)			f_{DAC} (MSPS)		
		DVDD18, CVDD18 =			DVDD18, CVDD18 =		
Bus Width	Interpolation Factor	1.8 V ± 5%	1.8 V ± 2%	1.9 V ± 2%	1.8 V ± 5%	1.8 V ± 2%	1.9 V ± 2%
Byte (7 Bits)	1×	1100	1200	1230	275	300	307.5
	2×	1100	1200	1230	550	600	615
	4×	1100	1200	1230	1100	1200	1230
	8×	550	600	615	1100	1200	1230
Word (14 Bits)	1×	1100	1200	1230	550	600	615
	2× (HB1)	900	1000	1000	900	1000	1000
	2× (HB2)	1100	1200	1230	1100	1200	1230
	4×	550	600	615	1100	1200	1230
	8×	275	300	307.5	1100	1200	1230

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
AVDD33 to AVSS, EPAD, CVSS, DVSS	−0.3 V to +3.6 V
IOVDD to AVSS, EPAD, CVSS, DVSS	−0.3 V to +3.6 V
DVDD18, CVDD18 to AVSS, EPAD, CVSS, DVSS	−0.3 V to +2.1 V
AVSS to EPAD, CVSS, DVSS	−0.3 V to +0.3 V
EPAD to AVSS, CVSS, DVSS	−0.3 V to +0.3 V
CVSS to AVSS, EPAD, DVSS	−0.3 V to +0.3 V
DVSS to AVSS, EPAD, CVSS	−0.3 V to +0.3 V
FSADJ, REFIO, IOUT1P, IOUT1N, IOUT2P, IOUT2N to AVSS	−0.3 V to AVDD33 + 0.3 V
D[15:0]P, D[15:0]N, FRAMEP, FRAMEN, DCIP, DCIN to EPAD, DVSS	−0.3 V to DVDD18 + 0.3 V
DACCLKP, DACCLKN, REFCLKP, REFCLKN to CVSS	−0.3 V to CVDD18 + 0.3 V
$\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, $\overline{\text{CS}}$, SCLK, SDIO, SDO to EPAD, DVSS	−0.3 V to IOVDD + 0.3 V
Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

The exposed pad (EPAD) of the 72-lead LFCSP must be soldered to the ground plane (AVSS). The EPAD provides an electrical, thermal, and mechanical connection to the board.

Typical θ_{JA}, θ_{JB}, and θ_{JC} values are specified for a 4-layer board in still air. Airflow increases heat dissipation, effectively reducing θ_{JA} and θ_{JB}.

Table 7. Thermal Resistance

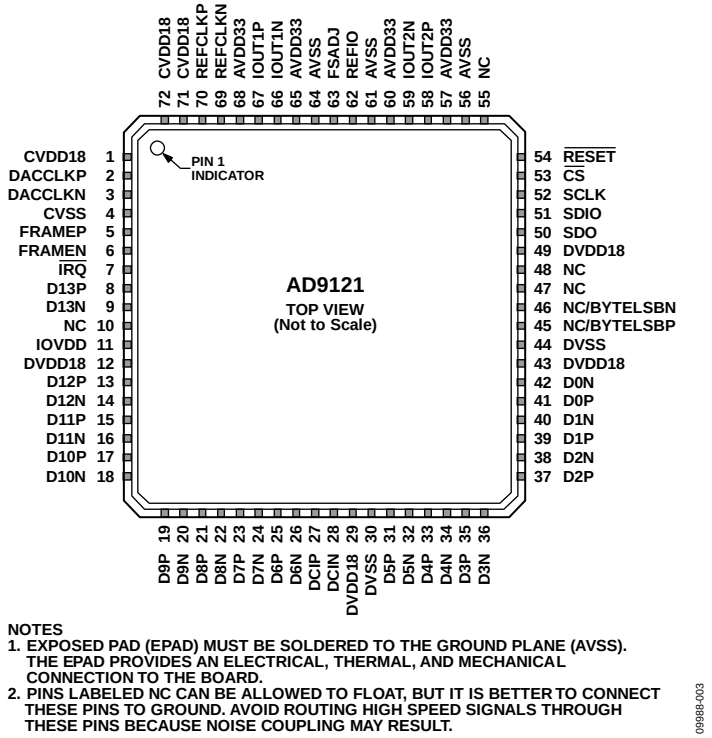
Package	θ_{JA}	θ_{JB}	θ_{JC}	Unit	Conditions
72-Lead LFCSP	20.7	10.9	1.1	°C/W	EPAD soldered to ground plane

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD (EPAD) MUST BE SOLDERED TO THE GROUND PLANE (AVSS). THE EPAD PROVIDES AN ELECTRICAL, THERMAL, AND MECHANICAL CONNECTION TO THE BOARD.
2. PINS LABELED NC CAN BE ALLOWED TO FLOAT, BUT IT IS BETTER TO CONNECT THESE PINS TO GROUND. AVOID ROUTING HIGH SPEED SIGNALS THROUGH THESE PINS BECAUSE NOISE COUPLING MAY RESULT.

Figure 3. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CVDD18	1.8 V Clock Supply. Supplies clock receivers, clock distribution, and PLL circuitry.
2	DACCLKP	DAC Clock Input, Positive.
3	DACCLKN	DAC Clock Input, Negative.
4	CVSS	Clock Supply Common.
5	FRAMEP	Frame Input, Positive. This pin must be tied to DVSS if not used.
6	FRAMEN	Frame Input, Negative. This pin must be tied to DVDD18 if not used.
7	IRQ	Interrupt Request. Open-drain, active low output. Connect an external pull-up to IOVDD through a 10 kΩ resistor.
8	D13P	Data Bit 13 (MSB), Positive.
9	D13N	Data Bit 13 (MSB), Negative.
10	NC	This pin is not connected internally (see Figure 3).
11	IOVDD	Supply Pin for Serial Port I/O Pins, RESET, and IRQ. 1.8 V to 3.3 V can be supplied to this pin.
12	DVDD18	1.8 V Digital Supply. Supplies power to digital core and digital data ports.
13	D12P	Data Bit 12, Positive.
14	D12N	Data Bit 12, Negative.
15	D11P	Data Bit 11, Positive.
16	D11N	Data Bit 11, Negative.
17	D10P	Data Bit 10, Positive.
18	D10N	Data Bit 10, Negative.
19	D9P	Data Bit 9, Positive.
20	D9N	Data Bit 9, Negative.
21	D8P	Data Bit 8, Positive.
22	D8N	Data Bit 8, Negative.

Pin No.	Mnemonic	Description
23	D7P	Data Bit 7, Positive.
24	D7N	Data Bit 7, Negative.
25	D6P	Data Bit 6, Positive.
26	D6N	Data Bit 6, Negative.
27	DCIP	Data Clock Input, Positive.
28	DCIN	Data Clock Input, Negative.
29	DVDD18	1.8 V Digital Supply. Supplies power to digital core and digital data ports.
30	DVSS	Digital Common.
31	D5P	Data Bit 5, Positive.
32	D5N	Data Bit 5, Negative.
33	D4P	Data Bit 4, Positive.
34	D4N	Data Bit 4, Negative.
35	D3P	Data Bit 3, Positive.
36	D3N	Data Bit 3, Negative.
37	D2P	Data Bit 2, Positive.
38	D2N	Data Bit 2, Negative.
39	D1P	Data Bit 1, Positive.
40	D1N	Data Bit 1, Negative.
41	D0P	Data Bit 0, Positive.
42	D0N	Data Bit 0, Negative.
43	DVDD18	1.8 V Digital Supply. Supplies power to digital core and digital data ports.
44	DVSS	Digital Common.
45	NC/ByteLSBP	This pin is not connected internally (see Figure 3) in word mode. LSB Positive (Data Bit 0) in byte mode.
46	NC/ByteLSBN	This pin is not connected internally (see Figure 3) in word mode. LSB Negative (Data Bit 0) in byte mode.
47	NC	This pin is not connected internally (see Figure 3).
48	NC	This pin is not connected internally (see Figure 3).
49	DVDD18	1.8 V Digital Supply. Supplies power to digital core and digital data ports.
50	SDO	Serial Port Data Output (CMOS Levels with Respect to IOVDD).
51	SDIO	Serial Port Data Input/Output (CMOS Levels with Respect to IOVDD).
52	SCLK	Serial Port Clock Input (CMOS Levels with Respect to IOVDD).
53	$\overline{CS}$	Serial Port Chip Select, Active Low (CMOS Levels with Respect to IOVDD).
54	$\overline{RESET}$	Reset, Active Low (CMOS Levels with Respect to IOVDD).
55	NC	This pin is not connected internally (see Figure 3).
56	AVSS	Analog Supply Common.
57	AVDD33	3.3 V Analog Supply.
58	IOUT2P	Q DAC Positive Current Output.
59	IOUT2N	Q DAC Negative Current Output.
60	AVDD33	3.3 V Analog Supply.
61	AVSS	Analog Supply Common.
62	REFIO	Voltage Reference. Nominally 1.2 V output. Should be decoupled to AVSS.
63	FSADJ	Full-Scale Current Output Adjust. Place a 10 kΩ resistor from this pin to AVSS.
64	AVSS	Analog Supply Common.
65	AVDD33	3.3 V Analog Supply.
66	IOUT1N	I DAC Negative Current Output.
67	IOUT1P	I DAC Positive Current Output.
68	AVDD33	3.3 V Analog Supply.
69	REFCLKN	PLL Reference Clock Input, Negative. This pin has a secondary function as a synchronization input.
70	REFCLKP	PLL Reference Clock Input, Positive. This pin has a secondary function as a synchronization input.
71	CVDD18	1.8 V Clock Supply. Supplies clock receivers, clock distribution, and PLL circuitry.
72	CVDD18	1.8 V Clock Supply. Supplies clock receivers, clock distribution, and PLL circuitry.
	EPAD	The exposed pad (EPAD) must be soldered to the ground plane (AVSS). The EPAD provides an electrical, thermal, and mechanical connection to the board.

TYPICAL PERFORMANCE CHARACTERISTICS

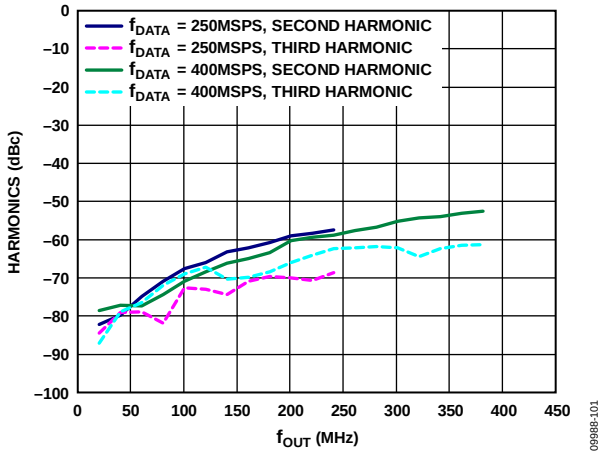


Figure 4. Harmonics vs. f_{OUT} over f_{DATA}, 2× Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA

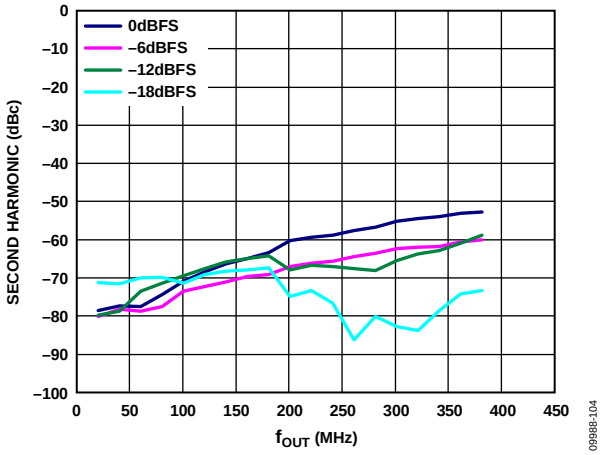


Figure 7. Second Harmonic vs. f_{OUT} over Digital Scale, 2× Interpolation, f_{DATA} = 400 MSPS, I_{FS} = 20 mA

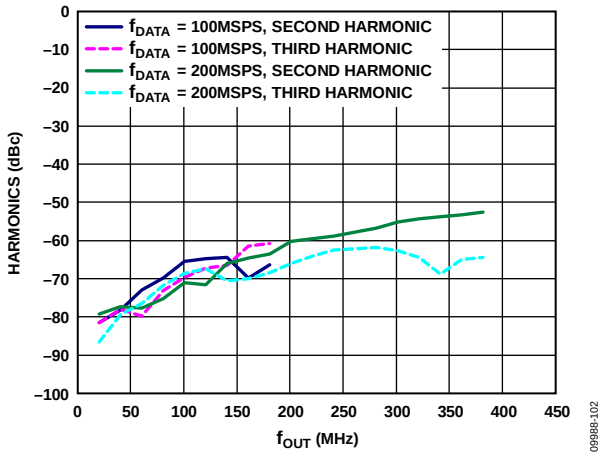


Figure 5. Harmonics vs. f_{OUT} over f_{DATA}, 4× Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA

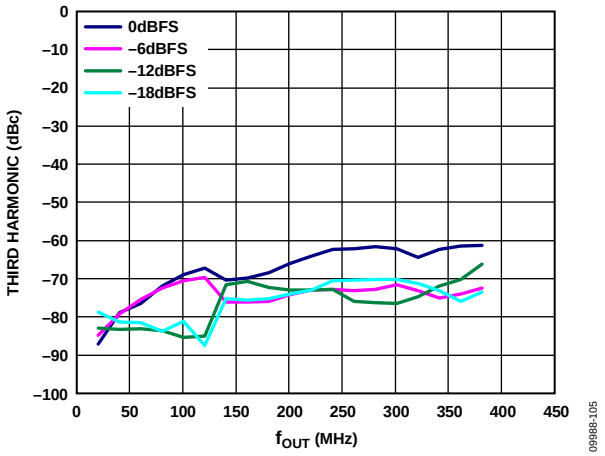


Figure 8. Third Harmonic vs. f_{OUT} over Digital Scale, 2× Interpolation, f_{DATA} = 400 MSPS, I_{FS} = 20 mA

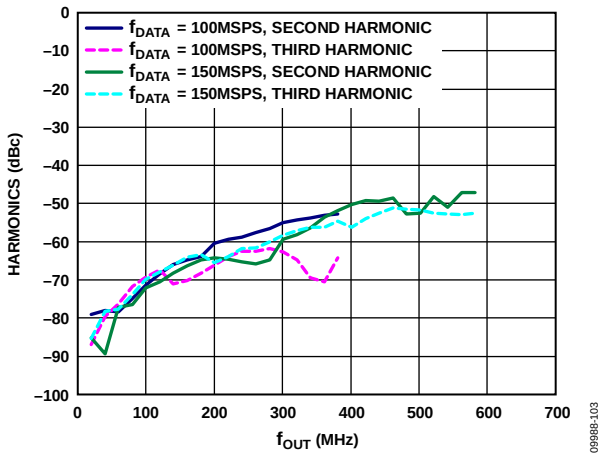


Figure 6. Harmonics vs. f_{OUT} over f_{DATA}, 8× Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA

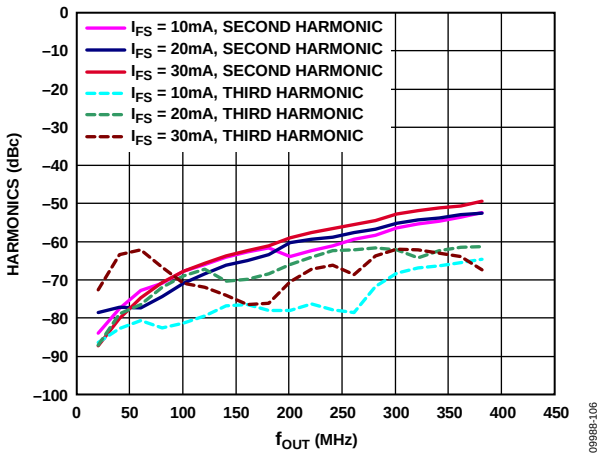


Figure 9. Harmonics vs. f_{OUT} over I_{FS}, 2× Interpolation, f_{DATA} = 400 MSPS, Digital Scale = 0 dBFS

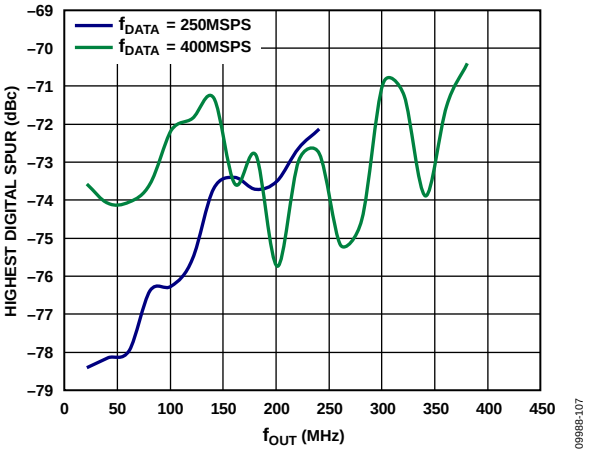


Figure 10. Highest Digital Spur vs. f_{OUT} over f_{DATA}, 2× Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA

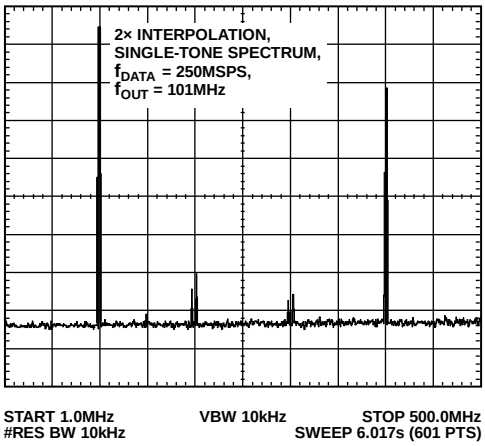


Figure 13. Single-Tone Spectrum, 2× Interpolation, f_{DATA} = 250 MSPS, f_{OUT} = 101 MHz

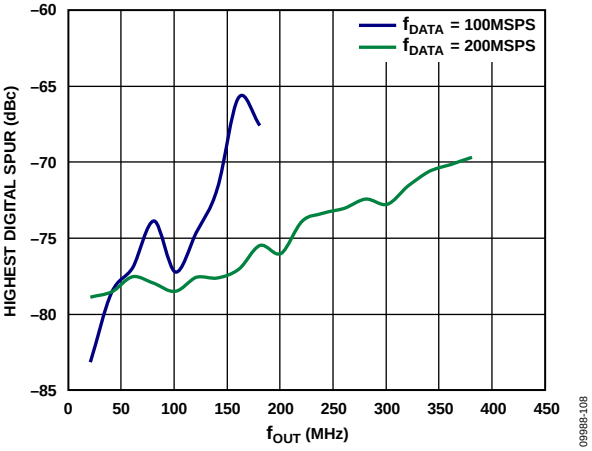


Figure 11. Highest Digital Spur vs. f_{OUT} over f_{DATA}, 4× Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA

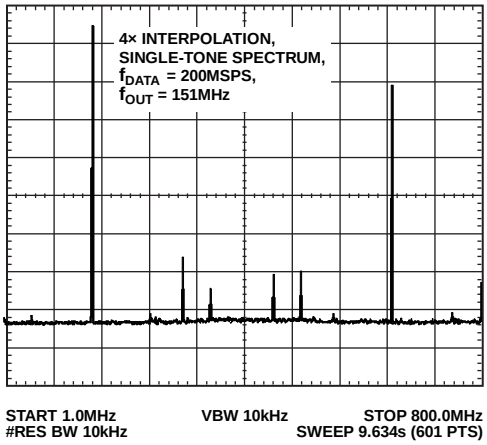


Figure 14. Single-Tone Spectrum, 4× Interpolation, f_{DATA} = 200 MSPS, f_{OUT} = 151 MHz

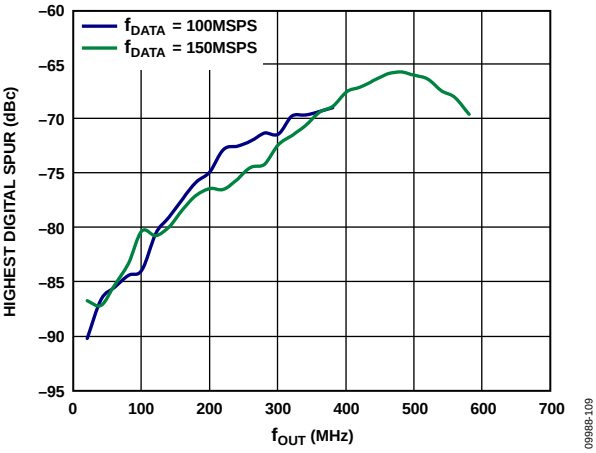


Figure 12. Highest Digital Spur vs. f_{OUT} over f_{DATA}, 8× Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA

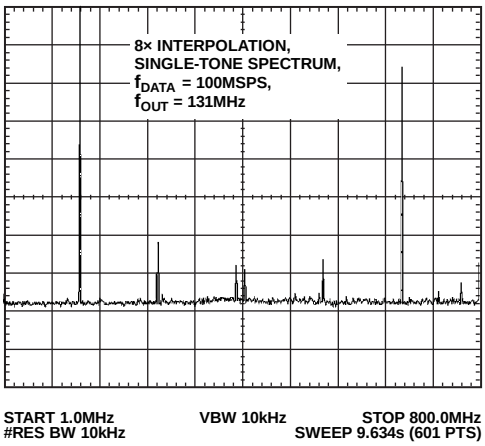


Figure 15. Single-Tone Spectrum, 8× Interpolation, f_{DATA} = 100 MSPS, f_{OUT} = 131 MHz

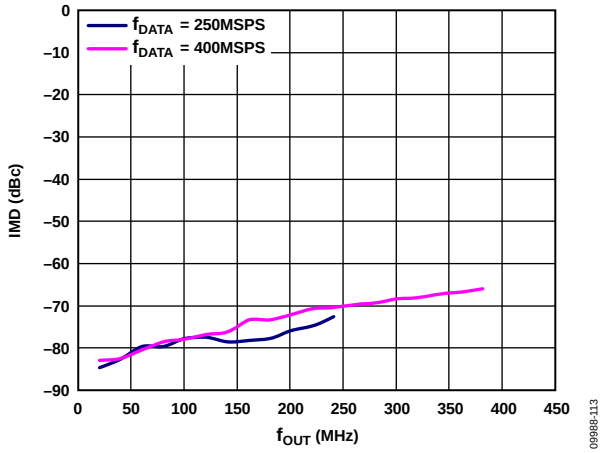


Figure 16. IMD vs. f_{OUT} over f_{DATA}, 2× Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA

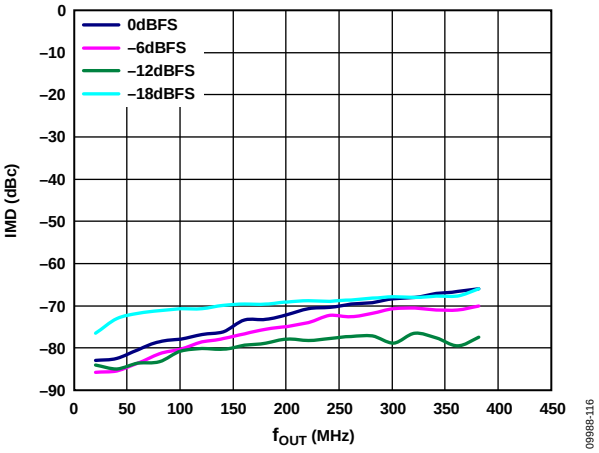


Figure 19. IMD vs. f_{OUT} over Digital Scale, 2× Interpolation, f_{DATA} = 400 MSPS, I_{FS} = 20 mA

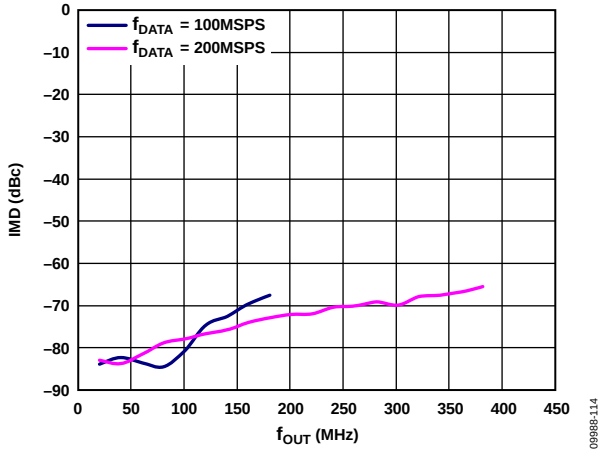


Figure 17. IMD vs. f_{OUT} over f_{DATA}, 4× Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA

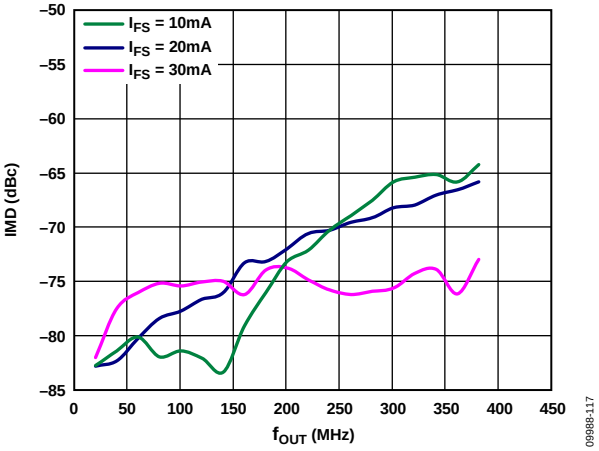


Figure 20. IMD vs. f_{OUT} over I_{FS}, 2× Interpolation, f_{DATA} = 400 MSPS, Digital Scale = 0 dBFS

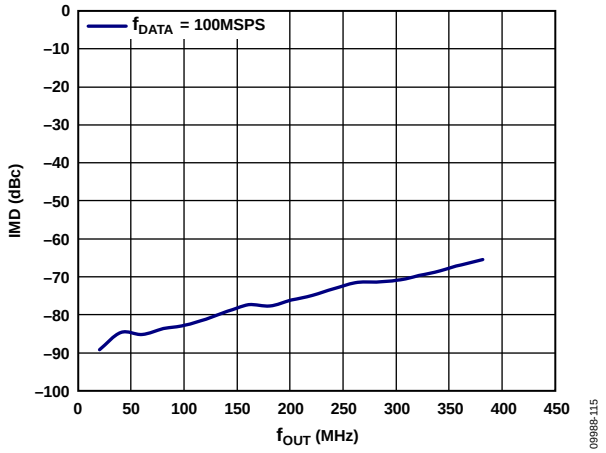


Figure 18. IMD vs. f_{OUT}, 8× Interpolation, f_{DATA} = 100 MSPS, Digital Scale = 0 dBFS, I_{FS} = 20 mA

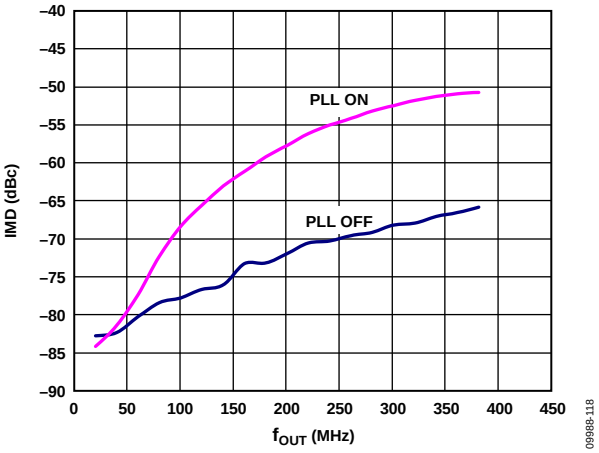


Figure 21. IMD vs. f_{OUT}, 4× Interpolation, f_{DATA} = 200 MSPS, Digital Scale = 0 dBFS, I_{FS} = 20 mA, PLL On and PLL Off

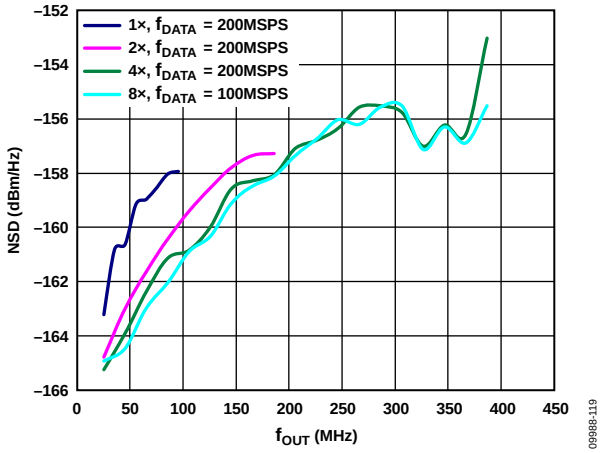


Figure 22. One-Tone NSD vs. f_{OUT} over Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA, PLL Off

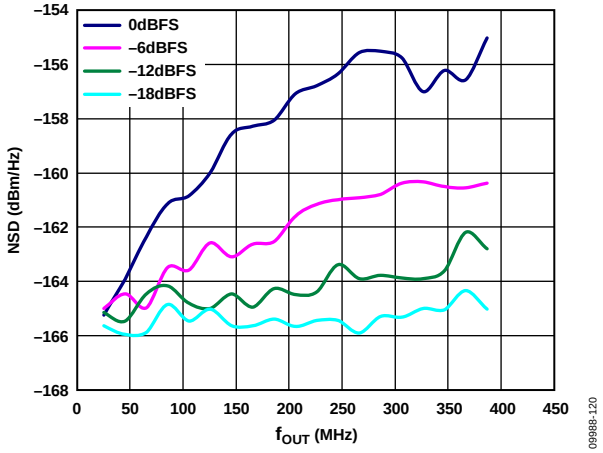


Figure 23. One-Tone NSD vs. f_{OUT} over Digital Scale, 4× Interpolation, f_{DATA} = 200 MSPS, I_{FS} = 20 mA, PLL Off

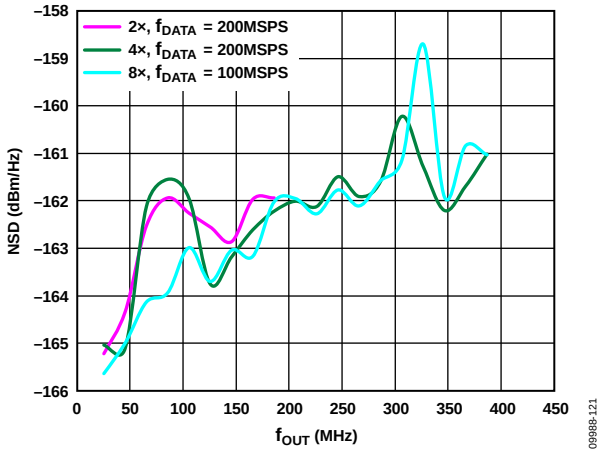


Figure 24. One-Tone NSD vs. f_{OUT} over Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA, PLL On

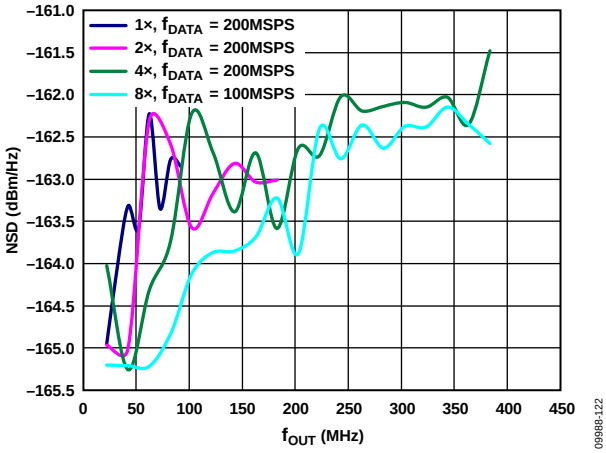


Figure 25. Eight-Tone NSD vs. f_{OUT} over Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA, PLL Off

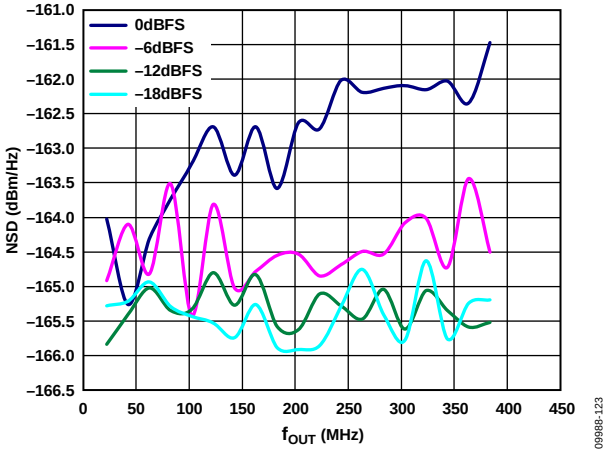


Figure 26. Eight-Tone NSD vs. f_{OUT} over Digital Scale, 4× Interpolation, f_{DATA} = 200 MSPS, I_{FS} = 20 mA, PLL Off

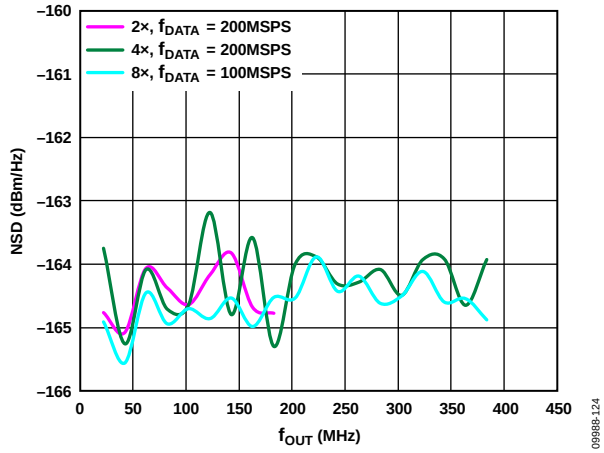


Figure 27. Eight-Tone NSD vs. f_{OUT} over Interpolation, Digital Scale = 0 dBFS, I_{FS} = 20 mA, PLL On

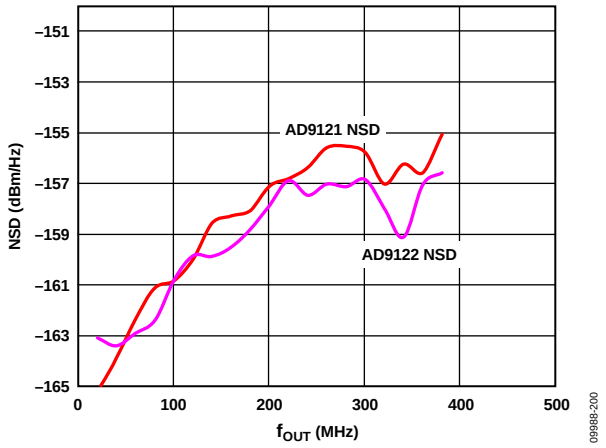


Figure 28. One-Tone NSD vs. f_{OUT}, f_{DATA} = 400 MSPS, 2× Interpolation, PLL Off (Comparison of AD9121 vs. AD9122)

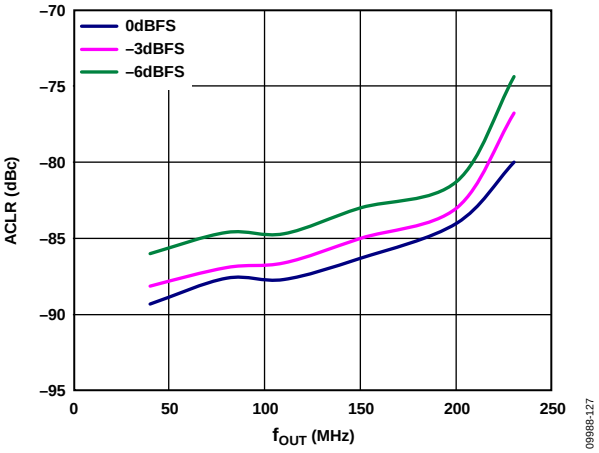


Figure 31. One-Carrier W-CDMA ACLR vs. f_{OUT} over Digital Scale, Second Alternate Channel, PLL Off

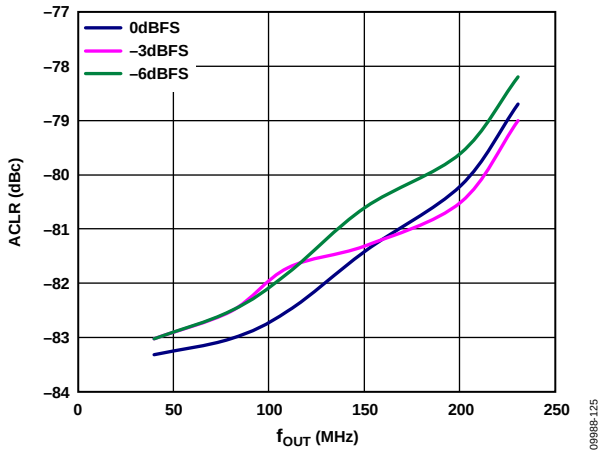


Figure 29. One-Carrier W-CDMA ACLR vs. f_{OUT} over Digital Scale, Adjacent Channel, PLL Off

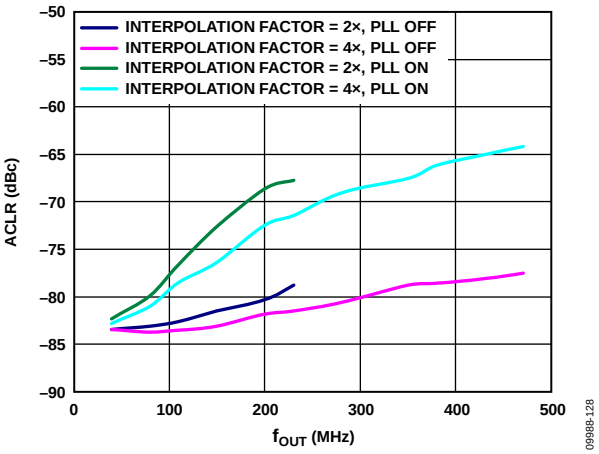


Figure 32. One-Carrier W-CDMA ACLR vs. f_{OUT} over Interpolation, Adjacent Channel, PLL On and PLL Off

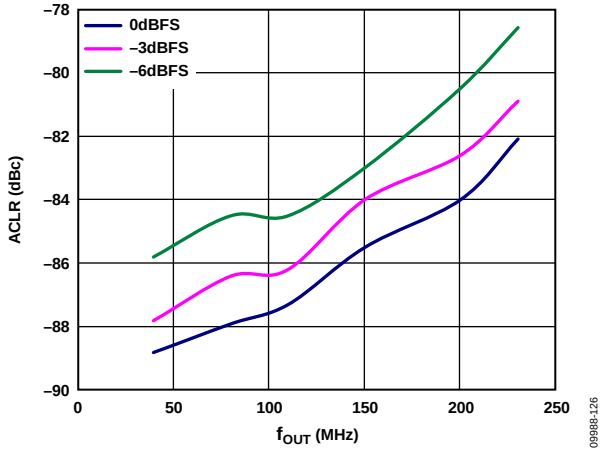


Figure 30. One-Carrier W-CDMA ACLR vs. f_{OUT} over Digital Scale, First Alternate Channel, PLL Off

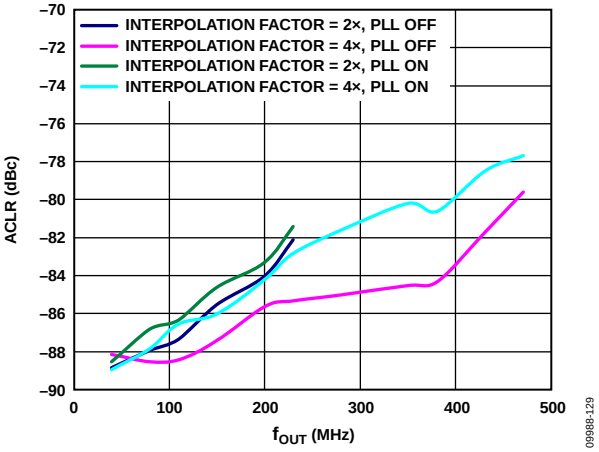


Figure 33. One-Carrier W-CDMA ACLR vs. f_{OUT} over Interpolation, First Alternate Channel, PLL On and PLL Off

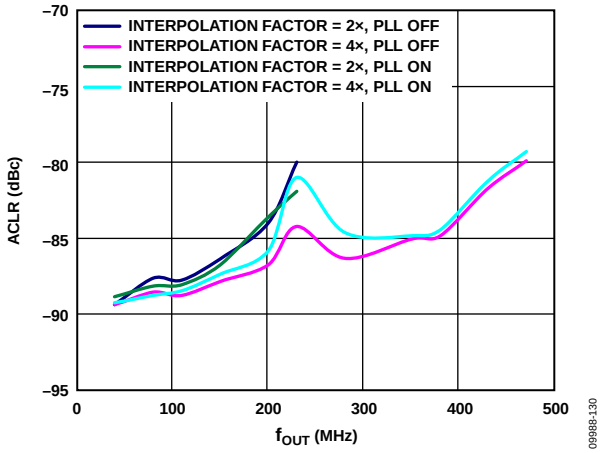
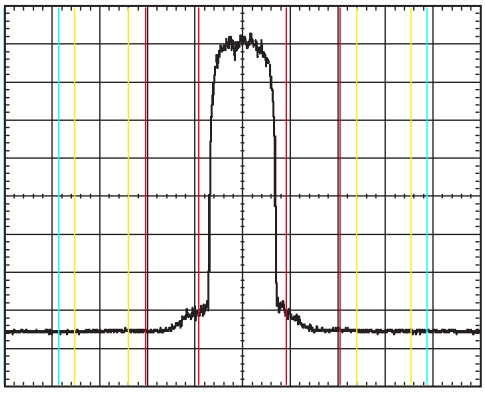


Figure 34. One-Carrier W-CDMA ACLR vs. f_{OUT} over Interpolation, Second Alternate Channel, PLL On and PLL Off



RMS RESULTS	FREQ OFFSET	REF BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm
CARRIER POWER –10.00dBm/ 3.840MHz	5.00MHz	3.840MHz	–75.96	–85.96	–77.13	–87.13
	10.00MHz	3.840MHz	–85.33	–95.33	–85.24	–95.25
	15.00MHz	2.888MHz	–95.81	–95.81	–85.43	–95.43

Figure 35. One-Carrier W-CDMA ACLR Performance, IF = ~150 MHz

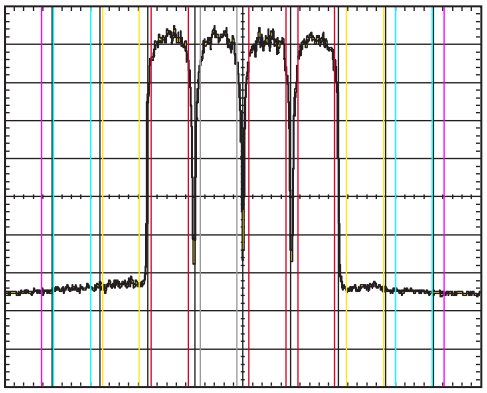


Figure 36. Four-Carrier W-CDMA ACLR Performance, IF = ~150 MHz

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Offset Error
Offset error is the deviation of the output current from the ideal of 0 mA. For IOUT1P, 0 mA output is expected when all inputs are set to 0. For IOUT1N, 0 mA output is expected when all inputs are set to 1.

Gain Error
Gain error is the difference between the actual and ideal output span. The actual span is determined by the difference between the output when all inputs are set to 1 and the output when all inputs are set to 0.

Output Compliance Range
The output compliance range is the range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree Celsius. For reference voltage drift, the drift is reported in ppm per degree Celsius.

Power Supply Rejection (PSR)
PSR is the maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time
Settling time is the time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal within the dc to Nyquist frequency of the DAC. Typically, energy in this band is rejected by the interpolation filters. This specification, therefore, defines how well the interpolation filters work and the effect of other parasitic coupling paths on the DAC output.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Interpolation Filter
If the digital inputs to the DAC are sampled at a multiple rate of f_{DATA} (interpolation rate), a digital filter can be constructed that has a sharp transition band near $f_{DATA}/2$. Images that typically appear around f_{DAC} (output data rate) can be greatly suppressed.

Adjacent Channel Leakage Ratio (ACLR)
ACLR is the ratio, in decibels relative to the carrier (dBc), between the measured power within a channel and that of its adjacent channel.

Complex Image Rejection
In a traditional two-part upconversion, two images are created around the second IF frequency. These images have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

THEORY OF OPERATION

The AD9121 combines many features that make it a very attractive DAC for wired and wireless communications systems. The dual digital signal path and dual DAC structure allow an easy interface to common quadrature modulators when designing single sideband (SSB) transmitters. The speed and performance of the AD9121 allow wider bandwidths and more carriers to be synthesized than in previously available DACs. In addition, the AD9121 includes an innovative low power, 32-bit, complex NCO that greatly increases the ease of frequency placement.

The AD9121 offers features that allow simplified synchronization with incoming data and between multiple devices. Auxiliary DACs are also provided on chip. The auxiliary DACs can be used for output dc offset compensation (for LO compensation in SSB transmitters) and for gain matching (for image rejection optimization in SSB transmitters).

SERIAL PORT OPERATION

The serial port is a flexible, synchronous serial communications port that allows easy interfacing to many industry-standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola SPI and Intel® SSR protocols. The interface allows read/write access to all registers that configure the AD9121. Single-byte or multiple-byte transfers are supported, as well as MSB first or LSB first transfer formats. The serial port interface can be configured as a single-pin I/O (SDIO) or as two unidirectional pins for input and output (SDIO and SDO).

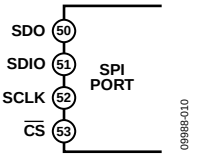


Figure 37. Serial Port Interface Pins

A communication cycle with the AD9121 has two phases. Phase 1 is the instruction cycle (the writing of an instruction byte into the device), coincident with the first eight SCLK rising edges. The instruction byte provides the serial port controller with information regarding the data transfer cycle—Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is a read or write, along with the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the device.

A logic high on the $\overline{CS}$ pin followed by a logic low resets the serial port timing to the initial state of the instruction cycle. From this state, the next eight rising SCLK edges represent the instruction bits of the current I/O operation.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the device and the system controller. Phase 2 of the communication cycle is a transfer of one or more data bytes. Registers change immediately upon writing to the last bit of each transfer byte, except for the frequency tuning word and NCO phase offsets, which change only when the frequency tuning word (FTW) update bit (Register 0x36, Bit 0) is set.

DATA FORMAT

The instruction byte contains the information shown in Table 9.

Table 9. Serial Port Instruction Byte

I7 (MSB)	I6	I5	I4	I3	I2	I1	I0 (LSB)
R/W	A6	A5	A4	A3	A2	A1	A0

R/$\overline{W}$, Bit 7 of the instruction byte, determines whether a read or a write data transfer occurs after the instruction byte write. Logic 1 indicates a read operation, and Logic 0 indicates a write operation.

A6 to A0, Bit 6 to Bit 0 of the instruction byte, determine the register that is accessed during the data transfer portion of the communication cycle. For multibyte transfers, A6 is the starting byte address. The remaining register addresses are generated by the device based on the LSB_FIRST bit (Register 0x00, Bit 6).

SERIAL PORT PIN DESCRIPTIONS

Serial Clock (SCLK)

The serial clock pin synchronizes data to and from the device and runs the internal state machines. The maximum frequency of SCLK is 40 MHz. All data input is registered on the rising edge of SCLK. All data is driven out on the falling edge of SCLK.

Chip Select ($\overline{CS}$)

An active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communications lines. When the $\overline{CS}$ pin is high, the SDO and SDIO pins go to a high impedance state. During the communication cycle, the $\overline{CS}$ pin should stay low.

Serial Data I/O (SDIO)

Data is always written into the device on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by Register 0x00, Bit 7. The default is Logic 0, configuring the SDIO pin as unidirectional.

Serial Data Output (SDO)

Data is read from this pin for protocols that use separate lines for transmitting and receiving data. If the device operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

SERIAL PORT OPTIONS

The serial port can support both MSB first and LSB first data formats. This functionality is controlled by the LSB_FIRST bit (Register 0x00, Bit 6). The default is MSB first (LSB_FIRST = 0).

When LSB_FIRST = 0 (MSB first), the instruction and data bits must be written from MSB to LSB. Multibyte data transfers in MSB first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes should follow from high address to low address. In MSB first mode, the serial port internal byte address generator decrements for each data byte of the multibyte communication cycle.

When LSB_FIRST = 1 (LSB first), the instruction and data bits must be written from LSB to MSB. Multibyte data transfers in LSB first format start with an instruction byte that includes the register address of the least significant data byte. Subsequent data bytes should follow from low address to high address. In LSB first mode, the serial port internal byte address generator increments for each data byte of the multibyte communication cycle.

If the MSB first mode is active, the serial port controller data address decrements from the data address written toward 0x00 for multibyte I/O operations. If the LSB first mode is active, the serial port controller data address increments from the data address written toward 0x7F for multibyte I/O operations.

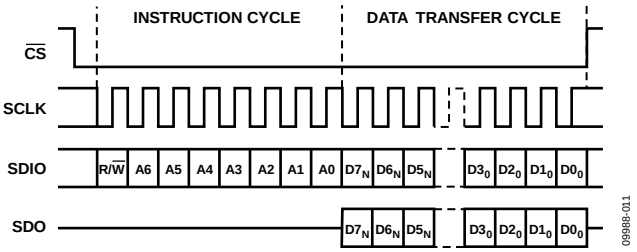


Figure 38. Serial Port Interface Timing, MSB First

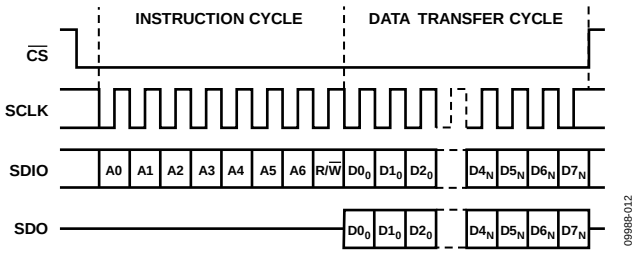


Figure 39. Serial Port Interface Timing, LSB First

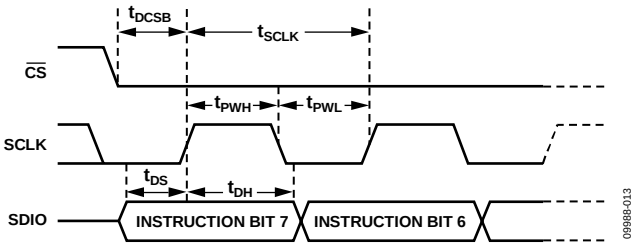


Figure 40. Timing Diagram for Serial Port Register Write

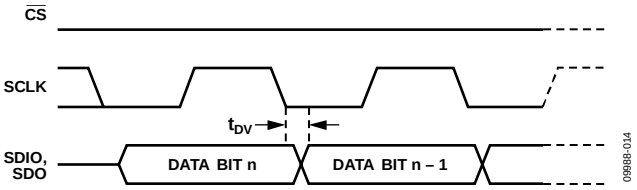


Figure 41. Timing Diagram for Serial Port Register Read

DEVICE CONFIGURATION REGISTER MAP AND DESCRIPTIONS

Table 10. Device Configuration Register Map

Addr (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x00	Comm	SDIO	LSB_FIRST	Reset						0x00
0x01	Power control	Power down I DAC	Power down Q DAC	Power down data receiver	Power down aux ADC					0x10
0x03	Data format	Binary data format	Q data first	MSB swap				Data Bus Width[1:0]		0x00
0x04	Interrupt enable	Enable PLL lock lost	Enable PLL locked	Enable sync signal lost	Enable sync signal locked			Enable FIFO Warning 1	Enable FIFO Warning 2	0x00
0x05	Interrupt enable	0	0	0	Enable AED compare pass	Enable AED compare fail	Enable SED compare fail	0	0	0x00
0x06	Event flag	PLL lock lost	PLL locked	Sync signal lost	Sync signal locked			FIFO Warning 1	FIFO Warning 2	N/A
0x07	Event flag				AED compare pass	AED compare fail	SED compare fail			N/A
0x08	Clock receiver control	DACCLK duty correction	REFCLK duty correction	DACCLK cross-correction	REFCLK cross-correction	1	1	1	1	0x3F
0x0A	PLL control	PLL enable	PLL manual enable	Manual VCO Band[5:0]						0x40
0x0C	PLL control	PLL Loop Bandwidth[1:0]			PLL Charge Pump Current[4:0]					0xD1
0x0D	PLL control	N2[1:0]			PLL cross-control enable	N0[1:0]		N1[1:0]		0xD9
0x0E	PLL status	PLL locked				VCO Control Voltage[3:0]				N/A
0x0F	PLL status			VCO Band Readback[5:0]						N/A
0x10	Sync control	Sync enable	Data/FIFO rate toggle			Rising edge sync	Sync Averaging[2:0]			0x48
0x11	Sync control			Sync Phase Request[5:0]						0x00
0x12	Sync status	Sync lost	Sync locked							N/A
0x13	Sync status	Sync Phase Readback[7:0] (6.2 format)								N/A
0x15	Data receiver status			LVDS FRAME level high	LVDS FRAME level low	LVDS DCI level high	LVDS DCI level low	LVDS data level high	LVDS data level low	N/A
0x16	DCI delay							DCI Delay[1:0]		0x00
0x17	FIFO control						FIFO Phase Offset[2:0]			0x04
0x18	FIFO status	FIFO Warning 1	FIFO Warning 2				FIFO soft align ack	FIFO soft align request		N/A
0x19	FIFO status	FIFO Level[7:0]								N/A
0x1B	Datapath control	Bypass premod	Bypass $sinc^{-1}$	Bypass NCO		NCO gain	Bypass phase comp and dc offset	Select sideband	Send I data to Q data	0xE4

Addr (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x1C	HB1 control						HB1[1:0]		Bypass HB1	0x00
0x1D	HB2 control		HB2[5:0]						Bypass HB2	0x00
0x1E	HB3 control		HB3[5:0]						Bypass HB3	0x00
0x1F	Chip ID	Chip ID[7:0]								0x08
0x30	FTW LSB	FTW[7:0]								0x00
0x31	FTW	FTW[15:8]								0x00
0x32	FTW	FTW[23:16]								0x00
0x33	FTW MSB	FTW[31:24]								0x00
0x34	NCO phase offset LSB	NCO Phase Offset[7:0]								0x00
0x35	NCO phase offset MSB	NCO Phase Offset[15:8]								0x00
0x36	NCO FTW update			FRAME FTW ack	FRAME FTW request			Update FTW ack	Update FTW request	0x00
0x38	I phase adj LSB	I Phase Adj[7:0]								0x00
0x39	I phase adj MSB							I Phase Adj[9:8]		0x00
0x3A	Q phase adj LSB	Q Phase Adj[7:0]								0x00
0x3B	Q phase adj MSB							Q Phase Adj[9:8]		0x00
0x3C	I DAC offset LSB	I DAC Offset[7:0]								0x00
0x3D	I DAC offset MSB	I DAC Offset[15:8]								0x00
0x3E	Q DAC offset LSB	Q DAC Offset[7:0]								0x00
0x3F	Q DAC offset MSB	Q DAC Offset[15:8]								0x00
0x40	I DAC FS adjust	I DAC FS Adj[7:0]								0xF9
0x41	I DAC control	I DAC sleep						I DAC FS Adj[9:8]		0x01
0x42	I aux DAC data	I Aux DAC[7:0]								0x00
0x43	I aux DAC control	I aux DAC sign	I aux DAC current direction	I aux DAC sleep				I Aux DAC[9:8]		0x00
0x44	Q DAC FS adjust	Q DAC FS Adj[7:0]								0xF9
0x45	Q DAC control	Q DAC sleep						Q DAC FS Adj[9:8]		0x01
0x46	Q aux DAC data	Q Aux DAC[7:0]								0x00
0x47	Q aux DAC control	Q aux DAC sign	Q aux DAC current direction	Q aux DAC sleep				Q Aux DAC[9:8]		0x00
0x48	Die temp range control		FS Current[2:0]			Reference Current[2:0]			Capacitor value	0x02
0x49	Die temp LSB	Die Temp[7:0]								N/A
0x4A	Die temp MSB	Die Temp[15:8]								N/A
0x67	SED control	SED compare enable		Sample error detected		Autoclear enable		Compare fail	Compare pass	0x00
0x68	Compare I0 LSBs	Compare Value I0[7:0]								0xB6
0x69	Compare I0 MSBs	Compare Value I0[15:8]								0x7A
0x6A	Compare Q0 LSBs	Compare Value Q0[7:0]								0x45
0x6B	Compare Q0 MSBs	Compare Value Q0[15:8]								0xEA

Addr (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x6C	Compare I1 LSBs	Compare Value I1[7:0]								0x16
0x6D	Compare I1 MSBs	Compare Value I1[15:8]								0x1A
0x6E	Compare Q1 LSBs	Compare Value Q1[7:0]								0xC6
0x6F	Compare Q1 MSBs	Compare Value Q1[15:8]								0xAA
0x70	SED I LSBs	Errors Detected I_BITS[7:0]								0x00
0x71	SED I MSBs	Errors Detected I_BITS[15:8]								0x00
0x72	SED Q LSBs	Errors Detected Q_BITS[7:0]								0x00
0x73	SED Q MSBs	Errors Detected Q_BITS[15:8]								0x00
0x7F	Revision	0	0	Revision[3:0]				0	0	N/A

Table 11. Device Configuration Register Descriptions

Register Name	Address (Hex)	Bits	Name	Description	Default
Comm	0x00	7	SDIO	SDIO pin operation. 0 = SDIO operates as an input only. 1 = SDIO operates as a bidirectional input/output.	0
		6	LSB_FIRST	Serial port communication, LSB or MSB first. 0 = MSB first. 1 = LSB first.	0
		5	Reset	The device is placed in reset when this bit is written high and remains in reset until the bit is written low.	0
Power Control	0x01	7	Power down I DAC	1 = power down I DAC.	0
		6	Power down Q DAC	1 = power down Q DAC.	0
		5	Power down data receiver	1 = power down the input data receiver.	0
		4	Power down auxiliary ADC	1 = power down the auxiliary ADC for temperature sensor.	1
Data Format	0x03	7	Binary data format	0 = input data is in twos complement format. 1 = input data is in binary format.	0
		6	Q data first	Indicates I/Q data pairing on data input. 0 = I data sent to data receiver first. 1 = Q data sent to data receiver first.	0
		5	MSB swap	Swaps the bit order of the data input port. 0 = order of the data bits corresponds to the pin descriptions. 1 = bit designations are swapped; most significant bits become the least significant bits.	0
		[1:0]	Data Bus Width[1:0]	Data receiver interface mode. See the LVDS Input Data Ports section for information about the operation of the different interface modes. 00 = word mode; 14-bit interface bus width. 01 = byte mode; 7-bit interface bus width. 10 = invalid. 11 = invalid.	00
Interrupt Enable	0x04	7	Enable PLL lock lost	1 = enable interrupt for PLL lock lost.	0
		6	Enable PLL locked	1 = enable interrupt for PLL locked.	0
		5	Enable sync signal lost	1 = enable interrupt for sync signal lost.	0
		4	Enable sync signal locked	1 = enable interrupt for sync signal locked.	0
		1	Enable FIFO Warning 1	1 = enable interrupt for FIFO Warning 1.	0
		0	Enable FIFO Warning 2	1 = enable interrupt for FIFO Warning 2.	0

Register Name	Address (Hex)	Bits	Name	Description	Default
Interrupt Enable	0x05	[7:5]	Set to 0	Set these bits to 0.	000
		4	Enable AED compare pass	1 = enable interrupt for AED comparison pass.	0
		3	Enable AED compare fail	1 = enable interrupt for AED comparison fail.	0
		2	Enable SED compare fail	1 = enable interrupt for SED comparison fail.	0
		[1:0]	Set to 0	Set these bits to 0.	00
Event Flag	0x06	7	PLL lock lost	1 = indicates that the PLL, which had been previously locked, has unlocked from the reference signal. This is a latched signal.	N/A
		6	PLL locked	1 = indicates that the PLL has locked to the reference clock input.	N/A
		5	Sync signal lost	1 = indicates that the sync logic, which had been previously locked, has lost alignment. This is a latched signal.	N/A
		4	Sync signal locked	1 = indicates that the sync logic has achieved sync alignment. This is indicated when no phase changes were requested for at least a few full averaging cycles.	N/A
		1	FIFO Warning 1	1 = indicates that the difference between the FIFO read and write pointers is 1.	N/A
		0	FIFO Warning 2	1 = indicates that the difference between the FIFO read and write pointers is 2.	N/A
			Note that all event flags are cleared by writing the respective bit high.		
	0x07	4	AED compare pass	1 = indicates that the SED logic detected a valid input data pattern compared against the preprogrammed expected values. This is a latched signal.	N/A
		3	AED compare fail	1 = indicates that the SED logic detected an invalid input data pattern compared against the preprogrammed expected values. This latched signal is automatically cleared when eight valid I/Q data pairs are received.	N/A
		2	SED compare fail	1 = indicates that the SED logic detected an invalid input data pattern compared against the preprogrammed expected values. This is a latched signal.	N/A
			Note that all event flags are cleared by writing the respective bit high.		
Clock Receiver Control	0x08	7	DACCLK duty correction	1 = enable duty cycle correction on the DACCLK input.	0
		6	REFCLK duty correction	1 = enable duty cycle correction on the REFCLK input.	0
		5	DACCLK cross-correction	1 = enable differential crossing correction on the DACCLK input.	1
		4	REFCLK cross-correction	1 = enable differential crossing correction on the REFCLK input.	1
PLL Control	0x0A	7	PLL enable	1 = enable the PLL clock multiplier. The REFCLK input is used as the PLL reference clock signal.	0
		6	PLL manual enable	1 = enable manual selection of the VCO band. The correct VCO band must be determined by the user and written to Bits[5:0].	1
		[5:0]	Manual VCO Band[5:0]	Selects the VCO band to be used.	000000
	0x0C	[7:6]	PLL Loop Bandwidth[1:0]	Selects the PLL loop filter bandwidth. 00 = widest bandwidth. … 11 = narrowest bandwidth.	11
		[4:0]	PLL Charge Pump Current[4:0]	Sets the nominal PLL charge pump current. 00000 = lowest current setting. … 11111 = highest current setting.	10001

Register Name	Address (Hex)	Bits	Name	Description	Default
PLL Control	0x0D	[7:6]	N2[1:0]	PLL control clock divider. This divider determines the ratio of the REFCLK frequency to the PLL controller clock frequency. f_{PC_CLK} must always be less than 75 MHz. 00 = f_{REFCLK}/f_{PC_CLK} = 2. 01 = f_{REFCLK}/f_{PC_CLK} = 4. 10 = f_{REFCLK}/f_{PC_CLK} = 8. 11 = f_{REFCLK}/f_{PC_CLK} = 16.	11
		4	PLL cross-control enable	1 = enable PLL cross-point controller.	1
		[3:2]	N0[1:0]	PLL VCO divider. This divider determines the ratio of the VCO frequency to the DACCLK frequency. 00 = f_{VCO}/f_{DACCLK} = 1. 01 = f_{VCO}/f_{DACCLK} = 2. 10 = f_{VCO}/f_{DACCLK} = 4. 11 = f_{VCO}/f_{DACCLK} = 4.	10
		[1:0]	N1[1:0]	PLL loop divider. This divider determines the ratio of the DACCLK frequency to the REFCLK frequency. 00 = f_{DACCLK}/f_{REFCLK} = 2. 01 = f_{DACCLK}/f_{REFCLK} = 4. 10 = f_{DACCLK}/f_{REFCLK} = 8. 11 = f_{DACCLK}/f_{REFCLK} = 16.	01
PLL Status	0x0E	7	PLL locked	1 = the PLL-generated clock is tracking the REFCLK input signal.	N/A
		[3:0]	VCO Control Voltage[3:0]	VCO control voltage readback. See Table 24.	N/A
	0x0F	[5:0]	VCO Band Readback[5:0]	Indicates the VCO band currently selected.	N/A
Sync Control	0x10	7	Sync enable	1 = enable the synchronization logic.	0
		6	Data/FIFO rate toggle	0 = operate the synchronization at the FIFO reset rate. 1 = operate the synchronization at the data rate.	1
		3	Rising edge sync	0 = sync is initiated on the falling edge of the sync input. 1 = sync is initiated on the rising edge of the sync input.	1
		[2:0]	Sync Averaging[2:0]	Sets the number of input samples that are averaged in determining the sync phase. 000 = 1. 001 = 2. 010 = 4. 011 = 8. 100 = 16. 101 = 32. 110 = 64. 111 = 128.	000
	0x11	[5:0]	Sync Phase Request[5:0]	This register sets the requested clock phase offset after sync. The offset unit is in DACCLK cycles. This register enables repositioning of the DAC output with respect to the sync input. The offset can also be used to skew the DAC outputs between the synchronized DACs. 000000 = 0 DACCLK cycles. 000001 = 1 DACCLK cycle. … 111111 = 63 DACCLK cycles.	000000

Register Name	Address (Hex)	Bits	Name	Description	Default
Sync Status	0x12	7	Sync lost	1 = synchronization was attained but has been lost.	N/A
		6	Sync locked	1 = synchronization has been attained.	N/A
	0x13	[7:0]	Sync Phase Readback[7:0]	Indicates the averaged sync phase offset (6.2 format). If this value differs from the Sync Phase Request[5:0] value in Register 0x11, a sync timing error has occurred. For more information, see the Sync Status Bits section. 00000000 = 0.0. 00000001 = 0.25. … 11111110 = 63.50. 11111111 = 63.75.	N/A
Data Receiver Status	0x15	5	LVDS FRAME level high	One or both LVDS FRAME input signals have exceeded 1.7 V.	N/A
		4	LVDS FRAME level low	One or both LVDS FRAME input signals have crossed below 0.7 V.	N/A
		3	LVDS DCI level high	One or both LVDS DCI input signals have exceeded 1.7 V.	N/A
		2	LVDS DCI level low	One or both LVDS DCI input signals have crossed below 0.7 V.	N/A
		1	LVDS data level high	One or more LVDS Dx input signals have exceeded 1.7 V.	N/A
		0	LVDS data level low	One or more LVDS Dx input signals have crossed below 0.7 V.	N/A
DCI Delay	0x16	[1:0]	DCI Delay[1:0]	This option is available for the Revision 2 silicon only. The DCI delay bits control the delay applied to the DCI signal. The DCI delay affects the sampling interval of the DCI with respect to the Dx inputs. See Table 13. 00 = 350 ps delay of DCI signal. 01 = 590 ps delay of DCI signal. 10 = 800 ps delay of DCI signal. 11 = 925 ps delay of DCI signal.	00
FIFO Control	0x17	[2:0]	FIFO Phase Offset[2:0]	FIFO write pointer phase offset following FIFO reset. This is the difference between the read pointer and the write pointer values upon FIFO reset. The optimal value is nominally 4 (100). 000 = 0. 001 = 1. … 111 = 7.	100
FIFO Status	0x18	7	FIFO Warning 1	1 = FIFO read and write pointers are within ±1.	N/A
		6	FIFO Warning 2	1 = FIFO read and write pointers are within ±2.	N/A
		2	FIFO soft align acknowledge	1 = FIFO read and write pointers are aligned after a serial port initiated FIFO reset.	N/A
		1	FIFO soft align request	1 = request FIFO read and write pointer alignment via the serial port.	0
	0x19	[7:0]	FIFO Level[7:0]	Thermometer encoded measure of the FIFO level.	N/A

Register Name	Address (Hex)	Bits	Name	Description	Default
Datapath Control	0x1B	7	Bypass premod	1 = bypass the $f_S/2$ premodulator.	1
		6	Bypass $sinc^{-1}$	1 = bypass the inverse sinc filter.	1
		5	Bypass NCO	1 = bypass the NCO.	1
		3	NCO gain	0 = no gain scaling is applied to the NCO input to the internal digital modulator (default). 1 = gain scaling of 0.5 is applied to the NCO input to the internal digital modulator. Gain scaling can eliminate saturation of the modulator output for some combinations of data inputs and NCO signals.	0
		2	Bypass phase compensation and dc offset	1 = bypass phase compensation and dc offset.	1
		1	Select sideband	0 = the modulator outputs the high-side image. 1 = the modulator outputs the low-side image. The image is spectrally inverted compared to the input data.	0
		0	Send I data to Q data	1 = ignore Q data from the interface and disable the clocks to the Q datapath. Send I data to both the I and Q DACs.	0
HB1 Control	0x1C	[2:1]	HB1[1:0]	Modulation mode for I Side Half-Band Filter 1. 00 = input signal not modulated; filter pass band is from −0.4 to +0.4 of f_{IN1}. 01 = input signal not modulated; filter pass band is from 0.1 to 0.9 of f_{IN1}. 10 = input signal modulated by f_{IN1}; filter pass band is from 0.6 to 1.4 of f_{IN1}. 11 = input signal modulated by f_{IN1}; filter pass band is from 1.1 to 1.9 of f_{IN1}.	00
		0	Bypass HB1	1 = bypass the first-stage interpolation filter.	0
HB2 Control	0x1D	[6:1]	HB2[5:0]	Modulation mode for I Side Half-Band Filter 2. 000000 = input signal not modulated; filter pass band is from −0.25 to +0.25 of f_{IN2}. 001001 = input signal not modulated; filter pass band is from 0.0 to 0.5 of f_{IN2}. 010010 = input signal not modulated; filter pass band is from 0.25 to 0.75 of f_{IN2}. 011011 = input signal not modulated; filter pass band is from 0.5 to 1.0 of f_{IN2}. 100100 = input signal modulated by f_{IN2}; filter pass band is from 0.75 to 1.25 of f_{IN2}. 101101 = input signal modulated by f_{IN2}; filter pass band is from 1.0 to 1.5 of f_{IN2}. 110110 = input signal modulated by f_{IN2}; filter pass band is from 1.25 to 1.75 of f_{IN2}. 111111 = input signal modulated by f_{IN2}; filter pass band is from 1.5 to 2.0 of f_{IN2}.	000000
		0	Bypass HB2	1 = bypass the second-stage interpolation filter.	0

Register Name	Address (Hex)	Bits	Name	Description	Default
HB3 Control	0x1E	[6:1]	HB3[5:0]	Modulation mode for I Side Half-Band Filter 3. 000000 = input signal not modulated; filter pass band is from −0.2 to +0.2 of f_{IN3}. 001001 = input signal not modulated; filter pass band is from 0.05 to 0.45 of f_{IN3}. 010010 = input signal not modulated; filter pass band is from 0.3 to 0.7 of f_{IN3}. 011011 = input signal not modulated; filter pass band is from 0.55 to 0.95 of f_{IN3}. 100100 = input signal modulated by f_{IN3}; filter pass band is from 0.8 to 1.2 of f_{IN3}. 101101 = input signal modulated by f_{IN3}; filter pass band is from 1.05 to 1.45 of f_{IN3}. 110110 = input signal modulated by f_{IN3}; filter pass band is from 1.3 to 1.7 of f_{IN3}. 111111 = input signal modulated by f_{IN3}; filter pass band is from 1.55 to 1.95 of f_{IN3}.	000000
		0	Bypass HB3	1 = bypass the third-stage interpolation filter.	0
Chip ID	0x1F	[7:0]	Chip ID[7:0]	This register identifies the device as an AD9121.	00001000
FTW LSB	0x30	[7:0]	FTW[7:0]	See Register 0x33.	00000000
FTW	0x31	[7:0]	FTW[15:8]	See Register 0x33.	00000000
FTW	0x32	[7:0]	FTW[23:16]	See Register 0x33.	00000000
FTW MSB	0x33	[7:0]	FTW[31:24]	FTW[31:0] is the 32-bit frequency tuning word that determines the frequency of the complex carrier generated by the on-chip NCO. The frequency is not updated when the FTW registers are written. The values are only updated when Bit 0 of Register 0x36 transitions from 0 to 1.	00000000
NCO Phase Offset LSB	0x34	[7:0]	NCO Phase Offset[7:0]	See Register 0x35.	00000000
NCO Phase Offset MSB	0x35	[7:0]	NCO Phase Offset[15:8]	The NCO sets the phase of the complex carrier signal when the NCO is reset. The phase offset spans from 0° to 360°. Each bit represents an offset of 0.0055°. This value is in twos complement format.	00000000
NCO FTW Update	0x36	5	FRAME FTW acknowledge	1 = the NCO has been reset due to an extended FRAME pulse signal.	0
		4	FRAME FTW request	0 = the NCO is reset on the first extended FRAME pulse after this bit is set to 1.	0
		1	Update FTW acknowledge	1 = the FTW has been updated.	0
		0	Update FTW request	The FTW is updated on the 0-to-1 transition of this bit.	0
I Phase Adj LSB	0x38	[7:0]	I Phase Adj[7:0]	See Register 0x39.	00000000
I Phase Adj MSB	0x39	[1:0]	I Phase Adj[9:8]	I Phase Adj[9:0] is used to insert a phase offset between the I and Q datapaths. This offset can be used to correct for phase imbalance in a quadrature modulator. See the Quadrature Phase Correction section for more information.	00
Q Phase Adj LSB	0x3A	[7:0]	Q Phase Adj[7:0]	See Register 0x3B.	00000000
Q Phase Adj MSB	0x3B	[1:0]	Q Phase Adj[9:8]	Q Phase Adj[9:0] is used to insert a phase offset between the I and Q datapaths. This offset can be used to correct for phase imbalance in a quadrature modulator. See the Quadrature Phase Correction section for more information.	00
I DAC Offset LSB	0x3C	[7:0]	I DAC Offset[7:0]	See Register 0x3D.	00000000
I DAC Offset MSB	0x3D	[7:0]	I DAC Offset[15:8]	I DAC Offset[15:0] is a value that is added directly to the samples written to the I DAC.	00000000

Register Name	Address (Hex)	Bits	Name	Description	Default
Q DAC Offset LSB	0x3E	[7:0]	Q DAC Offset[7:0]	See Register 0x3F.	00000000
Q DAC Offset MSB	0x3F	[7:0]	Q DAC Offset[15:8]	Q DAC Offset[15:0] is a value that is added directly to the samples written to the Q DAC.	00000000
I DAC FS Adjust	0x40	[7:0]	I DAC FS Adj[7:0]	See Register 0x41, Bits[1:0].	11111001
I DAC Control	0x41	7	I DAC sleep	1 = puts the I DAC into sleep mode (fast wake-up mode).	0
		[1:0]	I DAC FS Adj[9:8]	I DAC FS Adj[9:0] sets the full-scale current of the I DAC. The full-scale current can be adjusted from 8.64 mA to 31.68 mA in step sizes of approximately 22.5 µA. 0x000 = 8.64 mA. … 0x200 = 20.16 mA. … 0x3FF = 31.68 mA.	01
I Aux DAC Data	0x42	[7:0]	I Aux DAC[7:0]	See Register 0x43, Bits[1:0].	00000000
I Aux DAC Control	0x43	7	I aux DAC sign	0 = the I auxiliary DAC sign is positive, and the current is directed to the IOUT1P pin (Pin 67). 1 = the I auxiliary DAC sign is negative, and the current is directed to the IOUT1N pin (Pin 66).	0
		6	I aux DAC current direction	0 = the I auxiliary DAC sources current. 1 = the I auxiliary DAC sinks current.	0
		5	I aux DAC sleep	1 = puts the I auxiliary DAC into sleep mode.	0
		[1:0]	I Aux DAC[9:8]	I Aux DAC[9:0] sets the magnitude of the auxiliary DAC current. The range is 0 mA to 2 mA, and the step size is 2 µA. 0x000 = 0.000 mA. 0x001 = 0.002 mA. … 0x3FF = 2.046 mA.	00
Q DAC FS Adjust	0x44	[7:0]	Q DAC FS Adj[7:0]	See Register 0x45, Bits[1:0].	11111001
Q DAC Control	0x45	7	Q DAC sleep	1 = puts the Q DAC into sleep mode (fast wake-up mode).	0
		[1:0]	Q DAC FS Adj[9:8]	Q DAC FS Adj[9:0] sets the full-scale current of the Q DAC. The full-scale current can be adjusted from 8.64 mA to 31.68 mA in step sizes of approximately 22.5 µA. 0x000 = 8.64 mA. … 0x200 = 20.16 mA. … 0x3FF = 31.68 mA.	01
Q Aux DAC Data	0x46	[7:0]	Q Aux DAC[7:0]	See Register 0x47, Bits[1:0].	00000000

Register Name	Address (Hex)	Bits	Name	Description	Default
Q Aux DAC Control	0x47	7	Q aux DAC sign	0 = the Q auxiliary DAC sign is positive, and the current is directed to the IOUT2P pin (Pin 58). 1 = the Q auxiliary DAC sign is negative, and the current is directed to the IOUT2N pin (Pin 59).	0
		6	Q aux DAC current direction	0 = the Q auxiliary DAC sources current. 1 = the Q auxiliary DAC sinks current.	0
		5	Q aux DAC sleep	1 = puts the Q auxiliary DAC into sleep mode.	0
		[1:0]	Q Aux DAC[9:8]	Q Aux DAC[9:0] sets the magnitude of the auxiliary DAC current. The range is 0 mA to 2 mA, and the step size is 2 µA. 0x000 = 0.000 mA. 0x001 = 0.002 mA. … 0x3FF = 2.046 mA.	00
Die Temp Range Control	0x48	[6:4]	FS Current[2:0]	Auxiliary ADC full-scale current. 000 = lowest current. … 111 = highest current.	000
		[3:1]	Reference Current[2:0]	Auxiliary ADC reference current. 000 = lowest current. … 111 = highest current.	001
		0	Capacitor value	Auxiliary ADC internal capacitor value. 0 = 5 pF. 1 = 10 pF.	0
Die Temp LSB	0x49	[7:0]	Die Temp[7:0]	See Register 0x4A.	N/A
Die Temp MSB	0x4A	[7:0]	Die Temp[15:8]	Die Temp[15:0] indicates the approximate die temperature. For more information, see the Temperature Sensor section.	N/A
SED Control	0x67	7	SED compare enable	1 = enable the SED circuitry. None of the flags in this register or the values in Register 0x70 through Register 0x73 are significant if the SED is not enabled.	0
		5	Sample error detected	1 = indicates that an error was detected. The bit remains set until cleared. Any write to this register clears this bit to 0.	0
		3	Autoclear enable	1 = enable autoclear mode. This activates Bit 1 and Bit 0 of this register and causes Register 0x70 through Register 0x73 to be autocleared when eight consecutive sample data sets are received error free.	0
		1	Compare fail	1 = indicates that an error was detected. This bit remains set until it is autocleared by the reception of eight consecutive error-free comparisons or is cleared by a write to this register.	0
		0	Compare pass	1 = indicates that the last sample comparison was error free.	0
Compare I0 LSBs	0x68	[7:0]	Compare Value I0[7:0]	See Register 0x69.	10110110
Compare I0 MSBs	0x69	[7:0]	Compare Value I0[15:8]	Compare Value I0[15:0] is the word that is compared with the I0 input sample captured at the input interface.	01111010
Compare Q0 LSBs	0x6A	[7:0]	Compare Value Q0[7:0]	See Register 0x6B.	01000101
Compare Q0 MSBs	0x6B	[7:0]	Compare Value Q0[15:8]	Compare Value Q0[15:0] is the word that is compared with the Q0 input sample captured at the input interface.	11101010
Compare I1 LSBs	0x6C	[7:0]	Compare Value I1[7:0]	See Register 0x6D.	00010110
Compare I1 MSBs	0x6D	[7:0]	Compare Value I1[15:8]	Compare Value I1[15:0] is the word that is compared with the I1 input sample captured at the input interface.	00011010

Register Name	Address (Hex)	Bits	Name	Description	Default
Compare Q1 LSBs	0x6E	[7:0]	Compare Value Q1[7:0]	See Register 0x6F.	11000110
Compare Q1 MSBs	0x6F	[7:0]	Compare Value Q1[15:8]	Compare Value Q1[15:0] is the word that is compared with the Q1 input sample captured at the input interface.	10101010
SED I LSBs	0x70	[7:0]	Errors Detected I_BITS[7:0]	See Register 0x71.	00000000
SED I MSBs	0x71	[7:0]	Errors Detected I_BITS[15:8]	Errors Detected I_BITS[15:0] indicates which bits were received in error.	00000000
SED Q LSBs	0x72	[7:0]	Errors Detected Q_BITS[7:0]	See Register 0x73.	00000000
SED Q MSBs	0x73	[7:0]	Errors Detected Q_BITS[15:8]	Errors Detected Q_BITS[15:0] indicates which bits were received in error.	00000000
Revision	0x7F	[5:2]	Revision[3:0]	This value corresponds to the die revision number.	0011

LVDS INPUT DATA PORTS

The AD9121 has one LVDS data port that receives data for both the I and Q transmit paths. The device can accept data in word and byte formats. In word mode, the data is sent over a 14-bit LVDS data bus. In byte mode, the data is sent over an 8-bit LVDS data bus in the format of MSB[D13:D6] + LSB[D5:D0]. The 14-bit word is split into an 8-bit MSB portion and a 6-bit LSB portion. The LSB portion should be MSB aligned with the 8-bit LVDS data bus. The pin assignments of the bus in each mode are shown in Table 12.

Table 12. Data Bit Pair Assignments for Data Input Modes

Mode	MSB to LSB
Word	D13, D12, …, D0
Byte[1]	D12, D10, D8, D6, D5, D3, D1, ByteLSB

[1] In byte mode, the unused pins can be left floating.

The data is accompanied by a reference bit (DCI) that is used to generate a double data rate (DDR) clock. In byte mode, a FRAME signal is required for controlling to which DAC the data is sent. All of the interface signals are time aligned, so there is a maximum skew requirement on the bus.

WORD INTERFACE MODE

In word mode, the DCI signal is a reference bit used to generate the data sampling clock. The DCI signal should be time aligned with the data. The I DAC data should correspond to DCI high, and the Q DAC data should correspond to DCI low, as shown in Figure 42.

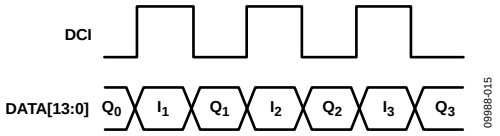


Figure 42. Timing Diagram for Word Mode

BYTE INTERFACE MODE

In byte mode, the DCI signal is a reference bit used to generate the data sampling clock. The DCI signal should be time aligned with the data. The most significant byte of the data should correspond to DCI high, and the least significant byte of the data should correspond to DCI low. The FRAME signal indicates to which DAC the data is sent. When FRAME is high, data is sent to the I DAC; when FRAME is low, data is sent to the Q DAC. The complete timing diagram is shown in Figure 43.

INTERFACE TIMING

The timing diagram for the digital interface port is shown in Figure 44. The sampling point of the data bus nominally occurs 350 ps after each edge of the DCI signal and has an uncertainty of ±300 ps, as illustrated by the sampling interval shown in Figure 44. The data and FRAME signals must be valid throughout this sampling interval. The data and FRAME signals may change at any time between sampling intervals.

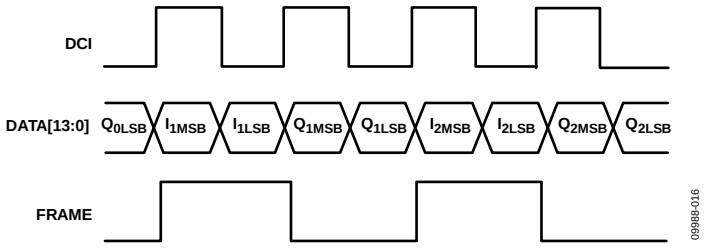


Figure 43. Timing Diagram for Byte Mode

The setup (t_S) and hold (t_H) times, with respect to the edges, are shown in Figure 44. The minimum setup and hold times are shown in Table 13.

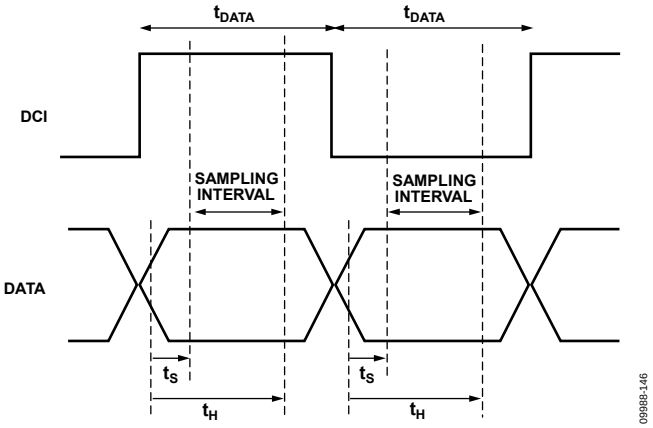


Figure 44. Timing Diagram for Input Data Port

Table 13. Data to DCI Setup and Hold Times

DCI Delay Register 0x16, Bits[1:0]	Minimum Setup Time, t_S (ns)	Minimum Hold Time, t_H (ns)	Sampling Interval (ns)
00	−0.05	0.65	0.6
01	−0.23	0.95	0.72
10	−0.38	1.22	0.84
11	−0.47	1.38	0.91

The data interface timing can be verified by using the sample error detection (SED) circuitry. See the Interface Timing Validation section for more information.

RECOMMENDED FRAME INPUT BIAS CIRCUITRY

Because the frame signal can be used as a reference clock in the byte mode or as a trigger to reset the FIFO, it is recommended that the frame input be tied to LVDS logic low when it is not used (that is, when it is not driven by an ASIC or FPGA). The external bias circuit shown in Figure 45 is recommended for this purpose.

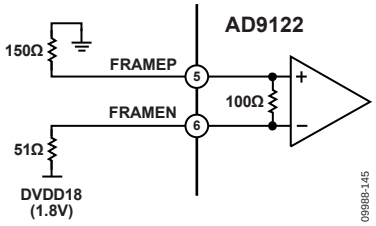


Figure 45. External Bias Circuit

FIFO OPERATION

The AD9121 contains a 2-channel, 14-bit wide, eight-word deep FIFO designed to relax the timing relationship between the data arriving at the DAC input ports and the internal DAC data rate clock. The FIFO acts as a buffer that absorbs timing variations between the data source and the DAC, such as the clock-to-data variation of an FPGA or ASIC, which significantly increases the timing budget of the interface.

Figure 46 shows the block diagram of the datapath through the FIFO. The data is latched into the device, is formatted, and is then written into the FIFO register determined by the FIFO write pointer. The value of the write pointer is incremented every time a new word is loaded into the FIFO. Meanwhile, data is read from the FIFO register determined by the read pointer and fed into the digital datapath. The value of the read pointer is incremented every time data is read into the datapath from the FIFO. The FIFO pointers are incremented at the data rate (DACCLK rate divided by the interpolation ratio).

Valid data is transmitted through the FIFO as long as the FIFO does not overflow or become empty. An overflow or empty condition of the FIFO occurs when the write pointer and read pointer point to the same FIFO location. This simultaneous access of data leads to unreliable data transfer through the FIFO and must be avoided.

Nominally, data is written to and read from the FIFO at the same rate. This keeps the FIFO depth constant. If data is written to the FIFO faster than data is read out, the FIFO depth increases. If data is read out of the FIFO faster than data is written to it, the FIFO depth decreases. For optimum timing margin, the FIFO depth should be maintained near half full (a difference of 4 between the write pointer and read pointer values). The FIFO depth represents the FIFO pipeline delay and is part of the overall latency of the AD9121.

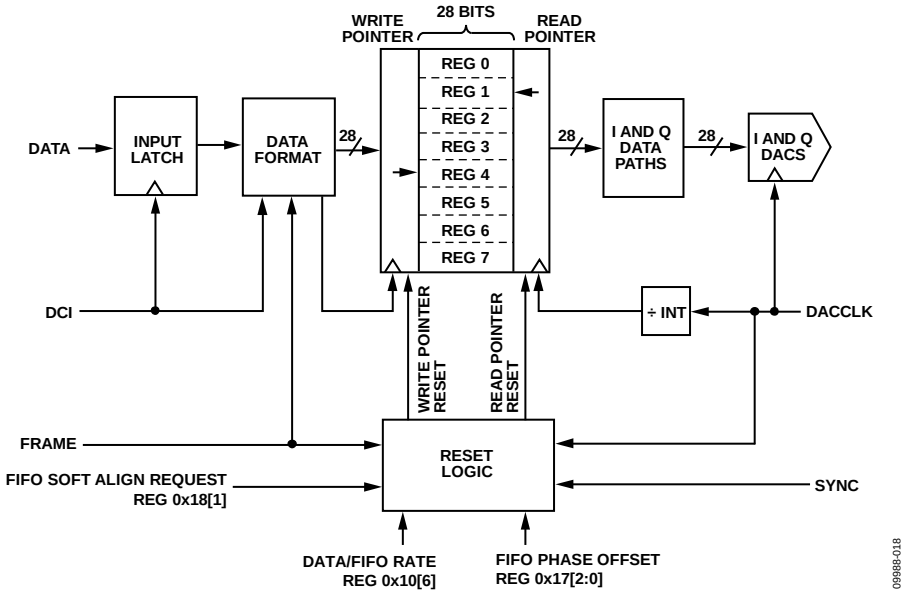


Figure 46. Block Diagram of FIFO

Resetting the FIFO

When the AD9121 is powered on, the FIFO depth is unknown. To avoid a concurrent read and write to the same FIFO address and to ensure a fixed pipeline delay, it is important to reset the FIFO pointers to known states. The FIFO pointers can be initialized in two ways: via a write sequence to the serial port or by strobing the FRAME input. There are two types of FIFO resets: a relative reset and an absolute reset. A relative reset enforces a defined FIFO depth. An absolute reset enforces a particular write pointer value when the reset is initiated. A serial port initiated FIFO reset is always a relative reset. A FRAME strobe initiated reset can be either a relative or an absolute reset.

If the FRAME differential inputs are not used for FIFO reset or for framing the word width, they must be tied to logic low. FRAMEP must be tied to DVSS, and FRAMEN must be tied to DVDD18 to avoid accidental reset of the FIFO due to noise.

The operation of the FRAME initiated FIFO reset depends on the synchronization mode chosen.

- When synchronization is disabled or when it is configured for data rate mode synchronization, the FRAME strobe initiates a relative FIFO reset. The reference point of the relative reset is the position of the read pointer.
- When FIFO mode synchronization is chosen, the FRAME strobe initiates an absolute FIFO reset.

For more information about the synchronization function, see the Multichip Synchronization section.

A summary of the synchronization modes and the types of FIFO reset used is provided in Table 14.

Table 14. Summary of FIFO Resets

	Synchronization Mode		
FIFO Reset Signal	**Disabled**	**Data Rate**	**FIFO Reset**
Serial Port	Relative	Relative	Relative
FRAME	Relative	Relative	Absolute

Serial Port Initiated FIFO Reset

A serial port initiated FIFO reset can be issued in any synchronization mode and always results in a relative FIFO reset. To initialize the FIFO data level through the serial port, Bit 1 of Register 0x18 should be toggled from 0 to 1 and back. When the write to this register is complete, the FIFO data level is initialized. When the initialization is triggered, the next time that the read pointer becomes 0, the write pointer is set to the value of the FIFO start level variable (Register 0x17, Bits[2:0]) upon initialization. By default, this value is 4, but it can be programmed to a value from 0 to 7. It is recommended that a value of 5 (0x05) be programmed in Register 0x17.

The recommended procedure for a serial port FIFO data level initialization is as follows:

1. Program Register 0x17 to 0x05.
2. Request FIFO level reset by setting Register 0x18, Bit 1, to 1.
3. Verify that the part acknowledges the request by ensuring that Register 0x18, Bit 2, is set to 1.
4. Remove the request by setting Register 0x18, Bit 1, to 0.
5. Verify that the part drops the acknowledge signal by ensuring that Register 0x18, Bit 2, is set to 0.
6. Read back Register 0x19 to verify that the pointer spacing is set to 3 (0x07) or 4 (0x0F).
7. If the readback of Register 0x19 shows a pointer spacing of 2 (0x03), increment Register 0x17 to a spacing of 0x06 and repeat Step 2 through Step 5. Read back Register 0x19 again to verify that the pointer spacing is now set to 3 (0x07).
8. If the readback of Register 0x19 shows a pointer spacing of 5 (0x1F) after Step 6, decrement Register 0x17 to a spacing of 0x04 and repeat Step 2 through Step 5. Read back Register 0x19 again to verify that the pointer spacing is now set to 4 (0x0F).

FRAME Initiated Relative FIFO Reset

The primary function of the FRAME input is to indicate to which DAC the input data is written. Another function of the FRAME input is to initialize the FIFO data level value. This is done by asserting the FRAME signal high for at least the time interval required to load complete data to the I and Q DACs. This corresponds to one DCI period in word mode and two DCI periods in byte mode.

To initiate a relative FIFO reset with the FRAME signal, the device must be configured in data rate mode (Register 0x10, Bit 6 = 1). When FRAME is asserted in data rate mode, the write pointer is set to 4 by default (or to the FIFO start level) the next time that the read pointer becomes 0 (see Figure 47).

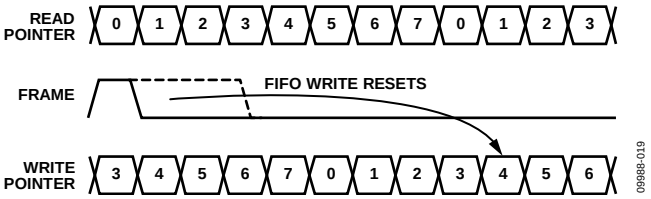


Figure 47. FRAME Input vs. Write Pointer Value, Data Rate Mode

FRAME Initiated Absolute FIFO Reset

In FIFO rate synchronization mode, the write pointer of the FIFO is reset in an absolute manner. The synchronization signal aligns the internal clocks on the part to a common reference clock so that the pipeline delay in the digital circuit stays the same during power cycles. The synchronization signal is sampled by the DAC clock in the AD9121. The edge of the DAC clock used to sample the synchronization signal is selected by Bit 3 of Register 0x10.

The FRAME signal is used to reset the FIFO write pointer. In the FIFO rate synchronization mode, the FIFO write pointer is reset immediately after the FRAME signal is asserted high for at least the time interval required to load complete data to the I and Q DACs. The FIFO write pointer is reset to the value of the FIFO Phase Offset[2:0] bits in Register 0x17. FIFO rate synchronization is selected by setting Bit 6 of Register 0x10 to 0.

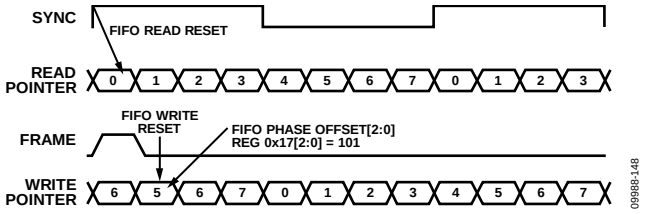


Figure 48. FRAME Input vs. Write Pointer Value, FIFO Rate Mode

Monitoring the FIFO Status

The FIFO initialization and status can be read from Register 0x18. This register provides information about the FIFO status and whether the initialization was successful. The MSB of Register 0x18 is a FIFO warning flag that can optionally trigger a device $\overline{\text{IRQ}}$. This flag indicates that the FIFO is close to emptying (FIFO level is 1) or overflowing (FIFO level is 7). In this case, data may soon be corrupted, and action should be taken.

The FIFO data level can be read from Register 0x19 at any time. The serial port reported FIFO data level is denoted as a 7-bit thermometer code (Base 1 code) of the write counter state relative to the absolute read counter being at 0. The optimum FIFO data level of 4 is therefore reported as a value of 00001111 in the status register.

Note that, depending on the timing relationship between the DCI and the main DACCLK, the FIFO level value can be off by a ±1 count, that is, the readback of Register 0x19 can be 00011111 in the case of a +1 count and 00000111 in the case of a −1 count. Therefore, it is important to keep the difference between the read and write pointers to a value of at least 2.

DIGITAL DATAPATH

The block diagram in Figure 49 shows the functionality of the digital datapath. The digital processing includes a premodulation block, three half-band (HB) interpolation filters, a quadrature modulator with a fine resolution NCO, phase and offset adjustment blocks, and an inverse sinc filter.

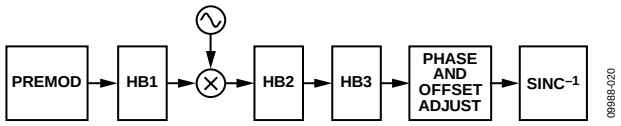


Figure 49. Block Diagram of Digital Datapath

The digital datapath accepts I and Q data streams and processes them as a quadrature data stream. The signal processing blocks can be used when the input data stream is represented as complex data.

The digital datapath can also be used to process an input data stream representing two independent real data streams, but the functionality is somewhat restricted. The premodulation block and any of the nonshifted interpolation filter modes can be used for an input data stream representing two independent real data streams. See the Coarse Modulation Mixing Sequences section for more information.

PREMODULATION

The half-band interpolation filters have selectable pass bands that allow the center frequencies to be moved in increments of one-half their input data rate. The premodulation block provides a digital upconversion of the incoming waveform by one-half the incoming data rate, f_{DATA}. This can be used to frequency-shift baseband input data to the center of the interpolation filter pass band.

INTERPOLATION FILTERS

The transmit path contains three interpolation filters. Each of the three interpolation filters provides a 2× increase in output data rate. The half-band (HB) filters can be individually bypassed or cascaded to provide 1×, 2×, 4×, or 8× interpolation ratios. Each half-band filter stage offers a different combination of bandwidths and operating modes.

The bandwidth of the three half-band filters with respect to the data rate at the filter input is as follows:

- Bandwidth of HB1 = $0.8 \times f_{IN1}$
- Bandwidth of HB2 = $0.5 \times f_{IN2}$
- Bandwidth of HB3 = $0.4 \times f_{IN3}$

The usable bandwidth is defined as the frequency over which the filters have a pass-band ripple of less than ±0.001 dB and an image rejection of greater than +85 dB. As described in the Half-Band Filter 1 (HB1) section, the image rejection usually sets the usable bandwidth of the filter, not the pass-band flatness.

The half-band filters operate in several modes, providing programmable pass-band center frequencies as well as signal modulation. The HB1 filter has four modes of operation, and the HB2 and HB3 filters each have eight modes of operation.

Half-Band Filter 1 (HB1)

HB1 has four modes of operation, as shown in Figure 50. The shape of the filter response is identical in each of the four modes. The four modes are distinguished by two factors: the filter center frequency and whether the input signal is modulated by the filter.

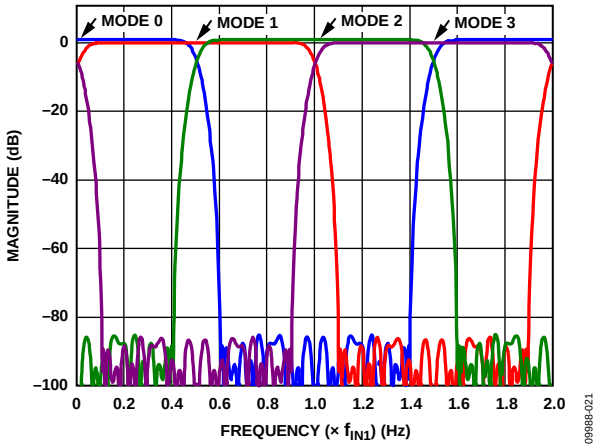


Figure 50. HB1 Filter Modes

As shown in Figure 50, the center frequency in each mode is offset by one-half the input data rate (f_{IN1}) of the filter. Mode 0 and Mode 1 do not modulate the input signal. Mode 2 and Mode 3 modulate the input signal by f_{IN1}. When operating in Mode 0 and Mode 2, the I and Q paths operate independently and no mixing of the data between channels occurs. When operating in Mode 1 and Mode 3, mixing of the data between the I and Q paths occurs; therefore, the data input into the filter is assumed to be complex. Table 15 summarizes the HB1 modes.

Table 15. HB1 Filter Modes

Mode	f_{CENTER}	f_{MOD}	Input Data
0	DC	None	Real or complex
1	$f_{IN}/2$	None	Complex
2	f_{IN}	f_{IN}	Real or complex
3	$3f_{IN}/2$	f_{IN}	Complex

Figure 51 shows the pass-band filter response for HB1. In most applications, the usable bandwidth of the filter is limited by the image suppression provided by the stop-band rejection and not by the pass-band flatness. Table 16 shows the pass-band flatness and stop-band rejection supported by the HB1 filter at different bandwidths.

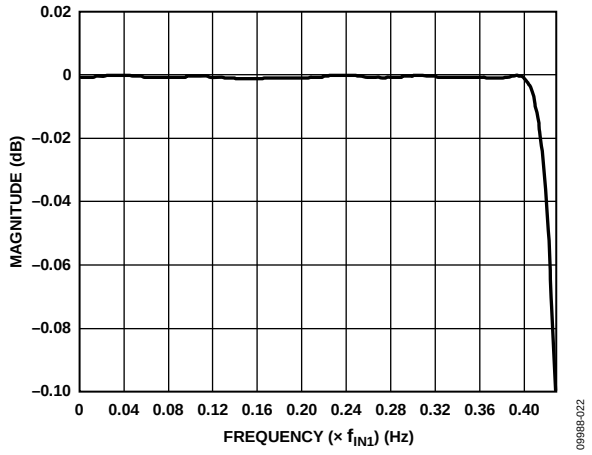


Figure 51. Pass-Band Detail of HB1

Table 16. HB1 Pass-Band and Stop-Band Performance by Bandwidth

Bandwidth (% of f_{IN1})	Pass-Band Flatness (dB)	Stop-Band Rejection (dB)
80	0.001	85
80.4	0.0012	80
81.2	0.0033	70
82	0.0076	60
83.6	0.0271	50
85.6	0.1096	40

Half-Band Filter 2 (HB2)

HB2 has eight modes of operation, as shown in Figure 52 and Figure 53. The shape of the filter response is identical in each of the eight modes. The eight modes are distinguished by two factors: the filter center frequency and whether the input signal is modulated by the filter.

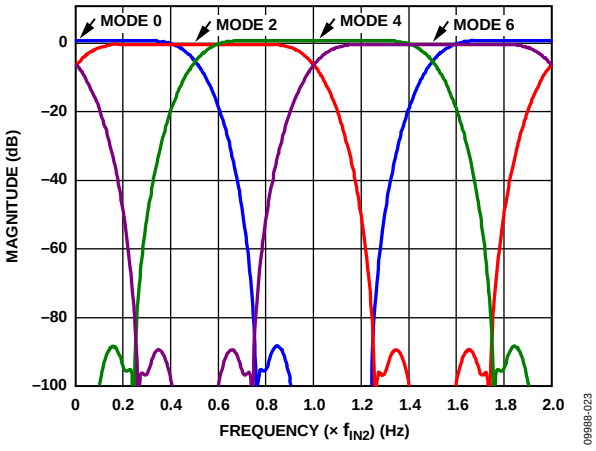


Figure 52. HB2, Even Filter Modes

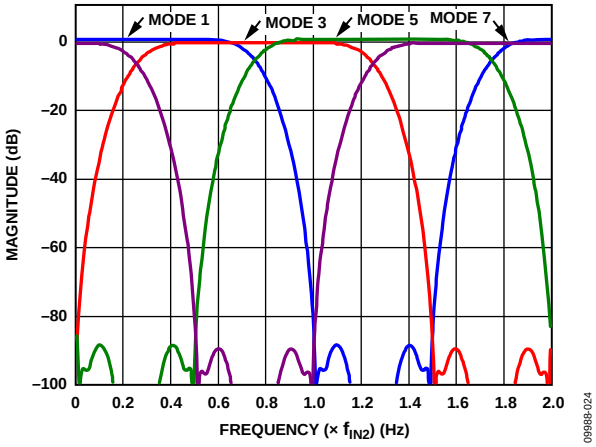


Figure 53. HB2, Odd Filter Modes

As shown in Figure 52 and Figure 53, the center frequency in each mode is offset by one-fourth the input data rate (f_{IN2}) of the filter. Mode 0 through Mode 3 do not modulate the input signal. Mode 4 through Mode 7 modulate the input signal by f_{IN2}. When operating in Mode 0 and Mode 4, the I and Q paths operate independently and no mixing of the data between channels occurs. When operating in the other six modes, mixing of the data between the I and Q paths occurs; therefore, the data input to the filter is assumed to be complex.

Table 17 summarizes the HB2 and HB3 modes.

Table 17. HB2 and HB3 Filter Modes

Mode	f_{CENTER}	f_{MOD}	Input Data
0	DC	None	Real or complex
1	$f_{IN}/4$	None	Complex
2	$f_{IN}/2$	None	Complex
3	$3f_{IN}/4$	None	Complex
4	f_{IN}	f_{IN}	Real or complex
5	$5f_{IN}/4$	f_{IN}	Complex
6	$3f_{IN}/2$	f_{IN}	Complex
7	$7f_{IN}/4$	f_{IN}	Complex

Figure 54 shows the pass-band filter response for HB2. In most applications, the usable bandwidth of the filter is limited by the image suppression provided by the stop-band rejection and not by the pass-band flatness. Table 18 shows the pass-band flatness and stop-band rejection supported by the HB2 filter at different bandwidths.

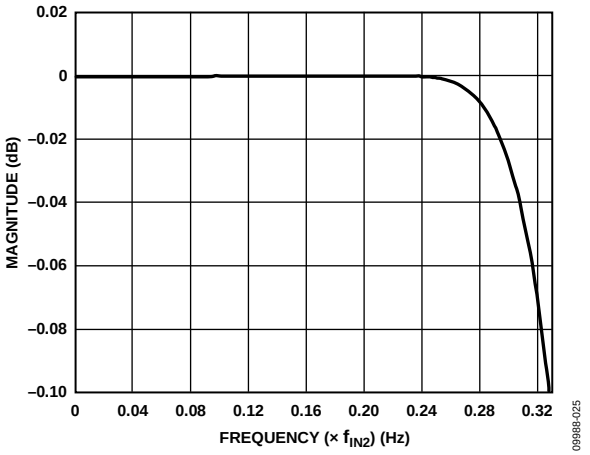


Figure 54. Pass-Band Detail of HB2

Table 18. HB2 Pass-Band and Stop-Band Performance by Bandwidth

Bandwidth (% of f_{IN2})	Pass-Band Flatness (dB)	Stop-Band Rejection (dB)
50	0.001	85
50.8	0.0012	80
52.8	0.0028	70
56	0.0089	60
60	0.0287	50
64.8	0.1877	40

Half-Band Filter 3 (HB3)

HB3 has eight modes of operation that function the same as HB2. The primary difference between HB2 and HB3 is the filter bandwidths.

Figure 55 shows the pass-band filter response for HB3. In most applications, the usable bandwidth of the filter is limited by the image suppression provided by the stop-band rejection and not by the pass-band flatness. Table 19 shows the pass-band flatness and stop-band rejection supported by the HB3 filter at different bandwidths.

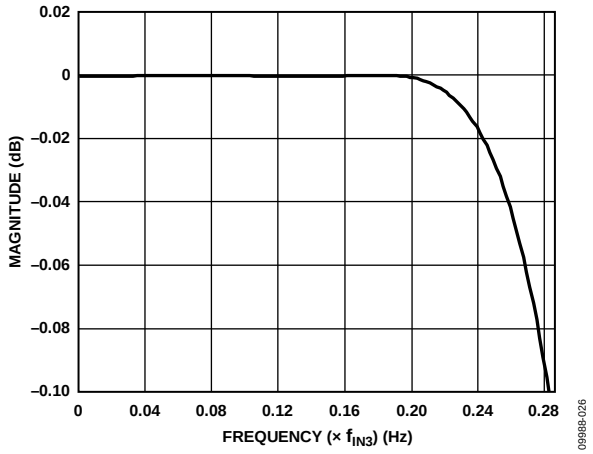


Figure 55. Pass-Band Detail of HB3

Table 19. HB3 Pass-Band and Stop-Band Performance by Bandwidth

Bandwidth (% of f_{IN3})	Pass-Band Flatness (dB)	Stop-Band Rejection (dB)
40	0.001	85
40.8	0.0014	80
42.4	0.002	70
45.6	0.0093	60
49.8	0.03	50
55.6	0.1	40

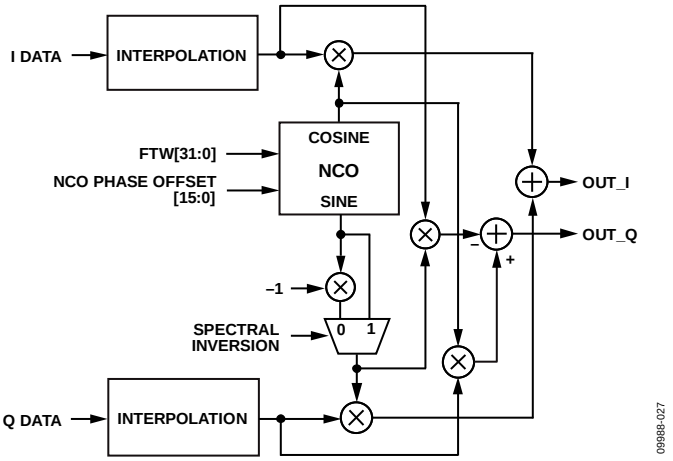


Figure 56. Digital Quadrature Modulator Block Diagram

NCO MODULATION

The digital quadrature modulator makes use of a numerically controlled oscillator (NCO), a phase shifter, and a complex modulator to provide a means for modulating the signal by a programmable carrier signal. A block diagram of the digital modulator is shown in Figure 56. The fine modulation provided by the digital modulator, in conjunction with the coarse modulation of the interpolation filters and premodulation block, allows the signal to be placed anywhere in the output spectrum with very fine frequency resolution.

The quadrature modulator is used to mix the carrier signal generated by the NCO with the I and Q signal. The NCO produces a quadrature carrier signal to translate the input signal to a new center frequency. A complex carrier signal is a pair of sinusoidal waveforms of the same frequency, offset 90° from each other. The frequency of the complex carrier signal is set via FTW[31:0] in Register 0x30 through Register 0x33.

The NCO operating frequency, f_{NCO}, is at either f_{DATA} (HB1 bypassed) or 2× f_{DATA} (HB1 enabled). The frequency of the complex carrier signal can be set from dc up to f_{NCO}. The frequency tuning word (FTW) is calculated as

$$FTW = \frac{f_{CARRIER}}{f_{NCO}} \times 2^{32}$$

The generated quadrature carrier signal is mixed with the I and Q data. The quadrature products are then summed into the I and Q datapaths, as shown in Figure 56.

Updating the Frequency Tuning Word

The frequency tuning word registers are not updated immediately upon writing, as other configuration registers are. After loading the FTW registers with the desired values, Bit 0 of Register 0x36 must transition from 0 to 1 for the new FTW to take effect.

DATAPATH CONFIGURATION

Configuring the AD9121 datapath starts with the application requirements of the input data rate, the interpolation ratio, the output signal bandwidth, and the output signal center frequency. Given these four parameters, the first step in configuring the datapath is to verify that the device supports the bandwidth requirements. The modes of the interpolation filters are then chosen. Finally, any additional frequency offset requirements are determined and applied with premodulation and NCO modulation.

Determining the Datapath Signal Bandwidth

The available signal bandwidth of the datapath is dependent on the center frequency of the output signal in relation to the center frequency of the interpolation filters used. Signal center frequencies offset from the center frequencies of the half-band filters lower the available signal bandwidth.

When correctly configured, the available complex signal bandwidth for 2× interpolation is always 80% of the input data rate. The available signal bandwidth for 4× interpolation vs. output frequency varies between 50% and 80% of the input data rate, as shown in Figure 57. Note that in 4× interpolation mode, $f_{DAC} = 4 \times f_{DATA}$; therefore, the data shown in Figure 57 repeats four times from dc to f_{DAC}.

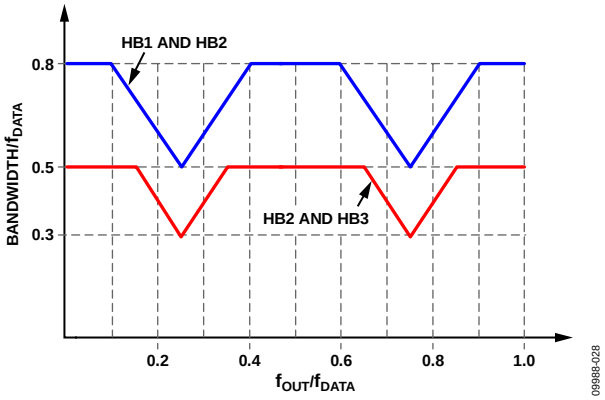


Figure 57. Signal Bandwidth vs. Center Frequency of the Output Signal, 4× Interpolation

Configuring 4× interpolation using the HB2 and HB3 filters can lower the power consumption of the device at the expense of bandwidth. The lower curve in Figure 57 shows that the supported bandwidth in this mode varies from 30% to 50% of f_{DATA}.

The available signal bandwidth for 8× interpolation vs. output frequency varies between 50% and 80% of the input data rate, as shown in Figure 58. Note that in 8× interpolation mode, $f_{DAC} = 8 \times f_{DATA}$; therefore, the data shown in Figure 58 repeats eight times from dc to f_{DAC}.

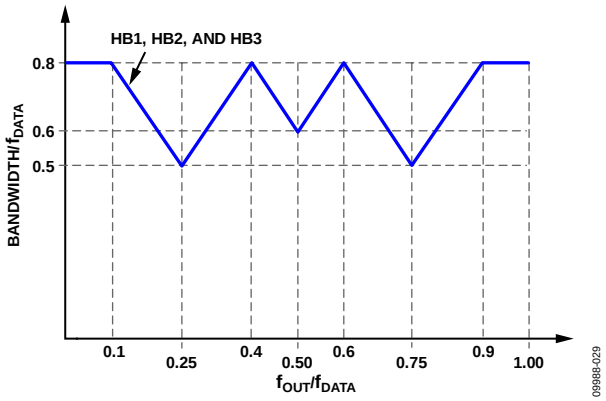


Figure 58. Signal Bandwidth vs. Center Frequency of the Output Signal, 8× Interpolation

DETERMINING INTERPOLATION FILTER MODES

Table 20 shows the recommended interpolation filter settings for a variety of filter interpolation factors, filter center frequencies, and signal modulation. The interpolation modes were chosen based on the final center frequency of the signal and by determining the frequency shift of the signal required. When these parameters are known and put in terms of the input data rate (f_{DATA}), the filter configuration that comes closest to matching is selected from Table 20.

Table 20. Recommended Interpolation Filter Modes (Register 0x1C Through Register 0x1E)

	Filter Modes				
Interpolation Factor	**HB1[1:0]**	**HB2[5:0]**	**HB3[5:0]**	**f_{SIGNAL} Modulation**	**f_{CENTER} Shift**
8	00 (Mode 0)	000000	000000	DC	0
8	01 (Mode 1)	001001	000000	DC[1]	$f_{DATA}/2$
8[2]	10 (Mode 2)	010010	001001	f_{DATA}	f_{DATA}
8	11 (Mode 3)	011011	001001	f_{DATA}[1]	$3f_{DATA}/2$
8	00 (Mode 0)	100100	010010	$2f_{DATA}$	$2f_{DATA}$
8	01 (Mode 1)	101101	010010	$2f_{DATA}$[1]	$5f_{DATA}/2$
8	10 (Mode 2)	110110	011011	$3f_{DATA}$	$3f_{DATA}$
8	11 (Mode 3)	111111	011011	$3f_{DATA}$[1]	$7f_{DATA}/2$
8	00 (Mode 0)	000000	100100	$4f_{DATA}$	$4f_{DATA}$
8	01 (Mode 1)	001001	100100	$4f_{DATA}$[1]	$9f_{DATA}/2$
8	10 (Mode 2)	010010	101101	$5f_{DATA}$	$5f_{DATA}$
8	11 (Mode 3)	011011	101101	$5f_{DATA}$[1]	$11f_{DATA}/2$
8	00 (Mode 0)	100100	110110	$6f_{DATA}$	$6f_{DATA}$
8	01 (Mode 1)	101101	110110	$6f_{DATA}$[1]	$13f_{DATA}/2$
8	10 (Mode 2)	110110	111111	$7f_{DATA}$	$7f_{DATA}$
8	11 (Mode 3)	111111	111111	$7f_{DATA}$[1]	$15f_{DATA}/2$
4	00 (Mode 0)	000000	Bypass	DC	0
4[3]	01 (Mode 1)	001001	Bypass	DC[1]	$f_{DATA}/2$
4	10 (Mode 2)	010010	Bypass	f_{DATA}	f_{DATA}
4	11 (Mode 3)	011011	Bypass	f_{DATA}[1]	$3f_{DATA}/2$
4	00 (Mode 0)	100100	Bypass	$2f_{DATA}$	$2f_{DATA}$
4	01 (Mode 1)	101101	Bypass	$2f_{DATA}$[1]	$5f_{DATA}/2$
4	10 (Mode 2)	110110	Bypass	$3f_{DATA}$	$3f_{DATA}$
4	11 (Mode 3)	111111	Bypass	$3f_{DATA}$[1]	$7f_{DATA}/2$
2	00 (Mode 0)	Bypass	Bypass	DC	0
2	01 (Mode 1)	Bypass	Bypass	DC[1]	$f_{DATA}/2$
2	10 (Mode 2)	Bypass	Bypass	f_{DATA}	f_{DATA}
2	11 (Mode 3)	Bypass	Bypass	f_{DATA}[1]	$3f_{DATA}/2$

[1] When HB1 Mode 1 or Mode 3 is used, enabling premodulation provides an additional frequency translation of the input signal by $f_{DATA}/2$, which centers a baseband input signal in the filter pass band.
[2] This configuration was used in the 8× interpolation without NCO example (see the 8× Interpolation Without NCO section).
[3] This configuration was used in the 4× interpolation with NCO example (see the 4× Interpolation with NCO section).

DATAPATH CONFIGURATION EXAMPLES

8× Interpolation Without NCO

For this example, the following parameters are given:

- f_{DATA} = 100 MSPS
- 8× interpolation
- f_{BW} = 75 MHz
- f_{CENTER} = 100 MHz

The desired 75 MHz of bandwidth is 75% of f_{DATA}. In this case, the ratio of f_{OUT}/f_{DATA} = 100/100 = 1.0. From Figure 58, the bandwidth supported at f_{DATA} is 0.8, which verifies that the AD9121 supports the bandwidth required in this configuration.

The signal center frequency is f_{DATA} and, assuming the input signal is at baseband, the frequency shift required is also f_{DATA}. Choosing the third row (highlighted by the superscripted number 2) of the Interpolation Factor column from Table 20 selects filter modes that give a center frequency of f_{DATA} and a frequency translation of f_{DATA}. The selected modes for the three half-band filters are HB1, Mode 2; HB2, Mode 2; and HB3, Mode 1. Figure 59 shows how the signal propagates through the interpolation filters.

Because $2 \times f_{IN1} = f_{IN2}$ and $2 \times f_{IN2} = f_{IN3}$, the signal appears frequency scaled by one-half into each consecutive stage. The output signal band spans 0.15 to 0.35 of f_{IN3} (400 MHz). Therefore, the output frequency supported is 60 MHz to 140 MHz, which covers the 75 MHz bandwidth centered at 100 MHz, as desired.

4× Interpolation with NCO

For this example, the following parameters are given:

- f_{DATA} = 250 MSPS
- 4× interpolation
- f_{BW} = 140 MHz
- f_{CENTER} = 175 MHz

The desired 140 MHz of bandwidth is 56% of f_{DATA}. As shown in Figure 57, the value at $0.7 \times f_{DATA}$ is 0.6. This is calculated as $0.8 - 2(0.7 - 0.6) = 0.6$. This verifies that the AD9121 supports a bandwidth of 60% of f_{DATA}, which exceeds the required 56%.

The signal center frequency is $0.7 \times f_{DATA}$ and, assuming the input signal is at baseband, the frequency shift required is also $0.7 \times f_{DATA}$. Choosing the second row in the Interpolation Factor column in the 4× interpolation section of Table 20 selects the filter modes that give a center frequency of $f_{DATA}/2$ with no frequency translation. The selected modes for the three half-band filters are HB1, Mode 1; HB2, Mode 1; and HB3, bypassed.

Because Mode 1 of HB1 was selected, the premodulation block should be enabled. This provides $f_{DATA}/2$ modulation, which centers the baseband input data at the center frequency of HB1. The digital modulator can be used to provide the final frequency translation of $0.2 \times f_{DATA}$ to place the output signal at $0.7 \times f_{DATA}$, as desired.

The formula for calculating the FTW of the NCO is as follows:

$$FTW = \frac{f_{CARRIER}}{f_{NCO}} \times 2^{32}$$

where:
$f_{CARRIER} = 0.2 \times f_{DATA}$.
$f_{NCO} = 2 \times f_{DATA}$.

Therefore, FTW = $2^{32}/10$.

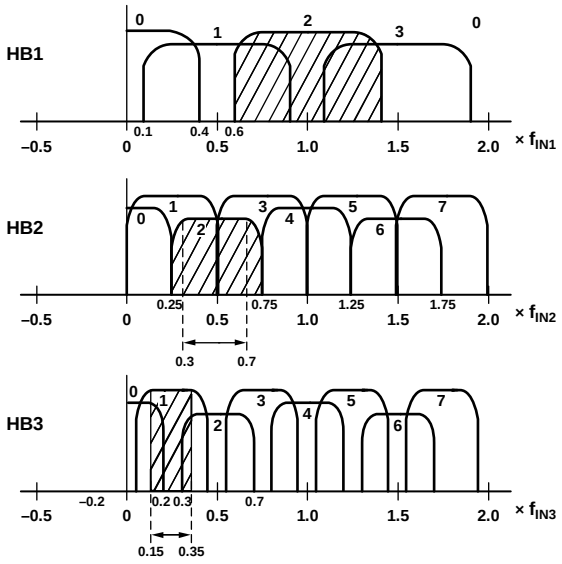


Figure 59. Signal Propagation for 8× Interpolation (f_{DATA} Modulation)

DATA RATES vs. INTERPOLATION MODES

Table 22 summarizes the maximum bus speed (f_{BUS}), supported input data rates, and signal bandwidths with the various combinations of bus width modes and interpolation rates. The real signal bandwidth supported is a fraction of the input data rate, which depends on the interpolation filters (HB1, HB2, or HB3) selected. The complex signal bandwidth supported is twice the real signal bandwidth.

In general, 2× interpolation is best supported by enabling HB1, and 4× interpolation is best supported by enabling HB1 and HB2. However, in some cases, power dissipation can be lowered by not using HB1. If the bandwidth required is low enough, 2× interpolation can be supported by using HB2, and 4× interpolation can be supported by using HB2 and HB3.

COARSE MODULATION MIXING SEQUENCES

The coarse digital quadrature modulation occurs within the interpolation filters. The modulation shifts the frequency spectrum of the incoming data by the frequency offset selected. The frequency offsets available are multiples of the input data rate. The modulation is equivalent to multiplying the quadrature input signal by a complex carrier signal, C(t), of the form

$$C(t) = \cos(\omega_c t) + j\sin(\omega_c t)$$

In practice, this modulation results in the mixing functions shown in Table 21.

Table 21. Modulation Mixing Sequences

Modulation	Mixing Sequence
$f_S/2$	I = I, –I, I, –I, … Q = Q, –Q, Q, –Q, …
$f_S/4$	I = I, Q, –I, –Q, … Q = Q, –I, –Q, I, …
$3f_S/4$	I = I, –Q, –I, Q, … Q = Q, I, –Q, –I, …
$f_S/8$	I = I, r(I + Q), Q, r(–I + Q), –I, –r(I + Q), –Q, r(I – Q), … Q = Q, r(Q – I), –I, –r(Q + I), –Q, r(–Q + I), I, r(Q + I), …

Note that $r = \frac{\sqrt{2}}{2}$

As shown in Table 21, the mixing functions of most of the modes cross-couple samples between the I and Q channels. The I and Q channels operate independently only in $f_S/2$ mode. This means that real modulation using both the I and Q DAC outputs can only be done in $f_S/2$ mode. All other modulation modes require complex input data and produce complex output signals.

Table 22. Summary of Data Rates and Bandwidths vs. Interpolation Modes (DVDD18, CVDD18 = 1.9 V ± 2%)

	Filter Modes						
Bus Width	HB3	HB2	HB1	f_{BUS} (Mbps)	f_{DATA} (Mbps)	Real Signal Bandwidth (MHz)	f_{DAC} (MHz)
Byte (8 Bits)	0	0	0	1230	307.5	150	307.5
	0	0	1	1230	307.5	120	615
	0	1	0	1230	307.5	75	615
	0	1	1	1230	307.5	120	1230
	1	1	0	1230	307.5	75	1230
	1	1	1	615	153.75	60	1230
Word (14 Bits)	0	0	0	1230	615	300	615
	0	0	1	1000	500	200	1000
	0	1	0	1230	615	150	1230
	0	1	1	615	307.5	120	1230
	1	1	0	615	307.5	75	1230
	1	1	1	307.5	153.75	60	1230

QUADRATURE PHASE CORRECTION

The purpose of the quadrature phase correction block is to enable compensation of the phase imbalance of the analog quadrature modulator following the DAC. If the quadrature modulator has a phase imbalance, the unwanted sideband appears with significant energy. Tuning the quadrature phase adjust value can optimize image rejection in single sideband radios.

Ordinarily, the I and Q channels have an angle of precisely 90° between them. The quadrature phase adjustment is used to change the angle between the I and Q channels. When I Phase Adj[9:0] (Register 0x38 and Register 0x39) is set to 1000000000, the I DAC output moves approximately 1.75° away from the Q DAC output, creating an angle of 91.75° between the channels. When I Phase Adj[9:0] is set to 0111111111, the I DAC output moves approximately 1.75° toward the Q DAC output, creating an angle of 88.25° between the channels.

Q Phase Adj[9:0] (Register 0x3A and Register 0x3B) works in a similar fashion. When Q Phase Adj[9:0] is set to 1000000000, the Q DAC output moves approximately 1.75° away from the I DAC output, creating an angle of 91.75° between the channels. When Q Phase Adj[9:0] is set to 0111111111, the Q DAC output moves approximately 1.75° toward the I DAC output, creating an angle of 88.25° between the channels.

Based on these two endpoints, the combined resolution of the phase compensation register is approximately 3.5°/1024 or 0.00342° per code.

DC OFFSET CORRECTION

The dc value of the I datapath and the Q datapath can be independently controlled by adjusting the I DAC Offset[15:0] and Q DAC Offset[15:0] values in Register 0x3C through Register 0x3F. These values are added directly to the datapath values. Care should be taken not to overrange the transmitted values.

Figure 60 shows how the DAC offset current varies as a function of the I DAC Offset[15:0] and Q DAC Offset[15:0] values. With the digital inputs fixed at midscale (0x0000, twos complement data format), Figure 60 shows the nominal I_{OUTxP} and I_{OUTxN} currents as the DAC offset value is swept from 0 to 65,535. Because I_{OUTxP} and I_{OUTxN} are complementary current outputs, the sum of I_{OUTxP} and I_{OUTxN} is always 20 mA.

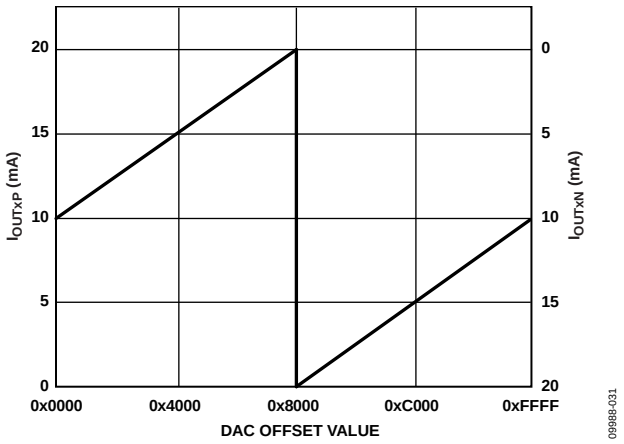


Figure 60. DAC Output Currents vs. DAC Offset Value

INVERSE SINC FILTER

The inverse sinc ($sinc^{-1}$) filter is a nine-tap FIR filter. The composite response of the $sinc^{-1}$ filter and the sin(x)/x response of the DAC is shown in Figure 61. The composite response has a pass-band ripple of less than ±0.05 dB up to a frequency of $0.4 \times f_{DACCLK}$. To provide the necessary peaking at the upper end of the pass band, the inverse sinc filters shown have an intrinsic insertion loss of about 3.2 dB. Figure 61 shows the composite frequency response.

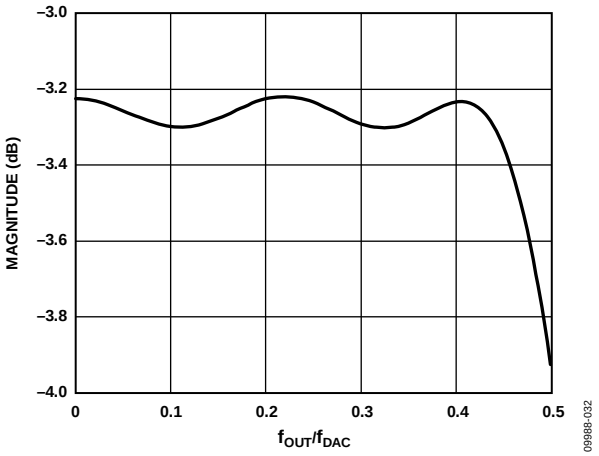


Figure 61. Sample Composite Responses of the $Sinc^{-1}$ Filter with sin(x)/x Roll-Off

The $sinc^{-1}$ filter is disabled by default. It can be enabled by setting the bypass $sinc^{-1}$ bit to 0 (Register 0x1B, Bit 6).

DAC INPUT CLOCK CONFIGURATIONS

The AD9121 DAC sampling clock (DACCLK) can be sourced directly or by clock multiplying. Clock multiplying uses the on-chip phase-locked loop (PLL), which accepts a reference clock operating at a submultiple of the desired DACCLK rate, most commonly the data input frequency. The PLL then multiplies the reference clock up to the desired DACCLK frequency, which can then be used to generate all the internal clocks required by the DAC. The clock multiplier provides a high quality clock that meets the performance requirements of most applications. Using the on-chip clock multiplier eliminates the need to generate and distribute the high speed DACCLK.

The second mode bypasses the clock multiplier circuitry and allows the DACCLK to be sourced directly to the DAC core. This mode enables the user to source a very high quality clock directly to the DAC core. Sourcing the DACCLK directly through the REFCLKP, REFCLKN, DACCLKP, and DACCLKN pins may be necessary in demanding applications that require the lowest possible DAC output noise, particularly when directly synthesizing signals above 150 MHz.

DRIVING THE DACCLK AND REFCLK INPUTS

The differential DACCLK and REFCLK inputs share similar clock receiver input circuitry. Figure 62 shows a simplified circuit diagram of the inputs. The on-chip clock receiver has a differential input impedance of about 10 kΩ. It is self-biased to a common-mode voltage of about 1.25 V. The inputs can be driven by direct coupling differential PECL or LVDS drivers. The inputs can also be ac-coupled if the driving source cannot meet the input compliance voltage of the receiver.

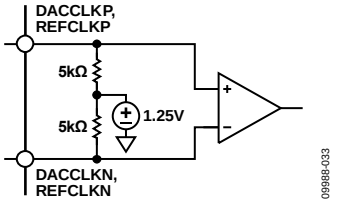


Figure 62. Clock Receiver Input Simplified Equivalent Circuit

The minimum input drive level to either of the clock inputs is 100 mV p-p differential. The optimal performance is achieved when the clock input signal is between 800 mV p-p differential and 1.6 V p-p differential. Whether using the on-chip clock multiplier or sourcing the DACCLK directly, it is necessary that the input clock signal to the device have low jitter and fast edge rates to optimize the DAC noise performance.

DIRECT CLOCKING

Direct clocking with a low noise clock produces the lowest noise spectral density at the DAC outputs. To select the differential CLK inputs as the source for the DAC sampling clock, set the PLL enable bit (Register 0x0A, Bit 7) to 0. This powers down the internal PLL clock multiplier and selects the input from the DACCLKP and DACCLKN pins as the source for the internal DAC sampling clock.

The device also has duty cycle correction circuitry and differential input level correction circuitry. Enabling these circuits can provide improved performance in some cases. The control bits for these functions are in Register 0x08 (see Table 11).

CLOCK MULTIPLICATION

The on-chip PLL clock multiplication circuit can be used to generate the DAC sampling clock from a lower frequency reference clock. When the PLL enable bit (Register 0x0A, Bit 7) is set to 1, the clock multiplication circuit generates the DAC sampling clock from the lower rate REFCLK input. The functional diagram of the clock multiplier is shown in Figure 63.

The clock multiplication circuit operates such that the VCO outputs a frequency, f_{VCO}, equal to the REFCLK input signal frequency multiplied by N1 × N0.

$$f_{VCO} = f_{REFCLK} \times (N1 \times N0)$$

The DAC sampling clock frequency, f_{DACCLK}, is equal to

$$f_{DACCLK} = f_{REFCLK} \times N1$$

The output frequency of the VCO must be chosen to keep f_{VCO} in the optimal operating range of 1.0 GHz to 2.1 GHz. The frequency of the reference clock and the values of N1 and N0 must be chosen so that the desired DACCLK frequency can be synthesized and the VCO output frequency is in the correct range.

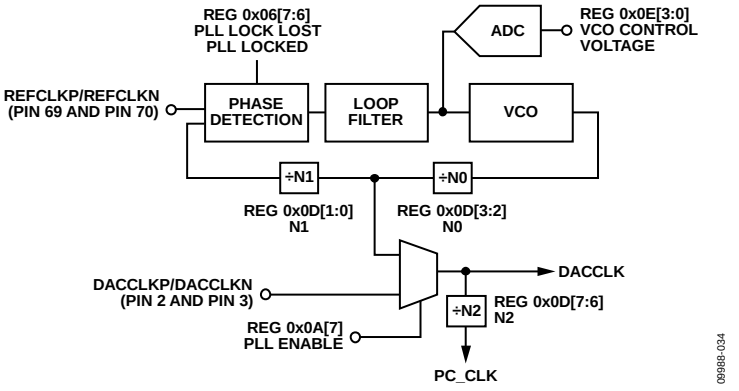


Figure 63. PLL Clock Multiplication Circuit

PLL SETTINGS

Three settings for the PLL circuitry should be programmed to their nominal values. The PLL values shown in Table 23 are the recommended settings for these parameters.

Table 23. PLL Settings

PLL Control Register	Register Address	Bits	Optimal Setting
PLL Loop Bandwidth[1:0]	0x0C	[7:6]	11
PLL Charge Pump Current[4:0]	0x0C	[4:0]	10001
PLL Cross-Control Enable	0x0D	4	1

CONFIGURING THE VCO TUNING BAND

The PLL VCO has a valid operating range from approximately 1.0 GHz to 2.1 GHz covered in 63 overlapping frequency bands. For any desired VCO output frequency, there may be several valid PLL band select values. The frequency bands of a typical device are shown in Figure 64. Device-to-device variations and operating temperature affect the actual band frequency range. Therefore, it is required that the optimal PLL band select value be determined for each individual device.

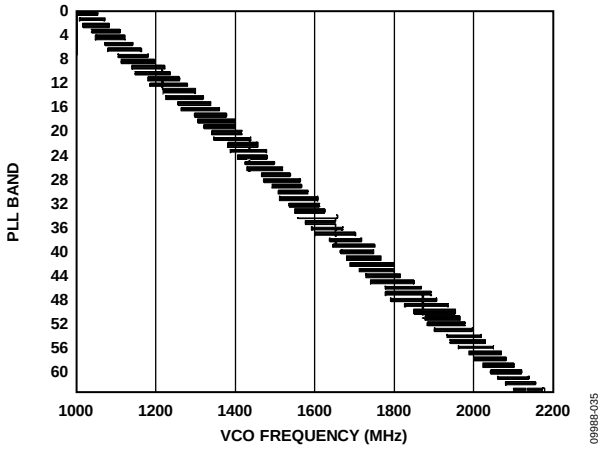


Figure 64. PLL Lock Range over Temperature for a Typical Device

Automatic VCO Band Select

The device has an automatic VCO band select feature on chip. Using the automatic VCO band select feature is a simple and reliable method of configuring the VCO frequency band. This feature is enabled by starting the PLL in manual mode, and then placing the PLL in auto band select mode. This is done by setting Register 0x0A to a value of 0xCF, and then to a value of 0xA0. When these values are written, the device executes an automated routine that determines the optimal VCO band setting for the device. The setting selected by the device ensures that the PLL remains locked over the full −40°C to +85°C operating temperature range of the device without further adjustment. (The PLL remains locked over the full temperature range even if the temperature during initialization is at one of the temperature extremes.)

Manual VCO Band Select

The device also has a manual band select mode (PLL manual enable, Register 0x0A, Bit 6 = 1) that allows the user to select the VCO tuning band. In manual mode, the VCO band is set directly with the value written to the manual VCO band bits (Register 0x0A, Bits[5:0]). To properly select the VCO band, follow these steps:

1. Put the device in manual band select mode by setting Register 0x0A, Bit 6 = 1.
2. Sweep the VCO band over a range of bands that results in the PLL being locked.
3. For each band, verify that the PLL is locked and read the PLL using the VCO control voltage bits (Register 0x0E, Bits[3:0]).
4. Select the band that results in the control voltage being closest to the center of the range, that is, 1001 or 1000 (see Table 24). The resulting VCO band should be the optimal setting for the device. Write this value to the manual VCO band bits (Register 0x0A, Bits[5:0]).
5. If desired, an indication of where the VCO is within the operating frequency band can be determined by querying the VCO control voltage. Table 24 shows how to interpret the PLL VCO control voltage value (Register 0x0E, Bits[3:0]).

Table 24. VCO Control Voltage Range Indications

VCO Control Voltage (Register 0x0E, Bits[3:0])	Indication
1111	Move to higher VCO band
1110	
1101	VCO is operating in the higher end of the frequency band
1100	
1011	
1010	
1001	VCO is operating within an optimal region of the frequency band
1000	
0111	
0110	
0101	VCO is operating in the lower end of the frequency band
0100	
0011	
0010	
0001	Move to lower VCO band
0000	

ANALOG OUTPUTS

TRANSMIT DAC OPERATION

Figure 65 shows a simplified block diagram of the transmit path DACs. The DAC core consists of a current source array, a switch core, digital control logic, and full-scale output current control. The DAC full-scale output current (I_{FS}) is nominally 20 mA. The output currents from the IOUT1P/IOUT2P and IOUT1N/IOUT2N pins are complementary, meaning that the sum of the two currents always equals the full-scale current of the DAC. The digital input code to the DAC determines the effective differential current delivered to the load.

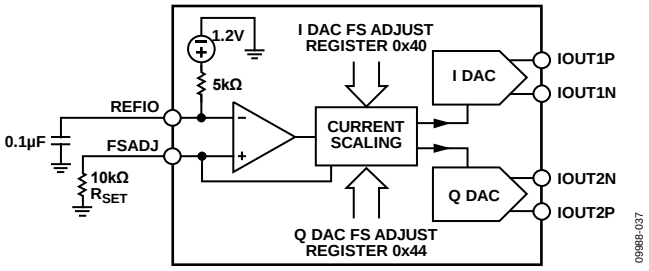


Figure 65. Simplified Block Diagram of DAC Core

The DAC has a 1.2 V band gap reference with an output impedance of 5 kΩ. The reference output voltage appears on the REFIO pin. When using the internal reference, decouple the REFIO pin to AVSS with a 0.1 µF capacitor. Use the internal reference only for external circuits that draw dc currents of 2 µA or less. For dynamic loads or static loads greater than 2 µA, buffer the REFIO pin. If desired, the internal reference can be overdriven by applying an external reference (from 1.10 V to 1.30 V) to the REFIO pin.

A 10 kΩ external resistor, R_{SET}, must be connected from the FSADJ pin to AVSS. This resistor, along with the reference control amplifier, sets up the correct internal bias currents for the DAC. Because the full-scale current is inversely proportional to this resistor, the tolerance of R_{SET} is reflected in the full-scale output amplitude.

The full-scale current equation, where the DAC gain is set individually for the I and Q DACs in Register 0x40 and Register 0x44, respectively, is as follows:

$$I_{FS} = \frac{V_{REF}}{R_{SET}} \times \left(72 + \left(\frac{3}{16} \times DAC\ gain\right)\right)$$

For the nominal values of V_{REF} (1.2 V), R_{SET} (10 kΩ), and DAC gain (512), the full-scale current of the DAC is typically 20.16 mA. The DAC full-scale current can be adjusted from 8.64 mA to 31.68 mA by setting the DAC gain parameter, as shown in Figure 66.

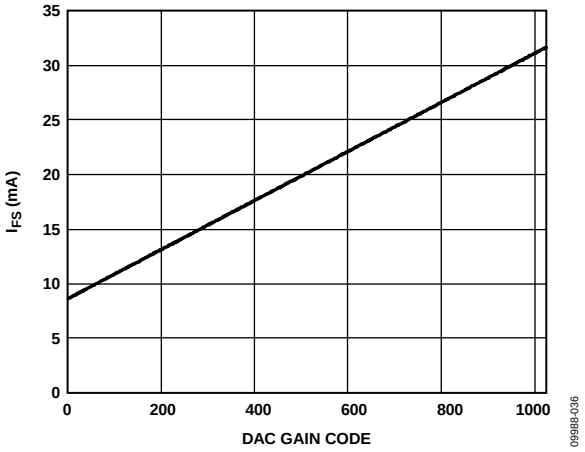


Figure 66. DAC Full-Scale Current vs. DAC Gain Code

Transmit DAC Transfer Function

The output currents from the IOUT1P/IOUT2P and IOUT1N/IOUT2N pins are complementary, meaning that the sum of the two currents always equals the full-scale current of the DAC. The digital input code to the DAC determines the effective differential current delivered to the load. IOUT1P/IOUT2P provide maximum output current when all bits are high. The output currents vs. DACCODE for the DAC outputs are expressed as

$$I_{OUTxP} = \left[\frac{DACCODE}{2^N}\right] \times I_{FS} \quad (1)$$

$$I_{OUTxN} = I_{FS} - I_{OUTxP} \quad (2)$$

where $DACCODE = 0$ to $2^N - 1$.

Transmit DAC Output Configurations

The optimum noise and distortion performance of the AD9121 is realized when it is configured for differential operation. The common-mode error sources of the DAC outputs are significantly reduced by the common-mode rejection of a transformer or differential amplifier. These common-mode error sources include even-order distortion products and noise. The enhancement in distortion performance becomes more significant as the frequency content of the reconstructed waveform increases and/or its amplitude increases. This is due to the first-order cancellation of various dynamic common-mode distortion mechanisms, digital feedthrough, and noise.

Figure 67 shows the most basic transmit DAC output circuitry. A pair of resistors, R_O, is used to convert each of the complementary output currents to a differential voltage output, V_{OUT}. Because the current outputs of the DAC are high impedance, the differential driving point impedance of the DAC outputs, R_{OUT}, is equal to $2 \times R_O$. Figure 68 illustrates the output voltage waveforms.

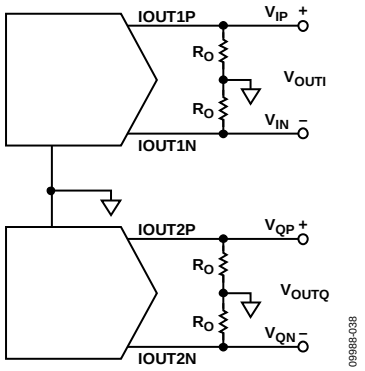


Figure 67. Basic Transmit DAC Output Circuit

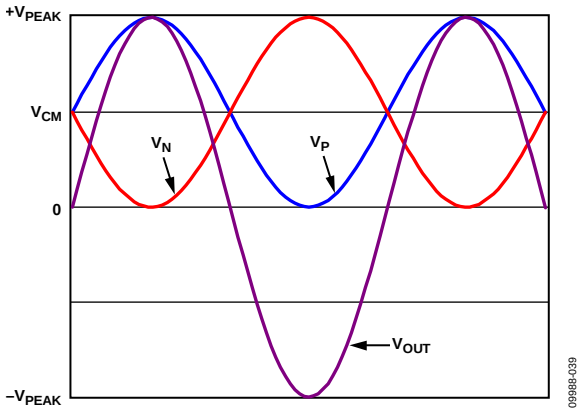


Figure 68. Output Voltage Waveforms

The common-mode signal voltage, V_{CM}, is calculated as

$$V_{CM} = \frac{I_{FS}}{2} \times R_O$$

The peak output voltage, V_{PEAK}, is calculated as

$$V_{PEAK} = I_{FS} \times R_O$$

With this circuit configuration, the single-ended peak voltage is the same as the peak differential output voltage.

Transmit DAC Linear Output Signal Swing

To achieve optimum performance, the DAC outputs have a linear output compliance voltage range that must be adhered to. The linear output signal swing is dependent on the full-scale output current, I_{FS}, and the common-mode level of the output. Figure 69 and Figure 70 show the IMD performance vs. the output common-mode voltage at different full-scale currents and output frequencies.

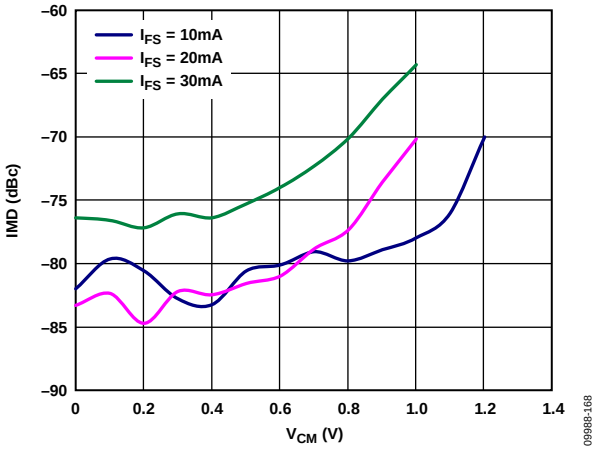


Figure 69. IMD vs. Output Common-Mode Voltage (f_{OUT} = 61 MHz, R_{LOAD} = 50 Ω Differential, I_{FS} = 10 mA, 20 mA, and 30 mA)

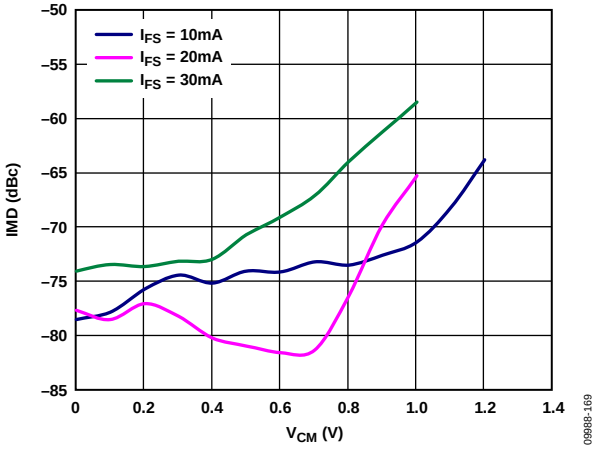


Figure 70. IMD vs. Output Common-Mode Voltage (f_{OUT} = 161 MHz, R_{LOAD} = 50 Ω Differential, I_{FS} = 10 mA, 20 mA, and 30 mA)

AUXILIARY DAC OPERATION

The AD9121 has two auxiliary DACs: one associated with the I path and one associated with the Q path. These auxiliary DACs can be used to compensate for dc offsets in the transmitted signal. Each auxiliary DAC has a single-ended current that can sink or source current into either the positive (P) or negative (N) output of the associated transmit DAC. The auxiliary DAC structure is shown in Figure 71.

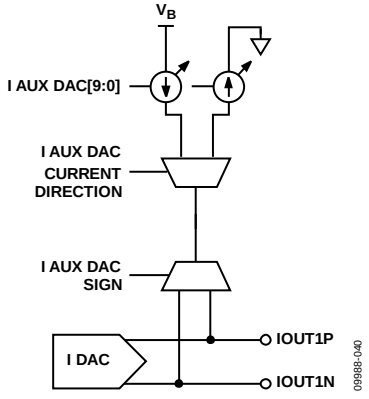


Figure 71. Auxiliary DAC Structure

The control registers for the I and Q auxiliary DACs are Register 0x42, Register 0x43, Register 0x46, and Register 0x47.

INTERFACING TO MODULATORS

The AD9121 interfaces to the ADL537x family of modulators with a minimal number of components. An example of the recommended interface circuitry is shown in Figure 72.

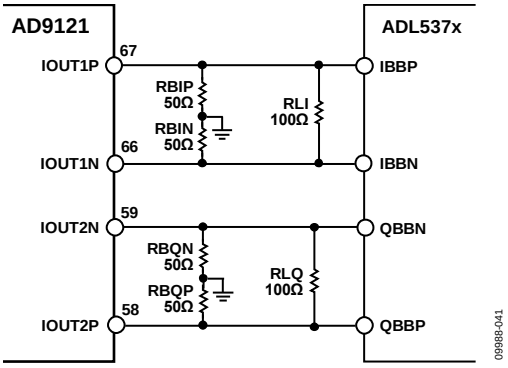


Figure 72. Typical Interface Circuitry Between the AD9121 and the ADL537x Family of Modulators

The baseband inputs of the ADL537x family require a dc bias of 500 mV. The nominal midscale output current on each output of the DAC is 10 mA (one-half the full-scale current). Therefore, a single 50 Ω resistor to ground from each of the DAC outputs results in the desired 500 mV dc common-mode bias for the inputs to the ADL537x. The signal level can be reduced through the addition of the load resistor in parallel with the modulator inputs. The peak-to-peak voltage swing of the transmitted signal is

$$V_{SIGNAL} = I_{FS} \times \frac{(2 \times R_B \times R_L)}{(2 \times R_B + R_L)}$$

BASEBAND FILTER IMPLEMENTATION

Most applications require a baseband anti-imaging filter between the DAC and the modulator to filter out Nyquist images and broadband DAC noise. The filter can be inserted between the I-V resistors at the DAC output and the signal level setting resistor across the modulator input. This establishes the input and output impedances for the filter.

Figure 74 shows a fifth-order, low-pass filter. A common-mode choke is used between the I-V resistors and the remainder of the filter. This removes the common-mode signal produced by the DAC and prevents the common-mode signal from being converted to a differential signal, which can appear as unwanted spurious signals in the output spectrum. Splitting the first filter capacitor into two and grounding the center point creates a common-mode low-pass filter, providing additional common-mode rejection of high frequency signals. A purely differential filter can pass common-mode signals.

DRIVING THE ADL5375-15

The ADL5375-15 requires a 1500 mV dc bias and, therefore, requires a slightly more complex interface than most other Analog Devices modulators. It is necessary to level-shift the DAC output from a 500 mV dc bias to the 1500 mV dc bias required by the ADL5375-15. Level-shifting can be achieved with a purely passive network, as shown in Figure 73. In this network, the dc bias of the DAC remains at 500 mV, whereas the input to the ADL5375-15 is 1500 mV. This passive, level-shifting network introduces approximately 2 dB of loss in the ac signal.

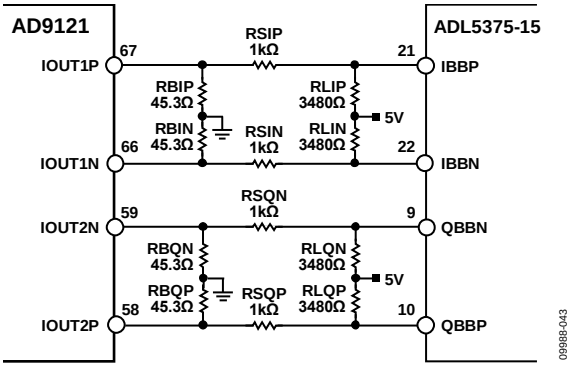


Figure 73. Passive, Level-Shifting Network for Biasing the ADL5375-15

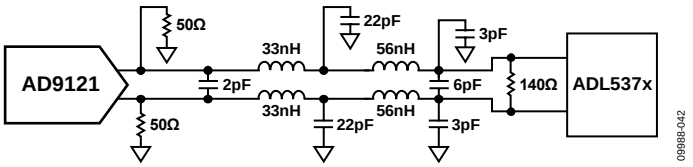


Figure 74. DAC Modulator Interface with Fifth-Order, Low-Pass Filter

REDUCING LO LEAKAGE AND UNWANTED SIDEBANDS

Analog quadrature modulators can introduce unwanted signals at the LO frequency due to dc offset voltages in the I and Q baseband inputs, as well as feedthrough paths from the LO input to the output. The LO feedthrough can be nulled by applying the correct dc offset voltages at the DAC output. This can be done using the auxiliary DACs (Register 0x42, Register 0x43, Register 0x46, and Register 0x47) or by using the digital dc offset adjustments (Register 0x3C through Register 0x3F).

The advantage of using the auxiliary DACs is that none of the main DAC dynamic range is used to perform the dc offset adjustment. The disadvantage is that the common-mode level of the output signal changes as a function of the auxiliary DAC current. The opposite is true when the digital offset adjustment is used.

Good sideband suppression requires both gain and phase matching of the I and Q signals. The I/Q phase adjust registers (Register 0x38 through Register 0x3B) and the DAC FS adjust registers (Register 0x40 and Register 0x44) can be used to calibrate the I and Q transmit paths to optimize sideband suppression.

DEVICE POWER MANAGEMENT

POWER DISSIPATION

The AD9121 has four supply rails: AVDD33, IOVDD, DVDD18, and CVDD18.

The AVDD33 supply powers the DAC core circuitry. The power dissipation of the AVDD33 supply rail is independent of the digital operating mode and sample rate. The current drawn from the AVDD33 supply rail is typically 55 mA (182 mW) when the full-scale current of the I and Q DACs is set to the nominal value of 20 mA. Changing the full-scale current directly affects the supply current drawn from the AVDD33 rail. For example, if the full-scale current of the I DAC and the Q DAC is changed to 10 mA, the AVDD33 supply current drops by 20 mA to 35 mA.

The IOVDD voltage supplies the serial port I/O pins, the $\overline{\text{RESET}}$ pin, and the $\overline{\text{IRQ}}$ pin. The voltage applied to the IOVDD pin can range from 1.8 V to 3.3 V. The current drawn by the IOVDD supply pin is typically 3 mA.

The DVDD18 supply powers all of the digital signal processing blocks of the device. The power consumption from this supply is a function of which digital blocks are enabled and the frequency at which the device is operating.

The CVDD18 supply powers the clock receiver and clock distribution circuitry. The power consumption from this supply varies directly with the operating frequency of the device. CVDD18 also powers the PLL. The power dissipation of the PLL is typically 80 mW when enabled.

Figure 75 through Figure 79 show the power dissipation of the AD9121 under a variety of operating conditions. All of the graphs were taken with data being supplied to both the I and Q DACs. The power consumption of the device does not vary significantly with changes in the coarse modulation mode selected or the analog output frequency. Figure 75 through Figure 79 show the total power dissipation, as well as the power dissipation of the DVDD18 and CVDD18 supplies.

Maximum power dissipation can be estimated to be 20% higher than the typical power dissipation.

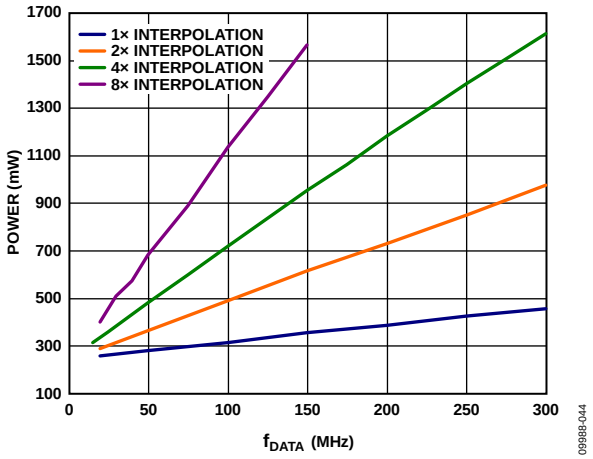


Figure 75. Total Power Dissipation vs. f_{DATA} Without PLL, Fine NCO, or Inverse Sinc

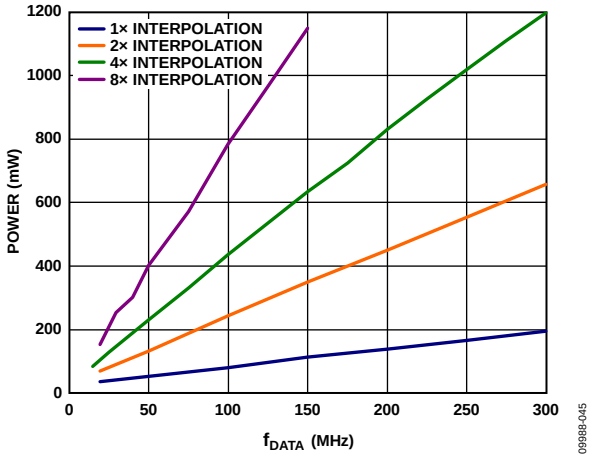


Figure 76. DVDD18 Power Dissipation vs. f_{DATA} Without Fine NCO or Inverse Sinc

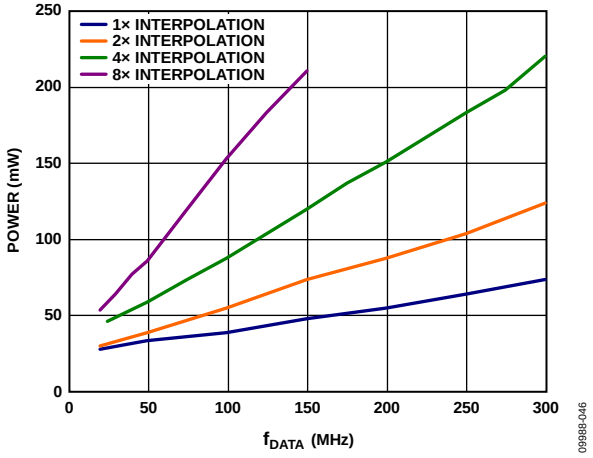


Figure 77. CVDD18 Power Dissipation vs. f_{DATA} with PLL Disabled

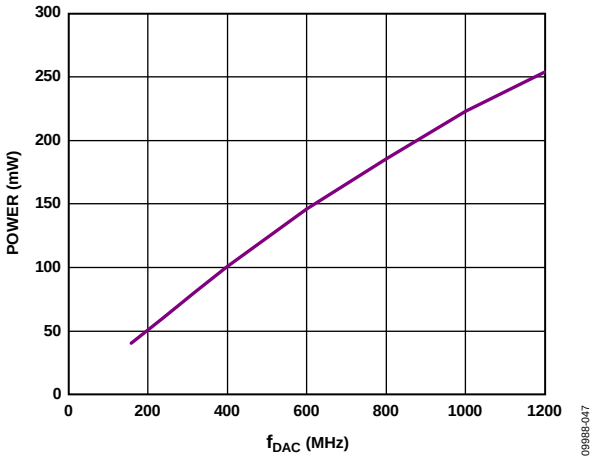


Figure 78. DVDD18 Power Dissipation vs. f_{DAC} Due to Inverse Sinc Filter

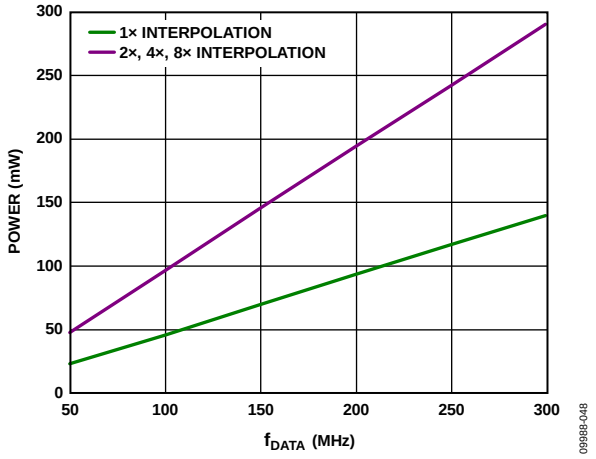


Figure 79. DVDD18 Power Dissipation vs. f_{DATA} Due to Fine NCO

TEMPERATURE SENSOR

The AD9121 has a band gap temperature sensor for monitoring the temperature change of the AD9121. The temperature must be calibrated against a known temperature to remove the part-to-part variation on the band gap circuit used to sense the temperature. The DACCLK must be running at a minimum of 100 MHz to obtain a reliable temperature measurement.

To monitor temperature change, the user must take a reading at a known ambient temperature for a single-point calibration of each AD9121 device.

$$Tx = T_{REF} + 7.7 \times (Code_x - Code_ref)/1000 + 1$$

where:
Code_x is the readback code at the unknown temperature, *Tx*.
Code_ref is the readback code at the calibrated temperature, T_{REF}.

To use the temperature sensor, it must be enabled by setting Register 0x01, Bit 4, to 0. In addition, to obtain accurate readings, the die temperature range control register (Register 0x48) should be set to 0x02.

MULTICHIP SYNCHRONIZATION

System demands may require that the outputs of multiple DACs be synchronized with each other or with a system clock. Systems that support transmit diversity or beamforming, where multiple antennas are used to transmit a correlated signal, require multiple DAC outputs to be phase aligned with each other. Systems with a time division multiplexing transmit chain may require one or more DACs to be synchronized with a system-level reference clock.

Multiple devices are considered synchronized to each other when the state of the clock generation state machines is identical for all parts and when time-aligned data is being read from the FIFOs of all parts simultaneously. Devices are considered synchronized to a system clock when there is a fixed and known relationship between the clock generation state machine and the data being read from the FIFO and a particular clock edge of the system clock. The AD9121 has provisions for enabling multiple devices to be synchronized to each other or to a system clock.

The AD9121 supports synchronization in two different modes: data rate mode and FIFO rate mode. In data rate mode, the input data rate represents the lowest synchronized clock rate. In FIFO rate mode, the FIFO rate, which is the data rate divided by the FIFO depth of 8, represents the lowest rate clock.

The advantage of FIFO rate synchronization is increased time between the setup and hold time windows for DCI changes relative to the DACCLK or REFCLK input. When the synchronization state machine is on in data rate mode, the elasticity of the FIFO is not used to absorb timing variations between the data source and the DAC, resulting in setup and hold time windows repeating at the input data rate.

The method chosen for providing the DAC sampling clock directly affects the synchronization methods available. When the device clock multiplier is used, only data rate mode is available. When the DAC sampling clock is sourced directly, both data rate mode and FIFO rate mode synchronization are available. The following sections describe the synchronization methods for enabling both clocking modes and querying the status of the synchronization logic.

The full synchronization methods described are used to align multiple dual DACs within one DACCLK cycle. To achieve synchronization within one DACCLK cycle, both the REFCLK and FRAME signals are required to perform back-end and front-end alignment. If synchronization does not need to be this accurate, other options can be used. In data rate mode or in FIFO rate mode, using soft alignment of the FIFO for multiple DACs synchronizes the DAC outputs within two data clock cycles (see the Serial Port Initiated FIFO Reset section). For more information about synchronization, see the AN-1093 Application Note, *Synchronization of Multiple AD9122 TxDAC+ Converters.*

SYNCHRONIZATION WITH CLOCK MULTIPLICATION

When using the clock multiplier to generate the DAC sample rate clock, the REFCLK input signal acts as both the reference clock for the PLL-based clock multiplier and the synchronization signal. To synchronize devices, distribute the REFCLK signal with low skew to all the devices that need to be synchronized. Skew between the REFCLK signals of the different devices shows up directly as a timing mismatch at the DAC outputs.

Because two clocks are shared on the same signal, an appropriate frequency must be chosen for the synchronization and REFCLK signals. The FRAME and DCI signals can be created in the FPGA along with the data. A circuit diagram of a typical configuration is shown in Figure 80.

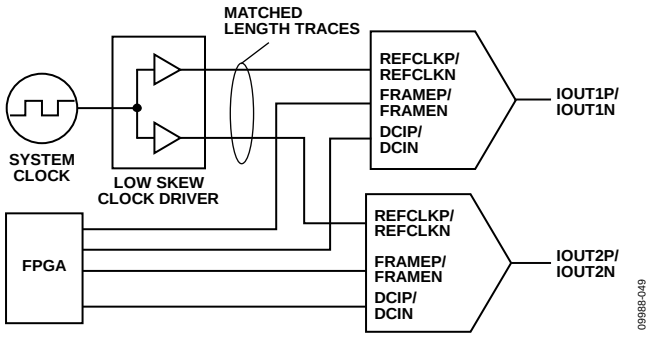


Figure 80. Typical Circuit Diagram for Synchronizing Devices

The Procedure for Synchronization When Using the PLL section outlines the steps required to synchronize multiple devices. The procedure assumes that the REFCLK signal is applied to all the devices and that the PLL of each device is phase locked to it. The procedure must be carried out on each individual device.

Procedure for Synchronization When Using the PLL

In the initialization of the AD9121, all the clock signals (DACCLK, DCI, FRAME, synchronization, and REFCLK) must be present and stable before the synchronization feature is turned on. Configure the AD9121 for periodic data rate synchronization by writing 0xC8 to the sync control register (Register 0x10). Additional synchronization options are available (see the Additional Synchronization Features section).

Read the sync status register (Register 0x12) to verify that the sync locked bit (Bit 6) is set high, indicating that the device achieved back-end synchronization, and that the sync lost bit (Bit 7) is low. These levels indicate that the clocks are running with a constant and known phase relative to the synchronization signal.

Reset the FIFO by strobing the FRAME signal high for the time interval required to write two complete input data words. Resetting the FIFO ensures that the correct data is being read from the FIFO.

This completes the synchronization procedure; all devices should now be synchronized.

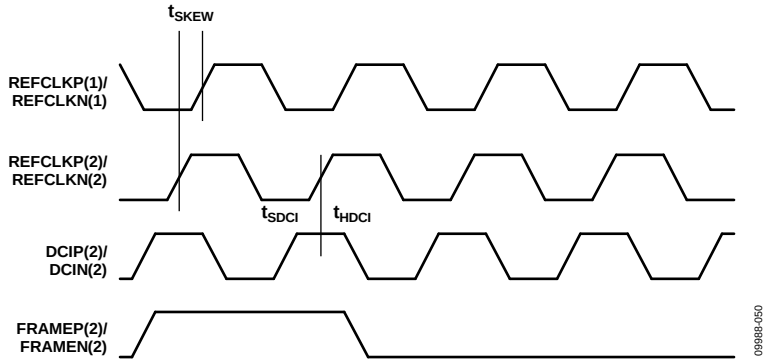


Figure 81. Timing Diagram Required for Synchronizing Devices

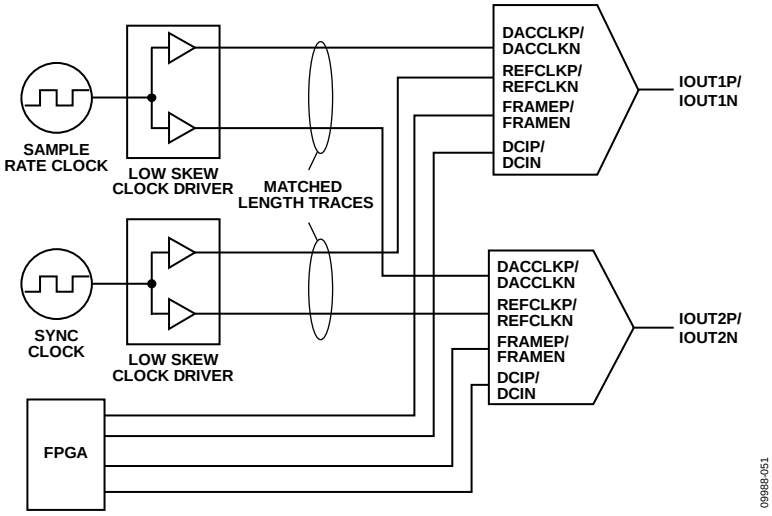


Figure 82. Typical Circuit Diagram for Synchronizing Devices to a System Clock

To maintain synchronization, the skew between the REFCLK signals of the devices must be less than t_{SKEW} ns. When resetting the FIFO, the FRAME signal must be held high for the time interval required to write two complete input data words. A timing diagram of the input signals is shown in Figure 81.

Figure 81 shows a REFCLK frequency equal to the data rate. Although this is the most common situation, it is not strictly required for proper synchronization. Any REFCLK frequency that satisfies the following equation is acceptable. (This equation is valid only when the PLL is used because only data rate mode is available with the PLL on.)

$$f_{SYNC_I} = f_{DACCLK}/2^N \text{ and } f_{SYNC_I} \leq f_{DATA}$$

where N = 0, 1, 2, or 3.

As an example, a configuration with 4× interpolation and clock frequencies of f_{VCO} = 1600 MHz, f_{DACCLK} = 800 MHz, f_{DATA} = 200 MHz, and f_{SYNC_I} = 100 MHz is a viable solution.

SYNCHRONIZATION WITH DIRECT CLOCKING

When directly sourcing the DAC sample rate clock, a separate REFCLK input signal is required for synchronization. To synchronize devices, the DACCLK signal and the REFCLK signal must be distributed with low skew to all the devices being synchronized. If the devices need to be synchronized to a master clock, use the master clock directly for generating the REFCLK input (see Figure 82).

DATA RATE MODE SYNCHRONIZATION

The Procedure for Data Rate Synchronization When Directly Sourcing the DAC Sampling Clock section outlines the steps required to synchronize multiple devices in data rate mode. The procedure assumes that the DACCLK and REFCLK signals are applied to all the devices. The procedure must be carried out on each individual device.

Procedure for Data Rate Synchronization When Directly Sourcing the DAC Sampling Clock

Configure the AD9121 for periodic data rate synchronization by writing 0xC8 to the sync control register (Register 0x10). Additional synchronization options are available (see the Additional Synchronization Features section).

Read the sync locked bit (Register 0x12, Bit 6) to verify that the device is back-end synchronized. A high level on this bit indicates that the clocks are running with a constant and known phase relative to the synchronization signal.

Reset the FIFO by strobing the FRAME signal high for one complete DCI period. Resetting the FIFO ensures that the correct data is being read from the FIFO of each of the devices simultaneously.

correct data is being read from the FIFO of each of the devices simultaneously.

This completes the synchronization procedure; all devices should now be synchronized.

To ensure that each DAC is updated with the correct data on the same CLK edge, two timing relationships must be met on each DAC.

- DCIP/DCIN and D[15:0]P/D[15:0]N must meet the setup and hold times with respect to the rising edge of DACCLK.
- Synchronization (REFCLK) must also meet the setup and hold times with respect to the rising edge of DACCLK.

When these conditions are met, the outputs of the DACs are updated within one DAC clock cycle of each other. The timing requirements of the input signals are shown in Figure 83.

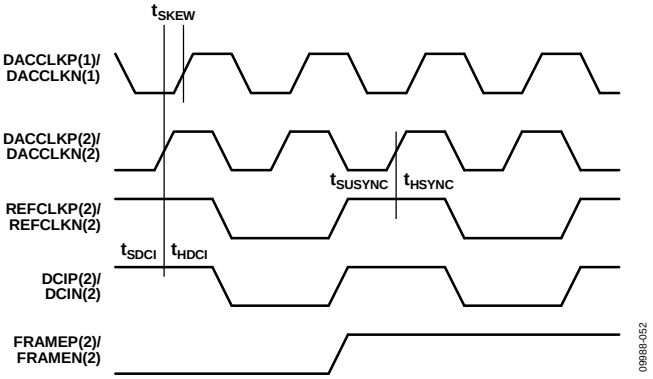


Figure 83. Data Rate Synchronization Signal Timing Requirements, 2× Interpolation

Figure 83 shows the synchronization signal timing with 2× interpolation; therefore, $f_{DCI} = ½ \times f_{CLK}$. The REFCLK input is shown to be equal to the data rate. The maximum frequency at which the device can be resynchronized in data rate mode can be expressed as

$$f_{SYNC_I} = f_{DATA}/2^N$$

where N is any non-negative integer.

Generally, for values of N greater than or equal to 3, select the FIFO rate synchronization mode.

When synchronization is used in data rate mode, the timing constraint between the DCI and DACCLK must be met according to Table 25. In data rate mode, the allowed phase drift between the DCI and DACCLK is limited to one DCI cycle. The DCI to DACCLK timing restriction is required to prevent corruption of the data transfer when the FIFO is constantly reset. The required timing between the DCI and DACCLK is shown in Figure 84.

Table 25. DCI to DACCLK Setup and Hold Times

DCI Delay Register 0x16, Bits[1:0]	Minimum Setup Time, t_{SDCI} (ns)	Minimum Hold Time, t_{HDCI} (ns)	Sampling Interval (ns)
00	−0.07	0.82	0.75
01	−0.24	1.13	0.89
10	−0.39	1.40	1.01
11	−0.49	1.55	1.06

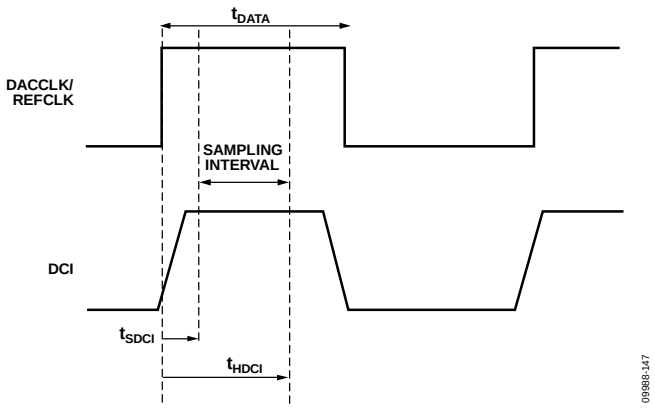


Figure 84. Timing Diagram for Input Data Port (Data Rate Mode)

FIFO RATE MODE SYNCHRONIZATION

The Procedure for FIFO Rate Synchronization When Directly Sourcing the DAC Sampling Clock section outlines the steps required to synchronize multiple devices in FIFO rate mode. The procedure assumes that the DACCLK and REFCLK signals are applied to all the devices. The procedure must be carried out on each individual device.

Procedure for FIFO Rate Synchronization When Directly Sourcing the DAC Sampling Clock

Configure the AD9121 for periodic FIFO rate synchronization by writing 0x88 to the sync control register (Register 0x10). Additional synchronization options are available (see the Additional Synchronization Features section).

Read the sync locked bit (Register 0x12, Bit 6) to verify that the device is back-end synchronized. A high level on this bit indicates that the clocks are running with a constant and known phase relative to the synchronization signal.

Reset the FIFO by strobing the FRAME signal high for one complete DCI period. Resetting the FIFO ensures that the correct data is being read from the FIFO of each of the devices simultaneously.

This completes the synchronization procedure; all devices should now be synchronized.

When these conditions are met, the outputs of the DACs are updated within one DAC clock cycle of each other. The timing requirements of the input signals are shown in Figure 85.

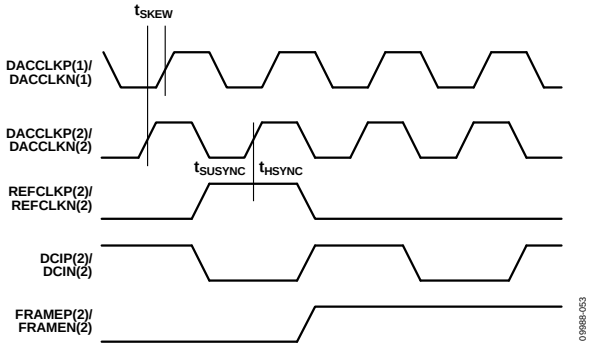


Figure 85. FIFO Rate Synchronization Signal Timing Requirements, 2× Interpolation

Figure 85 shows the synchronization signal timing with 2× interpolation; therefore, $f_{DCI} = ½ \times f_{CLK}$. The REFCLK input is shown to be equal to the FIFO rate. The maximum frequency at which the device can be resynchronized in FIFO rate mode can be expressed as

$$f_{SYNC_I} = f_{DATA}/(8 \times 2^N)$$

where N is any non-negative integer.

ADDITIONAL SYNCHRONIZATION FEATURES

Table 26 shows the required timing between the DACCLK and the synchronization clock when synchronization is used. This timing restriction applies to both data rate mode and FIFO rate mode.

Table 26. Synchronization Setup and Hold Times

Parameter	Min	Max	Unit
t_{SKEW}	$-t_{DACCLK}/2$	$+t_{DACCLK}/2$	ps
t_{SUSYNC}	100		ps
t_{HSYNC}	330		ps

One-Time Synchronization

When implementing the full multichip synchronization feature (with the REFCLK and FRAME signals aligned within one DACCLK cycle), the user may experience difficulty meeting the DACCLK to synchronization clock timing. In this case, a one-time synchronization method can be used. Before implementing the one-time synchronization, make sure that the synchronization signal is locked by checking both the sync signal locked and the sync signal lost flags (Bit 4 and Bit 5 in Register 0x06). It is also important that synchronization not be enabled before stable REFCLK signals are present from the FPGA or ASIC. For more information and a detailed flowchart of the one-time synchronization feature, see the AN-1093 Application Note, *Synchronization of Multiple AD9122 TxDAC+ Converters*.

Sync Status Bits

When the sync locked bit (Register 0x12, Bit 6) is set, it indicates that the synchronization logic has reached alignment. This alignment is determined when the clock generation state machine phase is constant.

Alignment takes from (11 + averaging) × 64 to (11 + averaging) × 128 DACCLK cycles. The sync locked bit can also trigger an $\overline{\text{IRQ}}$, as described in the Interrupt Request Operation section.

When the sync lost bit (Register 0x12, Bit 7) is set, it indicates that a previously synchronized device has lost alignment. This bit is latched and remains set until cleared by overwriting the register. This bit can also trigger an $\overline{\text{IRQ}}$, as described in the Interrupt Request Operation section.

The sync phase readback bits (Register 0x13, Bits[7:0]) report the current clock phase in a 6.2 format. Bits[7:2] report which of the 64 states (0 to 63) the clock is currently in. When averaging is enabled, Bits[1:0] provide ¼ state accuracy (for 0, ¼, ½, ¾). The lower two bits give an indication of the timing margin issues that may exist. If the synchronization sampling is error free, the fractional clock state should be 00.

Timing Optimization

The synchronization signal (REFCLK) is sampled by a version of the DACCLK. If sampling errors are detected, the opposite sampling edge can be selected to improve the sampling point. The sampling edge can be selected by setting Register 0x10, Bit 3 (1 = rising and 0 = falling).

The synchronization logic resynchronizes when a phase change between the synchronization signal (REFCLK) and the state of the clock generation state machine exceeds a threshold. To mitigate the effects of jitter and prevent erroneous resynchronizations, the relative phase can be averaged. The amount of averaging is set by the sync averaging bits (Register 0x10, Bits[2:0]) and can be set from 1 to 128. The higher the number of averages, the more slowly the device recognizes and resynchronizes to a legitimate phase correction. Generally, the averaging should be made as large as possible while still meeting the allotted resynchronization time interval. Note that, if the average synchronization sampling result is in approximately the middle of the probability curve, the synchronization engine can be unstable, resulting in corrupted output.

The value of the Sync Phase Request[5:0] bits (Register 0x11, Bits[5:0]) is the state to which the clock generation state machine resets upon initialization. By varying this value, the timing of the internal clocks, with respect to the synchronization signal (REFCLK), can be adjusted. Every increment of the Sync Phase Request[5:0] value advances the internal clocks by one DACCLK cycle. This offset can be used for two purposes: to skew the outputs of two synchronized DAC outputs in increments of the DACCLK cycle, and to change the relative timing between the DAC output and the SYNC input (REFCLK). This may allow for a more optimal placement of the DCI sampling point in data rate synchronization mode.

INTERRUPT REQUEST OPERATION

The AD9121 provides an interrupt request output signal on Pin 7 ($\overline{IRQ}$) that can be used to notify an external host processor of significant device events. Upon assertion of the interrupt, the device should be queried to determine the precise event that occurred. The $\overline{IRQ}$ pin is an open-drain, active low output. Pull the $\overline{IRQ}$ pin high external to the device. This pin can be tied to the interrupt pins of other devices with open-drain outputs to wire-OR these pins together.

The event flags provide visibility into the device. These flags are located in the two event flag registers, Register 0x06 and Register 0x07. The behavior of each event flag is independently selected in the interrupt enable registers, Register 0x04 and Register 0x05. When the flag interrupt enable is active, the event flag latches and triggers an external interrupt. When the flag interrupt is disabled, the event flag monitors the source signal, but the $\overline{IRQ}$ pin remains inactive.

Figure 86 shows the $\overline{IRQ}$-related circuitry and how the event flag signals propagate to the $\overline{IRQ}$ output. The INTERRUPT_ENABLE signal represents one bit from the interrupt enable register. The EVENT_FLAG_SOURCE signal represents one bit from the event flag register. The EVENT_FLAG_SOURCE signal represents one of the device signals that can be monitored, such as the PLL_LOCKED signal from the PLL phase detector or the FIFO_WARNING_1 signal from the FIFO controller.

When an interrupt enable bit is set high, the corresponding event flag bit reflects a positively tripped version of the EVENT_FLAG_SOURCE signal; that is, the event flag bit is latched on the rising edge of the EVENT_FLAG_SOURCE signal. This signal also asserts the external $\overline{IRQ}$ pin.

When an interrupt enable bit is set low, the event flag bit reflects the current status of the EVENT_FLAG_SOURCE signal, and the event flag has no effect on the external $\overline{IRQ}$ pin.

The latched version of an event flag (the INTERRUPT_SOURCE signal) can be cleared in two ways. The recommended way is by writing 1 to the corresponding event flag bit. A hardware or software reset also clears the INTERRUPT_SOURCE signal.

INTERRUPT SERVICE ROUTINE

Interrupt request management starts by selecting the set of event flags that require host intervention or monitoring. The events that require host action should be enabled so that the host is notified when they occur. For events requiring host intervention upon $\overline{IRQ}$ activation, run the following routine to clear an interrupt request:

1. Read the status of the event flag bits that are being monitored.
2. Set the interrupt enable bit low so that the unlatched EVENT_FLAG_SOURCE signal can be monitored directly.
3. Perform any actions that may be required to clear the EVENT_FLAG_SOURCE. In many cases, no specific actions may be required.
4. Read the event flag to verify that the actions taken have cleared the EVENT_FLAG_SOURCE.
5. Clear the interrupt by writing 1 to the event flag bit.
6. Set the interrupt enable bits of the events to be monitored.

Note that some EVENT_FLAG_SOURCE signals are latched signals. These signals are cleared by writing to the corresponding event flag bit. For more information about each event flag, see Register 0x06 and Register 0x07 in Table 11.

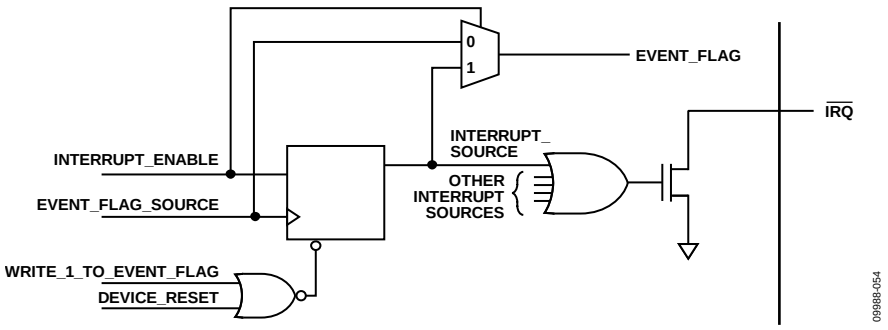


Figure 86. Simplified Schematic of $\overline{IRQ}$ Circuitry

INTERFACE TIMING VALIDATION

The AD9121 provides on-chip sample error detection (SED) circuitry that simplifies verification of the input data interface. The SED circuitry compares the input data samples captured at the digital input pins with a set of comparison values. The comparison values are loaded into registers through the SPI port. Differences between the captured values and the comparison values are detected and stored. Options are available for customizing SED test sequencing and error handling.

SED OPERATION

The SED circuitry operates on a data set made up of four 14-bit input words, denoted as I0, Q0, I1, and Q1. To properly align the input samples, the first I data-word (that is, I0) is indicated by asserting FRAME for at least one complete input sample.

Figure 87 shows the input timing of the interface in word mode. The FRAME signal can be issued once at the start of the data transmission, or it can be asserted repeatedly at intervals coinciding with the I0 and Q0 data-words.

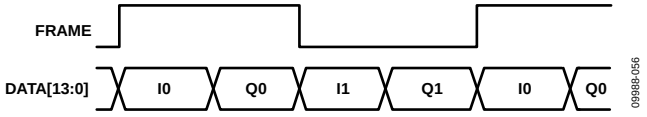


Figure 87. Timing Diagram of Extended FRAME Signal Required to Align Input Data for SED

The SED has three flag bits (Register 0x67, Bit 5, Bit 1, and Bit 0) that indicate the results of the input sample comparisons. The sample error detected bit (Register 0x67, Bit 5) is set when an error is detected and remains set until cleared. The SED also provides registers that indicate which input data bits experienced errors (Register 0x70 through Register 0x73). These bits are latched and indicate the accumulated errors detected until cleared.

Autosample error detection (AED) is an autoclear function in the SED. The autoclear mode has two effects: it activates the compare fail bit and the compare pass bit (Register 0x67, Bit 1 and Bit 0) and changes the behavior of Register 0x70 through Register 0x73. The compare pass bit is set if the last comparison indicated that the sample was error free. The compare fail bit is set if an error is detected. The compare fail bit is automatically cleared by the reception of eight consecutive error-free comparisons. When autoclear mode is enabled, Register 0x70 through Register 0x73 accumulate errors as previously described but are reset to all 0s after eight consecutive error-free sample comparisons are made.

If desired, the sample error detected, compare pass, and compare fail flags can be configured to trigger the IRQ pin when active. This is done by enabling the appropriate bits in the event flag register (Register 0x07).

Table 27 shows a progression of the input sample comparison results and the corresponding states of the error flags.

Table 27. Progression of Input Sample Comparison Results and the Resulting SED Register Values

Compare Results (Pass/Fail)	P	F	F	F	P	P	P	P	P	P	P	P	P	F	P	F
Register 0x67, Bit 5 (Sample Error Detected)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Register 0x67, Bit 1 (Compare Fail)	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
Register 0x67, Bit 0 (Compare Pass)	1	0	0	0	1	1	1	1	1	1	1	1	1	0	1	0
Register 0x70 to Register 0x73 (Errors Detected x_BITS[15:0])	Z[1]	N[2]	N[2]	N[2]	N[2]	N[2]	N[2]	N[2]	N[2]	N[2]	N[2]	N[2]	Z[1]	N[2]	N[2]	N[2]

[1] Z = all 0s.
[2] N = nonzero.

SED EXAMPLE

Normal Operation

The following example illustrates the SED configuration for continuously monitoring the input data and assertion of the $\overline{\text{IRQ}}$ pin when a single error is detected.

1. Load the following comparison values. (Comparison values can be chosen arbitrarily; however, choosing values that require frequent bit toggling provides the most robust test.)
   Register 0x68: I0[7:0]
   Register 0x69: I0[15:8]
   Register 0x6A: Q0[7:0]
   Register 0x6B: Q0[15:8]
   Register 0x6C: I1[7:0]
   Register 0x6D: I1[15:8]
   Register 0x6E: Q1[7:0]
   Register 0x6F: Q1[15:8]
2. Enable the SED error detect flag to assert the $\overline{\text{IRQ}}$ pin. (Set Register 0x05 to 0x04.)
3. Begin transmitting the input data pattern.
4. Write to Register 0x67 to enable the SED. (Set Register 0x67 to 0x80.)
5. Clear the SED errors in Register 0x67 and Register 0x07. When the SED is first turned on, the FRAME signal may be detected immediately; therefore, the SED failure bit may be asserted due to the unknown initial FRAME status. For this reason, the SED compare fail status bit must be cleared at least once immediately after enabling the SED.

If $\overline{\text{IRQ}}$ is asserted, read Register 0x67 and Register 0x70 through Register 0x73 to verify that a SED error was detected and to determine which input bits were in error. The bits in Register 0x70 through Register 0x73 are latched; therefore, the bits indicate any errors that occurred on those bits throughout the test (not only the errors that caused the error detected flag to be set).

Note that the FRAME signal is not required during normal operation when the device is configured for word mode. Enabling the alignment of the I0 sample as described in the SED Operation section requires the use of the FRAME signal. The timing diagram for byte mode is the same as during normal operation and is shown in Figure 43.

EXAMPLE START-UP ROUTINE

To ensure reliable start-up of the AD9121, certain sequences should be followed. This section shows an example start-up routine. This example uses the configuration described in the Device Configuration section.

DEVICE CONFIGURATION

The following device configuration is used for this example:

- f_{DATA} = 122.88 MSPS
- Interpolation is 4×, using HB1 = 10 and HB2 = 010010
- Input data is baseband data
- f_{OUT} = 140 MHz
- f_{REFCLK} = 122.88 MHz
- PLL is enabled
- Fine NCO is enabled
- Inverse sinc filter is enabled
- Synchronization is enabled
- Silicon revision is R2

DERIVED PLL SETTINGS

The following PLL settings can be derived from the device configuration:

- $f_{DACCLK} = f_{DATA} \times$ interpolation = 491.52 MHz
- $f_{VCO} = 4 \times f_{DACCLK}$ = 1966.08 MHz (1 GHz < f_{VCO} < 2 GHz)
- $N1 = f_{DACCLK}/f_{REFCLK} = 4$
- $N2 = f_{VCO}/f_{DACCLK} = 4$

DERIVED NCO SETTINGS

The following NCO settings can be derived from the device configuration:

- $f_{NCO} = 2 \times f_{DATA}$
- $f_{CARRIER} = f_{OUT} - f_{MODHB1} = 140 - 122.88 = 17.12$ MHz
- $FTW = 17.12/(2 \times 122.8) \times 2^{32} =$ 0x11D55555

START-UP SEQUENCE

The following sequence configures the power clock and register write sequencing for reliable device start-up in PLL on mode:

```
Power up Device (no specific power supply
sequence is required)
Apply stable REFCLK input signal.
Apply stable DCI input signal.
Issue H/W RESET (Optional).

Device Configuration Register Write Sequence:
0x00 → 0x20   /* Issue Software Reset */
0x00 → 0x00

/* Start PLL */
0x0D → 0xD9
0x0A → 0xC0
0x0A → 0x80

/* Verify PLL is Locked */
Read 0x0E     /* Expect bit 7 = 1 */

/* Configure Interpolation Filters */
0x1B → 0x84
0x1C → 0x04
0x1D → 0x24

/* Configure NCO */
0x1E → 0x01
0x30 → 0x55
0x31 → 0x55
0x32 → 0xD5
0x33 → 0x11

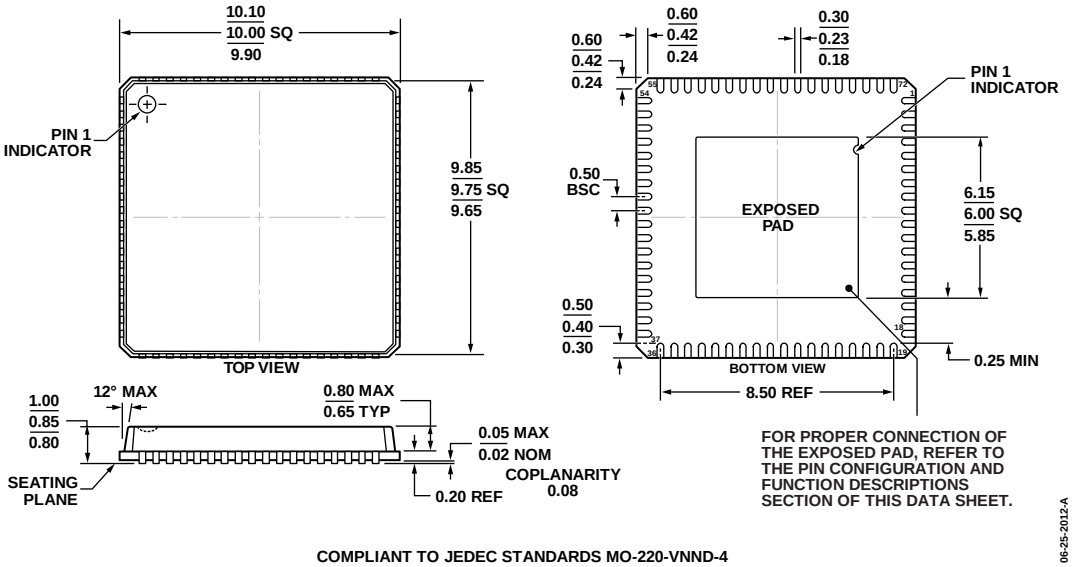
/* Update Frequency Tuning Word */
0x36 → 0x01
0x36 → 0x00

/* Choose Data Rate Mode */
0x10 → 0x48

/* Issue Software FIFO Reset */
0x17 → 0x04
0x18 → 0x02

/* Verify FIFO Reset */
Read 0x18     /* Expect 0x07 */
0x18 → 0x00
Read 0x19     /* Expect 0x1F or 0x0F or 0x07 */
```

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VNND-4

Figure 88. 72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
10 mm × 10 mm Body, Very Thin Quad
(CP-72-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9121BCPZ	−40°C to +85°C	72-lead LFCSP_VQ	CP-72-7
AD9121BCPZRL	−40°C to +85°C	72-lead LFCSP_VQ	CP-72-7
AD9121-M5372-EBZ		Evaluation Board Connected to ADL5372 Modulator	
AD9121-M5375-EBZ		Evaluation Board Connected to ADL5375 Modulator	

[1] Z = RoHS Compliant Part.

©2012 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D09988-0-10/12(B)