8-Bit 40 MSPS/60 MSPS/80 MSPS A/D Converter

AD9057

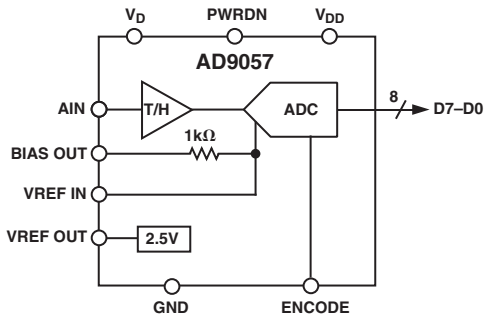
FEATURES

8-Bit, Low Power ADC: 200 mW Typical
120 MHz Analog Bandwidth
On-Chip 2.5 V Reference and Track-and-Hold
1 V p-p Analog Input Range
Single 5 V Supply Operation
5 V or 3 V Logic Interface
Power-Down Mode: <10 mW
3 Performance Grades (40 MSPS, 60 MSPS, 80 MSPS)

APPLICATIONS

Digital Communications (QAM Demodulators)
RGB and YC/Composite Video Processing
Digital Data Storage Read Channels
Medical Imaging
Digital Instrumentation

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9057 is an 8-bit monolithic analog-to-digital converter optimized for low cost, low power, small size, and ease of use. With 40 MSPS, 60 MSPS, or 80 MSPS encode rate capability and full-power analog bandwidth of 120 MHz, the component is ideal for applications requiring excellent dynamic performance.

To minimize system cost and power dissipation, the AD9057 includes an internal 2.5 V reference and a track-and-hold (T/H) circuit. The user must provide only a 5 V power supply and an encode clock. No external reference or driver components are required for many applications.

The AD9057's encode input is TTL/CMOS compatible, and the 8-bit digital outputs can be operated from 5 V or 3 V supplies. A power-down function may be exercised to bring total consumption to <10 mW. In power-down mode, the digital outputs are driven to a high impedance state.

Fabricated on an advanced BiCMOS process, the AD9057 is available in a space-saving 20-lead shrink small outline package (20-lead SSOP) and is specified over the industrial temperature range (–40°C to +85°C).

Customers desiring multichannel digitization may consider the AD9059, a dual 8-bit, 60 MSPS monolithic based on the AD9057 ADC core. The AD9059 is available in a 28-lead surface-mount plastic package (28-lead SSOP) and is specified over the industrial temperature range.

REV. D

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AD9057* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-348: Avoiding Passive-Component Pitfalls
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-715: A First Approach to IBIS Models: What They Are and How They Are Generated
- AN-737: How ADIsimADC Models an ADC
- AN-741: Little Known Characteristics of Phase Noise
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter

Data Sheet

- AD9057: 8-Bit, 40/60/80 MSPS A/D Converter Data Sheet

TOOLS AND SIMULATIONS

- AD9057 IBIS Models

REFERENCE MATERIALS

Technical Articles

- Correlating High-Speed ADC Performance to Multicarrier 3G Requirements
- DNL and Some of its Effects on Converter Performance
- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD9057 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9057 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

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AD9057–SPECIFICATIONS (V_D = 5 V, V_{DD} = 3 V; external reference, unless otherwise noted.)

Parameter	Temp	Test Level	AD9057BRS-40 Min	AD9057BRS-40 Typ	AD9057BRS-40 Max	AD9057BRS-60 Min	AD9057BRS-60 Typ	AD9057BRS-60 Max	AD9057BRS-80 Min	AD9057BRS-80 Typ	AD9057BRS-80 Max	Unit
RESOLUTION				8			8			8		Bits
DC ACCURACY												
Differential Nonlinearity	25°C	I		0.75	1.9		0.75	1.9		0.75	1.9	LSB
	Full	VI			2.0			2.0			2.0	LSB
Integral Nonlinearity	25°C	I		0.75	1.9		0.75	1.9		0.75	1.9	LSB
	Full	VI			2.0			2.0			2.0	LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed			Guaranteed		
Gain Error[1]	25°C	I	–6	–2.5	+6	–6	–2.5	+6	–6	–2.5	+6	% FS
	Full	VI	–8		+8	–8		+8	–8		+8	% FS
Gain Tempco[1]	Full	V		±70			±70			±70		ppm/°C
ANALOG INPUT												
Input Voltage Range												
(Centered at 2.5 V)	25°C	V		1.0			1.0			1.0		V p-p
Input Offset Voltage	25°C	I	–15	0	+15	–15	0	+15	–15	0	+15	mV
	Full	VI	–25		+25	–25		+25	–25		+25	mV
Input Resistance	25°C	V		150			150			150		kΩ
Input Capacitance	25°C	V		2			2			2		pF
Input Bias Current	25°C	I		6	16		6	16		6	16	µA
	Full	VI			25			25			25	µA
Analog Bandwidth	25°C	V		120			120			120		MHz
BAND GAP REFERENCE												
Output Voltage	Full	VI	2.4	2.5	2.6	2.4	2.5	2.6	2.4	2.5	2.6	V
Temperature Coefficient	Full	V		±10			±10			±10		ppm/°C
SWITCHING PERFORMANCE												
Maximum Conversion Rate	Full	VI	40			60			80			MSPS
Minimum Conversion Rate	Full	IV			5			5			5	MSPS
Aperture Delay (t_A)	25°C	V		2.7			2.7			2.7		ns
Aperture Uncertainty (Jitter)	25°C	V		5			5			5		ps rms
Output Valid Time (t_V)[2]	Full	IV	4.0	6.6		4.0	6.6		4.0	6.6		ns
Output Propagation Delay (t_{PD})[2]	Full	IV		11.5	18.0		9.5	14.2		8.0	11.3	ns
DYNAMIC PERFORMANCE[3]												
Transient Response	25°C	V		9			9			9		ns
Overvoltage Recovery Time	25°C	V		9			9			9		ns
Signal-to-Noise Ratio (SINAD)												
(With Harmonics)												
f_{IN} = 10.3 MHz	25°C	I	42	45.5		42	45		41.5	45		dB
f_{IN} = 76 MHz	25°C	V		44.0			43.5			43.5		dB
Effective Number of Bits (ENOB)												
f_{IN} = 10.3 MHz	25°C	I	6.7	7.2		6.7	7.2		6.6	7.2		Bits
f_{IN} = 76 MHz	25°C	V		7.0			6.9			6.9		Bits
Signal-to-Noise Ratio (SNR)												
(Without Harmonics)												
f_{IN} = 10.3 MHz	25°C	I	43	46.5		43	46		42.5	46		dB
f_{IN} = 76 MHz	25°C	V		45.5			45			45		dB
Second Harmonic Distortion												
f_{IN} = 10.3 MHz	25°C	I	–50	–62		–50	–62		–50	–62		dBc
f_{IN} = 76 MHz	25°C	V		–54			–54			–54		dBc
Third Harmonic Distortion												
f_{IN} = 10.3 MHz	25°C	I	–46	–60		–46	–60		–46	–60		dBc
f_{IN} = 76 MHz	25°C	V		–54			–54			–54		dBc
Two Tone Intermodulation												
Distortion (IMD)	25°C	V		–52			–52			–52		dBc
Differential Phase	25°C	V		0.8			0.8			0.8		Degrees
Differential Gain	25°C	V		1.0			1.0			1.0		%
DIGITAL INPUTS												
Logic 1 Voltage	Full	VI	2.0			2.0			2.0			V
Logic 0 Voltage	Full	VI			0.8			0.8			0.8	V
Logic 1 Current	Full	VI			±1			±1			±1	µA
Logic 0 Current	Full	VI			±1			±1			±1	µA
Input Capacitance	25°C	V		4.5			4.5			4.5		pF
Encode Pulsewidth High (t_{EH})	25°C	IV	9.0		166	6.7		166	5.5		166	ns
Encode Pulsewidth Low (t_{EL})	25°C	IV	9.0		166	6.7		166	5.5		166	ns

Parameter	Temp	Test Level	AD9057BRS-40 Min	AD9057BRS-40 Typ	AD9057BRS-40 Max	AD9057BRS-60 Min	AD9057BRS-60 Typ	AD9057BRS-60 Max	AD9057BRS-80 Min	AD9057BRS-80 Typ	AD9057BRS-80 Max	Unit
DIGITAL OUTPUTS												
Logic 1 Voltage (V_{DD} = 3 V)	Full	VI	2.95			2.95			2.95			V
Logic 1 Voltage (V_{DD} = 5 V)	Full	IV	4.95			4.95			4.95			V
Logic 0 Voltage	Full	VI			0.05			0.05			0.05	V
Output Coding			Offset Binary Code			Offset Binary Code			Offset Binary Code			
POWER SUPPLY												
V_D Supply Current (V_D = 5 V)	Full	VI		36	48		38	48		40	51	mA
V_{DD} Supply Current (V_{DD} = 3 V)[4]	Full	VI		4.0	6.5		5.5	6.5		7.4	8.8	mA
Power Dissipation[5, 6]	Full	VI		192	260		205	260		220	281	mW
Power-Down Dissipation	Full	VI		6	10		6	10		6	10	mW
Power Supply Rejection Ratio (PSRR)	25°C	V		3			3			3		mV/V

NOTES

[1]Gain error and gain temperature coefficient are based on the ADC only (with a fixed 2.5 V external reference).

[2]t_V and t_{PD} are measured from the 1.5 V level of the encode to the 10%/90% levels of the digital output swing. The digital output load during test is not to exceed an ac load of 10 pF or a dc current of ±40 μA.

[3]SNR/harmonics based on an analog input voltage of –0.5 dBFS referenced to a 1.0 V full-scale input range.

[4]Digital supply current based on V_{DD} = 3 V output drive with <10 pF loading under dynamic test conditions.

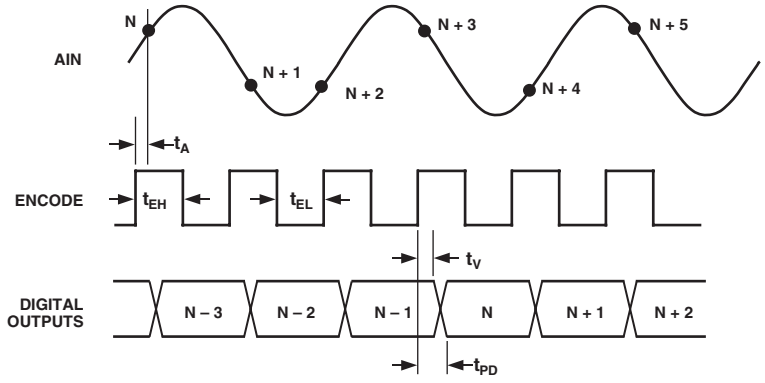
[5]Power dissipation is based on specified encode and 10.3 MHz analog input dynamic test conditions (V_D = 5 V ± 5%, V_{DD} = 3 V ± 5%).

[6]Typical thermal impedance for the RS style (SSOP) 20-lead package: θ_{JC} = 46°C/W, θ_{CA} = 80°C/W, and θ_{JA} = 126°C/W.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level	Description
I	100% production tested.
II	100% production tested at 25°C and sample tested at specified temperatures.
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
VI	100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range.



		MIN	TYP	MAX
t_A	APERTURE DELAY		2.7 ns	
t_{EH}	PULSEWIDTH HIGH			166 ns
t_{EL}	PULSEWIDTH LOW			166 ns
t_V	OUTPUT VALID TIME	4.0 ns	6.6 ns	
t_{PD}	OUTPUT PROP DELAY		9.5 ns	

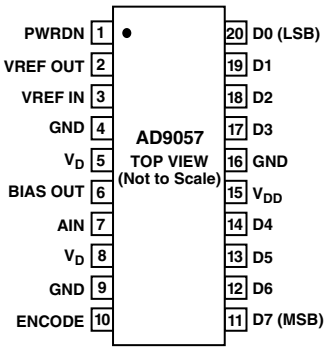
Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

V_D, V_{DD} . . . . . 7 V
Analog Inputs . . . . . –0.5 V to V_D + 0.5 V
Digital Inputs . . . . . –0.5 V to V_{DD} + 0.5 V
VREF Input . . . . . –0.5 V to V_D + 0.5 V
Digital Output Current . . . . . 20 mA
Operating Temperature . . . . . –55°C to +125°C
Storage Temperature . . . . . –65°C to +150°C
Maximum Junction Temperature . . . . . 150°C
Maximum Case Temperature . . . . . 150°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Option*
AD9057BRS-40	–40°C to +85°C	RS-20
AD9057BRS-60	–40°C to +85°C	RS-20
AD9057BRS-80	–40°C to +85°C	RS-20
AD9057/PCB	25°C	Evaluation Board

*RS = Shrink Small Outline Package (SSOP).

Table I. Digital Coding (VREF = 2.5 V)

Analog Input	Voltage Level	Digital Output
3.0 V	Positive Full Scale	1111 1111
2.502 V	Midscale +1/2 LSB	1000 0000
2.498 V	Midscale –1/2 LSB	0111 1111
2.0 V	Negative Full Scale	0000 0000

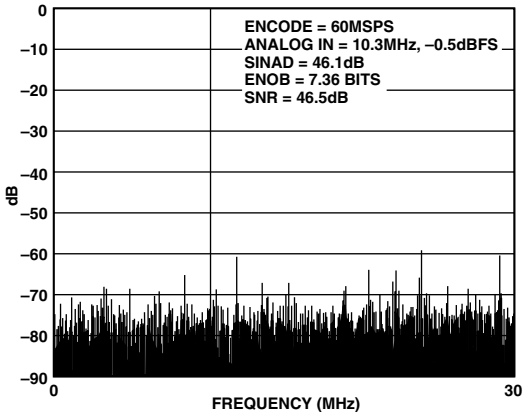
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	PWRDN	Power-Down Function Select; Logic High for Power-Down Mode (Digital Outputs Go to High Impedance State).
2	VREF OUT	Internal Reference Output (2.5 V typ); Bypass with 0.1 μF to Ground.
3	VREF IN	Reference Input for ADC (2.5 V typ, ±10%).
4, 9, 16	GND	Ground (Analog/Digital).
5, 8	V_D	Analog 5 V Power Supply.
6	BIAS OUT	Bias Pin for AC Coupling (1 kΩ to REF IN).
7	AIN	Analog Input for ADC.
10	ENCODE	Encode Clock for ADC (ADC Samples on Rising Edge of Encode).
11–14, 17–20	D7–D0	Digital Outputs of ADC.
15	V_{DD}	Digital Output Power Supply; Nominally 3 V to 5 V.

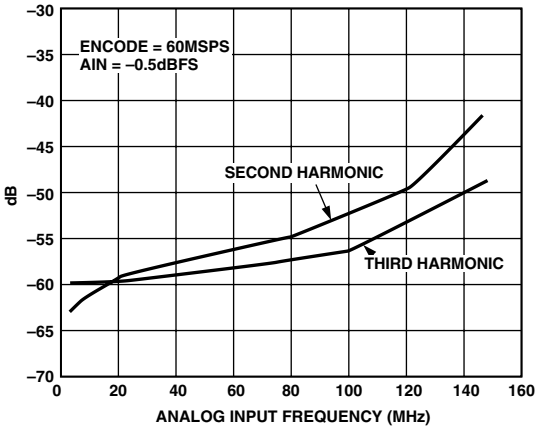
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9057 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

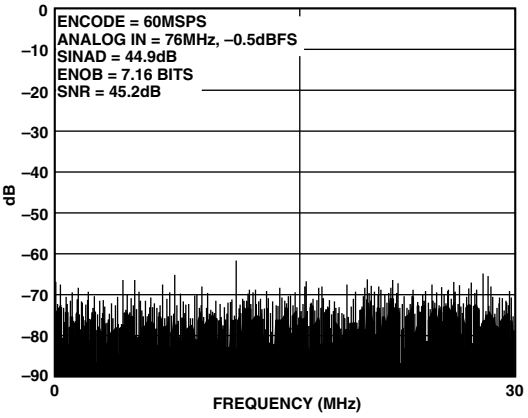




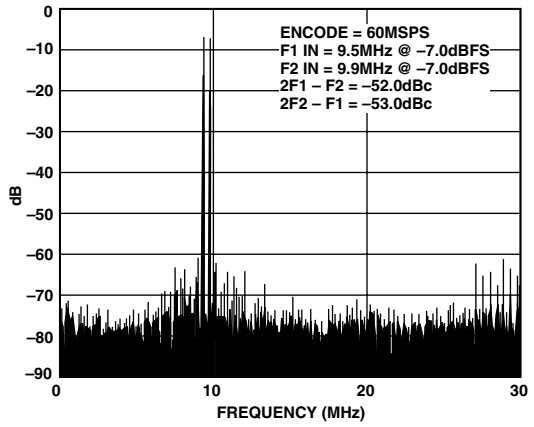
TPC 1. Spectral Plot 60 MSPS, 10.3 MHz



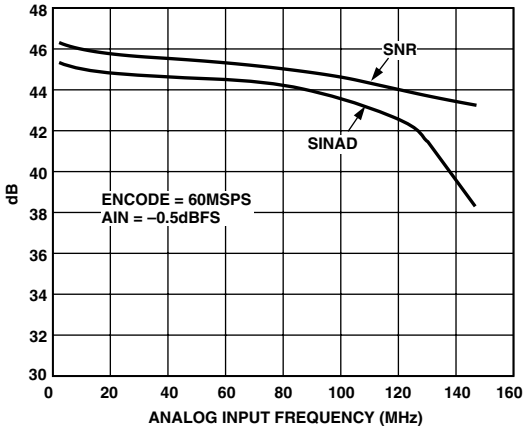
TPC 4. Harmonic Distortion vs. AIN Frequency



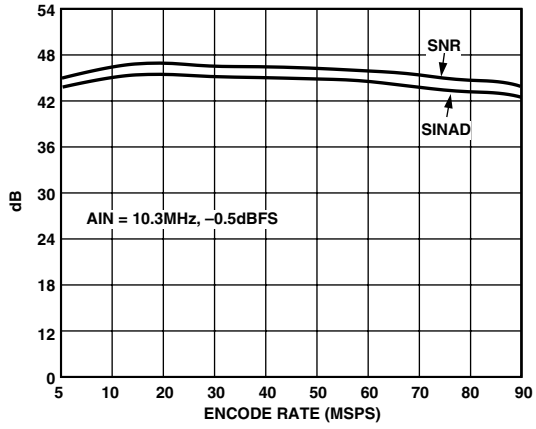
TPC 2. Spectral Plot 60 MSPS, 76 MHz



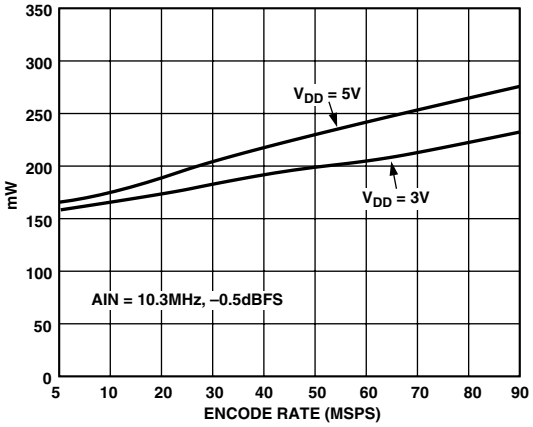
TPC 5. Two-Tone Intermodulation Distortion



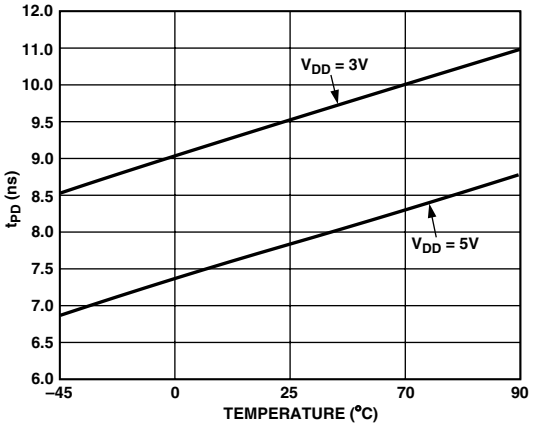
TPC 3. SINAD/SNR vs. AIN Frequency



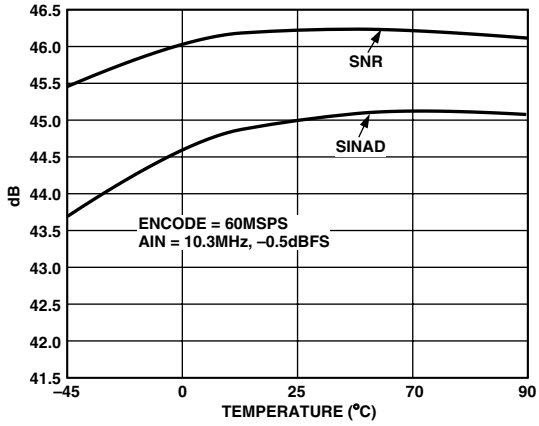
TPC 6. SINAD/SNR vs. Encode Rate



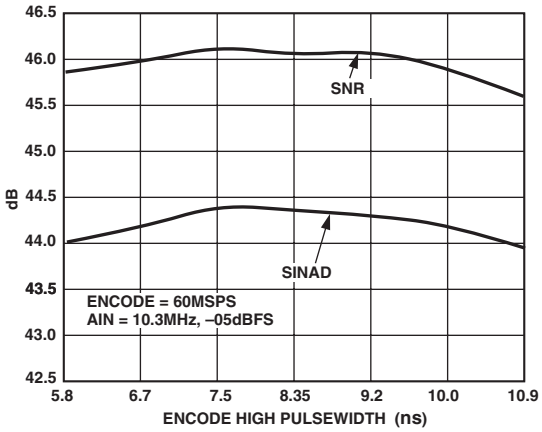
TPC 7. Power Dissipation vs. Encode Rate



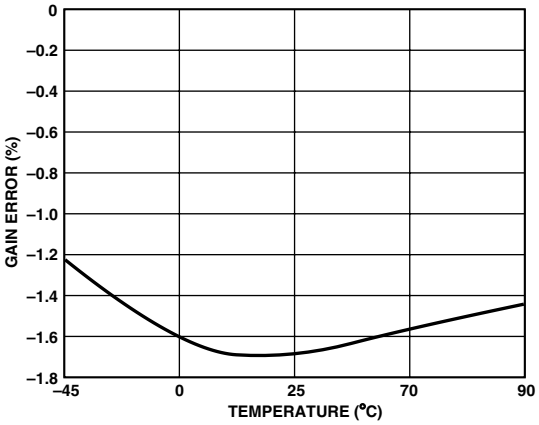
TPC 10. t_{PD} vs. Temperature/Supply (V_{DD} = 3 V/5 V)



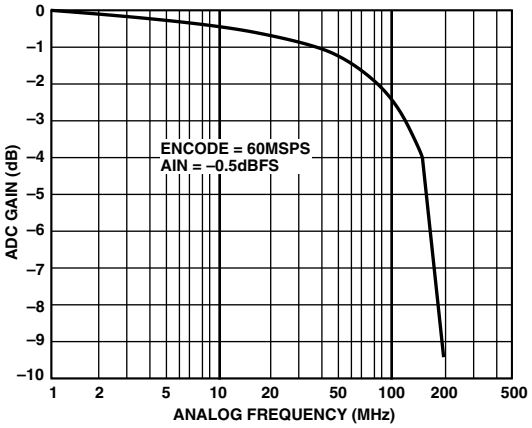
TPC 8. SINAD/SNR vs. Temperature



TPC 11. SINAD/SNR vs. Encode Pulsewidth



TPC 9. ADC Gain vs. Temperature (with External 2.5 V Reference)



TPC 12. ADC Frequency Response

THEORY OF OPERATION

The AD9057 combines Analog Devices' proprietary MagAmp gray code conversion circuitry with flash converter technology to provide a high performance, low cost ADC. The design architecture ensures low power, high speed, and 8-bit accuracy. A single-ended TTL/CMOS compatible ENCODE input controls ADC timing for sampling the analog input pin and strobing the digital outputs (D7–D0). An internal voltage reference (VREF OUT) may be used to control ADC gain and offset or an external reference may be applied.

The analog input signal is buffered at the input of the ADC and applied to a high speed track-and-hold. The track-and-hold circuit holds the analog input value during the conversion process (beginning with the rising edge of the encode command). The track-and-hold's output signal passes through the gray code and flash conversion stages to generate coarse and fine digital representations of the held analog input level. Decode logic combines the multistage data and aligns the 8-bit word for strobed outputs on the rising edge of the encode command. The MagAmp/Flash architecture of the AD9057 results in three pipeline delays for the output data.

USING THE AD9057

Analog Inputs

The AD9057 provides a single-ended analog input impedance of 150 kΩ. The input requires a dc bias current of 6 μA (typical) centered near 2.5 V (±10%). The dc bias may be provided by the user or may be derived from the ADC's internal voltage reference. Figure 2 shows a low cost dc bias implementation allowing the user to capacitively couple ac signals directly into the ADC without additional active circuitry. For best dynamic performance, the VREF OUT pin should be decoupled to ground with a 0.1 μF capacitor (to minimize modulation of the reference voltage) and the bias resistor should be approximately 1 kΩ. A 1 kΩ bias resistor (±20%) is included within the AD9057 and may be used to reduce application board size and complexity.

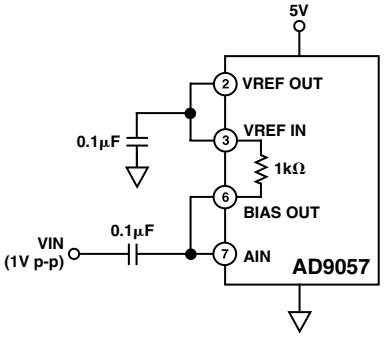


Figure 2. Capacitively Coupled AD9057

Figure 3 shows typical connections for high performance dc biasing using the ADC's internal voltage reference. All components may be powered from a single 5 V supply. In the example, analog input signals are referenced to ground.

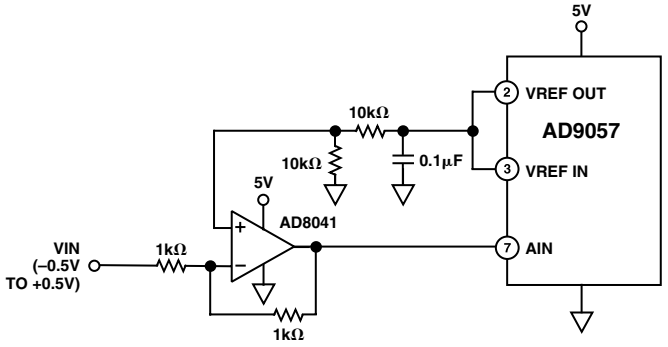


Figure 3. DC-Coupled AD9057 (Inverted VIN)

Voltage Reference

A stable and accurate 2.5 V voltage reference is built into the AD9057 (VREF OUT). The reference output may be used to set the ADC gain/offset by connecting VREF OUT to VREF IN. The internal reference is capable of providing 300 μA of drive current (for dc biasing the analog input or other user circuitry).

Some applications may require greater accuracy, improved temperature performance, or gain adjustments that cannot be obtained using the internal reference. An external voltage may be applied to the VREF IN with VREF OUT disconnected for gain adjustment of up to ±10% (the VREF IN pin is internally tied directly to the ADC circuitry). ADC gain and offset will vary simultaneously with external reference adjustment with a 1:1 ratio (a 2% or 50 mV adjustment to the 2.5 V reference varies ADC gain by 2% and ADC input range center offset by 50 mV). Theoretical input voltage range versus reference input voltage may be calculated from the following equations:

$$V_{RANGE\ (p\text{-}p)} = VREF\ IN/2.5$$

$$V_{MIDSCALE} = VREF\ IN$$

$$V_{TOP\text{-}OF\text{-}RANGE} = VREF\ IN + V_{RANGE}/2$$

$$V_{BOTTOM\text{-}OF\text{-}RANGE} = VREF\ IN - V_{RANGE}/2$$

Digital Logic (5 V/3 V Systems)

The digital inputs and outputs of the AD9057 can easily be configured to interface directly with 3 V or 5 V logic systems. The encode and power-down (PWRDN) inputs are CMOS stages with TTL thresholds of 1.5 V, making the inputs compatible with TTL, 5 V CMOS, and 3 V CMOS logic families. As with all high speed data converters, the encode signal should be clean and jitter free to prevent degradation of ADC dynamic performance.

The AD9057's digital outputs will also interface directly with 5 V or 3 V CMOS logic systems. The voltage supply pin (V_{DD}) for these CMOS stages is isolated from the analog V_D voltage supply. By varying the voltage on this supply pin, the digital output high level will change for 5 V or 3 V systems. Optimum SNR is obtained running the outputs at 3 V. Care should be taken to isolate the V_{DD} supply voltage from the 5 V analog supply to minimize digital noise coupling into the ADC.

The AD9057 provides high impedance digital output operation when the ADC is driven into power-down mode (PWRDN, logic high). A 200 ns (minimum) power-down time should be provided before a high impedance characteristic is required at the outputs. A 200 ns power-up period should be provided to ensure accurate ADC output data after reactivation (valid output data is available three clock cycles after the 200 ns delay).

Timing

The AD9057 is guaranteed to operate with conversion rates from 5 MSPS to 80 MSPS depending on grade. The ADC is designed to operate with an encode duty cycle of 50%, but performance is insensitive to moderate variations. Pulsewidth variations of up to ±10% (allowing the encode signal to meet the minimum/maximum high/low specifications) will cause no degradation in ADC performance (see Figure 1 timing diagram).

Power Dissipation

The power dissipation of the AD9057 is specified to reflect a typical application setup under the following conditions: analog input is –0.5 dBFS at 10.3 MHz, V_D is 5 V, V_{DD} is 3 V, and digital outputs are loaded with 7 pF typical (10 pF maximum). The actual dissipation will vary as these conditions are modified in user applications. TPC 7 shows typical power consumption for the AD9057 versus ADC encode frequency and V_{DD} supply voltage.

A power-down function allows users to reduce power dissipation when ADC data is not required. A TTL/CMOS high signal (PWRDN) shuts down portions of the ADC and brings total power dissipation to less than 10 mW. The internal band gap voltage reference remains active during power-down mode to minimize ADC reactivation time. If the power-down function is not desired, Pin 1 should be tied to ground.

APPLICATIONS

The wide analog bandwidth of the AD9057 makes it attractive for a variety of high performance receiver and encoder applications. Figure 4 shows two ADCs in a typical low cost I and Q demodulator implementation for cable, satellite, or wireless LAN modem receivers. The excellent dynamic performance of the ADC at higher analog input frequencies and encode rates empowers users to employ direct IF sampling techniques (refer to TPC 2 spectral plot). IF sampling eliminates or simplifies analog mixer and filter stages to reduce total system cost and power.

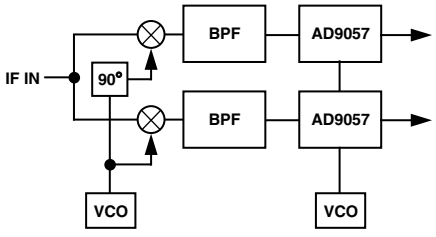


Figure 4. I and Q Digital Receiver

The high sampling rate and analog bandwidth of the AD9057 are ideal for computer RGB video digitizer applications. With a full-power analog bandwidth of 2× the maximum sampling rate, the ADC provides sufficient pixel-to-pixel transient settling time to ensure accurate 60 MSPS video digitization. Figure 5 shows a typical RGB video digitizer implementation for the AD9057.

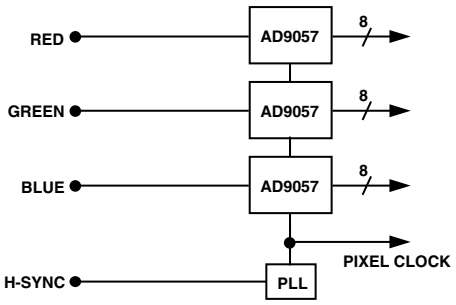


Figure 5. RGB Video Encoder

Evaluation Board

The AD9057/PCB evaluation board provides an easy-to-use analog/digital interface for the 8-bit, 60 MSPS ADC. The board includes typical hardware configurations for a variety of high speed digitization evaluations. On-board components include the AD9057 (in the 20-lead SSOP package), an optional analog input buffer amplifier, a digital output latch, board timing drivers, an analog reconstruction digital-to-analog converter, and configurable jumpers for ac coupling, dc coupling, and power-down function testing. The board is configured at shipment for dc coupling using the AD9057's internal voltage reference.

For dc-coupled analog input applications, amplifier U2 is configured to operate as a unity gain inverter with adjustable offset for the analog input signal. For full-scale ADC drive, the analog input signal should be 1 V p-p into 50 Ω (R1) referenced to ground (0 V). The amplifier offsets the analog signal by +VREF (2.5 V typical) to center the voltage for proper ADC input drive. For dc-coupled operation, connect E1 to E2 (analog input to R2) and E11 to E12 (amplifier output to analog input of AD9057) using the board jumper connectors. DC offset of the analog input signal can be modified by adjusting potentiometer R10.

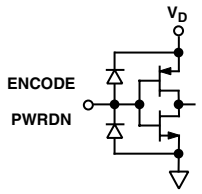
For ac-coupled analog input applications, amplifier U2 is removed from the analog signal path. The analog signal is coupled into the input of the AD9057 through capacitor C2. The ADC pulls analog input bias current from the VREF IN voltage through the 1 kΩ resistor internal to the AD9057 (BIAS OUT). The analog input signal to the board should be 1 V p-p into 50 Ω (R1) for full-scale ADC drive. For ac-coupled operation, connect E1 to E3 (analog input A to C2 feedthrough capacitor) and E10 to E12 (C2 to the analog input and internal bias resistor) using the board jumper connectors.

The on-board reference voltage may be used to drive the ADC or an external reference may be applied. To use the internal voltage reference, connect E6 to E5 (VREF OUT to VREF IN). To apply an external voltage reference, connect E4 to E5 (external reference from the REF banana jack to VREF IN). The external voltage reference should be 2.5 V ± 10%.

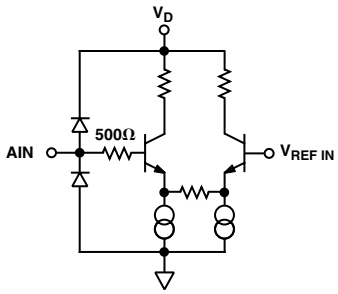
The power-down function of the AD9057 can be done through a board jumper connection. Connect E7 to E9 (5 V to PWRDN) for power-down operation. For normal operation, connect E8 to E9 (ground to PWRDN).

The encode signal source should be TTL/CMOS compatible and capable of driving a 50 Ω termination (R7). The digital outputs of the AD9057 are buffered through latches on the evaluation board (U3) and are available for the user at connector Pins 30 to 37. Latch timing is derived from the ADC encode clock and a digital clocking signal is provided for the board user at connector Pins 2 and 21.

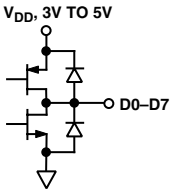
An on-board reconstruction digital-to-analog converter is available for quick evaluations of ADC performance using an oscilloscope or spectrum analyzer. The DAC converts the ADC's digital outputs to an analog signal for examination at the DAC OUT connector. The DAC is clocked at the ADC encode frequency. The AD9760 is a 10-bit/100 MSPS single 5 V supply DAC. The reconstruction signal facilitates quick system trouble-shooting or confirmation of ADC functionality without requiring external digital memory, timing, or display interfaces. The DAC can be used for limited dynamic testing, but customers should note that test results will be based on the combined performance of the ADC and DAC (the best ADC performance will be recognized by evaluating the digital outputs of the ADC directly).



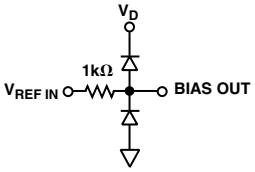
Digital Inputs



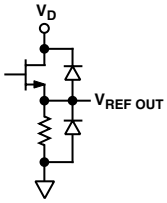
Analog Input



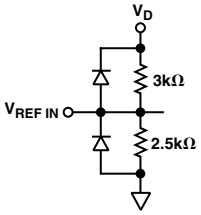
Digital Outputs



Bias Output



V_{REF} Output



V_{REF} Input

Figure 6. Equivalent Circuits

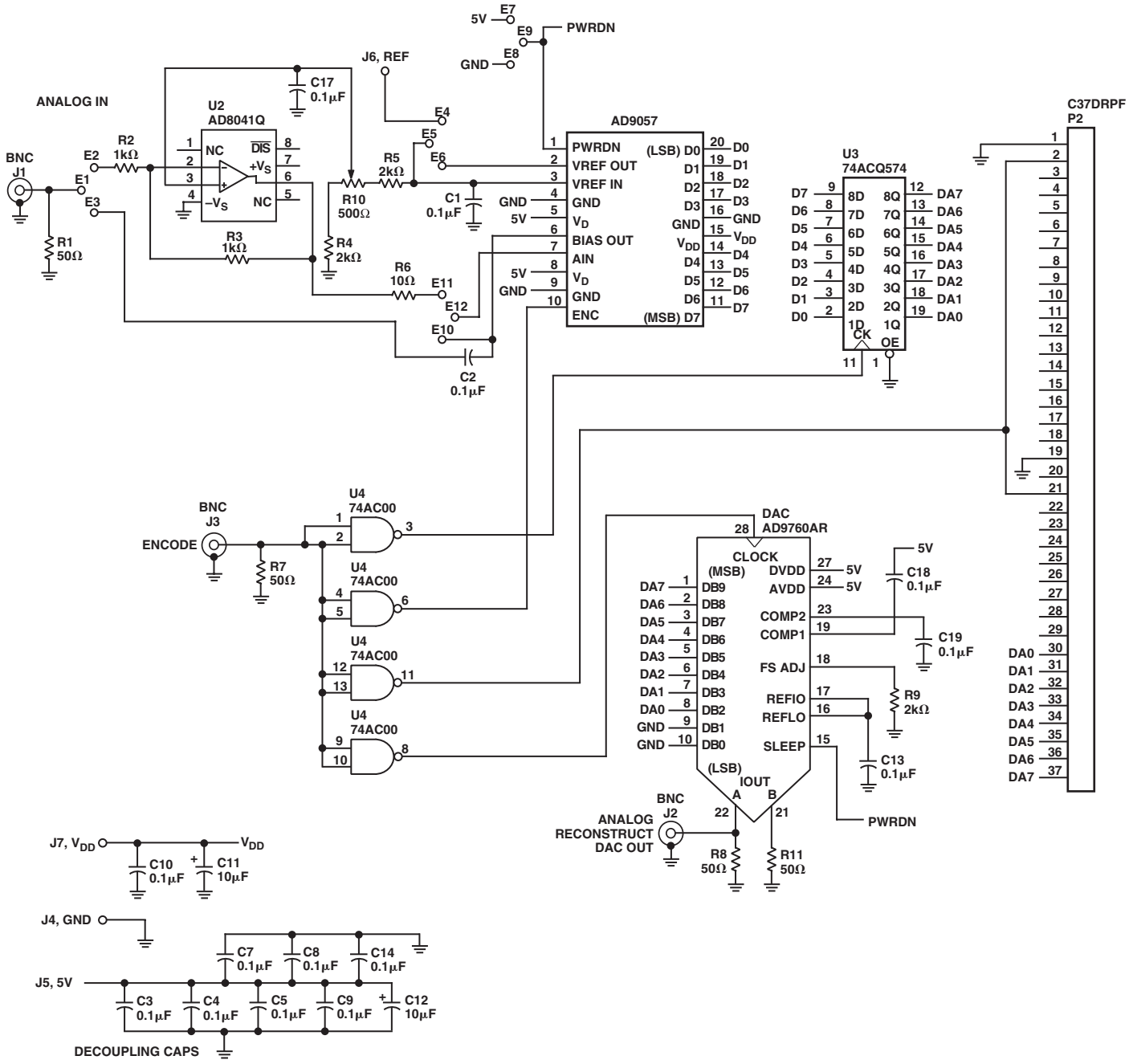


Figure 7. Evaluation Board Schematic

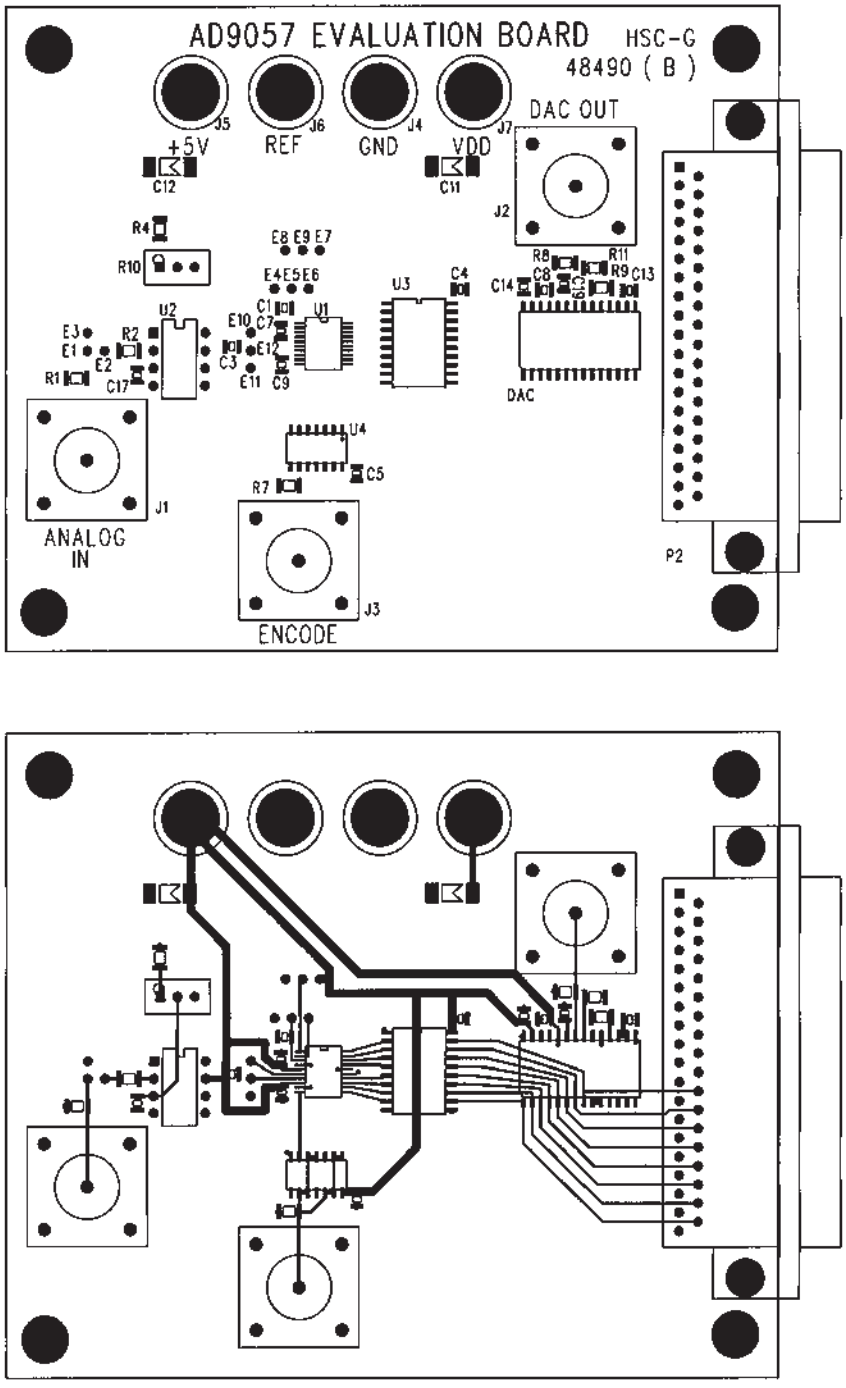
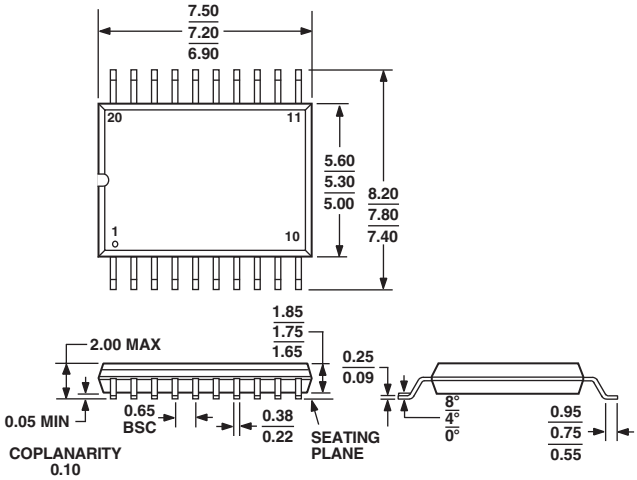


Figure 8. Evaluation Board Layout

OUTLINE DIMENSIONS

20-Lead Shrink Small Outline Package [SSOP]
(RS-20)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-150AE

C00561–0–5/03(D)

Revision History

Location	Page
5/03—Data Sheet changed from REV. C to REV. D.	
Change to SPECIFICATIONS	3
Updated OUTLINE DIMENSIONS	12
9/01—Data Sheet changed from REV. B to REV. C.	
Edit to ABSOLUTE MAXIMUM RATINGS	4