Precision, Very Low Noise, Low Input Bias Current Operational Amplifiers

AD8671/AD8672/AD8674

FEATURES

Very low noise: 2.8 nV/√Hz, 77 nV p-p
Wide bandwidth: 10 MHz
Low input bias current: 12 nA max
Low offset voltage: 75 µV max
High open-loop gain: 120 dB min
Low supply current: 3 mA per amplifier
Dual-supply operation: ±5 V to ±15 V
Unity-gain stable
No phase reversal

APPLICATIONS

PLL filters
Filters for GPS
Instrumentation
Sensors and controls
Professional quality audio

GENERAL DESCRIPTION

The AD8671/AD8672/AD8674 are very high precision amplifiers featuring very low noise, very low offset voltage and drift, low input bias current, 10 MHz bandwidth, and low power consumption. Outputs are stable with capacitive loads of over 1000 pF. Supply current is less than 3 mA per amplifier at 30 V.

The AD8671/AD8672/AD8674's combination of ultralow noise, high precision, speed, and stability is unmatched. The MSOP version of the AD8671/AD8672 requires only half the board space of comparable amplifiers.

Applications for these amplifiers include high quality PLL filters, precision filters, medical and analytical instrumentation, precision power supply controls, ATE, data acquisition, and precision controls as well as professional quality audio.

The AD8671/AD8672/AD8674 are specified over the extended industrial temperature range (–40°C to +125°C).

The AD8671/AD8672 are available in the 8-lead SOIC and 8-lead MSOP packages. The AD8674 is available in 14-lead SOIC and 14-lead TSSOP packages.

Surface-mount devices in MSOP packages are available in tape and reel only.

PIN CONFIGURATIONS

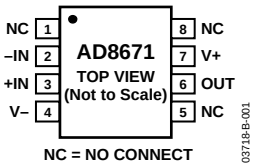


Figure 1. 8-Lead SOIC_N (R-8)

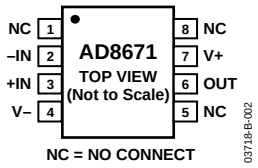


Figure 2. 8-Lead MSOP (RM-8)

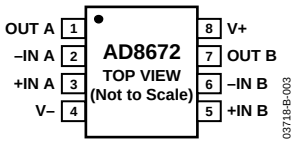


Figure 3. 8-Lead SOIC-N (R-8)

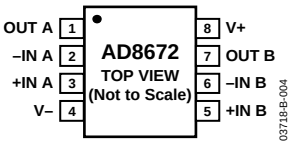


Figure 4. 8-Lead MSOP (RM-8)

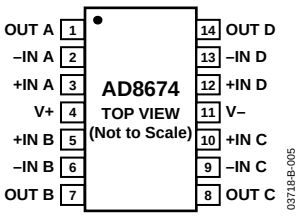


Figure 5. 14-Lead SOIC_N (R-14)

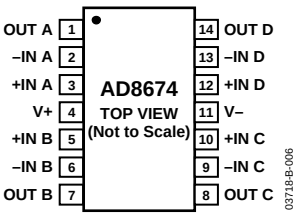


Figure 6. 14-Lead TSSOP (RU-14)

Rev. C

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
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REVISION HISTORY

6/05—Rev. B to Rev. C

Changes to Figure 6 ... 1
Updated Outline Dimensions ... 14
Changes to Ordering Guide ... 16

4/04—Rev. A to Rev. B

Changes to Figure 32 ... 11
Changes to Figures 36, 37, and 38 ... 12

1/04—Rev. 0 to Rev. A

Added AD8672 and AD8674 parts ... Universal
Changes to Specifications ... 3
Deleted Figure 3 ... 6
Changes to Figures 7, 8, and 9 ... 6
Changes to Figure 37 ... 12
Added new Figure 32 ... 10

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS, ±5.0 V

V_S = ±5.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			20	75	μV
		–40°C < T_A < +125°C		30	125	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	–40°C < T_A < +125°C				
AD8671				0.3	0.5	μV/°C
AD8672/AD8674				0.3	0.8	μV/°C
Input Bias Current	I_B		–12	+3	+12	nA
		+25°C < T_A < +125°C	–20	+5	+20	nA
		–40°C < T_A < +125°C	–40	+8	+40	nA
Input Offset Current	I_{OS}		–12	+6	+12	nA
		+25°C < T_A < +125°C	–20	+6	+20	nA
		–40°C < T_A < +125°C	–40	+8	+40	nA
Input Voltage Range			–2.5		+2.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –2.5 V to +2.5 V	100	120		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = –3 V to +3 V	1000	6000		V/mV
Input Capacitance, Common Mode	C_{INCM}			6.25		pF
Input Capacitance, Differential Mode	C_{INDM}			7.5		pF
Input Resistance, Common Mode	R_{IN}			3.5		GΩ
Input Resistance, Differential Mode	R_{INDM}			15		MΩ
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ, –40°C to +125°C	+3.8	+4.0		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ, –40°C to +125°C		–3.9	–3.8	V
Output Voltage High	V_{OH}	R_L = 600 Ω	+3.7	+3.9		V
Output Voltage Low	V_{OL}	R_L = 600 Ω		–3.8	–3.7	V
Output Current	I_{OUT}			±10		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4 V to ±18 V				
AD8671/AD8672			110	130		dB
AD8674			106	115		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		3	3.5	mA
		–40°C < T_A < +125°C			4.2	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		4		V/μs
Settling Time	t_S	To 0.1% (4 V step, G = 1)		1.4		μs
		To 0.01% (4 V step, G = 1)		5.1		μs
Gain Bandwidth Product	GBP			10		MHz
NOISE PERFORMANCE						
Peak-to-Peak Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		77	100	nV p-p
Voltage Noise Density	e_n	f = 1 kHz		2.8	3.8	nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.3		pA/√Hz
Channel Separation						
AD8672/AD8674	C_S	f = 1 kHz		–130		dB
		f = 10 kHz		–105		dB

ELECTRICAL CHARACTERISTICS, ±15 V

V_S = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			20	75	µV
		−40°C < T_A < +125°C		30	125	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C				
AD8671				0.3	0.5	µV/°C
AD8672/AD8674				0.3	0.8	µV/°C
Input Bias Current	I_B		−12	+3	+12	nA
		+25°C < T_A < +125°C	−20	+5	+20	nA
		−40°C < T_A < +125°C	−40	+8	+40	nA
Input Offset Current	I_{OS}		−12	+6	+12	nA
		+25°C < T_A < +125°C	−20	+6	+20	nA
		−40°C < T_A < +125°C	−40	+8	+40	nA
Input Voltage Range			−12		+12	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −12 V to +12 V	100	120		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = −10 V to +10 V	1000	6000		V/mV
Input Capacitance, Common Mode	C_{INCM}			6.25		pF
Input Capacitance, Differential Mode	C_{INDM}			7.5		pF
Input Resistance, Common Mode	R_{IN}			3.5		GΩ
Input Resistance, Differential Mode	R_{INDM}			15		MΩ
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ, −40°C to +125°C	+13.2	+13.8		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ, −40°C to +125°C		−13.8	−13.2	V
Output Voltage High	V_{OH}	R_L = 600 Ω	+11	+12.3		V
Output Voltage Low	V_{OL}	R_L = 600 Ω		−12.4	−11	V
Output Current	I_{OUT}			±20		mA
Short Circuit Current	I_{SC}			±30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4 V to ±18 V				
AD8671/AD8672			110	130		dB
AD8674			106	115		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		3	3.5	mA
		−40°C < T_A < +125°C			4.2	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		4		V/µs
Settling Time	t_S	To 0.1% (10 V step, G = 1)		2.2		µs
		To 0.01% (10 V step, G = 1)		6.3		µs
Gain Bandwidth Product	GBP			10		MHz
NOISE PERFORMANCE						
Peak-to-Peak Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		77	100	nV p-p
Voltage Noise Density	e_n	f = 1 kHz		2.8	3.8	nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.3		pA/√Hz
Channel Separation						
AD8672/AD8674	C_S	f = 1 kHz		−130		dB
		f = 10 kHz		−105		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.[1]

Parameter	Rating
Supply Voltage	36 V
Input Voltage	V_S- to V_S+
Differential Input Voltage	±0.7 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
All Packages	–65°C to +150°C
Operating Temperature Range	
All Packages	–40°C to +125°C
Junction Temperature Range	
All Packages	–65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

[1] Absolute maximum ratings apply at 25°C, unless otherwise noted.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Package Characteristics

Package Type	θ_{JA}[1]	θ_{JC}	Unit
8-Lead MSOP (RM)	190	44	°C/W
8-Lead SOIC_N (R)	158	43	°C/W
14-Lead SOIC_N (R)	120	36	°C/W
14-Lead TSSOP (RU)	180	35	°C/W

[1] θ_{JA} is specified for the worst-case conditions, that is., θ_{JA} is specified for the device soldered in circuit board for surface-mount packages.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TYPICAL PERFORMANCE CHARACTERISTICS

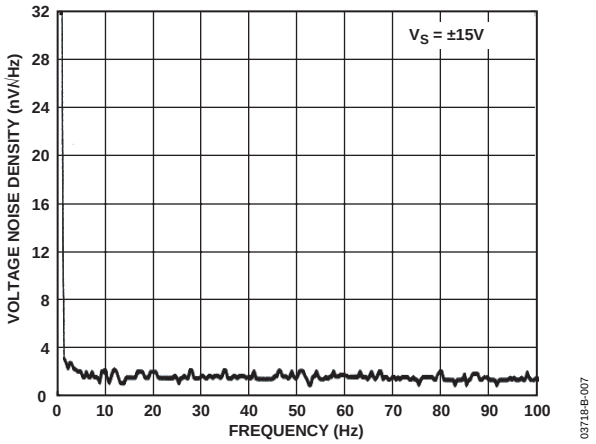


Figure 7. Voltage Noise Density vs. Frequency

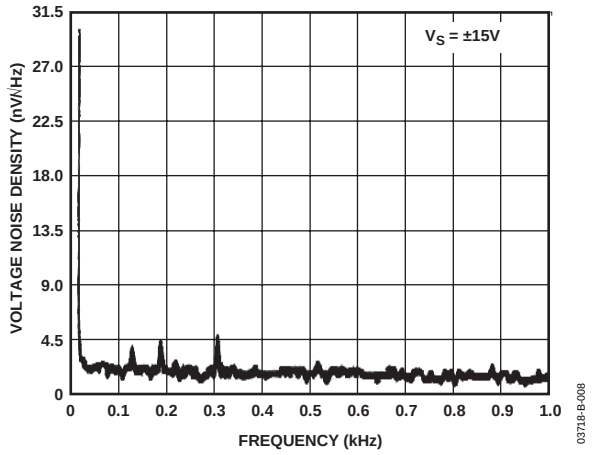


Figure 8. Voltage Noise Density vs. Frequency

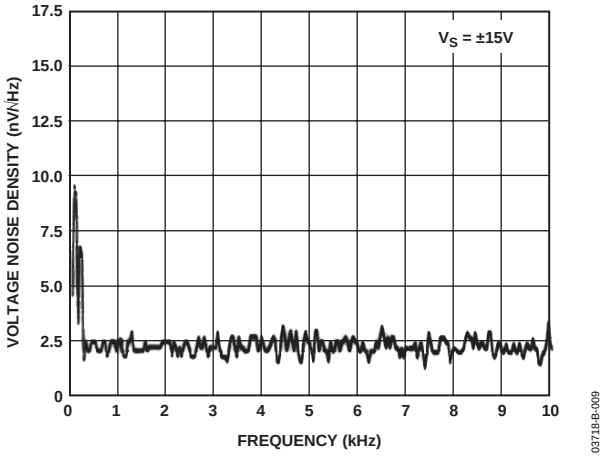


Figure 9. Voltage Noise Density vs. Frequency

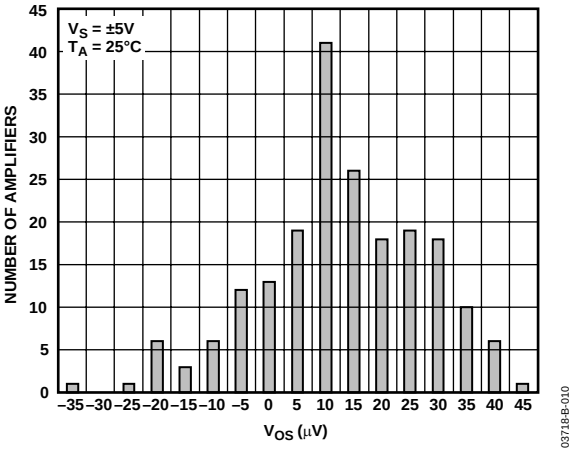


Figure 10. Input Offset Voltage Distribution

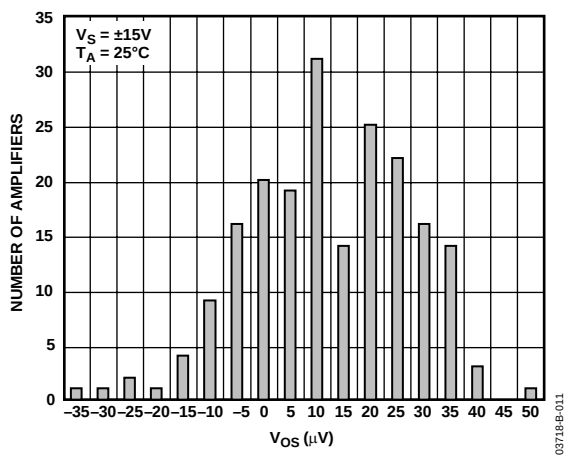


Figure 11. Input Offset Voltage Distribution

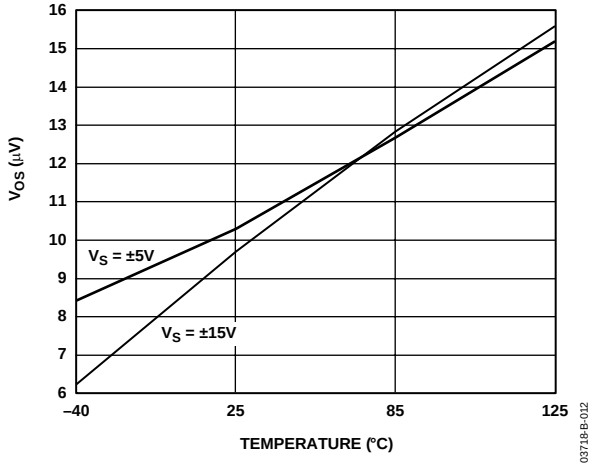


Figure 12. Input Offset Voltage vs. Temperature

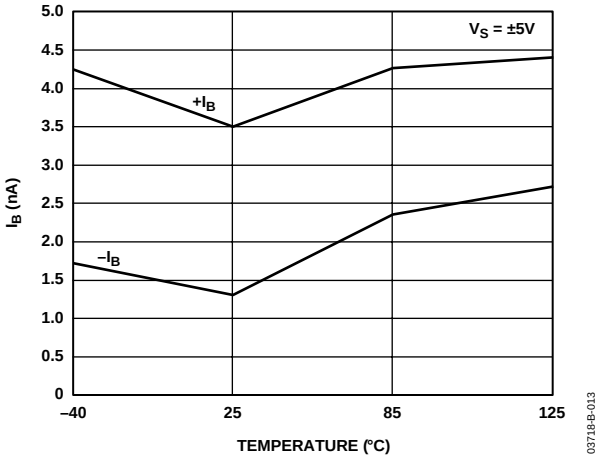


Figure 13. Input Bias Current vs. Temperature

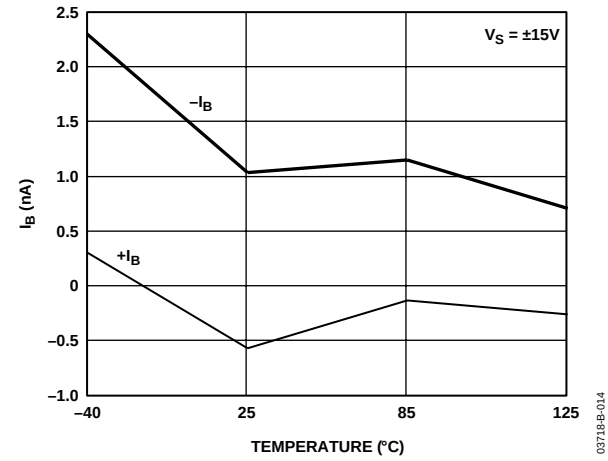


Figure 14. Input Bias Current vs. Temperature

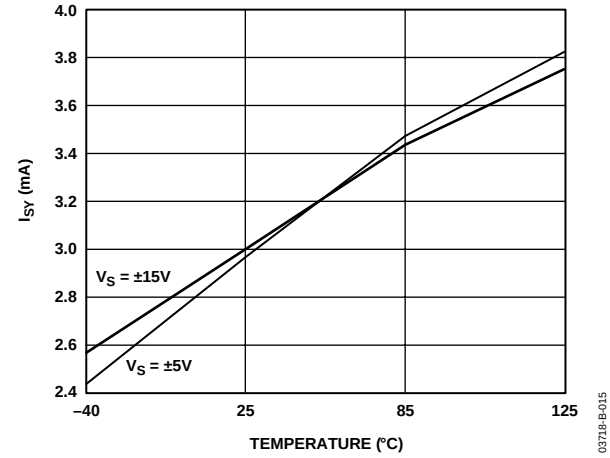


Figure 15. Supply Current vs. Temperature

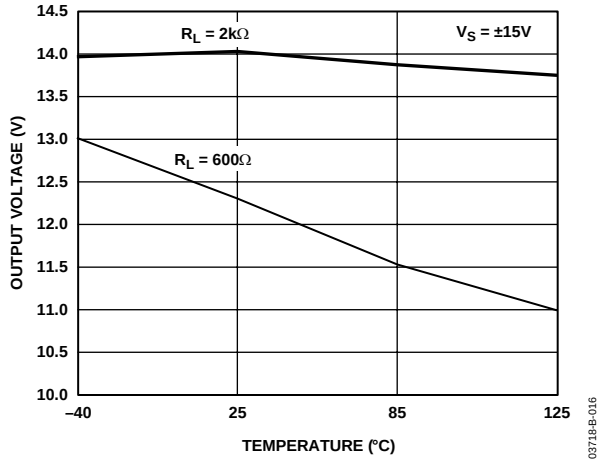


Figure 16. Output Voltage High vs. Temperature

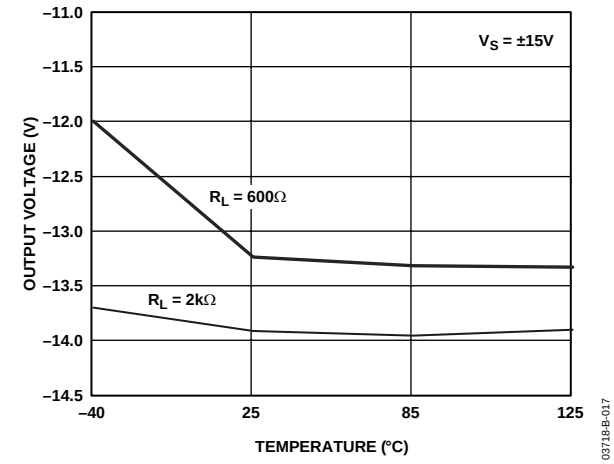


Figure 17. Output Voltage Low vs. Temperature

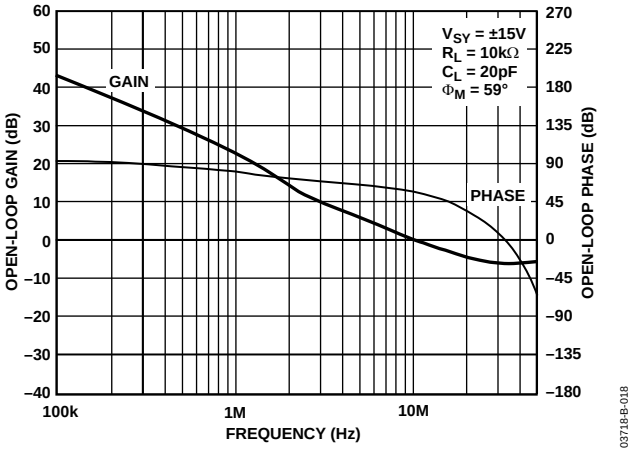


Figure 18. Open-Loop Gain and Phase Shift vs. Frequency

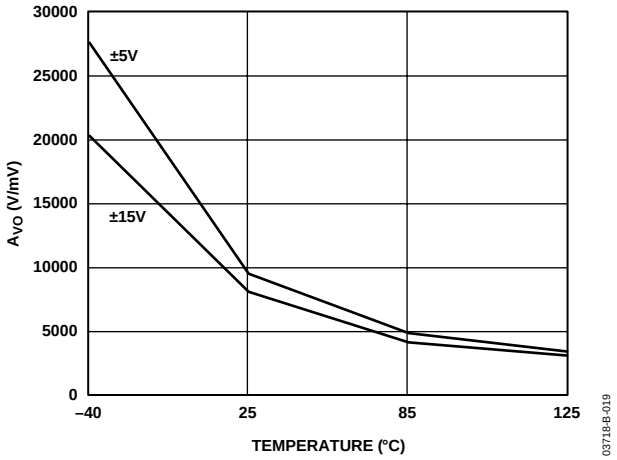


Figure 19. Open-Loop Gain vs. Temperature

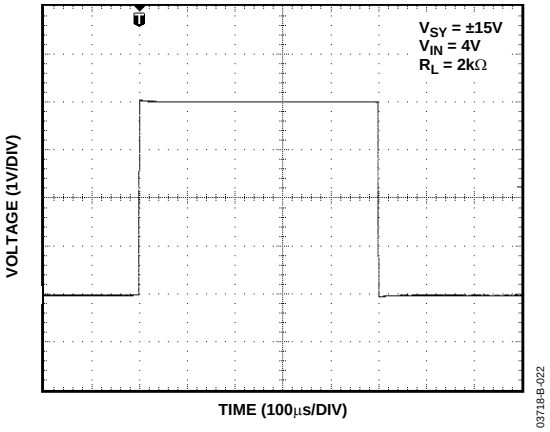


Figure 22. Large Signal Transient Response

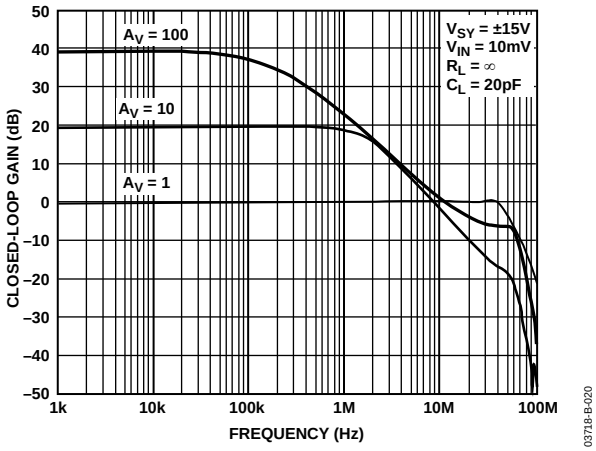


Figure 20. Closed-Loop Gain vs. Frequency

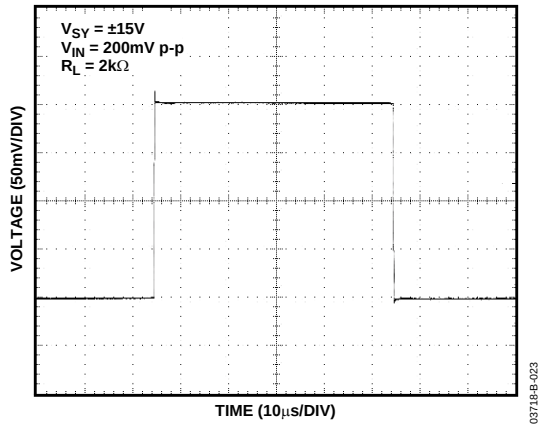


Figure 23. Small Signal Transient Response

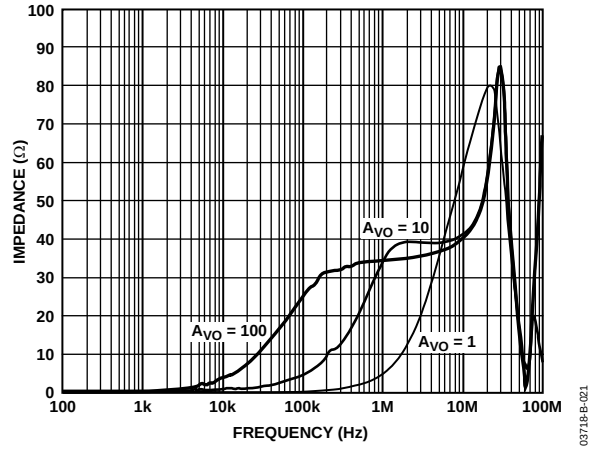


Figure 21. Output Impedance vs. Frequency

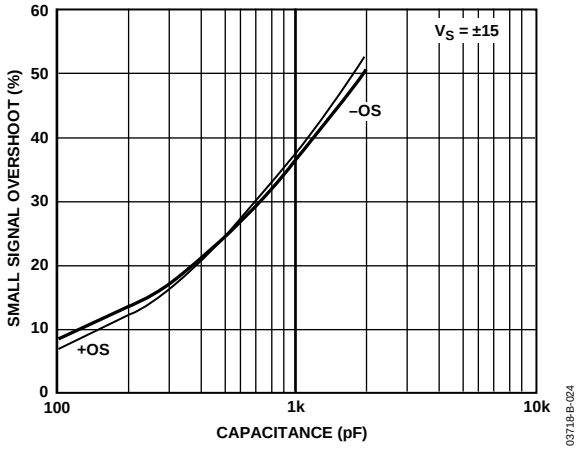


Figure 24. Small Signal Overshoot vs. Load Capacitance

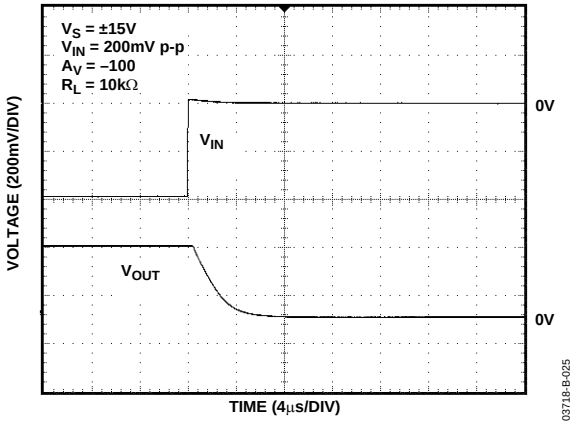


Figure 25. Positive Overdrive Recovery

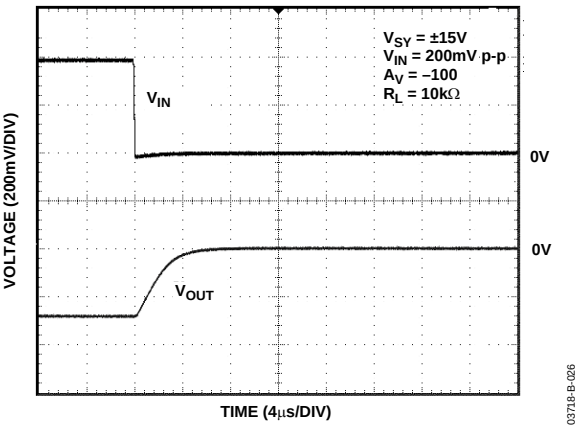


Figure 26. Negative Overdrive Recovery

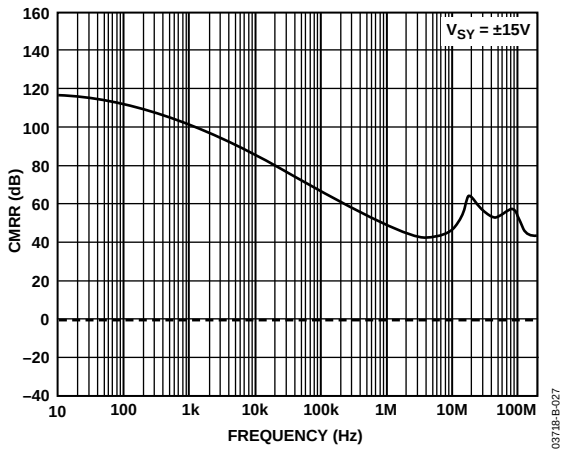


Figure 27. CMRR vs. Frequency

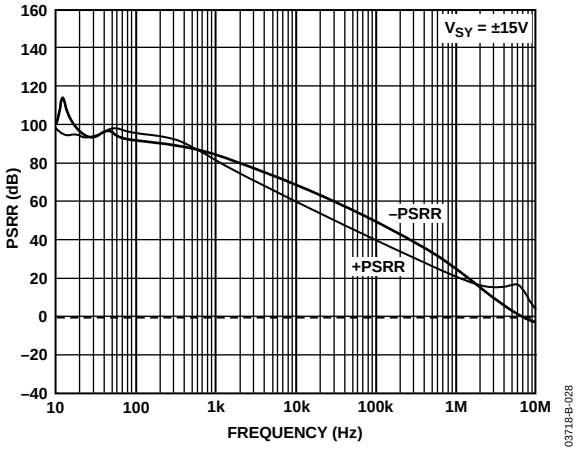


Figure 28. PSRR vs. Frequency

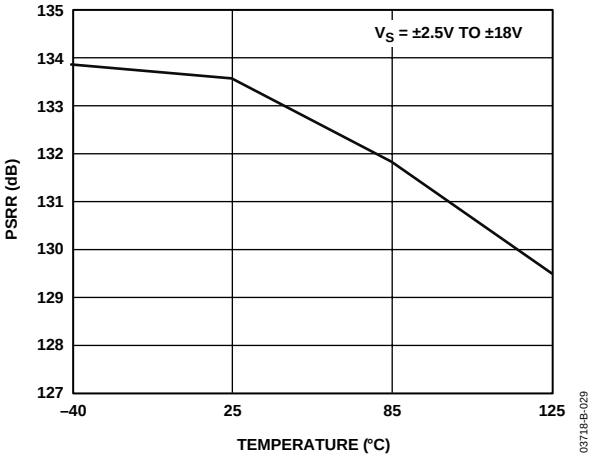


Figure 29. PSRR vs. Temperature

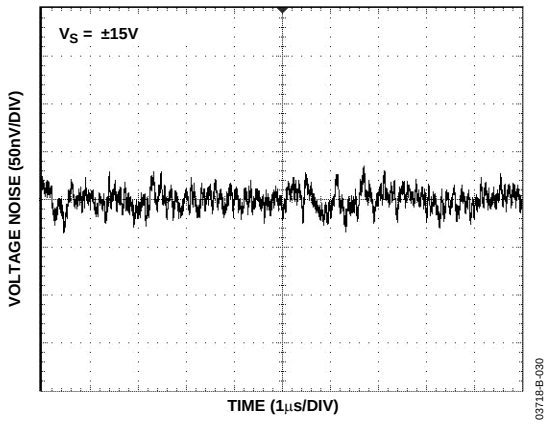


Figure 30. 0.1 Hz to 10 Hz Input Voltage Noise

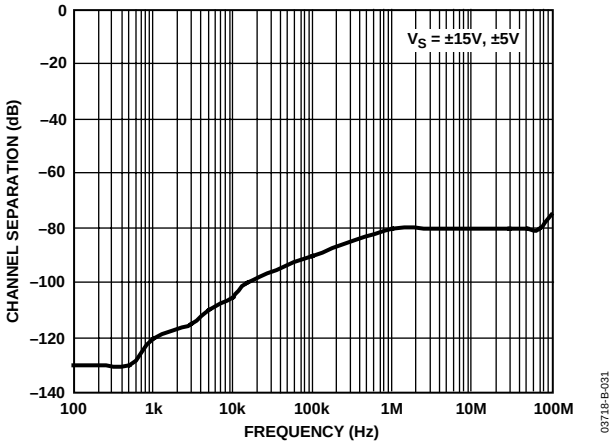


Figure 31. Channel Separation

APPLICATIONS

UNITY-GAIN FOLLOWER APPLICATIONS

When large transient pulses (>1 V) are applied at the positive terminal of amplifiers (such as the OP27, LT1007, OPA227, and AD8671) with back-to-back diodes at the input stage, the use of a resistor in the feedback loop is recommended to avoid having the amplifier load the signal generator. The feedback resistor, R_F, should be at least 500 Ω. However, if large values must be used for R_F, a small capacitor, C_F, should be inserted in parallel with R_F to compensate for the pole introduced by the input capacitance and R_F.

Figure 32 shows the uncompensated output response with a 10 kΩ resistor in the feedback and the compensated response with C_F = 15 pF.

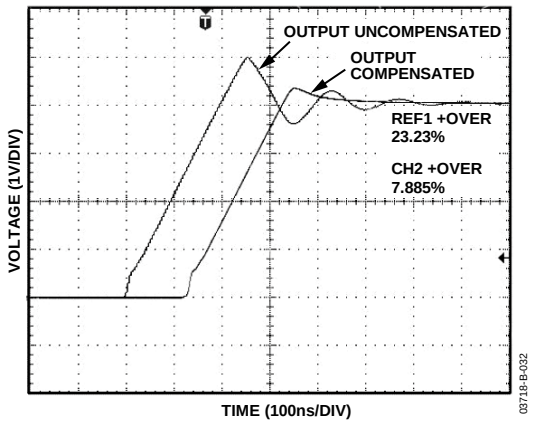


Figure 32. Transient Output Response

OUTPUT PHASE REVERSAL

Phase reversal is a change of polarity in the amplifier transfer function that occurs when the input voltage exceeds the supply voltage. The AD8671/AD8672/AD8674 do not exhibit phase reversal even when the input voltage is 1 V beyond the supplies.

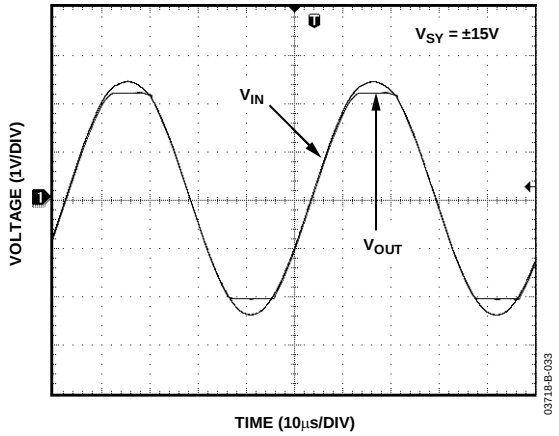


Figure 33. Output Phase Reversal

TOTAL NOISE VS. SOURCE RESISTANCE

The low input voltage noise of the AD8671/AD8672/AD8674 makes them a great choice for applications with low source resistance. However, because they have low input current noise, they can also be used in circuits with substantial source resistance.

Figure 34 shows the voltage noise, current noise, thermal noise, and total rms noise of the AD8671 as a function of the source resistance.

For R_S < 475 Ω, the input voltage noise, e_n, dominates.
For 475 Ω < R_S < 412 kΩ, thermal noise dominates.
For R_S > 412 kΩ, the input current noise dominates.

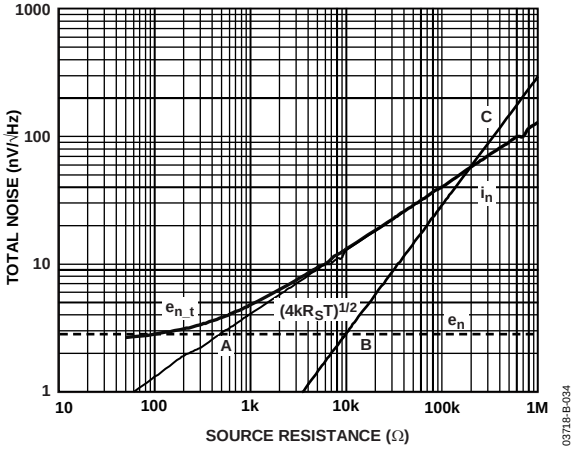


Figure 34. Noise vs. Source Resistance

TOTAL HARMONIC DISTORTION (THD) AND NOISE

The AD8671/AD8672/AD8674 exhibit low total harmonic distortion (THD) over the entire audio frequency range. This makes them suitable for applications with high closed-loop gains, including audio applications. Figure 35 shows approximately 0.0006% of THD + N in a positive unity gain, the worst-case configuration for distortion.

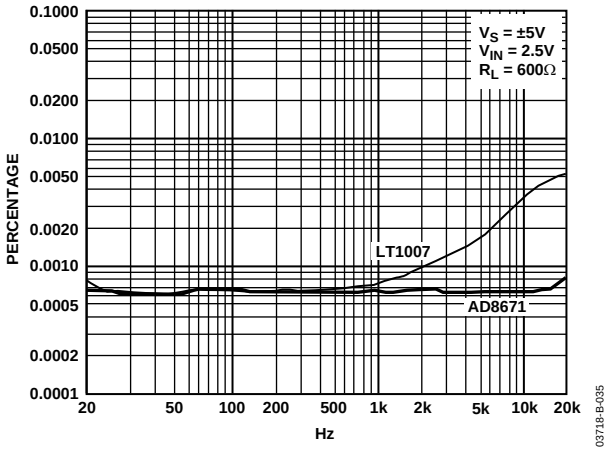


Figure 35. Total Harmonic Distortion and Noise

DRIVING CAPACITIVE LOADS

The AD8671/AD8672/AD8674 can drive large capacitive loads without causing instability. However, when configured in unity gain, driving very large loads can cause unwanted ringing or instability.

Figure 36 shows the output of the AD8671 with a capacitive load of 1 nF. If heavier loads are used in low closed-loop gain or unity-gain configurations, it is recommended to use external compensation as shown in the circuit in Figure 37. This technique reduces the overshoot and prevents the op amp from oscillation. The trade-off of this circuit is a reduction in output swing. However, a great added benefit stems from the fact that the input signal and the op amp's noise are filtered, and thus the overall output noise is kept to a minimum.

The output response of the circuit is shown in Figure 38.

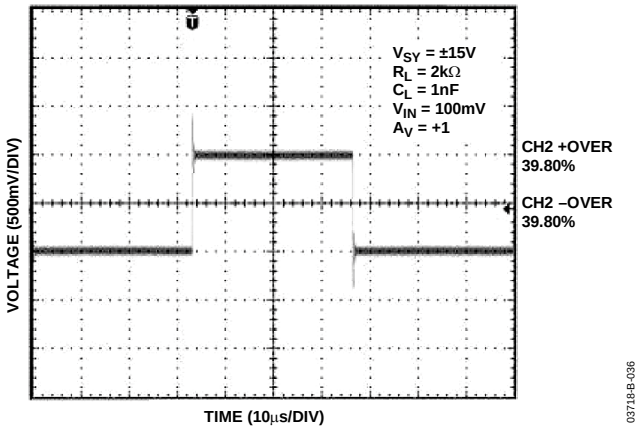


Figure 36. AD8671 Capacitive Load Drive

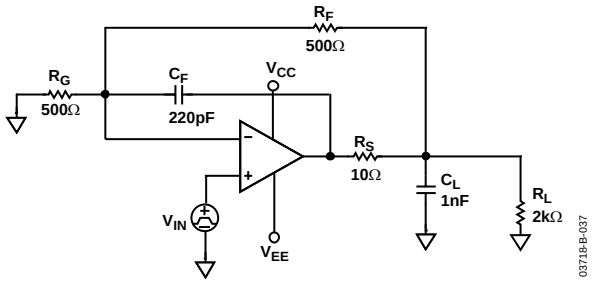


Figure 37. Recommended Capacitive Load Circuit

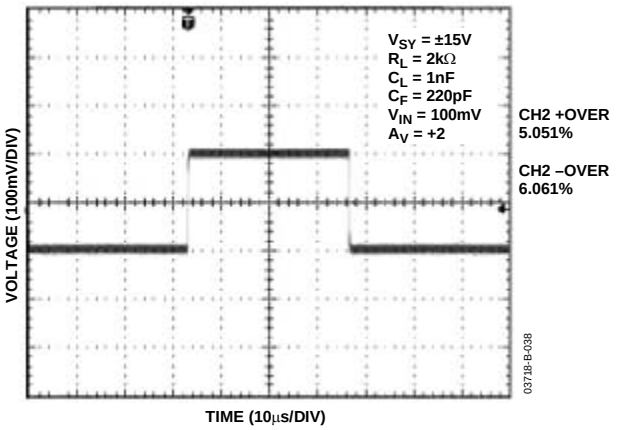


Figure 38. Compensated Load Drive

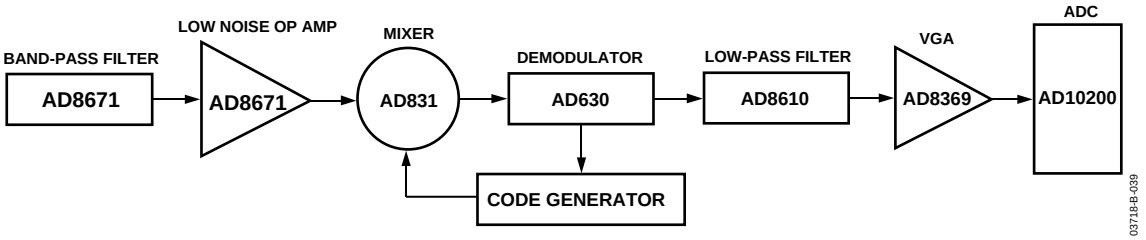


Figure 39. Simplified Block Diagram of a GPS Receiver

GPS RECEIVER

GPS receivers require low noise to minimize RF effects. The precision of the AD8671 makes it an excellent choice for such applications. Its very low noise and wide bandwidth make it suitable for band-pass and low-pass filters without the penalty of high power consumption.

Figure 39 shows a simplified block diagram of a GPS receiver. The next section details the design equations.

BAND-PASS FILTER

Filters are useful in many applications; for example, band-pass filters are used in GPS systems, as discussed in the previous section. Figure 40 shows a second-order band-pass KRC filter.

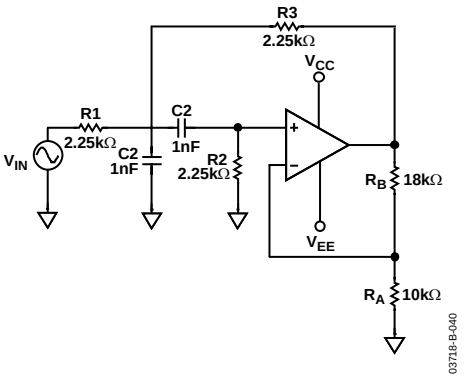


Figure 40. Band-Pass KRC Filter

The equal component topology yields a center frequency

$$fo = \frac{\sqrt{2}}{2\pi RC}$$

$$\text{and } Q = \frac{\sqrt{2}}{4-K}$$

where:

$$K = 1 + \frac{R_B}{R_A}$$

The band-pass response is shown in Figure 41.

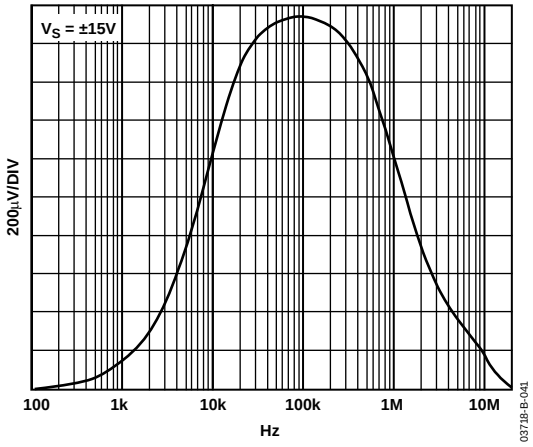


Figure 41. Band-Pass Response

PLL SYNTHESIZERS AND LOOP FILTERS

Phase-lock loop filters are used in AM/FM modulation.

Loop filters in PLL design require accuracy and care in their implementation. The AD8671/AD8672/AD8674 are ideal candidates for such filter design; the low offset voltage and low input bias current minimize the output error. In addition to the excellent dc specifications, the AD8671/AD8672/AD8674 have a unique performance at high frequencies; the high open-loop gain and wide bandwidth allow the user to design a filter with a high closed-loop gain if desirable. To optimize the filter design, it is recommended to use small value resistors to minimize the thermal noise. A simple example is shown in Figure 42.

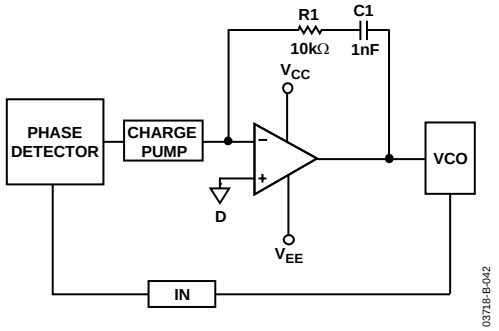
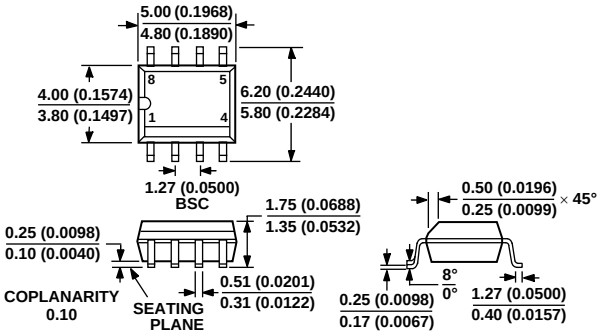


Figure 42. PLL Filter Simplified Block Diagram

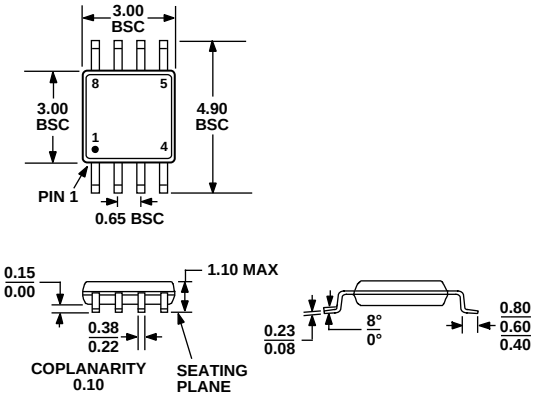
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA

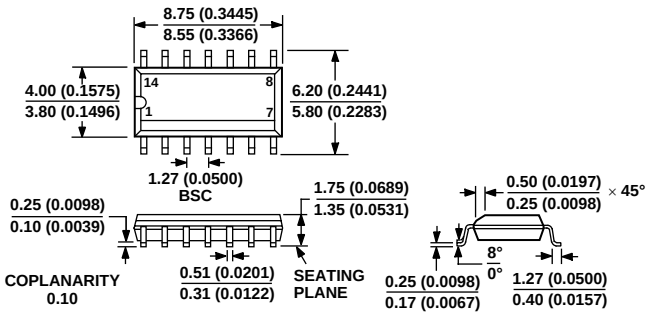
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 43. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



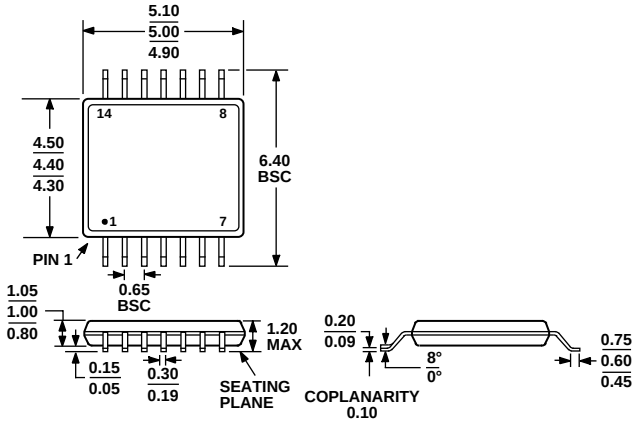
COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 44. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 45. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 46. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8671AR	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8671AR-REEL	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8671AR-REEL7	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8671ARZ[1]	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8671ARZ-REEL[1]	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8671ARZ-REEL7[1]	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8671ARM-R2	–40°C to +125°C	8-Lead MSOP	RM-8	BGA
AD8671ARM-REEL	–40°C to +125°C	8-Lead MSOP	RM-8	BGA
AD8671ARMZ-R2[1]	–40°C to +125°C	8-Lead MSOP	RM-8	A0V
AD8671ARMZ-REEL[1]	–40°C to +125°C	8-Lead MSOP	RM-8	A0V
AD8672AR	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8672AR-REEL	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8672AR-REEL7	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8672ARZ[1]	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8672ARZ-REEL[1]	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8672ARZ-REEL7[1]	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8672ARM-R2	–40°C to +125°C	8-Lead MSOP	RM-8	BHA
AD8672ARM-REEL	–40°C to +125°C	8-Lead MSOP	RM-8	BHA
AD8672ARMZ-R2[1]	–40°C to +125°C	8-Lead MSOP	RM-8	A0W
AD8672ARMZ-REEL[1]	–40°C to +125°C	8-Lead MSOP	RM-8	A0W
AD8674AR	–40°C to +125°C	14-Lead SOIC_N	R-14	
AD8674AR-REEL	–40°C to +125°C	14-Lead SOIC_N	R-14	
AD8674AR-REEL7	–40°C to +125°C	14-Lead SOIC_N	R-14	
AD8674ARZ[1]	–40°C to +125°C	14-Lead SOIC_N	R-14	
AD8674ARZ-REEL[1]	–40°C to +125°C	14-Lead SOIC_N	R-14	
AD8674ARZ-REEL7[1]	–40°C to +125°C	14-Lead SOIC_N	R-14	
AD8674ARU	–40°C to +125°C	14-Lead TSSOP	RU-14	
AD8674ARU-REEL	–40°C to +125°C	14-Lead TSSOP	RU-14	
AD8674ARUZ[1]	–40°C to +125°C	14-Lead TSSOP	RU-14	
AD8674ARUZ-REEL[1]	–40°C to +125°C	14-Lead TSSOP	RU-14	

[1] Z = Pb-free part.

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