50 MHz, Precision, Low Distortion, Low Noise CMOS Amplifiers

AD8651/AD8652

FEATURES

Bandwidth: 50 MHz @ 5 V
Low noise: 4.5 nV/√Hz
Offset voltage: 100 µV typical, specified over entire common-mode range
Slew rate: 41 V/µs
Rail-to-rail input and output swing
Input bias current: 1 pA
Single-supply operation: 2.7 V to 5.5 V
Space-saving MSOP and SOIC_N packaging

APPLICATIONS

Optical communications
Laser source drivers/controllers
Broadband communications
High speed ADCs and DACs
Microwave link interface
Cell phone PA control
Video line drivers
Audio

PIN CONFIGURATIONS

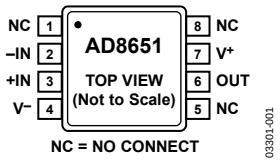


Figure 1. 8-Lead MSOP (RM-8)

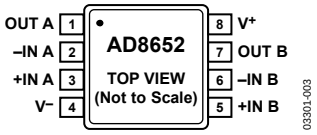


Figure 2. 8-Lead MSOP (RM-8)

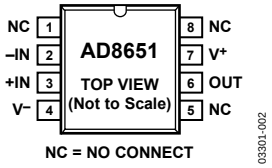


Figure 3. 8-Lead SOIC_N (R-8)

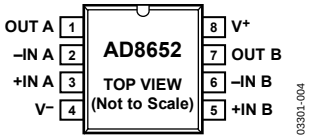


Figure 4. 8-Lead SOIC_N (R-8)

GENERAL DESCRIPTION

The AD865x family consists of high precision, low noise, low distortion, rail-to-rail CMOS operational amplifiers that run from a single-supply voltage of 2.7 V to 5.5 V.

The AD865x family is made up of rail-to-rail input and output amplifiers with a gain bandwidth of 50 MHz and a typical voltage offset of 100 µV across common mode from a 5 V supply. It also features low noise—4.5 nV/√Hz.

The AD865x family can be used in communications applications, such as cell phone transmission power control, fiber optic networking, wireless networking, and video line drivers.

The AD865x family features the newest generation of DigiTrim® in-package trimming. This new generation measures and corrects the offset over the entire input common-mode range, providing less distortion from V_{OS} variation than is typical of other rail-to-rail amplifiers. Offset voltage and CMRR are both specified and guaranteed over the entire common-mode range as well as over the extended industrial temperature range.

The AD865x family is offered in the narrow 8-lead SOIC package and the 8-lead MSOP package. The amplifiers are specified over the extended industrial temperature range (−40°C to +125°C).

Rev. C
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9/04—Rev. A to Rev. B

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10/03 Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V^+ = 2.7 V, V^- = 0 V, V_{CM} = V^+/2, T_A = 25°C, unless otherwise specified.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
AD8651		0 V ≤ V_{CM} ≤ 2.7 V		100	350	µV
		−40°C ≤ T_A ≤ +85°C, 0 V ≤ V_{CM} ≤ 2.7 V			1.4	mV
		−40°C ≤ T_A ≤ +125°C, 0 V ≤ V_{CM} ≤ 2.7 V			1.6	mV
AD8652		0 V ≤ V_{CM} ≤ 2.7 V		90	300	µV
		−40°C ≤ T_A ≤ +125°C, 0 V ≤ V_{CM} ≤ 2.7 V		0.4	1.3	mV
Offset Voltage Drift	TCV_{OS}			4		µV/°C
Input Bias Current	I_B			1	10	pA
		−40°C ≤ T_A ≤ +125°C			600	pA
Input Offset Current	I_{OS}			1	10	pA
		−40°C ≤ T_A ≤ +85°C			30	pA
		−40°C ≤ T_A ≤ +125°C			600	pA
Input Voltage Range	V_{CM}		−0.1		+2.8	V
Common-Mode Rejection Ratio	CMRR					
AD8651		V^+ = 2.7 V, −0.1 V < V_{CM} < +2.8 V	75	95		dB
		−40°C ≤ T_A ≤ +85°C, −0.1 V < V_{CM} < +2.8 V	70	88		dB
		−40°C ≤ T_A ≤ +125°C, −0.1 V < V_{CM} < +2.8 V	65	85		dB
AD8652		V^+ = 2.7 V, −0.1 V < V_{CM} < +2.8 V	77	95		dB
		−40°C ≤ T_A ≤ +125°C, −0.1 V < V_{CM} < +2.8 V	73	90		dB
Large Signal Voltage Gain	A_{VO}	R_L = 1 kΩ, 200 mV < V_O < 2.5 V	100	115		dB
		R_L = 1 kΩ, 200 mV < V_O < 2.5 V, T_A = 85°C	100	114		dB
		R_L = 1 kΩ, 200 mV < V_O < 2.5 V, T_A = 125°C	95	108		dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 250 µA, −40°C ≤ T_A ≤ +125°C	2.67			V
Output Voltage Low	V_{OL}	I_L = 250 µA, −40°C ≤ T_A ≤ +125°C			30	mV
Short-Circuit Limit	I_{SC}	Sourcing		80		mA
		Sinking		80		mA
Output Current	I_O			40		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 5.5 V, V_{CM} = 0 V	76	94		dB
		−40°C ≤ T_A ≤ +125°C	74	93		dB
Supply Current	I_{SY}					
AD8651		I_O = 0		9	12	mA
		−40°C ≤ T_A ≤ +125°C			14.5	mA
AD8652		I_O = 0		17.5	19.5	mA
		−40°C ≤ T_A ≤ +125°C			22.5	mA
INPUT CAPACITANCE	C_{IN}					
Differential				6		pF
Common Mode				9		pF
DYNAMIC PERFORMANCE						
Slew Rate	SR	G = 1, R_L = 10 kΩ		41		V/µs
Gain Bandwidth Product	GBP	G = 1		50		MHz
Settling Time, 0.01%		G = ±1, 2 V step		0.2		µs
Overload Recovery Time		V_{IN} × G = 1.48 V^+		0.1		µs
Total Harmonic Distortion + Noise	THD + N	G = 1, R_L = 600 Ω, f = 1 kHz, V_{IN} = 2 V p-p		0.0006		%
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 10 kHz		5		nV/√Hz
		f = 100 kHz		4.5		nV/√Hz
Current Noise Density	i_n	f = 10 kHz		4		fA/√Hz

V^+ = 5 V, V^- = 0 V, V_{CM} = V^+/2, T_A = 25°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
AD8651		0 V ≤ V_{CM} ≤ 5 V		100	350	µV
		–40°C ≤ T_A ≤ +85°C, 0 V ≤ V_{CM} ≤ 5 V			1.4	mV
		–40°C ≤ T_A ≤ +125°C, 0 V ≤ V_{CM} ≤ 5 V			1.7	mV
AD8652		0 V ≤ V_{CM} ≤ 5 V		90	300	µV
		–40°C ≤ T_A ≤ +125°C, 0 V ≤ V_{CM} ≤ 5 V		0.4	1.4	mV
Offset Voltage Drift	TCV_{OS}			4		µV/°C
Input Bias Current	I_B			1	10	pA
		–40°C ≤ T_A ≤ +85°C			30	pA
		–40°C ≤ T_A ≤ +125°C			600	pA
Input Offset Current	I_{OS}			1	10	pA
		–40°C ≤ T_A ≤ +85°C			30	pA
		–40°C ≤ T_A ≤ +125°C			600	pA
Input Voltage Range	V_{CM}		–0.1		+5.1	V
Common-Mode Rejection Ratio	CMRR					
AD8651		0.1 V < V_{CM} < 5.1 V	80	95		dB
		–40°C ≤ T_A ≤ +85°C, 0.1 V < V_{CM} < 5.1 V	75	94		dB
		–40°C ≤ T_A ≤ +125°C, 0.1 V < V_{CM} < 5.1 V	70	90		dB
AD8652		0.1 V < V_{CM} < 5.1 V	84	100		dB
		–40°C ≤ T_A ≤ +125°C, 0.1 V < V_{CM} < 5.1 V	76	95		dB
Large Signal Voltage Gain	A_{VO}	R_L = 1 kΩ, 200 mV < V_O < 4.8 V	100	115		dB
		R_L = 1 kΩ, 200 mV < V_O < 4.8 V, T_A = 85°C	98	114		dB
		R_L = 1 kΩ, 200 mV < V_O < 4.8 V, T_A = 125°C	95	111		dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 250 µA, –40°C ≤ T_A ≤ +125°C	4.97			V
Output Voltage Low	V_{OL}	I_L = 250 µA, –40°C ≤ T_A ≤ +125°C			30	mV
Short-Circuit Limit	I_{SC}	Sourcing		80		mA
		Sinking		80		mA
Output Current	I_O			40		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 5.5 V, V_{CM} = 0 V	76	94		dB
		–40°C ≤ T_A ≤ +125°C	74	93		dB
Supply Current	I_{SY}					
AD8651		I_O = 0		9.5	14.0	mA
		–40°C ≤ T_A ≤ +125°C			15	mA
AD8652		I_O = 0		17.5	20.0	mA
		–40°C ≤ T_A ≤ +125°C			23.5	mA
INPUT CAPACITANCE	C_{IN}					
Differential				6		pF
Common Mode				9		pF
DYNAMIC PERFORMANCE						
Slew Rate	SR	G = 1, R_L = 10 kΩ		41		V/µs
Gain Bandwidth Product	GBP	G = 1		50		MHz
Settling Time, 0.01%		G = ±1, 2 V step		0.2		µs
Overload Recovery Time		V_{IN} × G = 1.2 V^+		0.1		µs
Total Harmonic Distortion + Noise	THD + N	G = 1, R_L = 600 Ω, f = 1 kHz, V_{IN} = 2 V p-p		0.0006		%
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 10 kHz		5		nV/√Hz
		f = 100 kHz		4.5		nV/√Hz
Current Noise Density	i_n	f = 10 kHz		4		fA/√Hz

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
Supply Voltage	6.0 V
Input Voltage	GND to V_S + 0.3 V
Differential Input Voltage	±6.0 V
Output Short-Circuit Duration to GND	Indefinite
Electrostatic Discharge (HBM)	4000 V
Storage Temperature Range	
RM, R Package	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	
RM, R Package	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

JA is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP (RM)	210	45	°C/W
8-Lead SOIC_N (R)	158	43	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TYPICAL PERFORMANCE CHARACTERISTICS

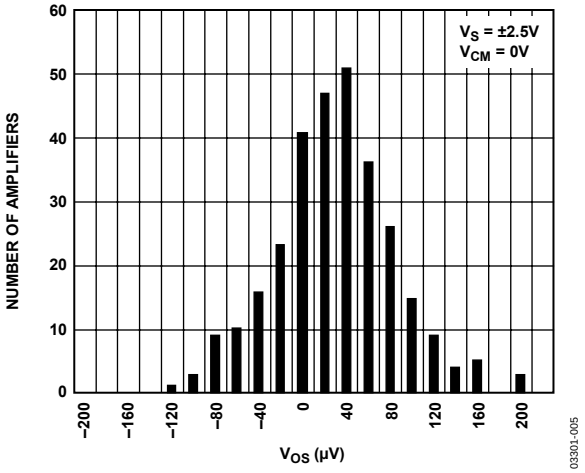


Figure 5. Input Offset Voltage Distribution

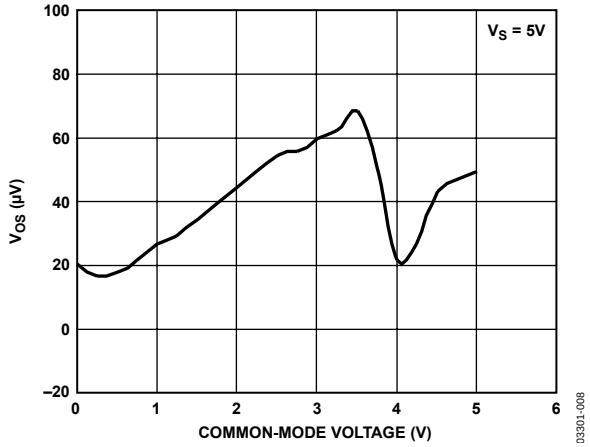


Figure 8. Input Offset Voltage vs. Common-Mode Voltage

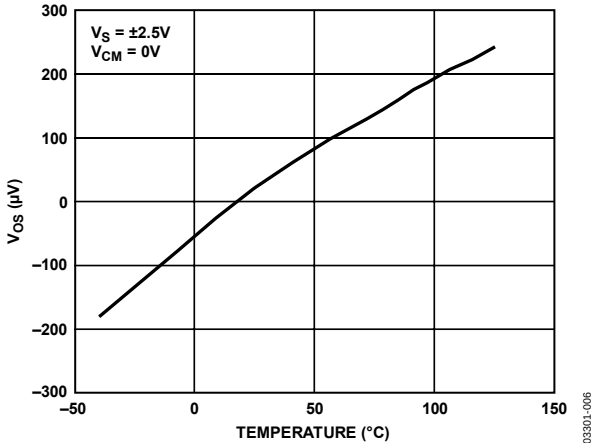


Figure 6. Input Offset Voltage vs. Temperature

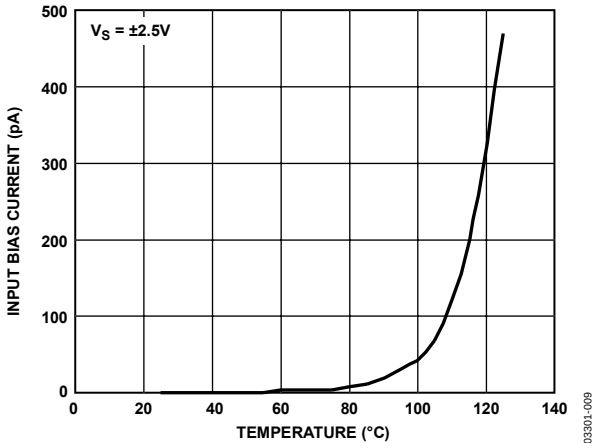


Figure 9. Input Bias Current vs. Temperature

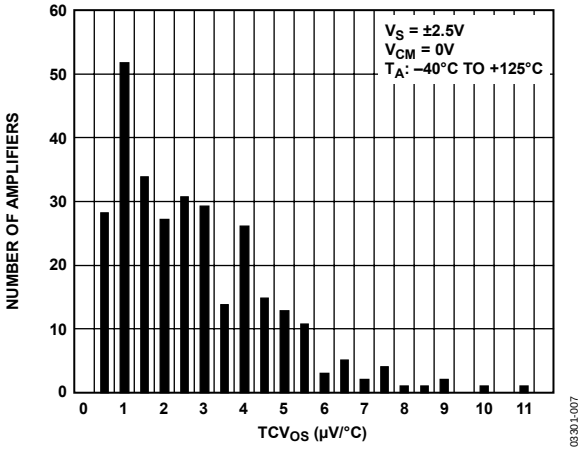


Figure 7. TCV_{OS} Distribution

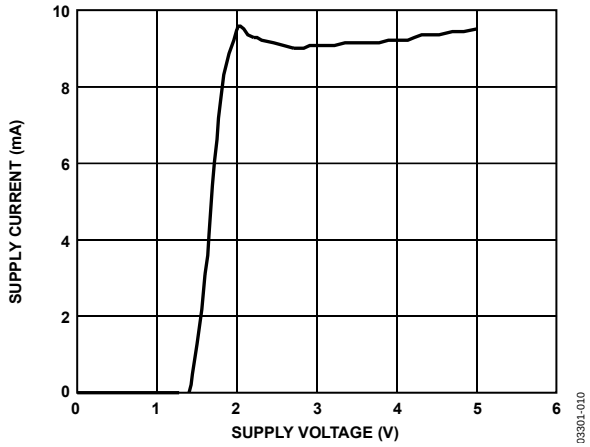


Figure 10. Supply Current vs. Supply Voltage

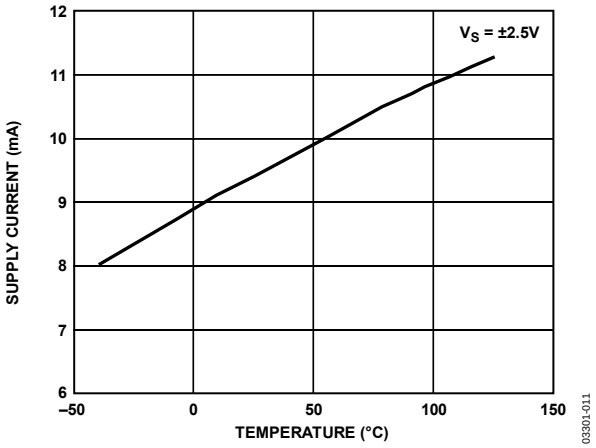


Figure 11. Supply Current vs. Temperature

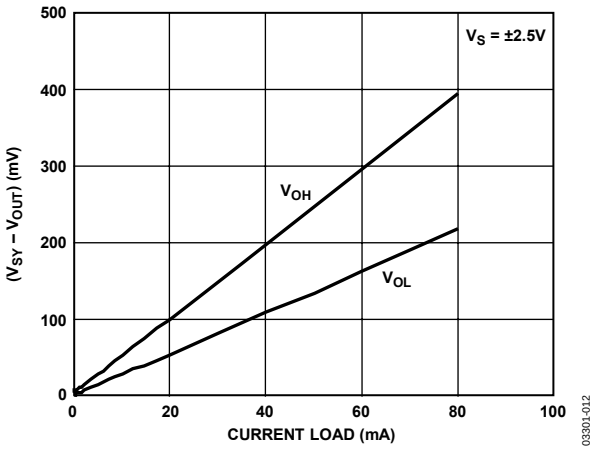


Figure 12. Output Voltage to Supply Rail vs. Load Current

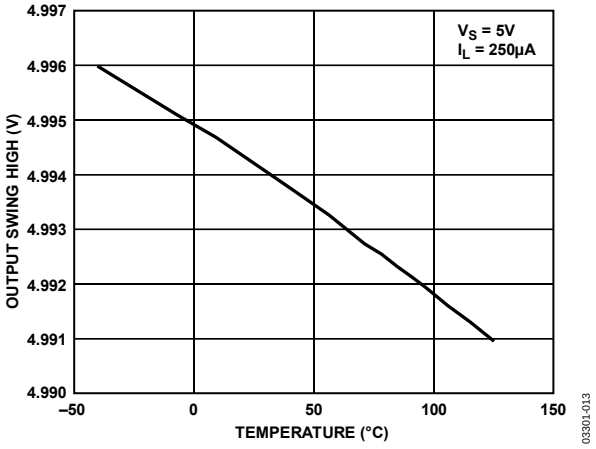


Figure 13. Output Voltage Swing High vs. Temperature

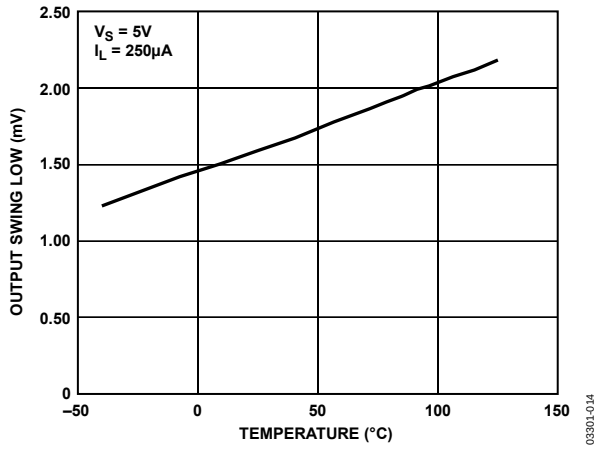


Figure 14. Output Voltage Swing Low vs. Temperature

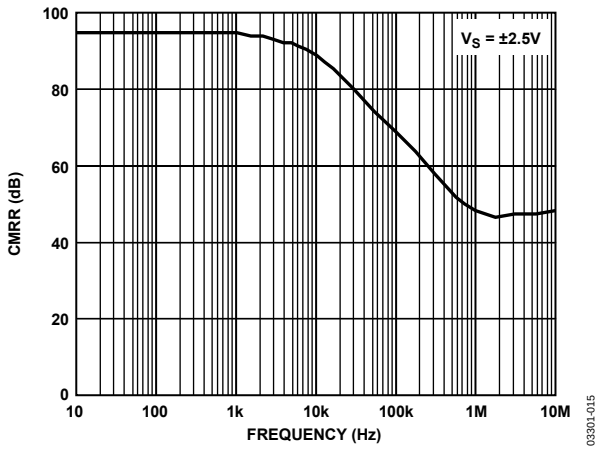


Figure 15. CMRR vs. Frequency

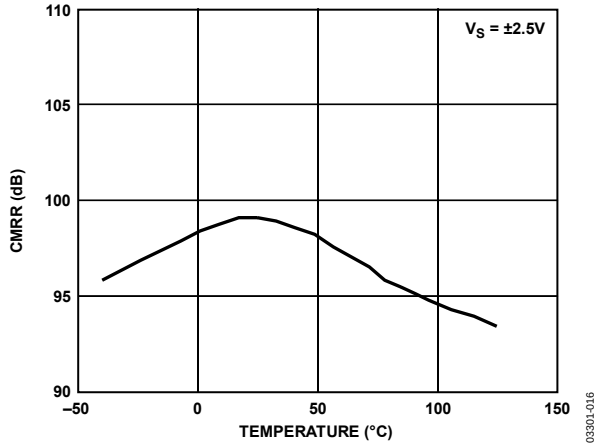


Figure 16. CMRR vs. Temperature

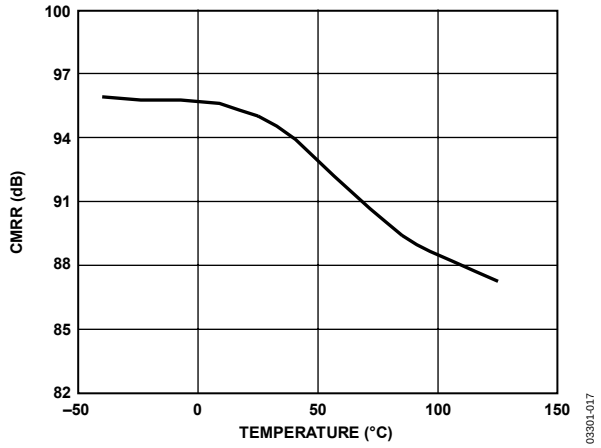


Figure 17. CMRR vs. Temperature

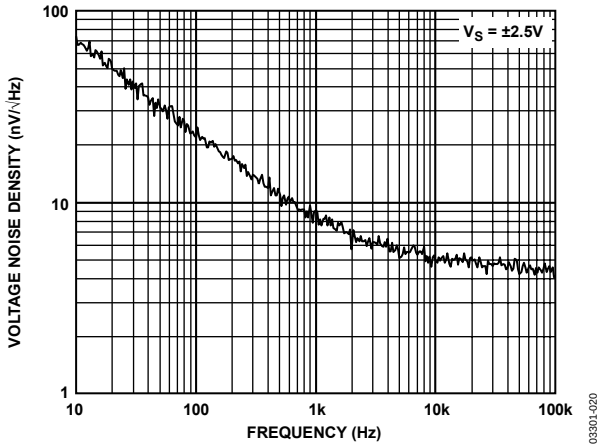


Figure 20. Voltage Noise Density vs. Frequency

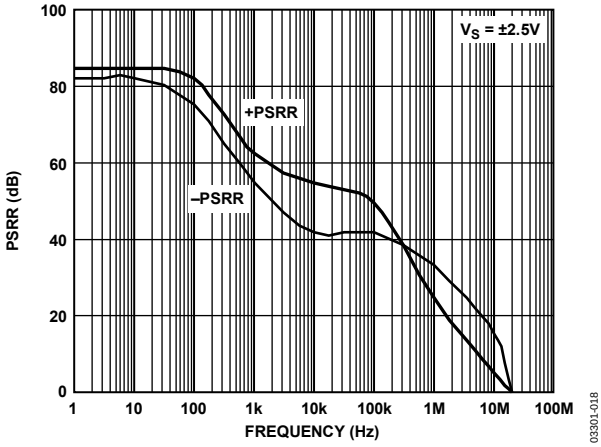


Figure 18. PSRR vs. Frequency

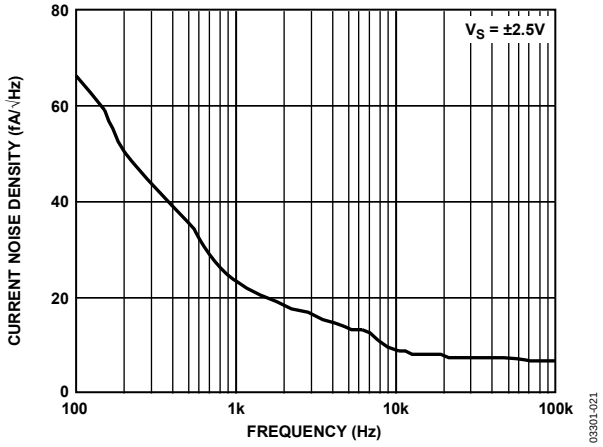


Figure 21. Current Noise Density vs. Frequency

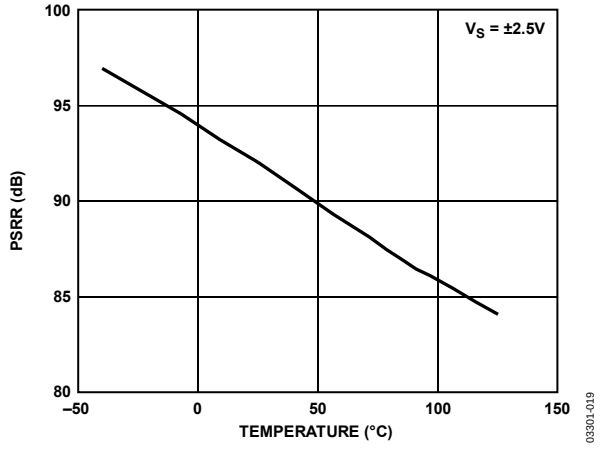


Figure 19. PSRR vs. Temperature

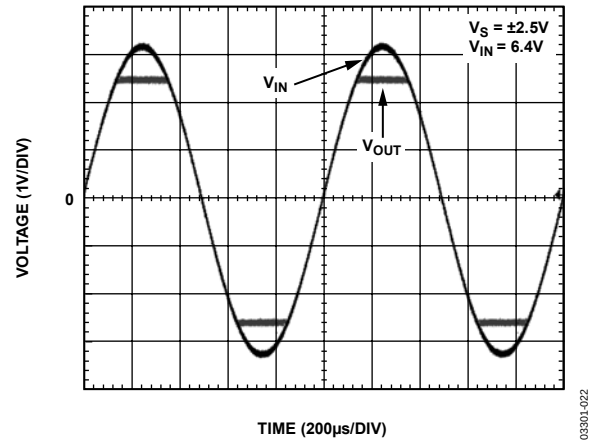


Figure 22. No Phase Reversal

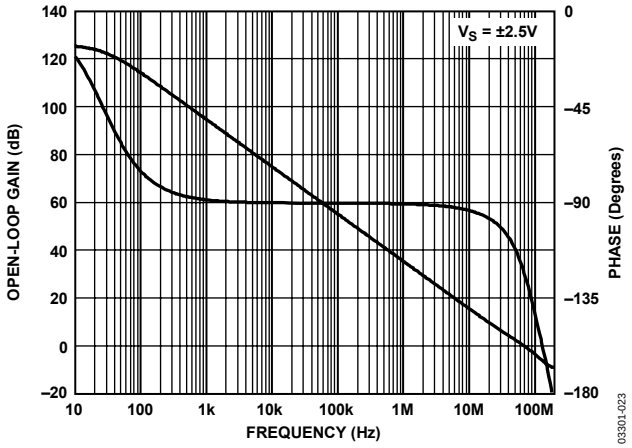


Figure 23. Open-Loop Gain and Phase vs. Frequency

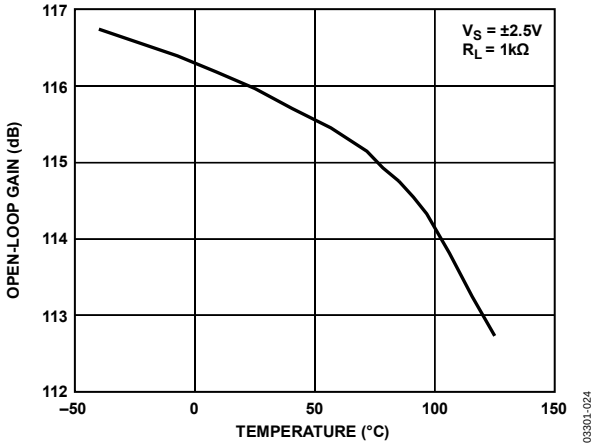


Figure 24. Open-Loop Gain vs. Temperature

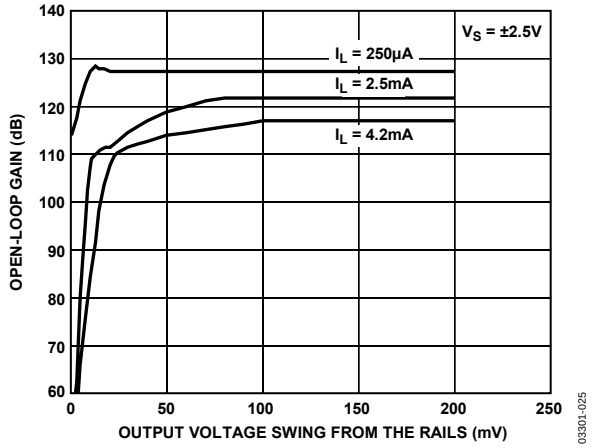


Figure 25. Open-Loop Gain vs. Output Voltage Swing

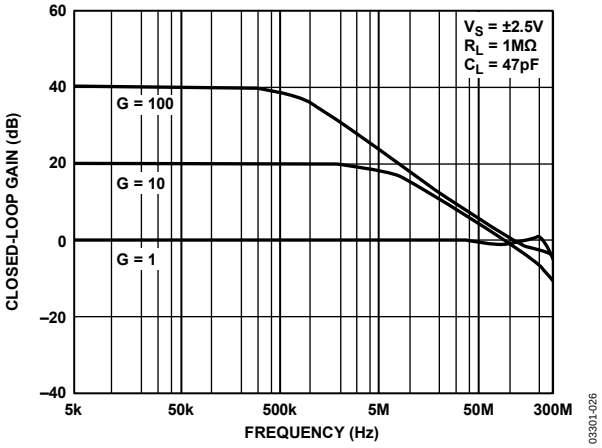


Figure 26. Closed-Loop Gain vs. Frequency

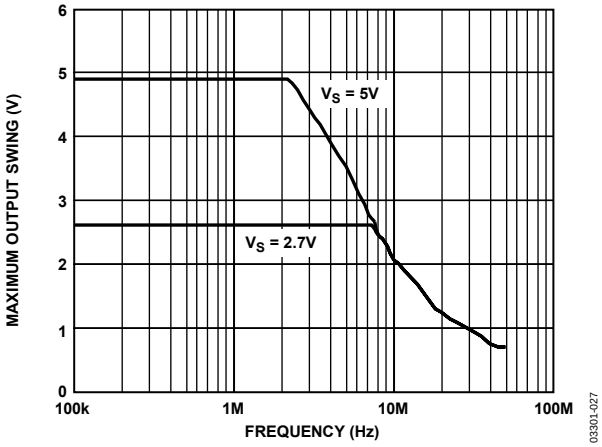


Figure 27. Maximum Output Swing vs. Frequency

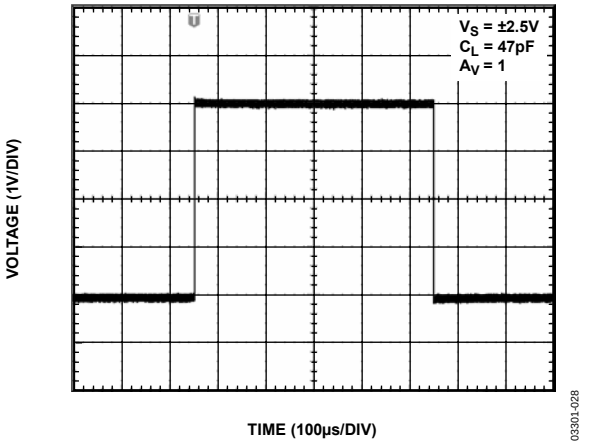


Figure 28. Large Signal Response

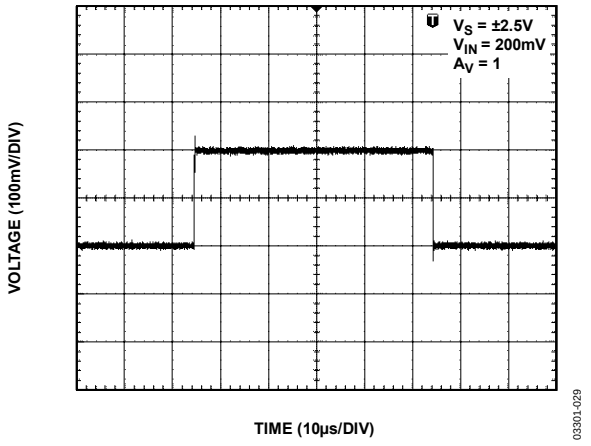


Figure 29. Small Signal Response

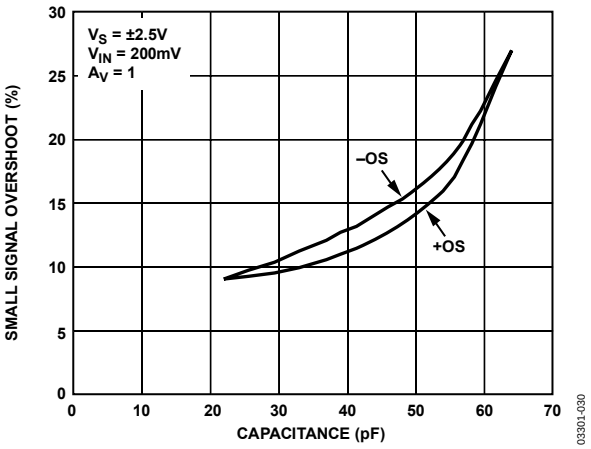


Figure 30. Small Signal Overshoot vs. Load Capacitance

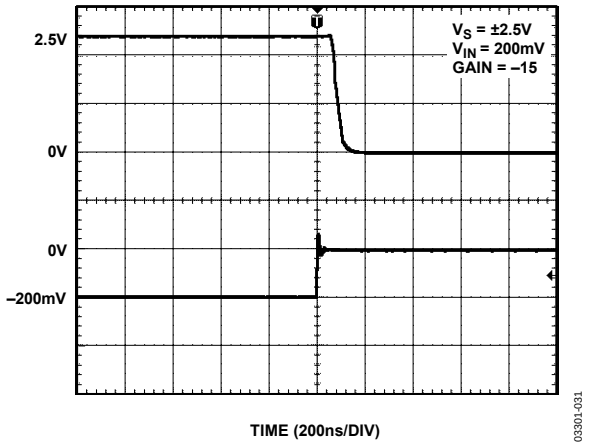


Figure 31. Negative Overload Recovery Time

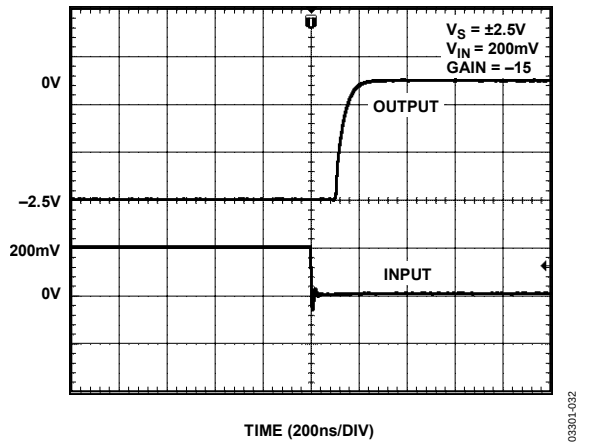


Figure 32. Positive Overload Recovery Time

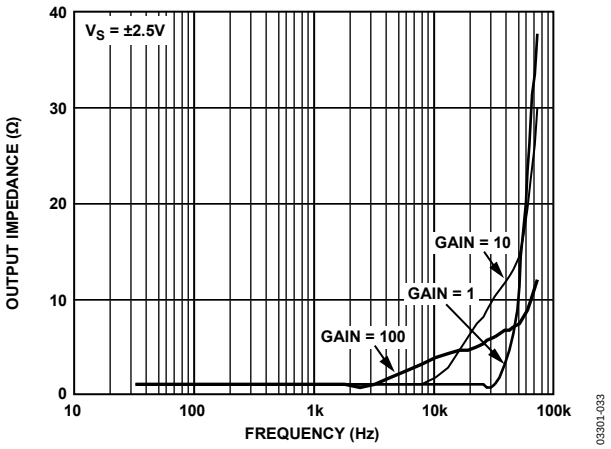


Figure 33. Output Impedance vs. Frequency

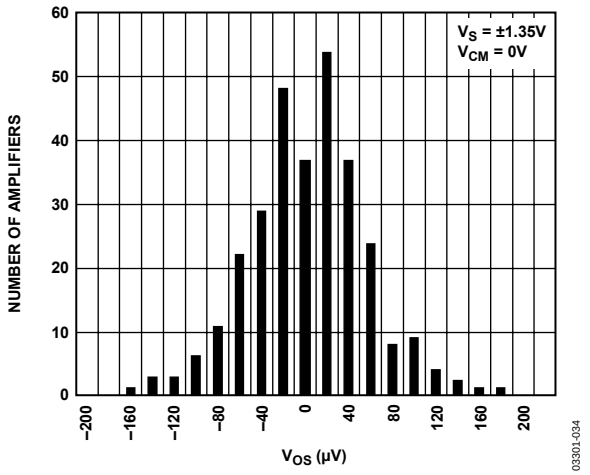


Figure 34. Input Offset Voltage Distribution

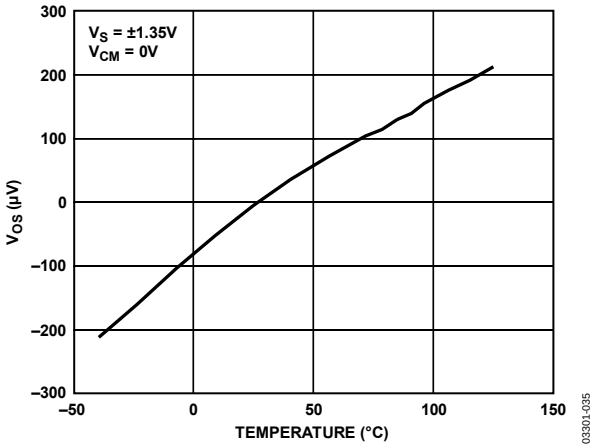


Figure 35. Input Offset Voltage vs. Temperature

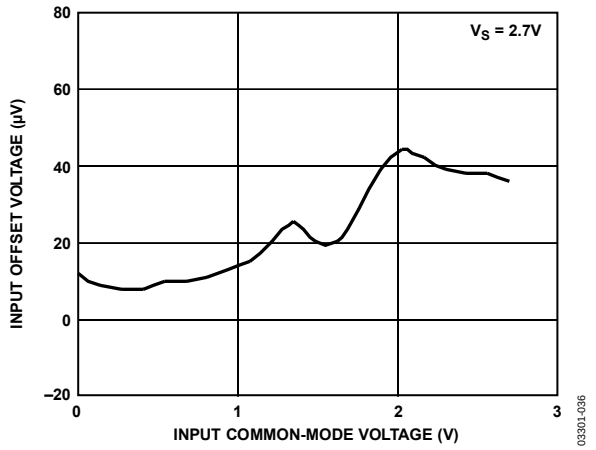


Figure 36. Input Offset Voltage vs. Common-Mode Voltage

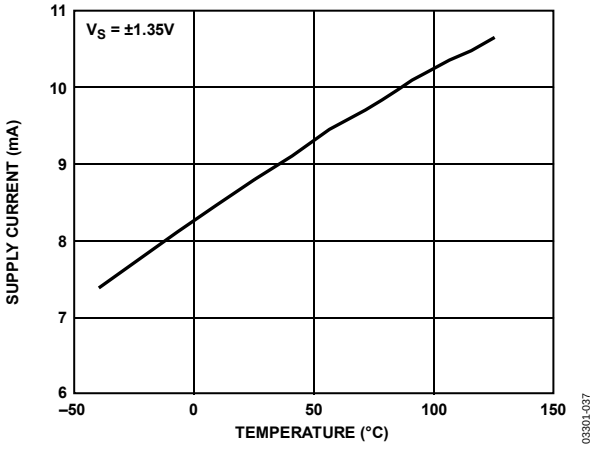


Figure 37. Supply Current vs. Temperature

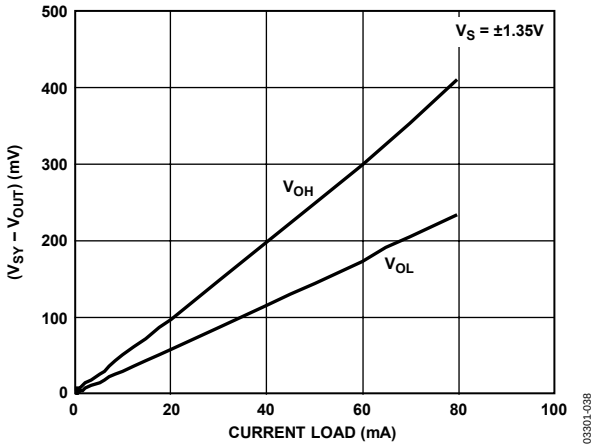


Figure 38. Output Voltage to Supply Rail vs. Load Current

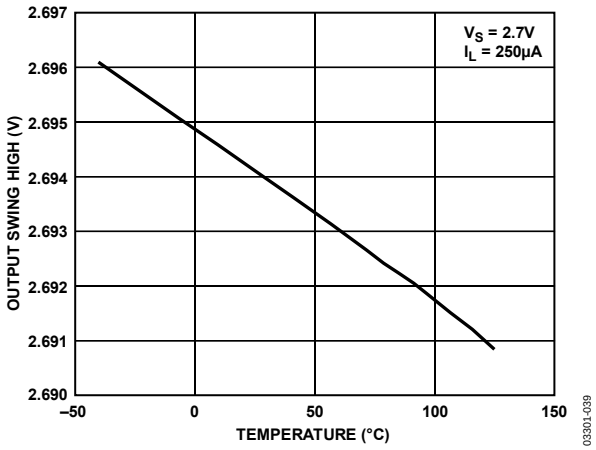


Figure 39. Output Voltage Swing High vs. Temperature

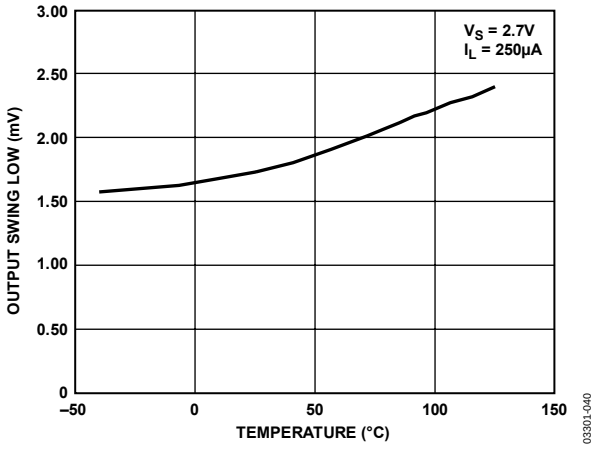


Figure 40. Output Voltage Swing Low vs. Temperature

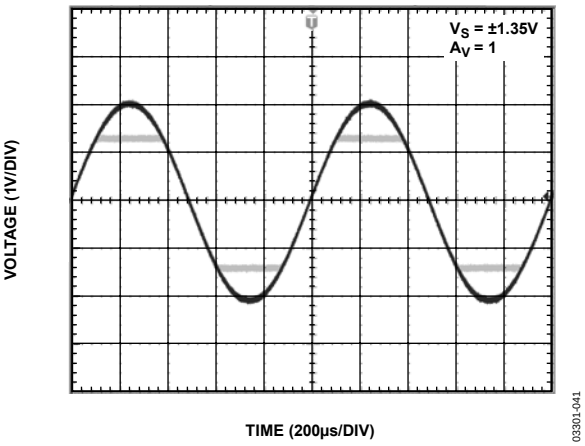


Figure 41. No Phase Reversal

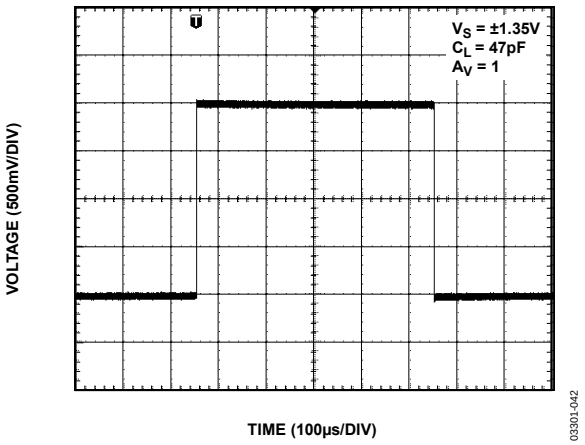


Figure 42. Large Signal Response

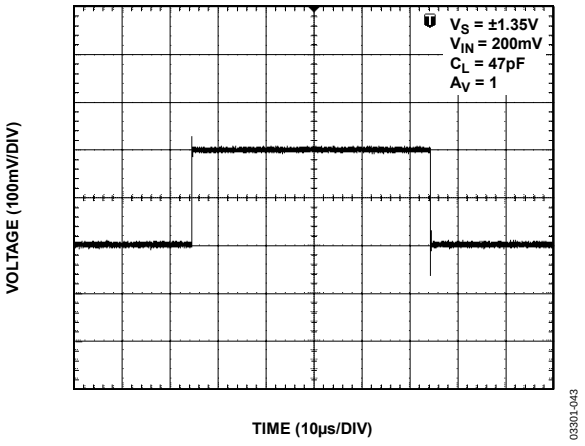


Figure 43. Small Signal Response

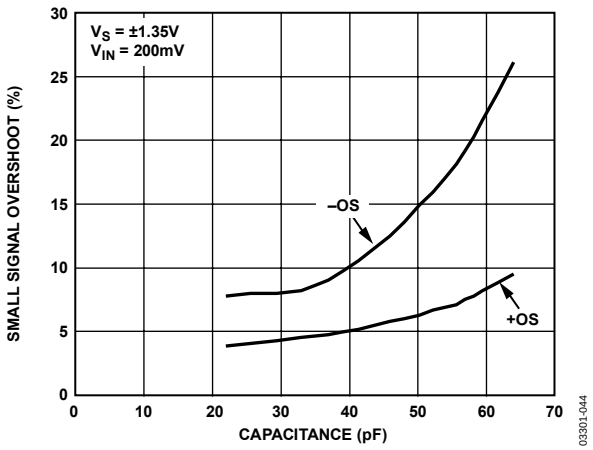


Figure 44. Small Signal Overshoot vs. Load Capacitance

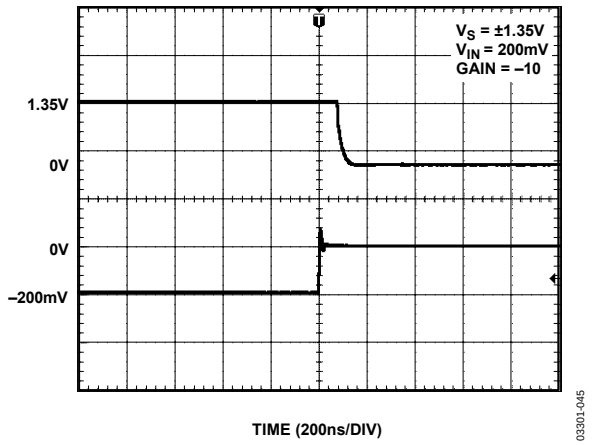


Figure 45. Negative Overload Recovery Time

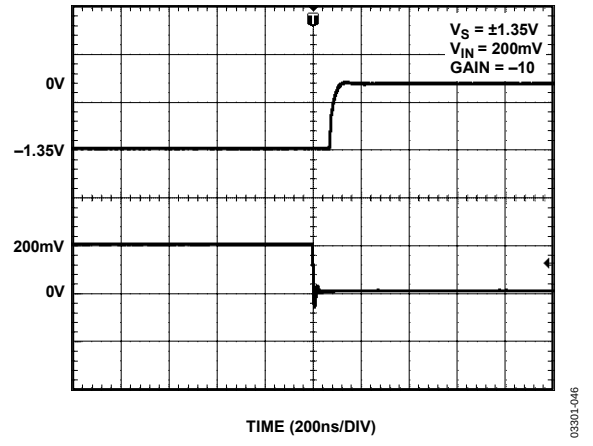


Figure 46. Positive Overload Recovery Time

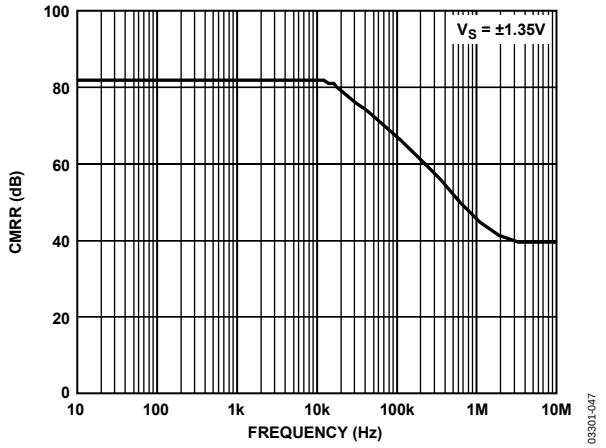


Figure 47. CMRR vs. Frequency

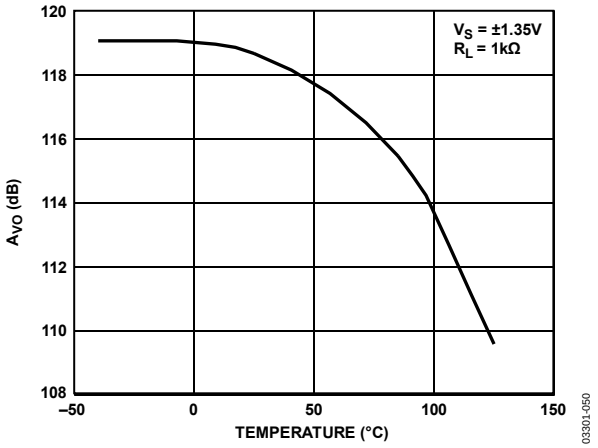


Figure 50. Open-Loop Gain vs. Temperature

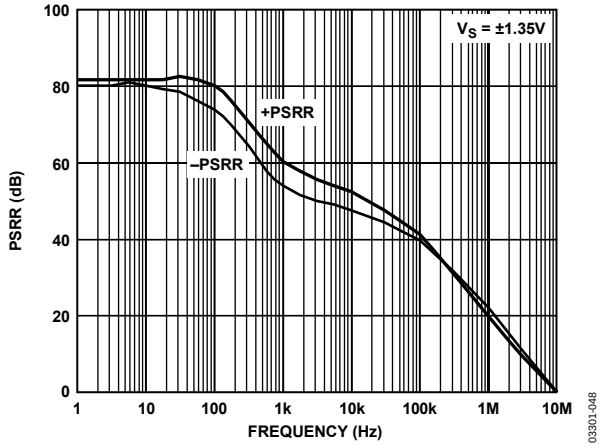


Figure 48. PSRR vs. Frequency

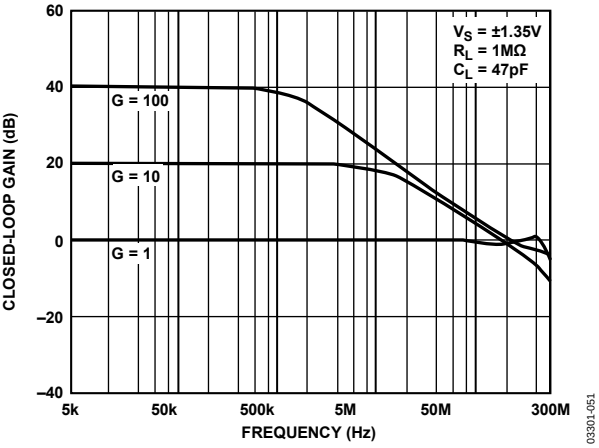


Figure 51. Closed-Loop Gain vs. Frequency

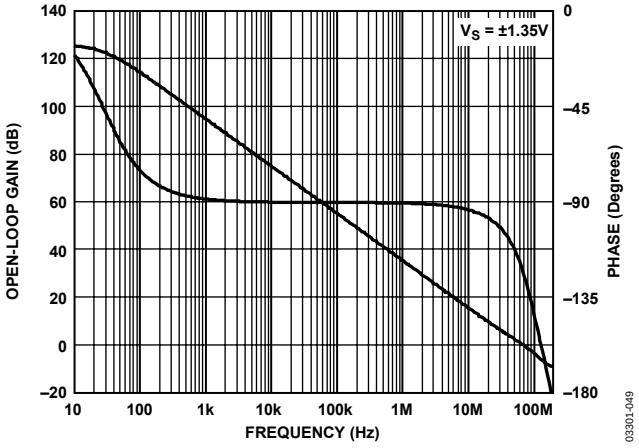


Figure 49. Open-Loop Gain and Phase vs. Frequency

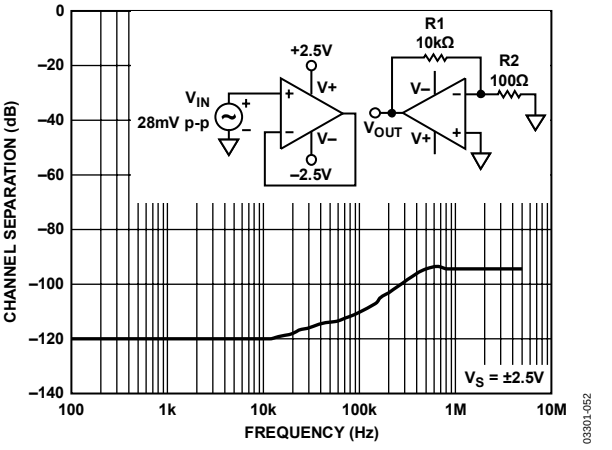


Figure 52. Channel Separation vs. Frequency.

APPLICATIONS

THEORY OF OPERATION

The AD865x family consists of voltage feedback, rail-to-rail input and output precision CMOS amplifiers that operate from 2.7 V to 5.5 V of power supply voltage. These amplifiers use Analog Devices, Inc. DigiTrim technology to achieve a higher degree of precision than is available from most CMOS amplifiers. DigiTrim technology, used in a number of Analog Devices amplifiers, is a method of trimming the offset voltage of the amplifier after it has been assembled. The advantage of post-package trimming is that it corrects any offset voltages caused by the mechanical stresses of assembly.

The AD865x family is available in standard op amp pinouts, making DigiTrim completely transparent to the user. The input stage of the amplifiers is a true rail-to-rail architecture, allowing the input common-mode voltage range of the op amp to extend to both positive and negative supply rails. The open-loop gain of the AD865x with a load of 1 kΩ is typically 115 dB.

The AD865x can be used in any precision op amp application. The amplifiers do not exhibit phase reversal for common-mode voltages within the power supply. With voltage noise of 4.5 nV/√Hz and –105 dB distortion for 10 kHz, 2 V p-p signals, the AD865x is a great choice for high resolution data acquisition systems. Their low noise, sub-pA input bias current, precision offset, and high speed make them superb preamps for fast photodiode applications. The speed and output drive capabilities of the AD865x also make the amplifiers useful in video applications.

Rail-to-Rail Output Stage

The voltage swing of the output stage is rail-to-rail and is achieved by using an NMOS and PMOS transistor pair connected in a common source configuration. The maximum output voltage swing is proportional to the output current, and larger currents will limit how close the output voltage can get to the proximity of the output voltage to the supply rail. This is a characteristic of all rail-to-rail output amplifiers. With 40 mA of output current, the output voltage can reach within 5 mV of the positive and negative rails. At light loads of >100 kΩ, the output swings within ~1 mV of the supplies.

Rail-to-Rail Input Stage

The input common-mode voltage range of the AD865x extends to both positive and negative supply voltages. This maximizes the usable voltage range of the amplifier, an important feature for single-supply and low voltage applications. This rail-to-rail input range is achieved by using two input differential pairs, one NMOS and one PMOS, placed in parallel. The NMOS pair is active at the upper end of the common-mode voltage range, and the PMOS pair is active at the lower end of the common-mode range.

The NMOS and PMOS input stages are separately trimmed using DigiTrim to minimize the offset voltage in both differential pairs. Both NMOS and PMOS input differential pairs are active in a 500 mV transition region when the input common-mode voltage is approximately 1.5 V below the positive supply voltage. A special design technique improves the input offset voltage in the transition region that traditionally exhibits a slight V_{OS} variation. As a result, the common-mode rejection ratio is improved within this transition band. Compared to the Burr Brown OPA350 amplifier, shown in Figure 53, the AD865x, shown in Figure 54, exhibits much lower offset voltage shift across the entire input common-mode range, including the transition region.

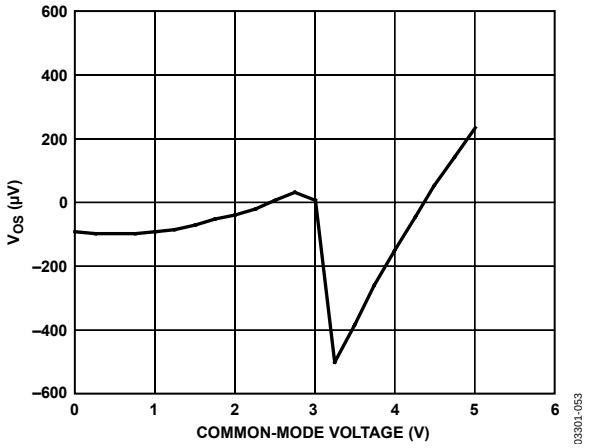


Figure 53. Input Offset Distribution over Common-Mode Voltage for the OPA350

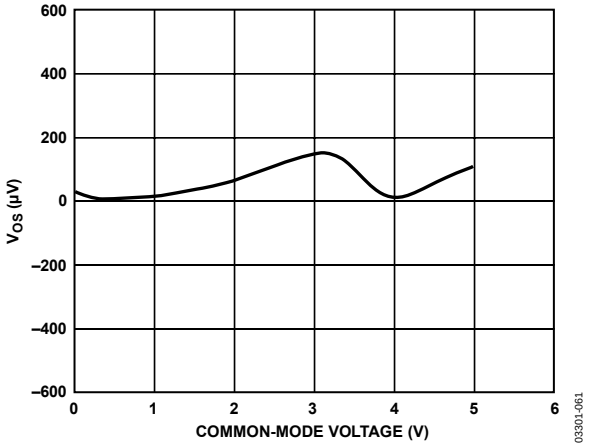


Figure 54. Input Offset Distribution over Common-Mode Input Protection for the AD865x

Input Protection

As with any semiconductor device, if a condition exists for the input voltage to exceed the power supply, the device input overvoltage characteristic must be considered. The inputs of the AD865x family are protected with ESD diodes to either power supply. Excess input voltage energizes internal PN junctions in the AD865x, allowing current to flow from the input to the supplies. This results in an input stage with picoamps of input current that can withstand up to 4000 V ESD events (human body model) with no degradation.

Excessive power dissipation through the protection devices destroys or degrades the performance of any amplifier. Differential voltages greater than 7 V result in an input current of approximately $(|V_{CC} - V_{EE}| - 0.7\ V)/R_I$, where R_I is the resistance in series with the inputs. For input voltages beyond the positive supply, the input current is approximately $(V_{IN} - V_{CC} - 0.7)/R_I$. For input voltages beyond the negative supply, the input current is about $(V_{IN} - V_{EE} + 0.7)/R_I$. If the inputs of the amplifier sustain differential voltages greater than 7 V or input voltages beyond the amplifier power supply, limit the input current to 10 mA by using an appropriately sized input resistor (R_I), as shown in Figure 55.

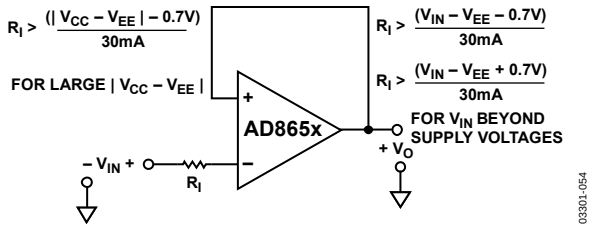


Figure 55. Input Protection Method

Overdrive Recovery

Overdrive recovery is defined as the time it takes for the output of an amplifier to come off the supply rail after an overload signal is initiated. This is usually tested by placing the amplifier in a closed-loop gain of 15 with an input square wave of 200 mV p-p while the amplifier is powered from either 5 V or 3 V. The AD865x family has excellent recovery time from overload conditions (see Figure 31 and Figure 32). The output recovers from the positive supply rail within 200 ns at all supply voltages. Recovery from the negative rail is within 100 ns at 5 V supply.

LAYOUT, GROUNDING, AND BYPASSING CONSIDERATIONS

Power Supply Bypassing

Power supply pins can act as inputs for noise, so care must be taken that a noise-free, stable dc voltage is applied. The purpose of bypass capacitors is to create low impedances from the supply to ground at all frequencies, thereby shunting or filtering most of the noise.

Bypassing schemes are designed to minimize the supply impedance at all frequencies with a parallel combination of capacitors of 0.1 μF and 4.7 μF. Chip capacitors of 0.1 μF (X7R or NPO) are critical and should be as close as possible to the amplifier package. The 4.7 μF tantalum capacitor is less critical for high frequency bypassing, and, in most cases, only one is needed per board at the supply inputs.

Grounding

A ground plane layer is important for densely packed PC boards to spread the current-minimizing parasitic inductances. However, an understanding of where the current flows in a circuit is critical to implementing effective high speed circuit design. The length of the current path is directly proportional to the magnitude of parasitic inductances and, therefore, the high frequency impedance of the path. High speed currents in an inductive ground return create an unwanted voltage noise.

The length of the high frequency bypass capacitor leads is critical. A parasitic inductance in the bypass grounding works against the low impedance created by the bypass capacitor. Place the ground leads of the bypass capacitors at the same physical location. Because load currents also flow from the supplies, the ground for the load impedance should be at the same physical location as the bypass capacitor grounds. For the larger value capacitors, intended to be effective at lower frequencies, the current return path distance is less critical.

Leakage Currents

Poor PC board layout, contaminants, and the board insulator material can create leakage currents that are much larger than the input bias current of the AD865x family. Any voltage differential between the inputs and nearby traces sets up leakage currents through the PC board insulator, for example 1 V/100 G = 10 pA. Similarly, any contaminants on the board can create significant leakage (skin oils are a common problem).

To significantly reduce leakages, put a guard ring (shield) around the inputs and the input leads that are driven to the same voltage potential as the inputs. This ensures that there is no voltage potential between the inputs and the surrounding area to set up any leakage currents. To be effective, the guard ring must be driven by a relatively low impedance source and should completely surround the input leads on all sides, above and below, using a multilayer board.

Another effect that can cause leakage currents is the charge absorption of the insulator material itself. Minimizing the amount of material between the input leads and the guard ring helps to reduce the absorption. Also, low absorption materials, such as Teflon® or ceramic, may be necessary in some instances.

Input Capacitance

Along with bypassing and grounding, high speed amplifiers can be sensitive to parasitic capacitance between the inputs and ground. A few picofarads of capacitance reduces the input impedance at high frequencies, which in turn increases the amplifier gain, causing peaking in the frequency response or oscillations. With the AD865x, additional input damping is required for stability with capacitive loads greater than 47 pF with direct input to output feedback (see the Output Capacitance section).

Output Capacitance

When using high speed amplifiers, it is important to consider the effects of the capacitive loading on amplifier stability. Capacitive loading interacts with the output impedance of the amplifier, causing reduction of the BW as well as peaking and ringing of the frequency response. To reduce the effects of the capacitive loading and allow higher capacitive loads, there are two commonly used methods.

- As shown in Figure 56, place a small value resistor (R_S) in series with the output to isolate the load capacitor from the amplifier output. Heavy capacitive loads can reduce the phase margin of an amplifier and cause the amplifier response to peak or become unstable. The AD865x is able to drive up to 47 pF in a unity gain buffer configuration without oscillation or external compensation. However, if an application requires a higher capacitive load drive when the AD865x is in unity gain, the use of external isolation networks can be used. The effect produced by this resistor is to isolate the op amp output from the capacitive load. The required amount of series resistance has been tabulated in Table 5 for different capacitive loads. While this technique improves the overall capacitive load drive for the amplifier, its biggest drawback is that it reduces the output swing of the overall circuit.

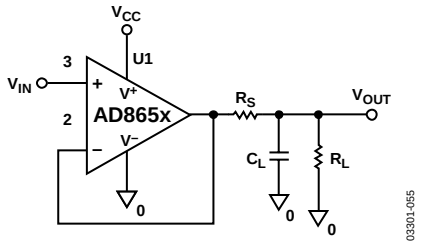


Figure 56. Driving Large Capacitive Loads

Table 5. Optimum Values for Driving Large Capacitive Loads

C_L	R_S
100 pF	50 Ω
500 pF	35 Ω
1.0 nF	25 Ω

- Another way to stabilize an op amp driving a large capacitive load is to use a snubber network, as shown in Figure 57. Because there is not any isolation resistor in the signal path, this method has the significant advantage of not reducing the output swing. The exact values of R_S and C_S are derived experimentally. In Figure 57, an optimum R_S and C_S combination for a capacitive load drive ranging from 50 pF to 1 nF was chosen. For this, R_S = 3 Ω and C_S = 10 nF were chosen.

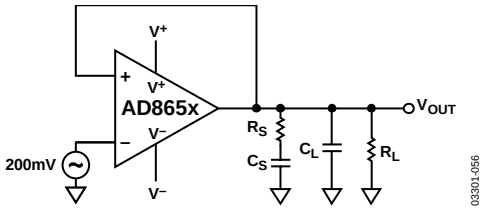


Figure 57. Snubber Network

Settling Time

The settling time of an amplifier is defined as the time it takes for the output to respond to a step change of input and enter and remain within a defined error band, as measured relative to the 50% point of the input pulse. This parameter is especially important in measurements and control circuits where amplifiers are used to buffer A/D inputs or DAC outputs. The design of the AD865x family combines a high slew rate and a wide gain bandwidth product to produce an amplifier with very fast settling time. The AD865x is configured in the noninverting gain of 1 with a 2 V p-p step applied to its input. The AD865x family has a settling time of about 130 ns to 0.01% (2 mV). The output is monitored with a 10×, 10 M, 11.2 pF scope probe.

THD Readings vs. Common-Mode Voltage

Total harmonic distortion of the AD865x family is well below 0.0004% with any load down to 600 Ω. The distortion is a function of the circuit configuration, the voltage applied, and the layout, in addition to other factors. The AD865x family outperforms its competitor for distortion, especially at frequencies below 20 kHz, as shown in Figure 58.

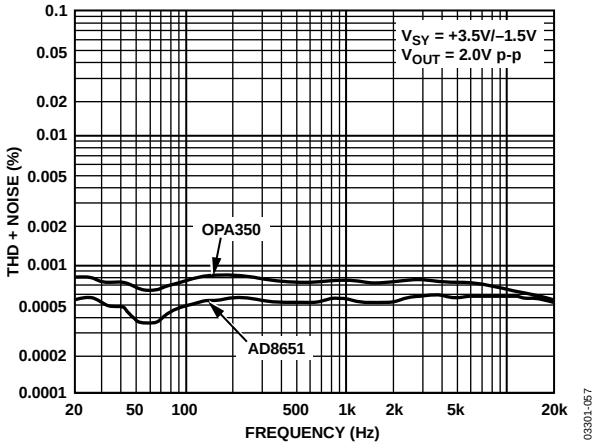


Figure 58. Total Harmonic Distortion

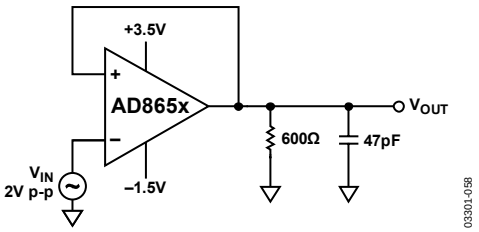


Figure 59. THD + N Test Circuit

Driving a 16-Bit ADC

The AD865x family is an excellent choice for driving high speed, high precision ADCs. The driver amplifier for this type of application needs low THD + N as well as quick settling time. Figure 61 shows a complete single-supply data acquisition solution. The AD865x family drives the AD7685, a 250 kSPS, 16-bit data converter.[1]

The AD865x is configured in an inverting gain of 1 with a 5 V single supply. Input of 45 kHz is applied, and the ADC samples at 250 kSPS. The results of this solution are listed in Table 6. The advantage of this circuit is that the amplifier and ADC can be powered with the same power supply. For the case of a noninverting gain of 1, the input common-mode voltage encompasses both supplies.

[1] For more information about the AD7685 data converter, go to http://www.analog.com/Analog_Root/productPage/productHome/0%2C2121%2CAD7685%2C00.html

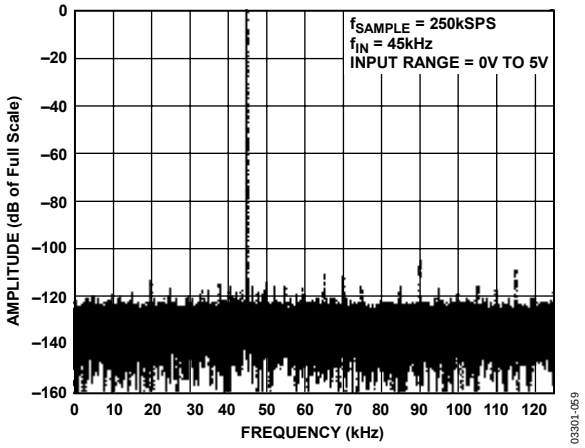


Figure 60. Frequency Response of AD865x Driving a 16-Bit ADC

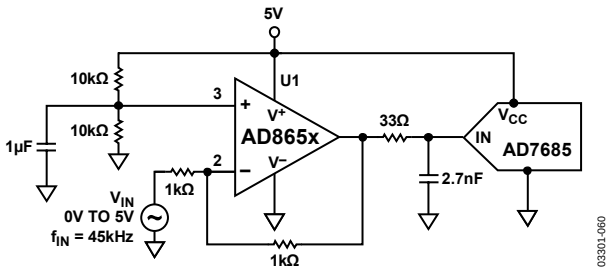
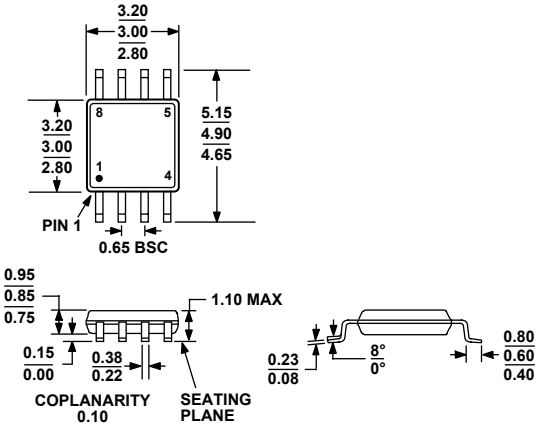


Figure 61. AD865x Driving a 16-Bit ADC

Table 6. Data Acquisition Solution of Figure 60

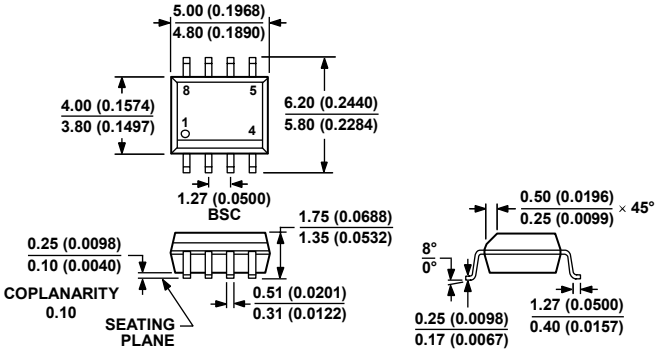
Parameter	Reading (dB)
THD + N	105.2
SFDR	106.6
2nd Harmonics	107.7
3rd Harmonics	113.6

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 62. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060506-A

Figure 63. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8651ARM-REEL	–40°C to +125°C	8-Lead MSOP	RM-8	BEA
AD8651ARM-R2	–40°C to +125°C	8-Lead MSOP	RM-8	BEA
AD8651ARMZ-REEL[1]	–40°C to +125°C	8-Lead MSOP	RM-8	BEA#
AD8651ARMZ-R2[1]	–40°C to +125°C	8-Lead MSOP	RM-8	BEA#
AD8651AR	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8651AR-REEL	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8651AR-REEL7	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8651ARZ[1]	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8651ARZ-REEL[1]	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8651ARZ-REEL7[1]	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8652ARMZ-R2[1]	–40°C to +125°C	8-Lead MSOP	RM-8	A05
AD8652ARMZ-REEL[1]	–40°C to +125°C	8-Lead MSOP	RM-8	A05
AD8652ARZ[1]	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8652ARZ-REEL[1]	–40°C to +125°C	8-Lead SOIC_N	R-8	
AD8652ARZ-REEL7[1]	–40°C to +125°C	8-Lead SOIC_N	R-8	

[1] Z = Pb-free part; # denotes lead-free product may be top or bottom marked.

NOTES

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