Low Cost, Precision Analog Front End and Controller for Battery Test/Formation Systems

Data Sheet **AD8451**

FEATURES

- **Integrated constant current and voltage modes with automatic switchover**
- **Charge and discharge modes**
- **Precision voltage and current measurement**
- **Integrated precision control feedback blocks**
- **Precision interface to PWM or linear power converters**
- **Fixed gain settings**
  - **Current sense gain: 26 V/V (typ)**
  - **Voltage sense gain: 0.8 V/V (typ)**
- **Excellent ac and dc performance**
- **Maximum offset voltage drift: 0.9 µV/°C**
- **Maximum gain drift: 3 ppm/°C**
- **Low current sense amplifier input voltage noise: 9 nV/√Hz typ**
- **Current sense CMRR: 108 dB min**
- **TTL compliant logic**

APPLICATIONS

- **Battery cell formation and testing**
- **Battery module testing**

GENERAL DESCRIPTION

The AD8451 is a precision analog front end and controller for testing and monitoring battery cells. A precision fixed gain instrumentation amplifier (IA) measures the battery charge/discharge current, and a fixed gain difference amplifier (DA) measures the battery voltage (see Figure 1). Internal laser trimmed resistor networks set the gains for the IA and the DA, optimizing the performance of the AD8451 over the rated temperature range. The IA gain is 26 V/V and the DA gain is 0.8 V/V.

Voltages at the ISET and VSET inputs set the desired constant current (CC) and constant voltage (CV) values. CC to CV switching is automatic and transparent to the system.

A TTL logic level input, MODE, selects the charge or discharge mode (high for charge, and low for discharge). An analog output, VCTRL, interfaces directly with the Analog Devices, Inc., ADP1972 pulse-width modulation (PWM) controller.

The AD8451 simplifies designs by providing excellent accuracy, performance over temperature, flexibility with functionality, and overall reliability in a space-saving package. The AD8451 is available in an 80-lead, 14 mm × 14 mm × 1.40 mm LQFP and is rated for an operating temperature of −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

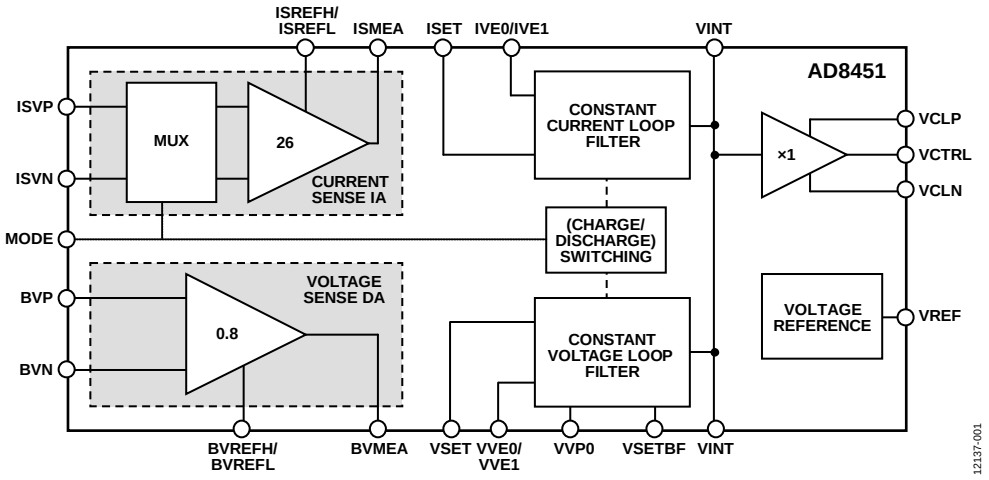


Figure 1.

Rev. 0 **Document Feedback**

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
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REVISION HISTORY

3/14—Revision 0: Initial Version

SPECIFICATIONS

AVCC = +15 V, AVEE = −15 V; DVCC = +5 V; T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENT SENSE INSTRUMENTATION AMPLIFIER					
Internal Fixed Gain			26		V/V
Gain Error	V_{ISMEA} = ±10 V			±0.1	%
Gain Drift	$T_A = T_{MIN}$ to T_{MAX}			3	ppm/°C
Gain Nonlinearity	V_{ISMEA} = ±10 V, R_L = 2 kΩ			3	ppm
Offset Voltage (RTI)	ISREFH and ISREFL pins grounded	−110		+110	µV
Offset Voltage Drift	$T_A = T_{MIN}$ to T_{MAX}			0.9	µV/°C
Input Bias Current			15	30	nA
Temperature Coefficient	$T_A = T_{MIN}$ to T_{MAX}			150	pA/°C
Input Offset Current				2	nA
Temperature Coefficient	$T_A = T_{MIN}$ to T_{MAX}			10	pA/°C
Input Common-Mode Voltage Range	$V_{ISVP} - V_{ISVN}$ = 0 V	AVEE + 2.3		AVCC − 2.4	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	AVEE + 2.6		AVCC − 2.6	V
Overvoltage Input Range		AVCC − 55		AVEE + 55	V
Differential Input Impedance			150		GΩ
Input Common-Mode Impedance			150		GΩ
Output Voltage Swing		AVEE + 1.5		AVCC − 1.2	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	AVEE + 1.7		AVCC − 1.4	V
Capacitive Load Drive				1000	pF
Short-Circuit Current			40		mA
Reference Input Voltage Range	ISREFH and ISREFL pins tied together	AVEE		AVCC	V
Reference Input Bias Current	$V_{ISVP} = V_{ISVN}$ = 0 V		5		µA
Output Voltage Level Shift	ISREFL pin grounded				
Maximum	ISREFH pin connected to VREF pin	17	20	23	mV
Scale Factor	V_{ISMEA}/V_{ISREFH}	6.8	8	9.2	mV/V
Common-Mode Rejection Ratio (CMRR)	ΔV_{CM} = 20 V	108			dB
Temperature Coefficient	$T_A = T_{MIN}$ to T_{MAX}			0.01	µV/V/°C
Power Supply Rejection Ratio (PSRR)	ΔV_S = 20 V	108	122		dB
Voltage Noise	f = 1 kHz		9		nV/√Hz
Voltage Noise, Peak to Peak	f = 0.1 Hz to 10 Hz		0.2		µV p-p
Current Noise	f = 1 kHz		80		fA/√Hz
Current Noise, Peak to Peak	f = 0.1 Hz to 10 Hz		5		pA p-p
Small Signal −3 dB Bandwidth			1.5		MHz
Slew Rate	ΔV_{ISMEA} = 10 V		5		V/µs
VOLTAGE SENSE DIFFERENCE AMPLIFER					
Internal Fixed Gains			0.8		V/V
Gain Error	V_{IN} = ±10 V			±0.1	%
Gain Drift	$T_A = T_{MIN}$ to T_{MAX}			3	ppm/°C
Gain Nonlinearity	V_{BVMEA} = ±10 V, R_L = 2 kΩ			3	ppm
Offset Voltage (RTO)	BVREFH and BVREFL pins grounded			500	µV
Offset Voltage Drift	$T_A = T_{MIN}$ to T_{MAX}			4	µV/°C
Differential Input Voltage Range	V_{BVN} = 0 V, V_{BVREFL} = 0 V	−16		+16	V
Input Common-Mode Voltage Range	V_{BVMEA} = 0 V	−27		+27	V
Differential Input Impedance			200		kΩ
Input Common-Mode Impedance			90		kΩ
Output Voltage Swing		AVEE + 1.5		AVCC − 1.5	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	AVEE + 1.7		AVCC − 1.7	V
Capacitive Load Drive				1000	pF
Short-Circuit Current			30		mA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Reference Input Voltage Range	BVREFH and BVREFL pins tied together	AVEE		AVCC	V
Output Voltage Level Shift	BVREFL pin grounded				
Maximum	BVREFH pin connected to VREF pin	4.5	5	5.5	mV
Scale Factor	V_{BVMEA}/V_{BVREFH}	1.8	2	2.2	mV/V
CMRR	ΔV_{CM} = 10 V, RTO	80			dB
Temperature Coefficient	$T_A = T_{MIN}$ to T_{MAX}			0.05	µV/V/°C
PSRR	ΔV_S = 20 V, RTO	100			dB
Output Voltage Noise	f = 1 kHz, RTI		105		nV/√Hz
Voltage Noise, Peak to Peak	f = 0.1 Hz to 10 Hz, RTI		2		µV p-p
Small Signal −3 dB Bandwidth			1		MHz
Slew Rate			0.8		V/µs
CONSTANT CURRENT AND CONSTANT VOLTAGE LOOP FILTER AMPLIFIERS					
Offset Voltage				150	µV
Offset Voltage Drift	$T_A = T_{MIN}$ to T_{MAX}			0.6	µV/°C
Input Bias Current		−5		+5	nA
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	−5		+5	nA
Input Common-Mode Voltage Range		AVEE + 1.5		AVCC − 1.8	V
Output Voltage Swing	V_{VCLN} = AVEE + 1 V, V_{VCLP} = AVCC − 1 V	AVEE + 1.5		AVCC − 1	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	AVEE + 1.7		AVCC − 1	V
Closed-Loop Output Impedance			0.01		Ω
Capacitive Load Drive				1000	pF
Source Short-Circuit Current			1		mA
Sink Short-Circuit Current			40		mA
Open-Loop Gain			140		dB
CMRR	ΔV_{CM} = 10 V			100	dB
PSRR	ΔV_S = 20 V			100	dB
Voltage Noise	f = 1 kHz		10		nV/√Hz
Voltage Noise, Peak to Peak	f = 0.1 Hz to 10 Hz		0.3		µV p-p
Current Noise	f = 1 kHz		80		fA/√Hz
Current Noise, Peak to Peak	f = 0.1 Hz to 10 Hz		5		pA p-p
Small Signal Gain Bandwidth Product			3		MHz
Slew Rate	ΔV_{VINT} = 10 V		1		V/µs
CC to CV Transition Time			1.5		µs
VINT AND CONSTANT VOLTAGE BUFFER					
Nominal Gain			1		V/V
Offset Voltage				150	µV
Offset Voltage Drift	$T_A = T_{MIN}$ to T_{MAX}			0.6	µV/°C
Input Bias Current	CV buffer only	−5		+5	nA
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	−5		+5	nA
Input Voltage Range		AVEE + 1.5		AVCC − 1.8	V
Output Voltage Swing					
Current Sharing and Constant Voltage Buffers		AVEE + 1.5		AVCC − 1.5	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	AVEE + 1.7		AVCC − 1.5	V
VINT Buffer		V_{VCLN} − 0.6		V_{VCLP} + 0.6	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	V_{VCLN} − 0.6		V_{VCLP} + 0.6	V
Output Clamps Voltage Range	VINT buffer only				
VCLP Pin		V_{VCLN}		AVCC − 1	V
VCLN Pin		AVEE + 1		V_{VCLP}	V
Closed-Loop Output Impedance			1		Ω
Capacitive Load Drive				1000	pF
Short-Circuit Current			40		mA
PSRR	ΔV_S = 20 V			100	dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Voltage Noise	f = 1 kHz		10		nV/√Hz
Voltage Noise, Peak to Peak	f = 0.1 Hz to 10 Hz		0.3		µV p-p
Current Noise	f = 1 kHz, CV buffer only		80		fA/√Hz
Current Noise, Peak to Peak	f = 0.1 Hz to 10 Hz		5		pA p-p
Small Signal −3 dB Bandwidth			3		MHz
Slew Rate	ΔV_{OUT} = 10 V		1		V/µs
VOLTAGE REFERENCE					
Nominal Output Voltage	With respect to AGND		2.5		V
Output Voltage Error				±1	%
Temperature Drift	$T_A = T_{MIN}$ to T_{MAX}			10	ppm/°C
Line Regulation	ΔV_S = 10 V			40	ppm/V
Load Regulation	ΔI_{VREF} = 1 mA (source only)			400	ppm/mA
Output Current, Sourcing				10	mA
Voltage Noise	f = 1 kHz		100		nV/√Hz
Voltage Noise, Peak to Peak	f = 0.1 Hz to 10 Hz		5		µV p-p
DIGITAL INTERFACE, MODE INPUT	MODE pin (Pin 39)				
Input Voltage High, V_{IH}	With respect to DGND	2.0		DVCC	V
Input Voltage Low, V_{IL}	With respect to DGND	DGND		0.8	V
Mode Switching Time			500		ns
POWER SUPPLY					
Operating Voltage Range					
AVCC		5		36	V
AVEE		−31		0	V
Analog Supply Range	AVCC − AVEE	5		36	V
DVCC		3		5	V
Quiescent Current					
AVCC			7	10	mA
AVEE			6.5	10	mA
DVCC			40	70	µA
TEMPERATURE RANGE					
For Specified Performance		−40		+85	°C
Operational		−55		+125	°C

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Analog Supply Voltage (AVCC – AVEE)	36 V
Digital Supply Voltage (DVCC – DGND)	36 V
Maximum Voltage at Any Input Pin	AVCC
Minimum Voltage at Any Input Pin	AVEE
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

The θ_{JA} value assumes a 4-layer JEDEC standard board with zero airflow.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
80-Lead LQFP	54.7	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

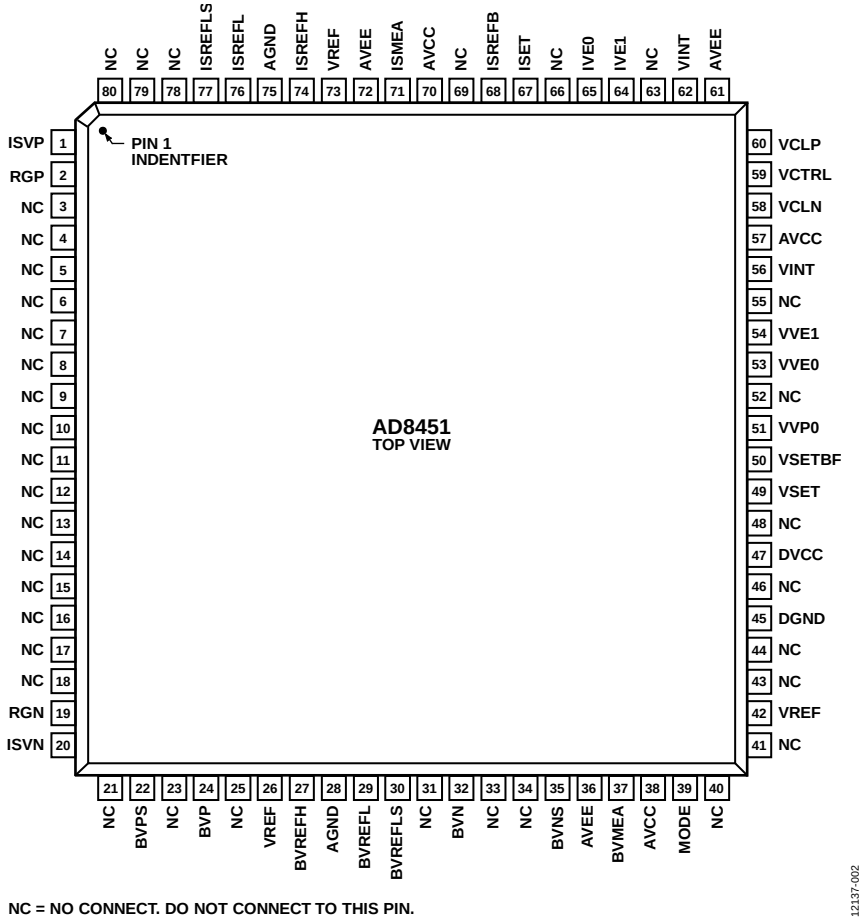


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Input/Output[1]	Description
1, 20	ISVP, ISVN	Input	Current Sense Instrumentation Amplifier Positive (Noninverting) and Negative (Inverting) Inputs. Connect these pins across the current sense shunt resistor.
2, 19	RGP, RGN	N/A	Negative Input of the Preamplifiers of the Current Sense Instrumentation Amplifier.
3 to 18, 21, 23, 25, 31, 33, 34, 40, 41, 43, 44, 46, 48, 52, 55, 63, 66, 69, 78 to 80	NC	N/A	No Connect. Do not connect to this pin.
22, 35	BVPS, BVNS	Input	Kelvin Sense Pins for the BVP and BVN Voltage Sense Difference Amplifier Inputs.
24, 32	BVP, BVN	Input	Voltage Sense Difference Amplifier Inputs.
26, 42, 73	VREF	Output	Voltage Reference Output Pins. VREF = 2.5 V.
27	BVREFH	Input	Reference Input for the Voltage Sense Difference Amplifier. To level shift the voltage sense difference amplifier output by approximately 5 mV, connect this pin to the VREF pin. Otherwise, connect this pin to the BVREFL pin.
28, 75	AGND	N/A	Analog Ground Pins.
29	BVREFL	Input	Reference Input for the Voltage Sense Difference Amplifier. The default connection is to ground.
30	BVREFLS	Input	Kelvin Sense Pin for the BVREFL Pin.

Pin No.	Mnemonic	Input/Output[1]	Description
36, 61, 72	AVEE	N/A	Analog Negative Supply Pins. The default voltage is −15 V.
37	BVMEA	Output	Voltage Sense Difference Amplifier Output.
38, 57, 70	AVCC	N/A	Analog Positive Supply Pins. The default voltage is 15 V.
39	MODE	Input	TTL Compliant Logic Input Selects Charge or Discharge Mode. Low = discharge, high = charge.
45	DGND	N/A	Digital Ground Pin.
47	DVCC	N/A	Digital Supply. The default voltage is 5 V.
49	VSET	Input	Target Voltage for the Voltage Sense Control Loop.
50	VSETBF	Output	Buffered Voltage VSET.
51	VVP0	Input	Noninverting Input of the Voltage Sense Integrator for Discharge Mode.
53	VVE0	Input	Inverting Input Voltage for the Voltage Sense Integrator for Discharge Mode.
54	VVE1	Input	Inverting Input of the Voltage Sense Integrator for Charge Mode.
56, 62	VINT	Output	Minimum Output of the Voltage Sense and Current Sense Integrator Amplifiers.
58	VCLN	Input	Low Clamp Voltage for VCTRL.
59	VCTRL	Output	Controller Output Voltage. Connect this pin to the input of the PWM controller (for example, the COMP pin of the ADP1972).
60	VCLP	Input	High Clamp Voltage for VCTRL.
64	IVE1	Input	Inverting Input of the Current Sense Integrator for Charge Mode.
65	IVE0	Input	Inverting Input of the Current Sense Integrator for Discharge Mode.
67	ISET	Input	Target Voltage for the Current Sense Control Loop.
68	ISREFB	Output	Buffered Voltage ISREFL.
71	ISMEA	Output	Current Sense Instrumentation Amplifier Output.
74	ISREFH	Input	Reference Input for the Current Sense Amplifier. To level shift the current sense instrumentation amplifier output by approximately 20 mV, connect this pin to the VREF pin. Otherwise, connect this pin to the ISREFL pin.
76	ISREFL	Input	Reference Input for the Current Sense Amplifier. The default connection is to ground.
77	ISREFLS	Input	Kelvin Sense Pin for the ISREFL Pin.

[1] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

AVCC = +15 V, AVEE = −15 V, T_A = 25°C, and R_L = ∞, unless otherwise noted.

IA CHARACTERISTICS

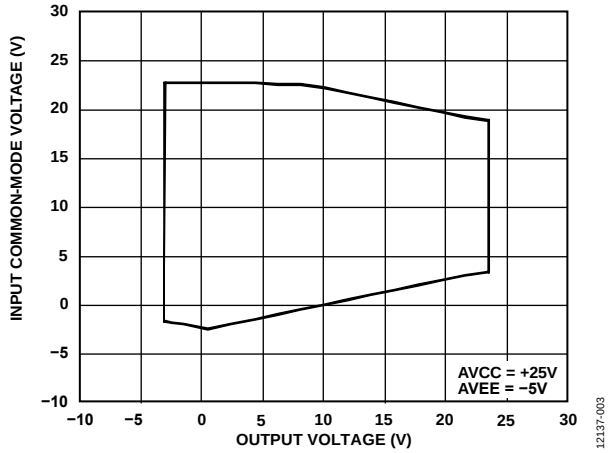


Figure 3. Input Common-Mode Voltage vs. Output Voltage for AVCC = +25 V and AVEE = −5 V

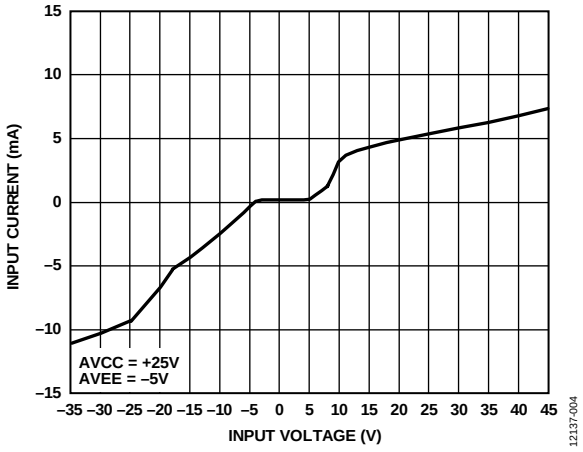


Figure 4. Input Overvoltage Performance for AVCC = +25 V and AVEE = −5 V

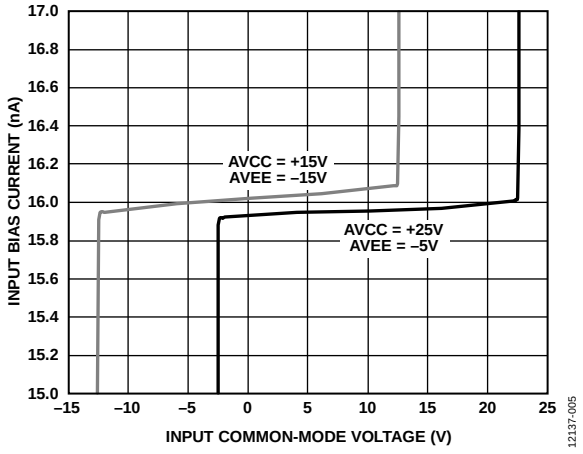


Figure 5. Input Bias Current vs. Input Common-Mode Voltage

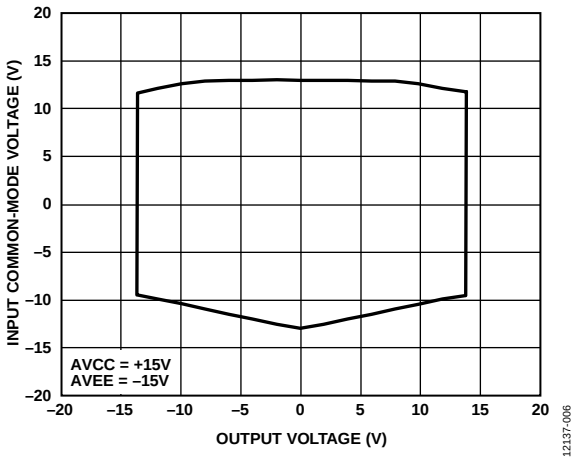


Figure 6. Input Common-Mode Voltage vs. Output Voltage for AVCC = +15 V and AVEE = −15 V

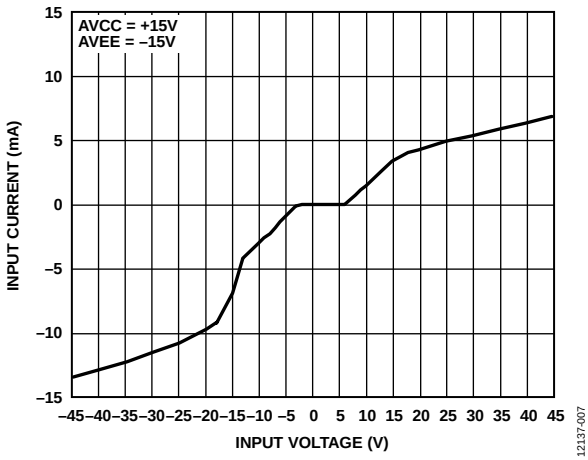


Figure 7. Input Overvoltage Performance for AVCC = +15 V and AVEE = −15 V

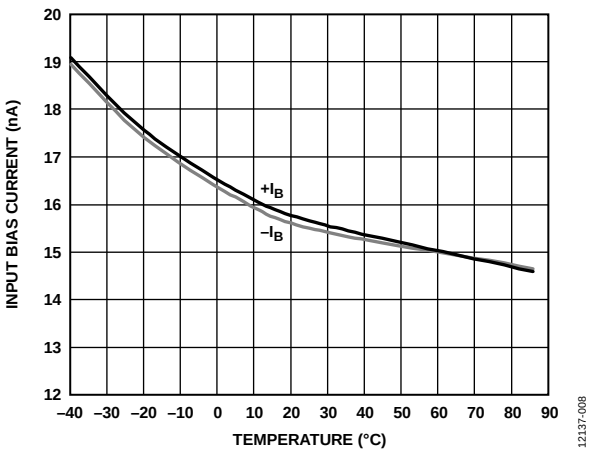


Figure 8. Input Bias Current vs. Temperature

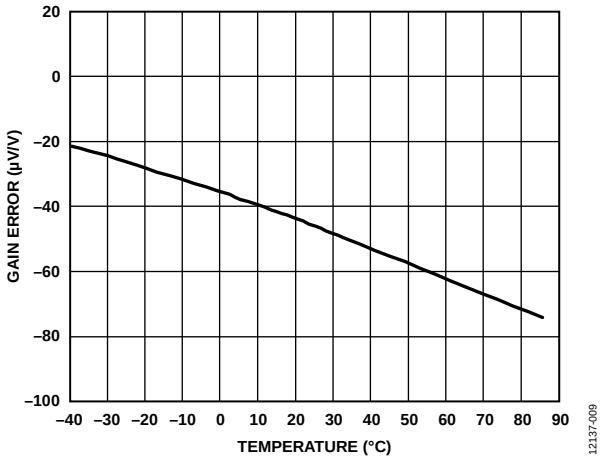


Figure 9. Gain Error vs. Temperature

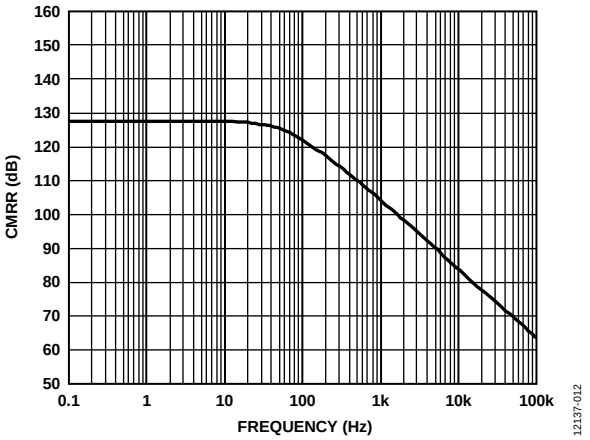


Figure 12. CMRR vs. Frequency

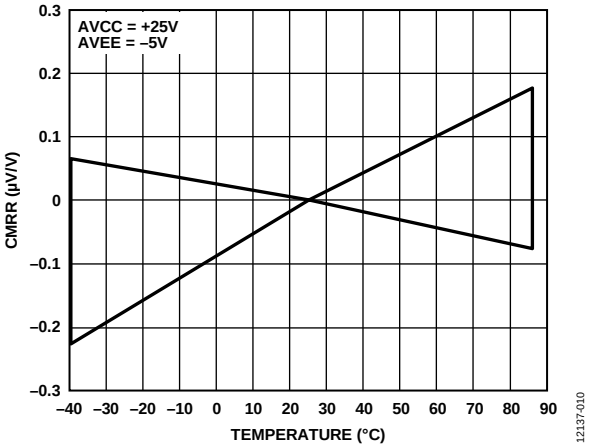


Figure 10. Normalized CMRR vs. Temperature

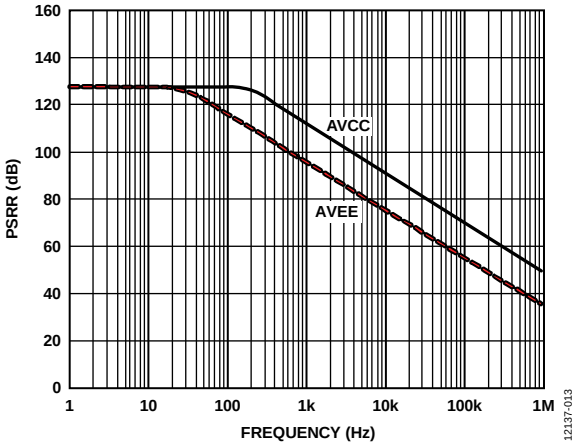


Figure 13. PSRR vs. Frequency

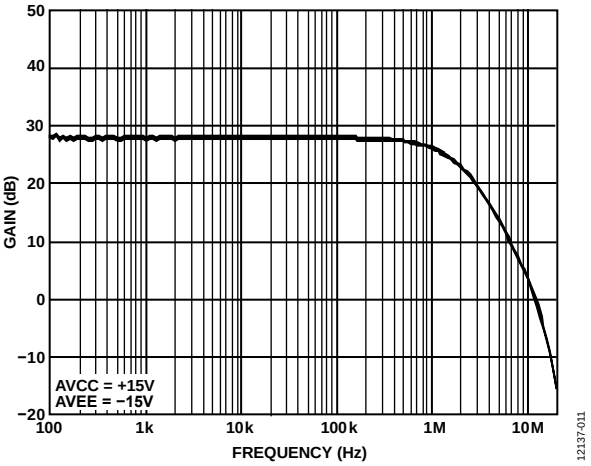


Figure 11. Gain vs. Frequency

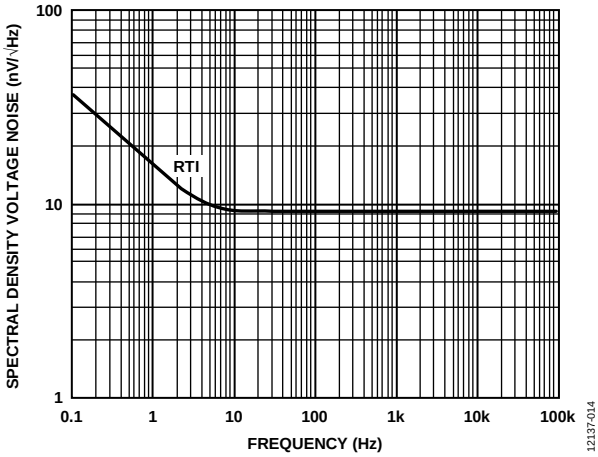


Figure 14. Spectral Density Voltage Noise, RTI vs. Frequency

DA CHARACTERISTICS

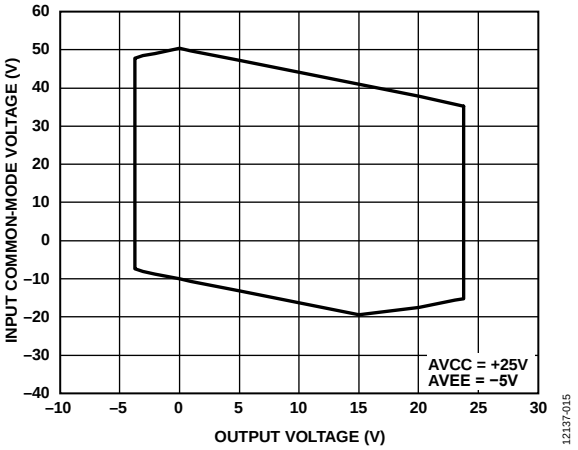


Figure 15. Input Common-Mode Voltage vs. Output Voltage for AVCC = +25 V and AVEE = −5 V

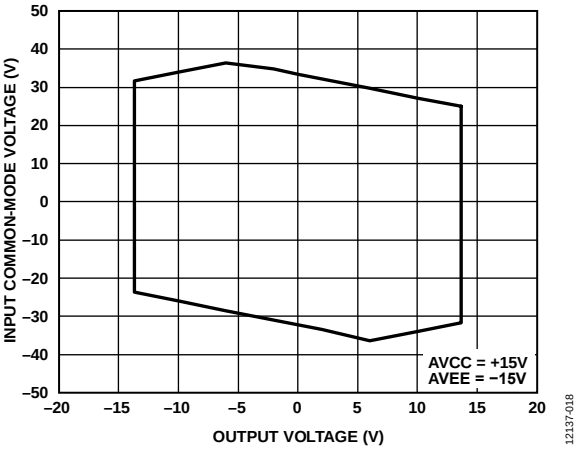


Figure 18. Input Common-Mode Voltage vs. Output Voltage for AVCC = +15 V and AVEE = −15 V

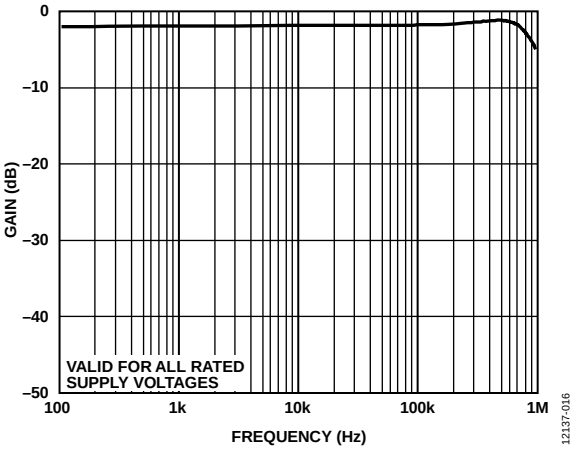


Figure 16. Gain vs. Frequency

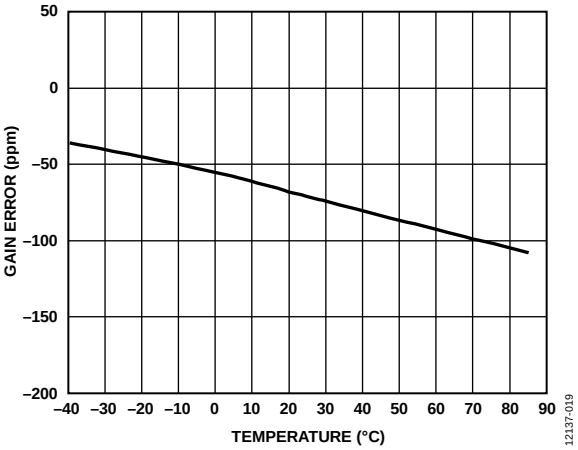


Figure 19. Gain Error vs. Temperature

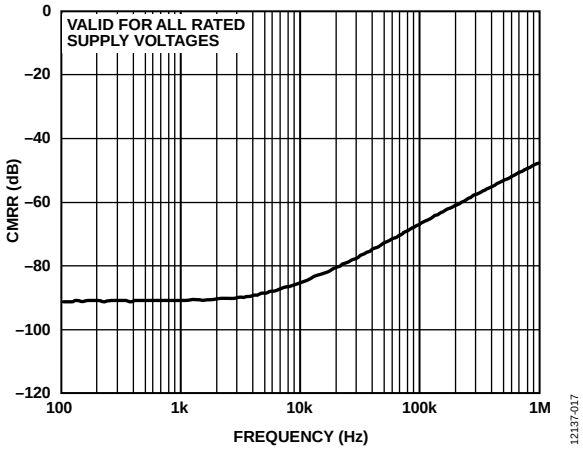


Figure 17. CMRR vs. Frequency

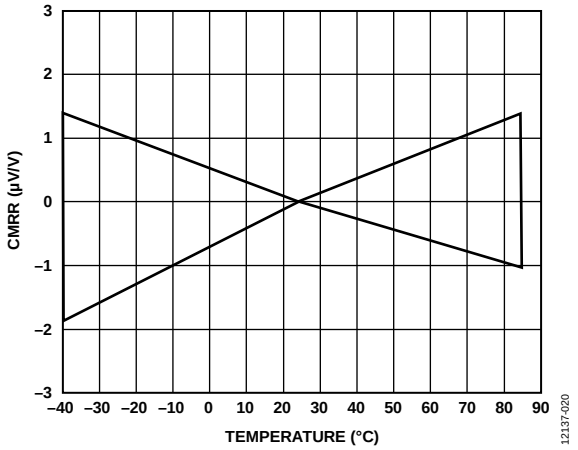


Figure 20. Normalized CMRR vs. Temperature

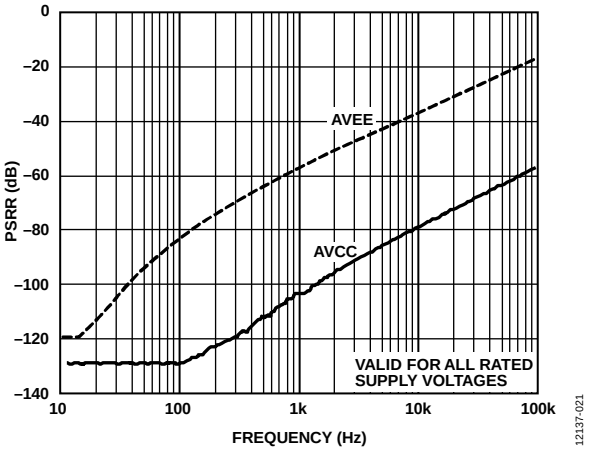


Figure 21. PSRR vs. Frequency

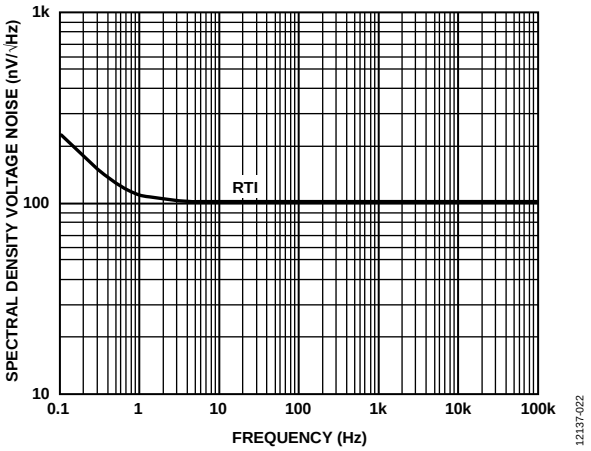


Figure 22. Spectral Density Voltage Noise, RTI vs. Frequency

CC AND CV LOOP FILTER AMPLIFIERS, AND VSET BUFFER

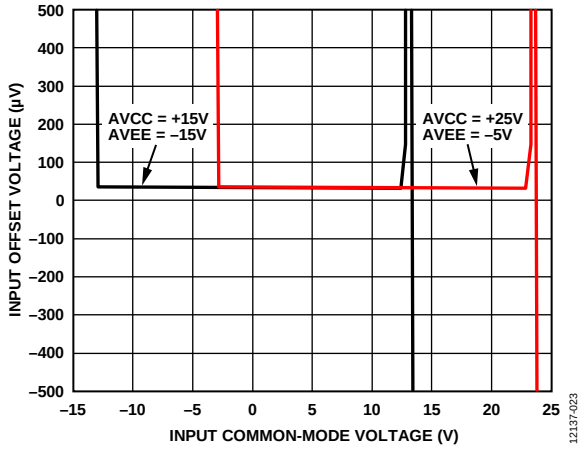


Figure 23. Input Offset Voltage vs. Input Common-Mode Voltage for Two Supply Voltage Combinations

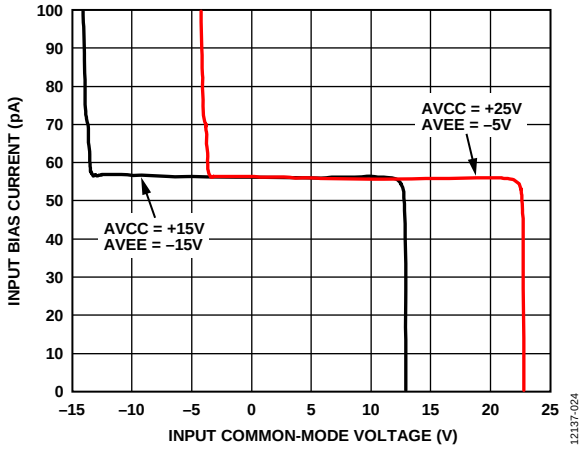


Figure 24. Input Bias Current vs. Input Common-Mode Voltage for Two Supply Voltage Combinations

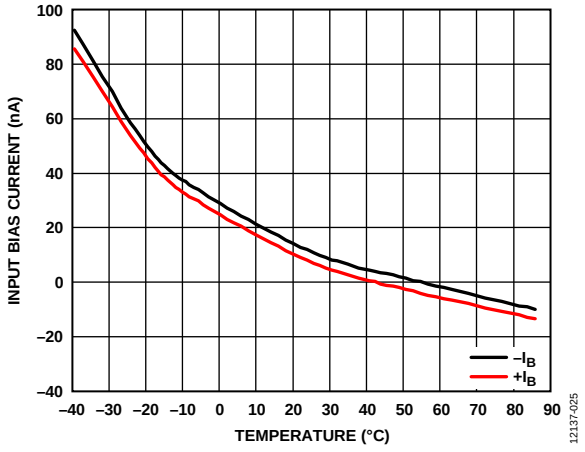


Figure 25. Input Bias Current vs. Temperature

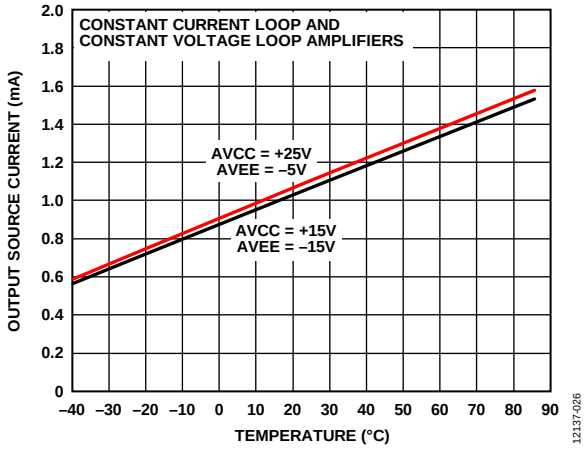


Figure 26. Output Source Current vs. Temperature for Two Supply Voltage Combinations

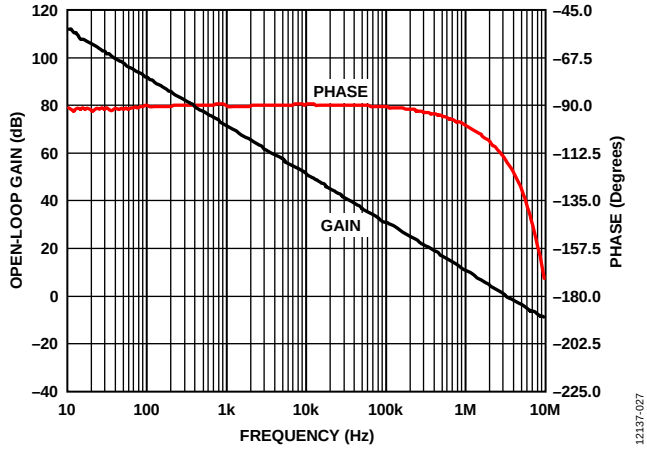


Figure 27. Open-Loop Gain and Phase vs. Frequency

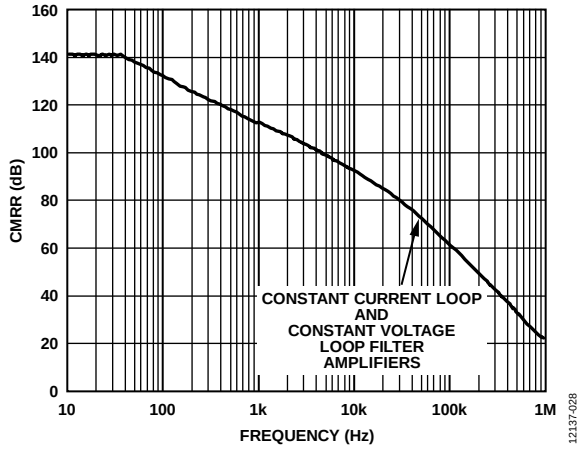


Figure 28. CMRR vs. Frequency

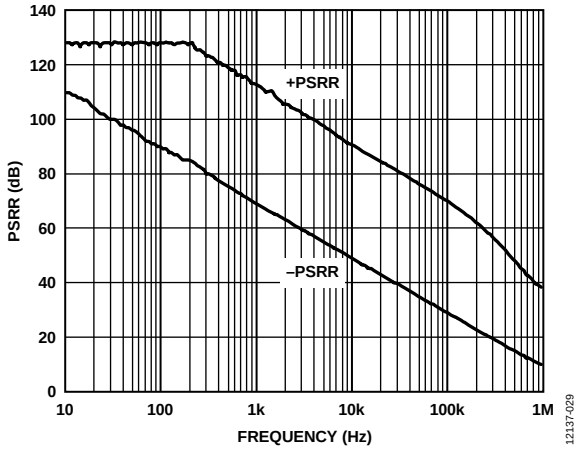


Figure 29. PSRR vs. Frequency

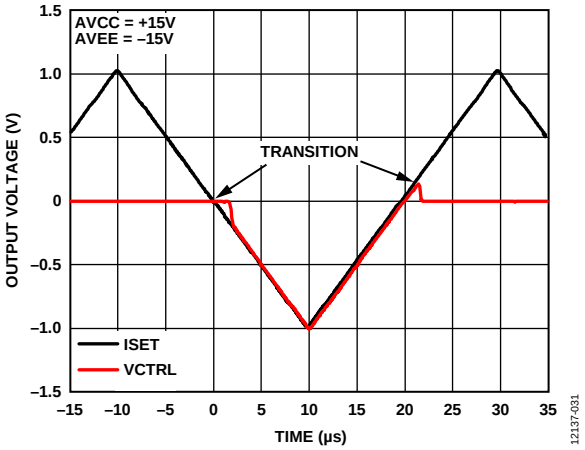


Figure 31. CC to CV Transition

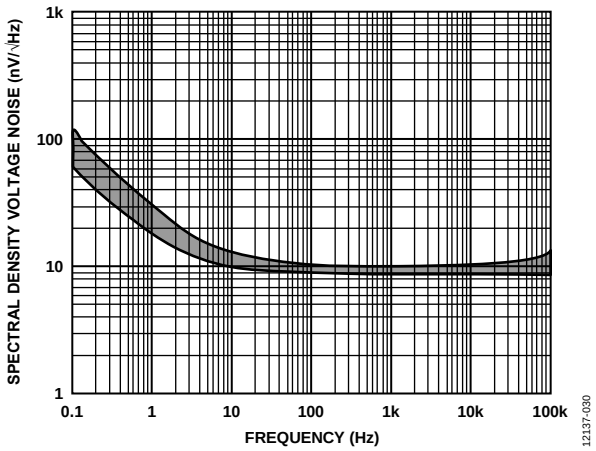


Figure 30. Range of Spectral Density Voltage Noise vs. Frequency for the Op Amps and Buffers

VINT BUFFER

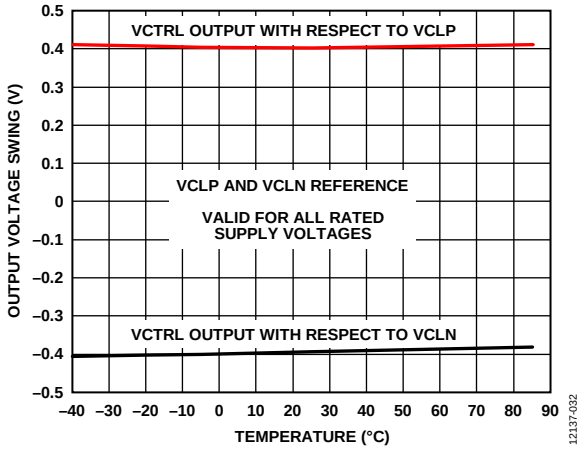


Figure 32. Output Voltage Swing with Respect to VCLP and VCLN vs. Temperature

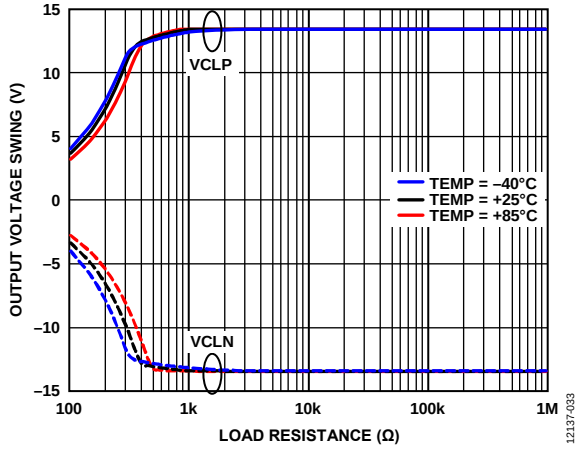


Figure 33. Output Voltage Swing vs. Load Resistance at Three Temperatures

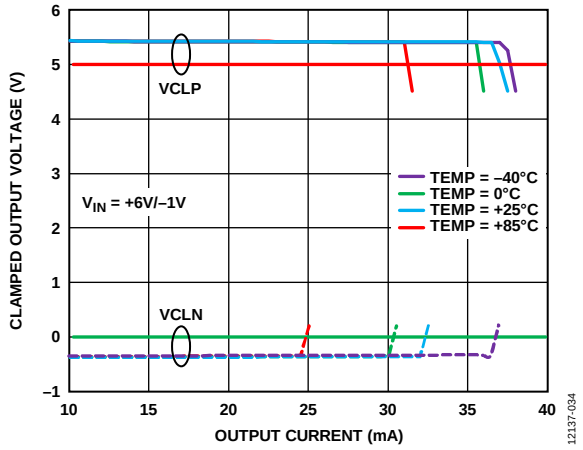


Figure 34. Clamped Output Voltage vs. Output Current at Four Temperatures

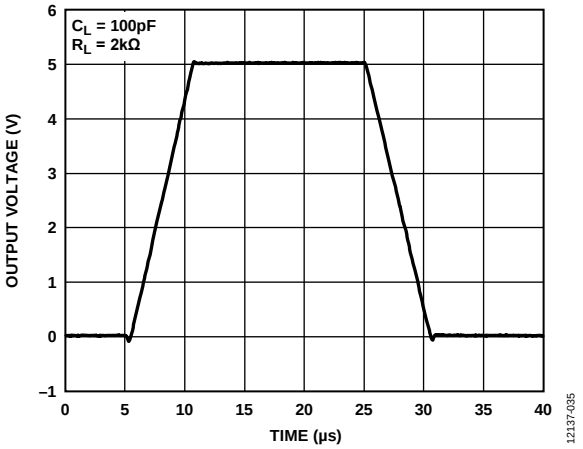


Figure 35. Large Signal Transient Response, R_L = 2 kΩ, C_L = 100 pF

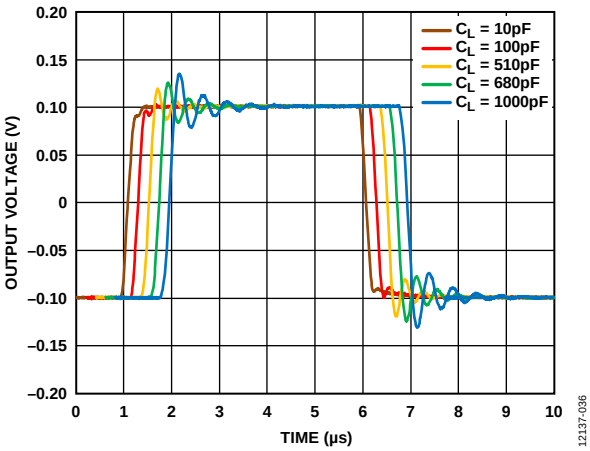


Figure 36. Small Signal Transient Response vs. Capacitive Load

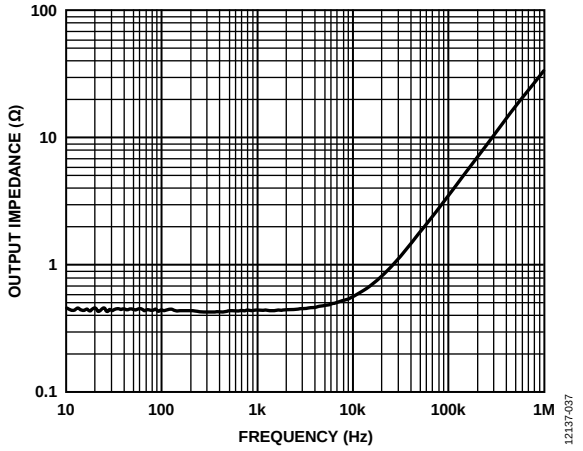


Figure 37. Output Impedance vs. Frequency

REFERENCE CHARACTERISTICS

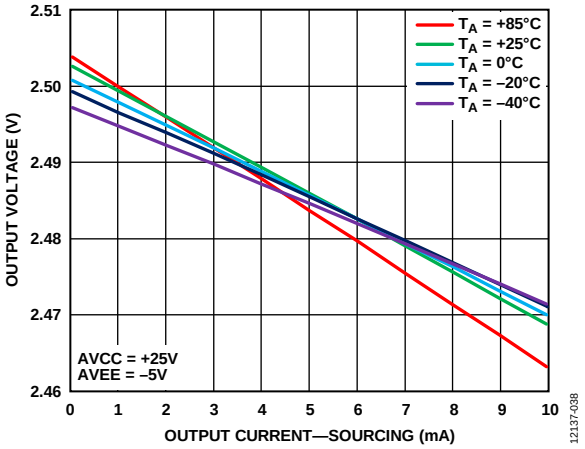


Figure 38. Output Voltage vs. Output Current (Sourcing) over Temperature

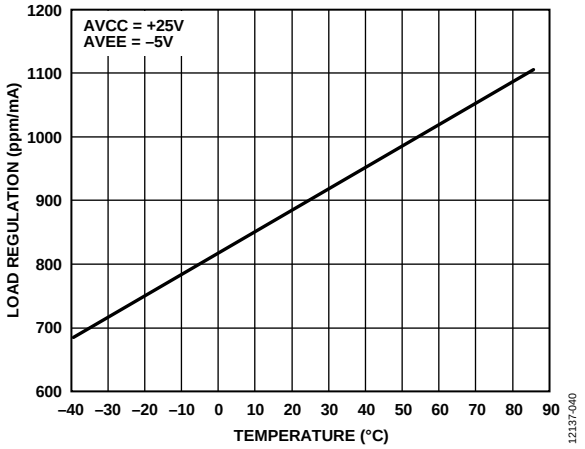


Figure 40. Source and Sink Load Regulation vs. Temperature

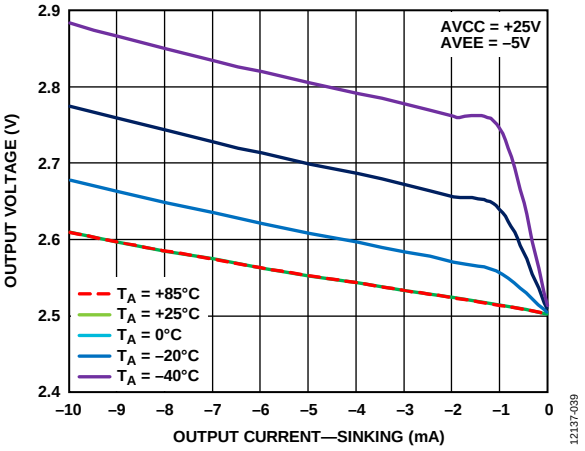


Figure 39. Output Voltage vs. Output Current (Sinking) over Temperature

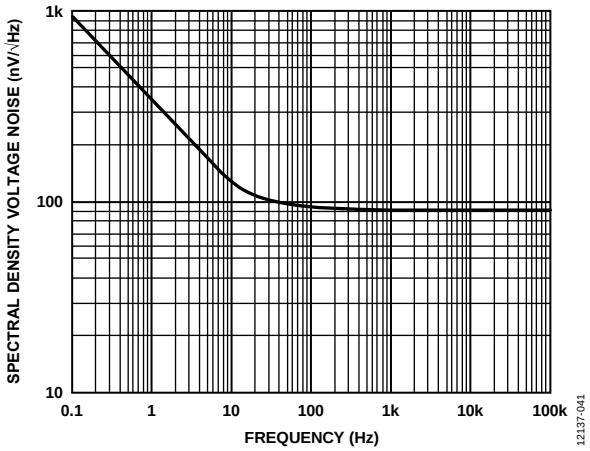


Figure 41. Spectral Density Voltage Noise vs. Frequency

THEORY OF OPERATION

OVERVIEW

To form and test a battery, the battery must undergo charge and discharge cycles. During these cycles, the battery terminal current and voltage must be precisely controlled to prevent battery failure or a reduction in the capacity of the battery. Therefore, battery formation and test systems require a high precision analog front end to monitor the battery current and terminal voltage. The analog front end of the AD8451 includes a precision current sense fixed gain instrumentation amplifier (IA) to measure the battery current and a precision voltage sense fixed gain difference amplifier (DA) to measure the battery voltage.

Battery formation and test systems charge and discharge batteries using a constant current/constant voltage (CC/CV) algorithm. In other words, the system first forces a set constant current into or out of the battery until the battery voltage reaches a target value. At this point, a set constant voltage is forced across the battery terminals.

The AD8451 provides two control loops—CC loop and a CV loop—that transition automatically after the battery reaches the user defined target voltage. These loops are implemented via two precision specialty amplifiers with external feedback networks that set the transfer function of the CC and CV loops. Moreover, in the AD8451, these loops reconfigure themselves to charge or discharge the battery by toggling the MODE pin.

Figure 42 is a block diagram of the AD8451 that illustrates the distinct sections of the AD8451, including the IA and DA measurement blocks, and the loop filter amplifiers. Figure 43 is a block diagram of a battery formation and test system.

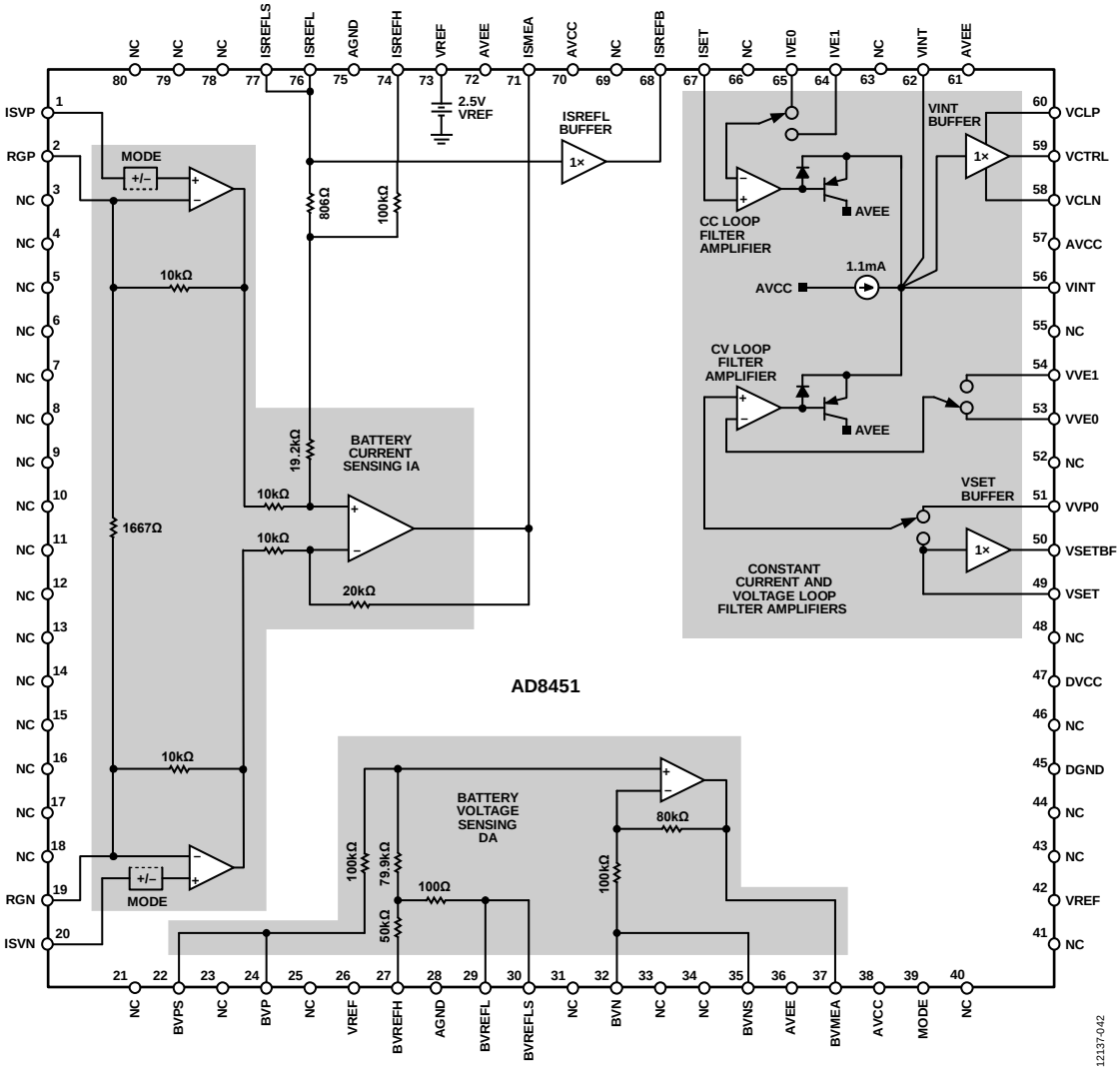


Figure 42. Detailed Block Diagram

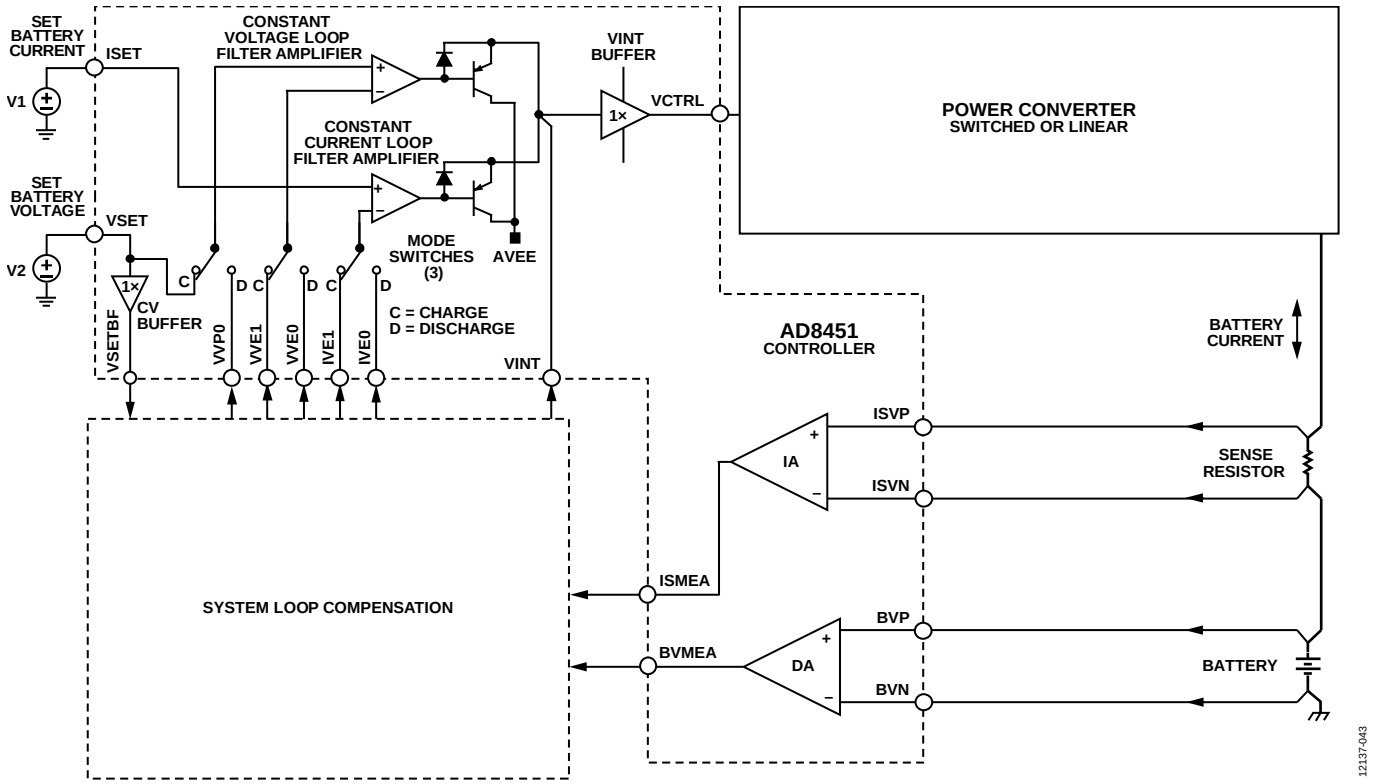


Figure 43. Signal Path of an Li-Ion Battery Formation and Test System Using the AD8451

INSTRUMENTATION AMPLIFIER (IA)

Figure 44 is a block diagram of the IA, which is used to monitor the battery current. The architecture of the IA is the classic 3-op-amp topology, similar to the Analog Devices industry-standard AD8221 and AD620, with a fixed gain of 26. This architecture provides the highest achievable CMRR at a given gain, enabling high-side battery current sensing without the introduction of significant errors in the measurement. For more information about instrumentation amplifiers, see *A Designer's Guide to Instrumentation Amplifiers*.

Reversing Polarity When Charging and Discharging

Figure 43 shows that during the charge cycle, the power converter feeds current into the battery, generating a positive voltage across the current sense resistor. During the discharge cycle, the power converter draws current from the battery, generating a negative voltage across the sense resistor. In other words, the battery current polarity reverses when the battery discharges.

In the CC control loop, this change in polarity can be problematic if the polarity of the target current is not reversed. To solve this problem, the AD8451 IA includes a multiplexer preceding its inputs that inverts the polarity of the IA gain. This multiplexer is controlled via the MODE pin. When the MODE pin is logic high (charge mode), the IA gain is noninverting, and when the MODE pin is logic low (discharge mode), the IA gain is inverting.

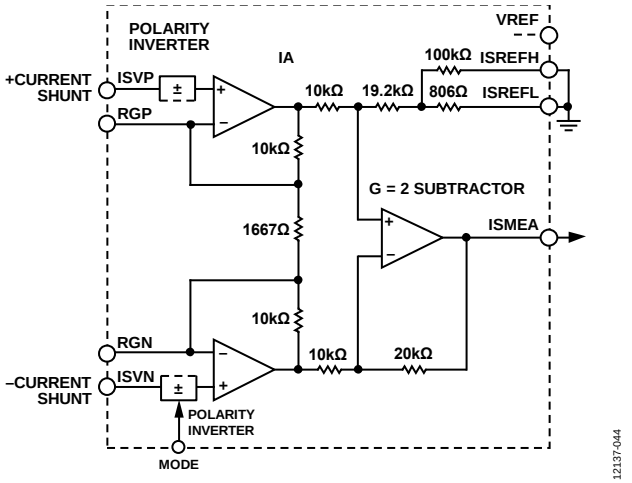


Figure 44. IA Simplified Block Diagram

IA Offset Option

As shown in Figure 44, the IA reference node is connected to the ISREFL and ISREFH pins via an internal resistor divider. This resistor divider can be used to introduce a temperature insensitive offset to the output of the IA such that it always reads a voltage higher than zero for a zero differential input. Because the output voltage of the IA is always positive, a unipolar analog-to-digital converter (ADC) can digitize it.

When the ISREFH pin is tied to the VREF pin with the ISREFL pin grounded, the voltage at the ISMEA pin is increased by 20 mV, guaranteeing that the output of the IA is always positive for zero differential inputs. Other voltage shifts can be realized by tying the ISREFH pin to an external voltage source. The gain from the ISREFH pin to the ISMEA pin is 8 mV/V. For zero offset, tie the ISREFL and ISREFH pins to ground.

Battery Reversal and Overvoltage Protection

The AD8451 IA can be configured for high-side or low-side current sensing. If the IA is configured for high-side current sensing (see Figure 43) and the battery is connected backward, the IA inputs may be held at a voltage that is below the negative power rail (AVEE), depending on the battery voltage.

To prevent damage to the IA under these conditions, the IA inputs include overvoltage protection circuitry that allows them to be held at voltages of up to 55 V from the opposite power rail. In other words, the safe voltage span for the IA inputs extends from AVCC − 55 V to AVEE + 55 V.

DIFFERENCE AMPLIFIER (DA)

Figure 45 is a block diagram of the DA, which is used to monitor the battery voltage. The architecture of the DA is a subtractor amplifier with a fixed gain of 0.8. This gain value allows the DA to funnel the voltage of a 5 V battery to a level that can be read by a 5 V ADC with a 4.096 V reference.

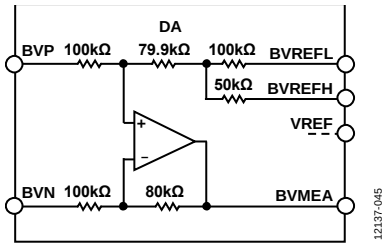


Figure 45. DA Simplified Block Diagram

The resistors that form the DA gain network are laser trimmed to a matching level better than ±0.1%. This level of matching minimizes the gain error and gain error drift of the DA while maximizing the CMRR of the DA. This matching also allows the controller to set a stable target voltage for the battery over temperature while rejecting the ground bounce in the battery negative terminal.

Like the IA, the DA can also level shift its output voltage via an internal resistor divider that is tied to the DA reference node. This resistor divider is connected to the BVREFH and BVREFL pins.

When the BVREFH pin is tied to the VREF pin with the BVREFL pin grounded, the voltage at the BVMEA pin is increased by 5 mV, guaranteeing that the output of the DA is always positive for zero differential inputs. Other voltage shifts can be realized by tying the BVREFH pin to an external voltage source. The gain from the BVREFH pin to the BVMEA pin is 2 mV/V. For zero offset, tie the BVREFL and BVREFH pins to ground.

CC AND CV LOOP FILTER AMPLIFIERS

The CC and CV loop filter amplifiers are high precision, low noise specialty amplifiers with very low offset voltage and very low input bias current. These amplifiers serve two purposes:

- Using external components, the amplifiers implement active loop filters that set the dynamics (transfer function) of the CC and CV loops.
- The amplifiers perform a seamless transition from CC to CV mode after the battery reaches its target voltage.

Figure 46 is the functional block diagram of the AD8451 CC and CV feedback loops for charge mode (MODE logic pin is high). For illustration purposes, the external networks connected to the loop amplifiers are simple RC networks configured to form single-pole inverting integrators. The outputs of the CC and CV loop filter amplifiers are coupled to the VINT pins via an analog NOR circuit (minimum output selector circuit), such that they can only pull the VINT node down. In other words, the loop amplifier that requires the lowest voltage at the VINT pins is in control of the node. Thus, only one loop amplifier, CC or CV, can be in control of the system charging control loop at any given time.

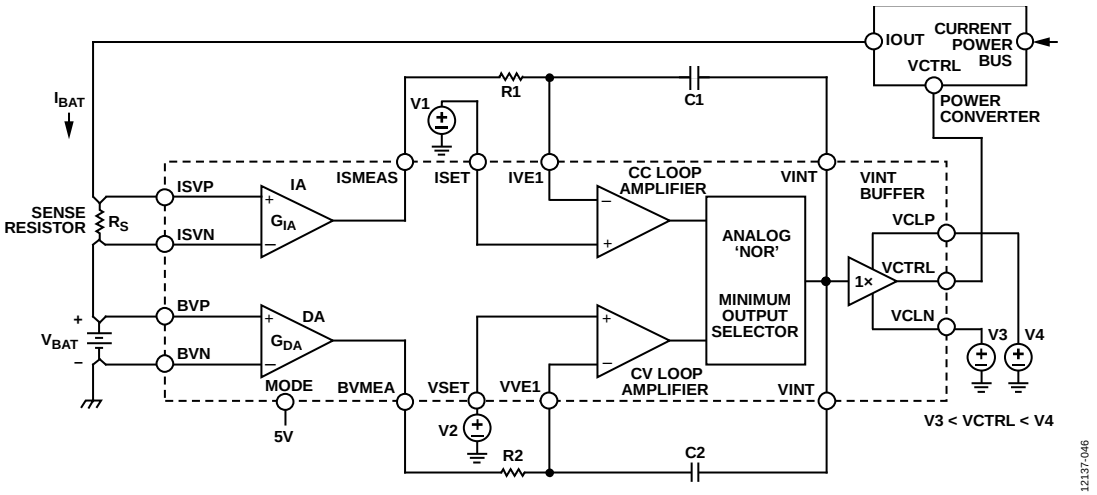


Figure 46. Functional Block Diagram of the CC and CV Loops in Charge Mode (MODE Pin High)

The unity-gain amplifier (VINT buffer) buffers the VINT pins and drives the VCTRL pin. The VCTRL pin is the control output of the AD8451 and the control input of the power converter. The V_{ISET} and V_{VSET} voltage sources set the target constant current and the target constant voltage, respectively. When the CC and CV feedback loops are in a steady state, the charging current is set at

$$I_{BAT_SS} = \frac{V_{ISET}}{G_{IA} \times R_S}$$

where:
I_{BAT_SS} = is the steady state charging current.
G_{IA} is the IA gain.
R_S is the value of the shunt resistor.

The target voltage is set at

$$V_{BAT_SS} = \frac{V_{VSET}}{G_{DA}}$$

where:
V_{BAT_SS} = steady state battery voltage.
G_{DA} is the DA gain.

Because the offset voltage of the loop amplifiers is in series with the target voltage sources, V_{ISET} and V_{VSET}, the high precision of these amplifiers minimizes this source of error.

Figure 47 shows a typical CC/CV charging profile for a Li-Ion battery. In the first stage of the charging process, the battery is charged with a CC of 1 A. When the battery voltage reaches a target voltage of 4.2 V, the charging process transitions such that the battery is charged with a CV of 4.2 V.

The following steps describe how the AD8451 implements the CC/CV charging profile (see Figure 46). In this scenario, the battery begins in the fully discharged state, and the system has just been turned on such that I_{BAT} = 0 A at Time 0.

1. Because the voltages at the ISMEA and BVMEA pins are less than the target voltages (V_{ISET} and V_{VSET}) at Time 0, both integrators begin to ramp, increasing the voltage at the VINT node.

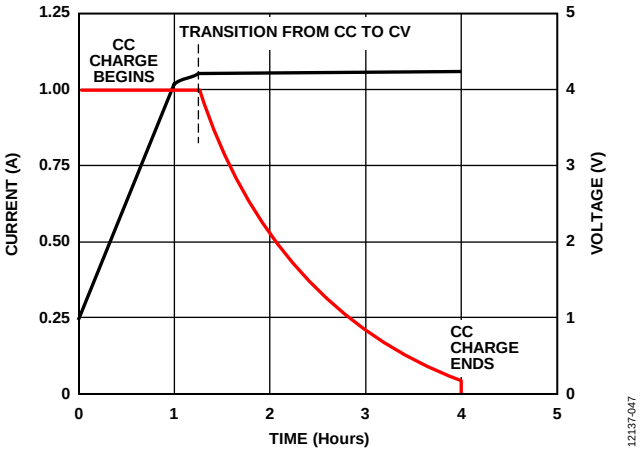


Figure 47. Representative Constant Current to Constant Voltage Transition near the End of a Battery Charging Cycle

2. As the voltage at the VINT node increases, the voltage at the VCRTL node rises, and the output current of the power converter, I_{BAT}, increases (assuming that an increasing voltage at the VCRTL node increases the output current of the power converter).
3. When the I_{BAT} current reaches the CC steady state value, I_{BAT_SS}, the battery voltage is still less than the target steady state value, V_{BAT_SS}. Therefore, the CV loop tries to keep pulling the VINT node up while the CC loop tries to keep it at its current voltage. At this point, the voltage at the ISMEA pin equals V_{ISET}; therefore, the CC loop stops integrating.
4. Because the loop amplifiers can only pull the VINT node down due to the analog NOR circuit, the CC loop takes control of the charging feedback loop, and the CV loop is disabled.
5. As the charging process continues, the battery voltage increases until it reaches the steady state value, V_{BAT_SS}, and the voltage at the BVMEA pin reaches the target voltage, V_{VSET}.

6. The CV loop tries to pull the VINT node down to reduce the charging current (I_{BAT}) and prevent the battery voltage from rising any further. At the same time, the CC loop tries to keep the VINT node at its current voltage to keep the battery current at I_{BAT_SS}.
7. Because the loop amplifiers can only pull the VINT node down due to the analog NOR circuit, the CV loop takes control of the charging feedback loop, and the CC loop is disabled.

The analog NOR (minimum output selector) circuit that couples the outputs of the loop amplifiers is optimized to minimize the transition time from CC to CV control. Any delay in the transition causes the CC loop to remain in control of the charge feedback loop after the battery voltage reaches its target value. Therefore, the battery voltage continues to rise beyond V_{BAT_SS} until the control loop transitions; that is, the battery voltage overshoots its target voltage. When the CV loop takes control of the charge feedback loop, it reduces the battery voltage to the target voltage. A large overshoot in the battery voltage due to transition delays can damage the battery; thus, it is crucial to minimize delays by implementing a fast CC to CV transition.

Figure 48 is the functional block diagram of the AD8451 CC and CV feedback loops for discharge mode (MODE logic pin is low). In discharge mode, the feedback loops operate in a similar manner as in charge mode. The only difference is in the CV loop amplifier, which operates as a noninverting integrator in discharge mode. For illustration purposes, the external networks connected to the loop amplifiers are simple RC networks configured to form single-pole integrators (see Figure 48).

Compensation

In battery formation and test systems, the CC and CV feedback loops have significantly different open-loop gain and crossover frequencies; therefore, each loop requires its own frequency compensation. The active filter architecture of the AD8451 CC and CV loops allows the frequency response of each loop to be set independently via external components. Moreover, due to the internal switches in the CC and CV amplifiers, the frequency response of the loops in charge mode does not affect the frequency response of the loops in discharge mode.

Unlike simpler controllers that use passive networks to ground for frequency compensation, the AD8451 allows the use of feedback networks for its CC and CV loop filter amplifiers. These networks enable the implementation of both proportional differentiator (PD) Type II and proportional integrator differentiator (PID) Type III compensators. Note that in charge mode, both the CC and CV loops implement inverting compensators, whereas in discharge mode, the CC loop implements an inverting compensator, and the CV loop implements a noninverting compensator. As a result, the CV loop in discharge mode includes an additional amplifier, VSET buffer, to buffer the VSET node from the feedback network (see Figure 48).

VINT Buffer

The unity-gain amplifier (VINT buffer) is a clamp amplifier that drives the VCTRL pin. The VCTRL pin is the control output of the AD8451 and the control input of the power converter (see Figure 46 and Figure 48). The output voltage range of this amplifier is bounded by the clamp voltages at the VCLP and VCLN pins such that

$$V_{VCLN} - 0.5\ V < V_{VCTRL} < V_{VCLP} + 0.5\ V$$

The reduction in the output voltage range of the amplifier is a safety feature that allows the AD8451 to drive devices such as the ADP1972 PWM controller, whose input voltage range must not exceed 5.5 V (that is, the voltage at the COMP pin of the ADP1972 must be below 5.5 V).

MODE PIN, CHARGE AND DISCHARGE CONTROL

The MODE pin is a TTL logic input that configures the AD8451 for either charge or discharge mode. A logic low (V_{MODE} < 0.8 V) corresponds to discharge mode, and a logic high (V_{MODE} > 2 V) corresponds to charge mode. Internal to the AD8451, the MODE pin toggles all single-pole, double throw (SPDT) switches in the CC and CV loop amplifiers and inverts the gain polarity of the IA.

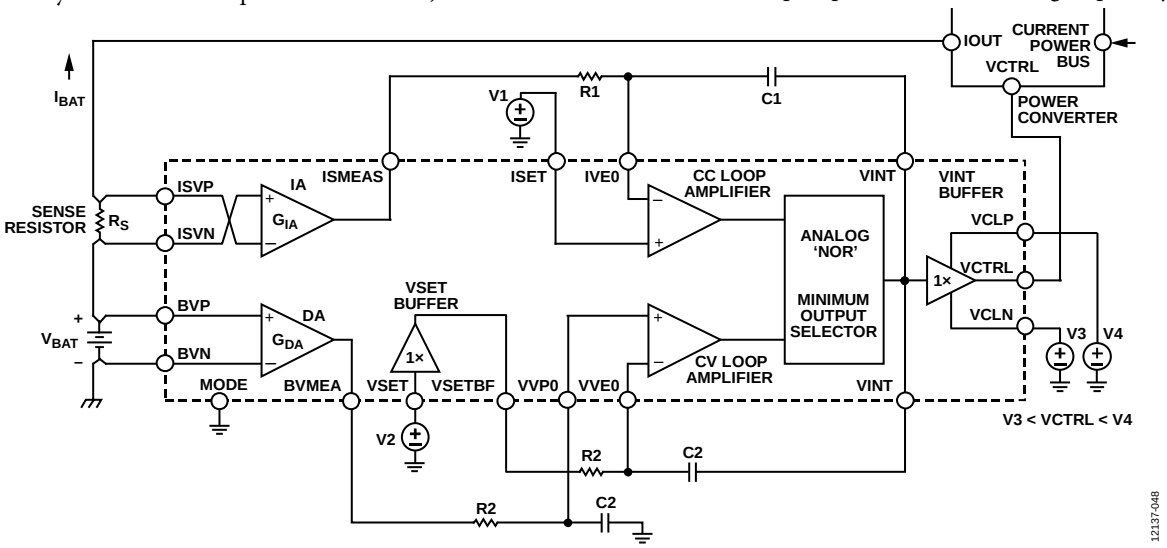


Figure 48. Functional Block Diagram of the CC and CV Loops in Discharge Mode (MODE Pin Low)

APPLICATIONS INFORMATION

This section describes how to use the AD8451 in the context of a battery formation and test system. This section includes a design example of a small scale model of an actual system.

FUNCTIONAL DESCRIPTION

The AD8451 is a precision analog front end and controller for battery formation and test systems. These systems use precision controllers and power stages to put batteries through charge and discharge cycles. Figure 49 shows the signal path of a simplified switching battery formation and test system using the AD8451 controller and the ADP1972 PWM controller. For more information on the ADP1972, see the ADP1972 data sheet.

The AD8451 is suitable for systems that form and test NiCad, NiMH, and Li-Ion batteries and is designed to operate in conjunction with both linear and switching power stages.

The AD8451 includes the following blocks (see Figure 42 and the Theory of Operation section for more information).

- A fixed gain IA that senses low-side or high-side battery current.
- A fixed gain DA that measures the terminal voltage of the battery.
- Two loop filter error amplifiers that receive the battery target current and voltage and establish the dynamics of the CC and CV feedback loops.
- A minimum output selector circuit that combines the outputs of the loop filter error amplifiers to perform automatic CC to CV switching.
- An output clamp amplifier that drives the VCTRL pin. The voltage range of this amplifier is limited by the voltage at the VCLP and VCLN pins such that it cannot overrange the subsequent stage. The output clamp amplifier can drive switching and linear power converters. Note that an increasing voltage at the VCTRL pin must translate to a larger output current in the power converter.
- A 2.5 V reference whose output node is the VREF pin.

A logic input pin (MODE) that changes the configuration of the controller from charge to discharge mode. A logic high at the MODE pin configures charge mode; a logic low configures discharge mode.

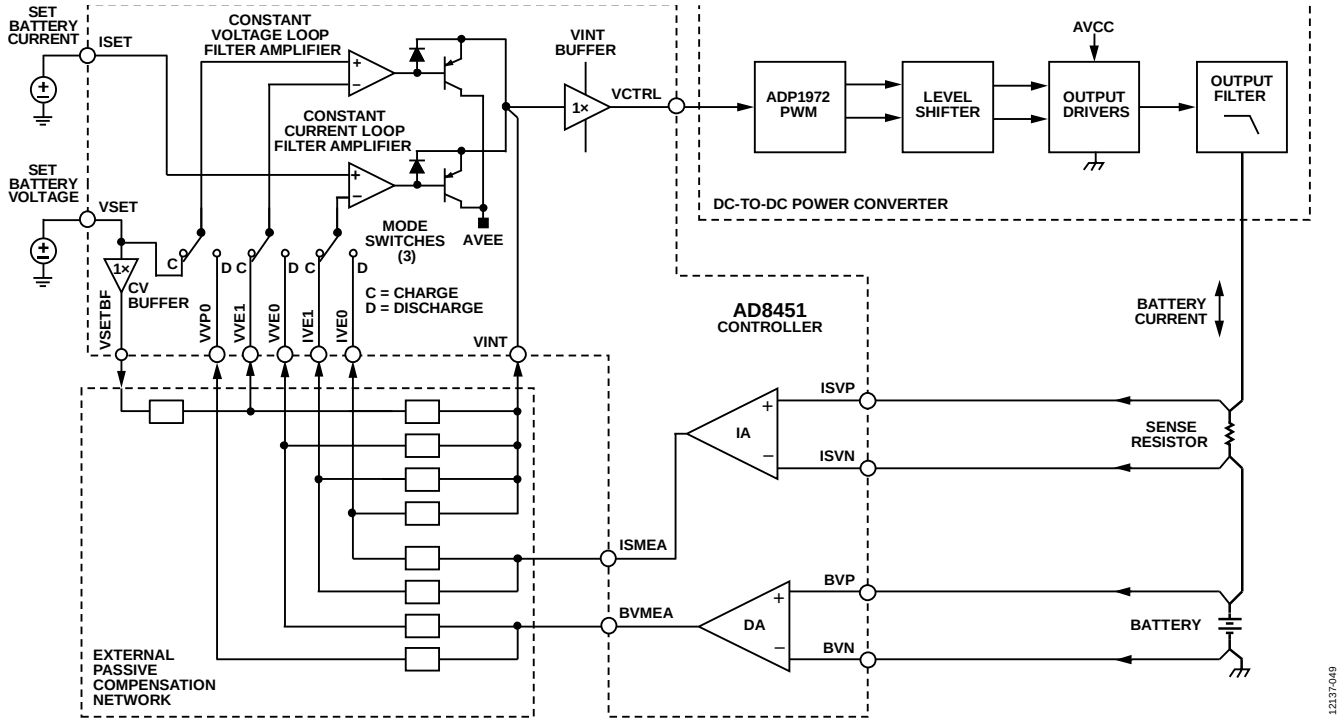


Figure 49. Complete Signal Path of a Battery Test or Formation System Suitable for Li-Ion Batteries

POWER SUPPLY CONNECTIONS

The AD8451 requires two analog power supplies (AVCC and AVEE), one digital power supply (DVCC), one analog ground (AGND), and one digital ground (DGND). AVCC and AVEE power all the analog blocks, including the IA, DA, and op amps, and DVCC powers the MODE input logic. AGND provides a reference and return path for the 2.5 V reference, and DGND provides a reference and return path for the digital circuitry.

The rated absolute maximum value for AVCC − AVEE is 36 V, and the minimum operating AVCC and AVEE voltages are +5 V and −5 V, respectively. Due to the high PSRR of the AD8451 analog blocks, AVCC can be connected directly to the high current power bus (the input voltage of the power converter) without risking the injection of supply noise to the controller outputs.

A commonly used power supply combination is +15 V for AVCC, −15 V for AVEE, and +5 V for DVCC. The +15 V rail for AVCC provides enough headroom to the IA such that it can be connected in a high-side current sensing configuration. The −15 V rail for AVEE allows the DA to sense accidental reverse battery conditions (see the Reverse Battery Conditions section).

Connect decoupling capacitors to all the supply pins. A 1 µF capacitor in parallel with a 0.1 µF capacitor is recommended.

CURRENT SENSE IA CONNECTIONS

For a description of the IA, see the Theory of Operation section, Figure 42, and Figure 44. The IA fixed gain is 26.

Current Sensors

Two common options for current sensors are isolated current sensing transducers and shunt resistors. Isolated current sensing transducers are galvanically isolated from the power converter and are affected less by the high frequency noise generated by switch mode power supplies. Shunt resistors are less expensive and easier to deploy.

If a shunt resistor sensor is used, a 4-terminal, low resistance shunt resistor is recommended. Two of the four terminals conduct the battery current, whereas the other two terminals conduct virtually no current. The terminals that conduct no current are sense terminals that are used to measure the voltage drop across the resistor (and, therefore, the current flowing through it) using an amplifier such as the IA of the AD8451. To interface the IA with the current sensor, connect the sense terminals of the sensor to the ISVP and ISVN pins of the AD8451 (see Figure 50).

Optional Low-Pass Filter

The AD8451 is designed to control both linear regulators and switching power converters. Linear regulators are generally noise free, whereas switch mode power converters generate switching noise. Connecting an external differential low-pass filter between the current sensor and the IA inputs reduces the injection of switching noise into the IA (see Figure 50).

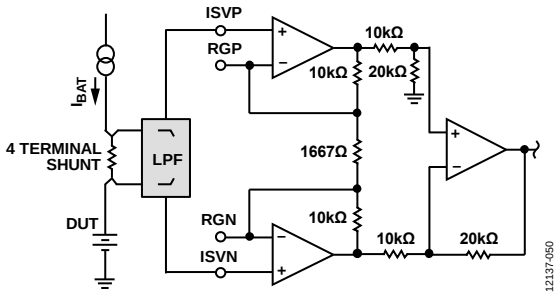


Figure 50. 4-Terminal Shunt Resistor Connected to the Current Sense IA

VOLTAGE SENSE DA CONNECTIONS

For a description of the DA, see the Theory of Operation section, Figure 42, and Figure 45. The DA fixed gain is 0.8.

Reverse Battery Conditions

The output voltage of the AD8451 DA can be used to detect a reverse battery connection. A −15 V rail for AVEE allows the output of the DA to go below ground when the battery is connected backward. Therefore, the condition can be detected by monitoring the BVMEA pin for a negative voltage.

BATTERY CURRENT AND VOLTAGE CONTROL INPUTS (ISET AND VSET)

The voltages at the ISET and VSET input pins set the target battery current and voltage for the CC and CV loops. These inputs must be driven by a precision voltage source (or a digital-to-analog converter [DAC] connected to a precision reference) whose output voltage is referenced to the same voltage as the IA and DA reference pins (ISREFH/ISREFL and BVREFH/BVREFL, respectively). For example, if the IA reference pins are connected to AGND, the voltage source connected to ISET must also be referenced to AGND. In the same way, if the DA reference pins are connected to AGND, the voltage source connected to VSET must also be referenced to AGND.

In constant current mode, when the CC feedback loop is in a steady state, the ISET input sets the battery current as follows:

$$I_{BAT_SS} = \frac{V_{ISET}}{G_{IA} \times R_S} = \frac{V_{ISET}}{26 \times R_S}$$

where:
G_{IA} is the IA gain.
R_S is the value of the shunt resistor.

In constant voltage mode, when the CV feedback loop is in steady state, the VSET input sets the battery voltage as follows:

$$V_{BAT_SS} = \frac{V_{VSET}}{G_{DA}} = \frac{V_{VSET}}{0.8}$$

where G_{DA} is the DA gain.

Therefore, the accuracy and temperature stability of the formation and test system are not only dependent on the precision of the AD8451, but also on the accuracy of the ISET and VSET inputs.

LOOP FILTER AMPLIFIERS

The AD8451 has two loop filter amplifiers, also known as error amplifiers (see Figure 49). One amplifier is for constant current control (CC loop filter amplifier), and the other amplifier is for constant voltage control (CV loop filter amplifier). The outputs of these amplifiers are combined using a minimum output selector circuit to perform automatic CC to CV switching.

Table 5 lists the inputs of the loop filter amplifiers for charge mode and discharge mode.

Table 5. Integrator Input Connections

Feedback Loop Function	Reference Input	Feedback Terminal
Control the Current While Discharging a Battery	ISET	IVE0
Control the Current While Charging a Battery	ISET	IVE1
Control the Voltage While Discharging a Battery	VSET	VVE0
Control the Voltage While Charging a Battery	VSET	VVE1

The CC and CV amplifiers in charge mode and the CC amplifier in discharge mode are inverting integrators, whereas the CV amplifier in discharge mode is a noninverting integrator. Therefore, the CV amplifier in discharge mode uses an extra amplifier, the VSET buffer, to buffer the VSET input pin (see Figure 42). In addition, the CV amplifier in discharge mode uses the VVP0 pin to couple the signal from the BVMEA pin to the integrator.

CONNECTING TO A PWM CONTROLLER (VCTRL PIN)

The VCTRL output pin of the AD8451 is designed to interface with linear power converters and with PWM controllers such as the ADP1972. The voltage range of the VCTRL output pin is bound by the voltages at the VCLP and VCLN pins, as follows:

$$V_{VCLN} - 0.5\ V < V_{VCTRL} < V_{VCLP} + 0.5\ V$$

Because the maximum rated input voltage at the COMP pin of the ADP1972 is 5.5 V, connect the clamp voltages of the output amplifier to 5 V (VCLP) and ground (VCLN) to prevent over-ranging of the COMP input. As an additional precaution, install an external 5.1 V Zener diode from the COMP pin to ground with a series 1 kΩ resistor connected between the VCTRL and COMP pins. Consult the ADP1972 data sheet for additional applications information.

Given the architecture of the AD8451, the controller requires that an increasing voltage at the VCTRL pin translates to a larger output current in the power converter. If this is not the case, a unity-gain inverting amplifier can be added in series with the AD8451 output to add an extra inversion.

STEP-BY-STEP DESIGN EXAMPLE

This section describes the systematic design of a 1 A battery charger/discharger using the AD8451 controller and the ADP1972 PWM controller. The power converter used in this design is a nonisolated buck boost dc-to-dc converter. The target battery is a 4.2 V fully charged, 2.7 V fully discharged Li-Ion battery.

Step 1: Design the Switching Power Converter

Select the switches and passive components of the buck boost power converter to support the 1 A maximum battery current. The design of the power converter is beyond the scope of this data sheet; however, there are many application notes and other helpful documents available from manufacturers of integrated driver circuits and power MOSFET output devices that can be used for reference.

Step 2: Identify the Control Voltage Range of the ADP1972

The control voltage range of the ADP1972 (voltage range of the COMP input pin) is 0.5 V to 4.5 V. An input voltage of 4.5 V results in the highest duty cycle and output current, whereas an input voltage of 0.5 V results in the lowest duty cycle and output current. Because the COMP pin connects directly to the VCTRL output pin of the AD8451, the battery current is proportional to the voltage at the VCTRL pin.

For information about how to interface the ADP1972 to the power converter switches, see the ADP1972 data sheet.

Step 3: Determine the Control Voltage for the CV Loop

The relationship between the control voltage for the CV loop (the voltage at the VSET pin), the target battery voltage, and the DA gain is as follows:

$$CV\ Battery\ Target\ Voltage = \frac{V_{VSET}}{G_{DA}} = \frac{V_{VSET}}{0.8}$$

In charge mode, for a CV battery target voltage of 4.2 V, select a CV control voltage of 3.36 V. In discharge mode, for a CV battery target voltage of 2.7 V, select a CV control voltage of 2.16 V.

Step 4: Determine the Control Voltage for the CC Loop and the Shunt Resistor

The relationship between the control voltage for the CC loop (the voltage at the ISET pin), the target battery current, and the IA gain is as follows:

$$CC\ Battery\ Target\ Current = \frac{V_{ISET}}{G_{IA} \times R_S} = \frac{V_{ISET}}{26 \times R_S}$$

The voltage across the shunt resistor is as follows:

$$Shunt\ Resistor\ Voltage = \frac{V_{ISET}}{G_{IA}} = \frac{V_{ISET}}{26}$$

For target current of 1 A, choosing a 20 mΩ shunt resistor results in a control voltage of 4 V.

When selecting a shunt resistor, consider the resistor style and construction. For low power dissipation applications, many temperature stable SMD styles can be soldered to a heat sink pad on a printed circuit board (PCB). For optimum accuracy, choose a shunt resistor that provides force and sense terminals. In these resistors, the battery current flows through the force terminals and the voltage drop in the resistor is read at the sense terminals.

Step 5: Choose the Control Voltage Sources

The input control voltages (the voltages at the ISET and VSET pins) can be generated by an analog voltage source such as a voltage reference or by a DAC. In both cases, select a device that provides a stable, low noise output voltage. If a DAC is preferred, Analog Devices offers a wide range of precision converters. For example, the AD5668 16-bit DAC provides up to eight 0 V to 4 V sources when connected to an external 2 V reference.

To maximize accuracy, the control voltage sources must be referenced to the same potential as the outputs of the IA and DA. For example, if the IA and DA reference pins are connected to AGND, connect the reference pins of the control voltage sources to AGND.

Step 6: Select the Compensation Devices

Feedback controlled switching power converters require frequency compensation to guarantee loop stability. There are many references available about how to design the compensation for such power converters. The AD8451 provides active loop filter error amplifiers for the CC and CV control loops that can implement proportional integrator (PI), PD, and PID compensators using external passive components.

EVALUATION BOARD

INTRODUCTION

The AD8451-EVALZ evaluation board is a convenient standalone platform for evaluating the major elements of the AD8451, either as a standalone component or connected to a battery test/formation system.

In the latter configuration, the AD8451-EVALZ operates just as it would within a system including the PWM and dc-to-dc power converter. Simply connect the current and voltage sense voltages from the system directly to the board terminus. This feature is used when setting or evaluating loop compensation using a field of passive compensation components. Figure 51 is a photograph of the AD8451-EVALZ.

FEATURES AND TESTS

SMA connectors provide access for input voltages to the sensitive instrumentation (IA) and difference (DA) amplifiers. ISVP and ISVN connectors are the IA inputs, and BVP and BVN are the DA inputs. These inputs accept the dc voltages from battery current and voltage measurement sources, or from a precision dc voltage source. SMA connectors ISET and VSET are available for precision dc control voltages for CC or CV battery charging voltages. SMA ISREFLO is available for applying a nonzero reference voltage to the IA. SMA VCTRL connects to the input of a dc-to-dc power converter as seen in Figure 52. Convenient test loops are provided connecting scope probes or instruments for the remainder of the input/output.

The MODE switch selects between the charge and discharge option. Figure 52 is a schematic of the AD8451-EVALZ. Table 6 lists and describes the various switches and functions.

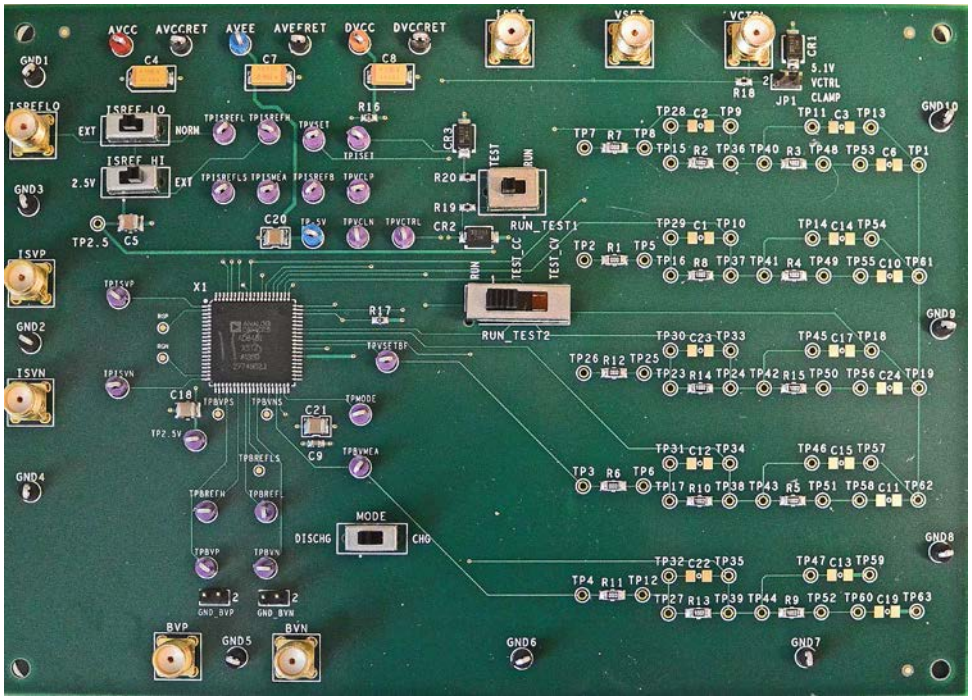


Figure 51. Photograph of the AD8451-EVALZ

Table 6. AD8451-EVALZ Test Switches and Functions

Switch	Function	Operation	Default Position
MODE	Selects the charge or the discharge mode.	The MODE switch selects CHG (logic high) or DISCH (logic low).	CHG
RUN_TEST1	Selects between the user inputs and the 2.5 V AD8451 reference voltage.	The AD8451 operates normally when the **RUN_TEST1** switch is in the **RUN** position. When in the **TEST** position, 2.5 V is applied to the ISET and VSET inputs.	RUN
RUN_TEST2	Tests the CC or CV loop filter amplifiers.	The voltage at the VCTRL output (TPVCTRL) for all positions is 0 V when **RUN_TEST1** is in **RUN** position and 2.5 V when **RUN_TEST1** in **TEST** position.	RUN
ISREF_HI	The ISREF_HI switch connects Pin 74 (ISREFH) to the internal 2.5 V reference (2.5 position) or to the SMA connector **EXT** (the external input for a user defined VREF input).	When in the **2.5V** position, the **ISREF_HI** switch connects Pin 74 (ISREFH, an internal 100 kΩ resistor) to Pin 73 (VREF, the 2.5 V reference). When the **ISREF_LO** switch is in the **NORM** position, the output at Pin 71 (ISMEA) shifts positive by 20 mV.	EXT
ISREF_LO	Connects Pin 76 (ISREFL) to ground (NORM) or to the ISREFL SMA input connector.	When in the **NORM** position and the ISREF_HI switch is in the **EXT** position, there is no offset applied to the ISMEA output. When in the **EXT** position, the ISREFLO SMA is selected.	NORM

EVALUATING THE AD8451

Test the Instrumentation Amplifier

Connect the TPISVN jumper to ground, and then apply 100 mV dc to TPISVP. Measure 2.6 V at the TPISMEA output. Subtract any offset voltages from the output reading before calculating the gain.

20 mV Offset at IMEAS Output

Connect a jumper from TPISVP to TPISVN to ground by using another jumper and any one of the convenient black test loops. Measure 0 V ± 2.86 mV at the TPISMEA output (that is, the IA residual offset voltage multiplied by gain). Move the ISREFLO switch to the **EXT** position, and the ISREFHI switch to the 20 mV (**EXT**) position. The output will then increase by 20 mV.

Test the Difference Amplifier

Insert a shorting jumper at Header GND_BVN. With 1 V dc applied to TPBVP, measure 0.8 V at TPBVMEA. For the most accurate gain measurement, subtract the offset voltage from the output voltage before calculating gain.

5 mV Offset at BVMEAS Output

Insert jumpers in the GND_BVP and GND_BVN headers. Measure 0 V ± 0.4mV at the TPBVMEA output (that is, the DA residual offset voltage multiplied by gain). Connect a jumper between TPBREFH and TP2.5V. The output will then increase by 5 mV.

CC and CV Integrator Tests

Switches RUN_TEST1 and RUN_TEST2 set up the required circuit conditions to test the integrators. RUN_TEST1 disconnects the external inputs ISET and VSET and applies 2.5 V dc from the reference, simultaneously, to both of the CC and CV.

RUN_TEST2 has three positions: **RUN**, **TEST_CC**, and **TEST_CV**.

Loop Compensation

The AD8451-EVALZ is suitable for use as a test platform for system loop compensation experiments. However, before installing the platform in a system, component changes are necessary.

Note the four compensation networks, CC-CHARGE, CC-DISCHARGE, CV-CHARGE, and CV-DISCHARGE, located on the right-hand side of the schematic shown in Figure 52. To make it easier to locate these components, the configuration of these networks on the AD8451-EVALZ PCB approximates that shown in the schematic (see Figure 52). Each of the components locations accommodates both standard, 1206 size, surface-mount chip resistors and capacitors or leaded components inserted into the pairs of TP thru holes spanning the SM footprints. The TP holes accept the popular 0.025" test pins if leaded devices are preferred for multiple loop tests.

As shipped, CC and CV loop amplifier filters are configured as voltage followers by replacing feedback capacitors to the inverting inputs with resistors, and removing the dc coupling resistors from the IA and DA outputs. The feedback loops must be reconfigured to close the loops to operate as precision feedback loops.

Loop compensation requires knowledge of the output dc-to-dc power converter. It is assumed that the AD8451 is most often used with a switching converter. The scope and breadth of this switching converter design architecture is quite broad, and a thorough discussion of all the types and variants of this type of converter is well beyond the scope of this data.

When the circuit and component details of the power converter are known, proceed with a calculation of the loop parameters and components, and the values necessary to achieve loop compensation.

Because the loop is of the type proportional/integrating (PI), a direct dc path is required from the IA and DA amplifiers to the error inputs of the CC and CV loop amplifiers. Install these resistors at the R1, R6, R7, R11, and R12 locations.

Likewise, the CC and CV amplifiers must be reconfigured from voltage followers to integrators by replacing the 0 Ω capacitors at C6, C10, C11, C19, and C24 with appropriate capacitors.

SCHEMATIC AND ARTWORK

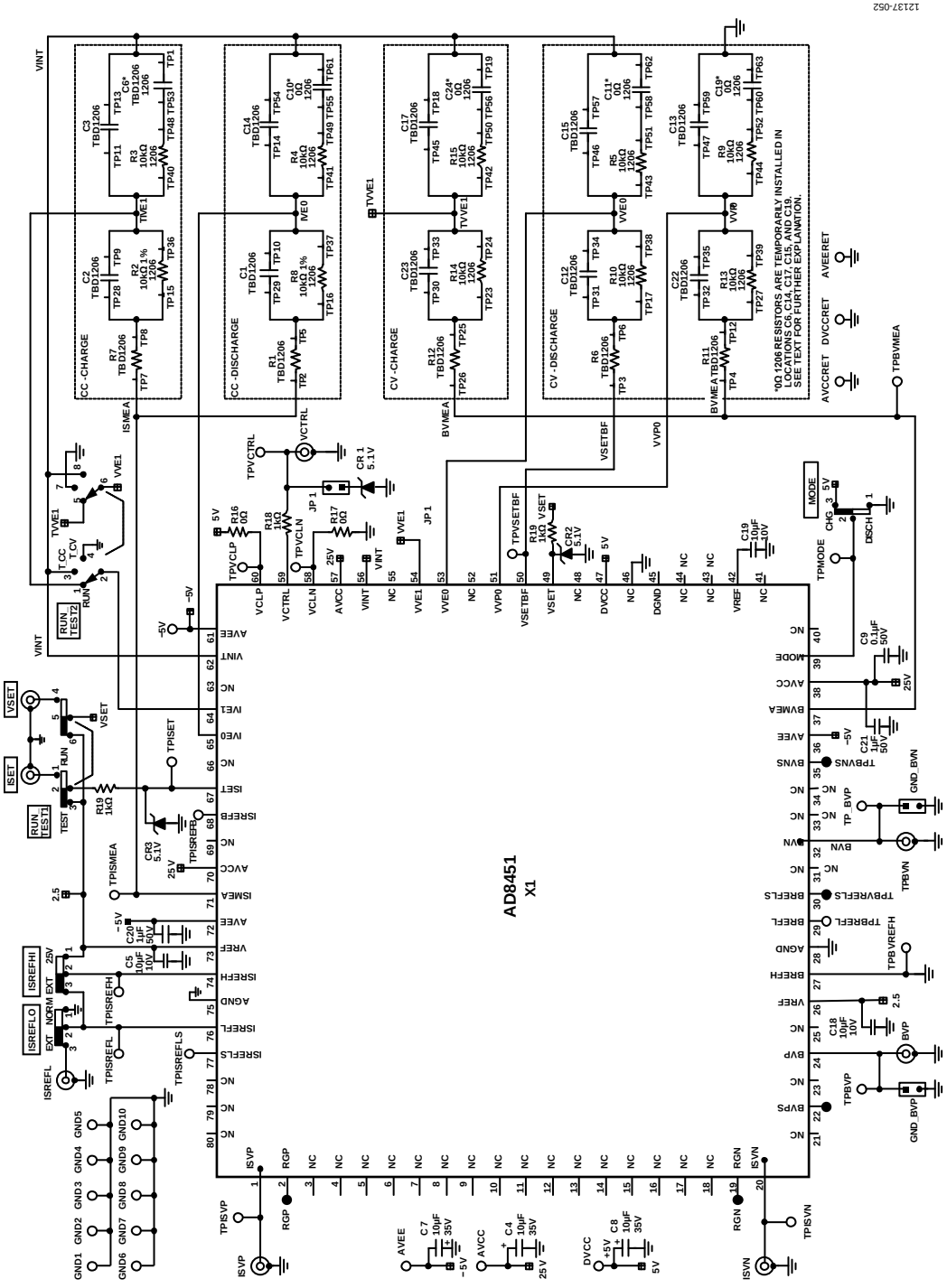


Figure 52. AD8451-EVALZ Schematic

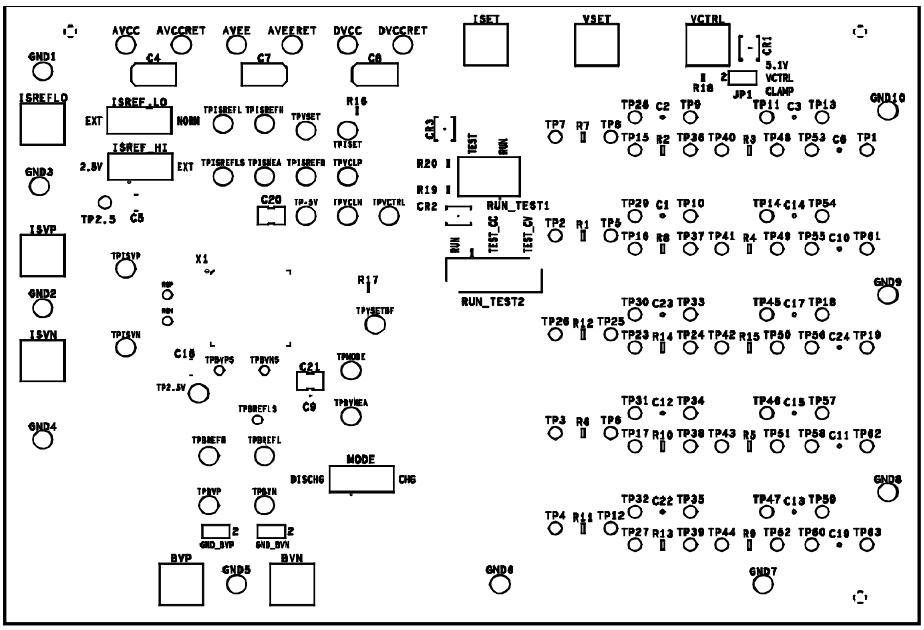


Figure 53. AD8451-EVALZ Top Silkscreen

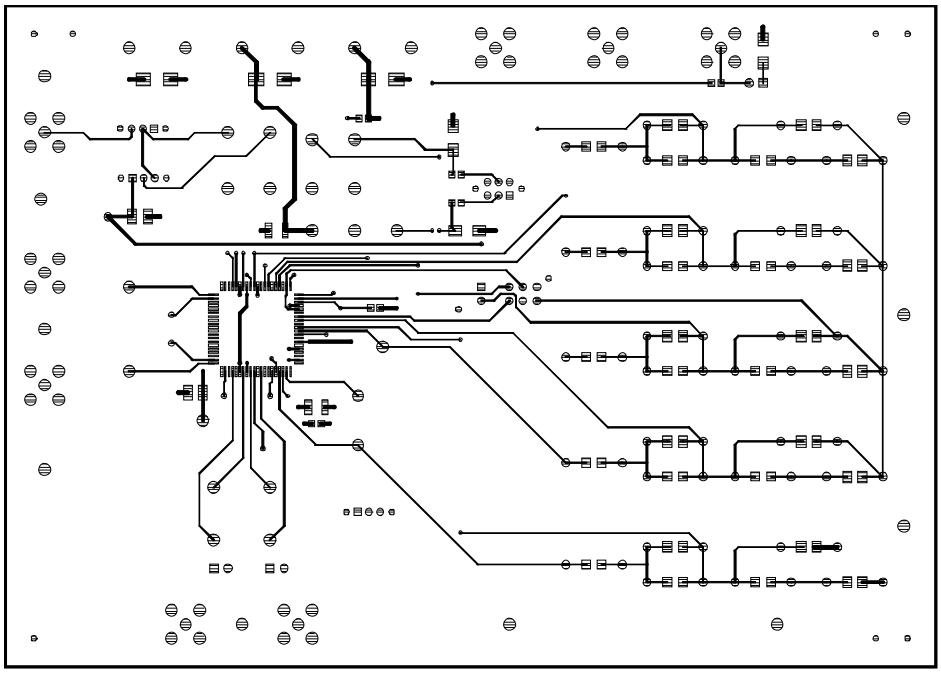


Figure 54. AD8451-EVALZ Primary Side Copper

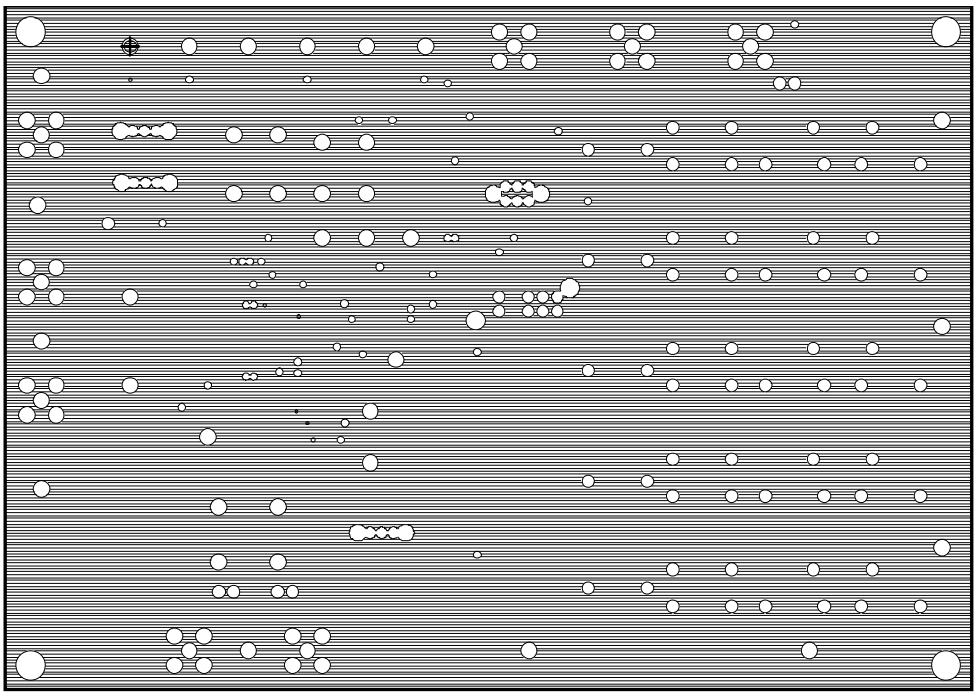


Figure 55. AD8451-EVALZ Secondary Side Copper

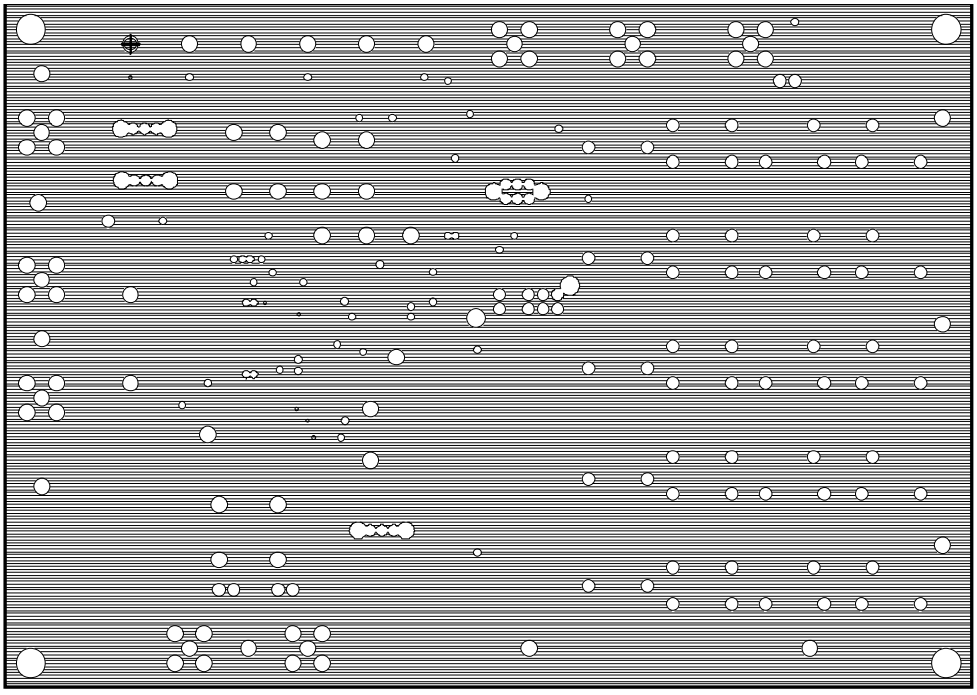


Figure 56. AD8451-EVALZ Power Plane

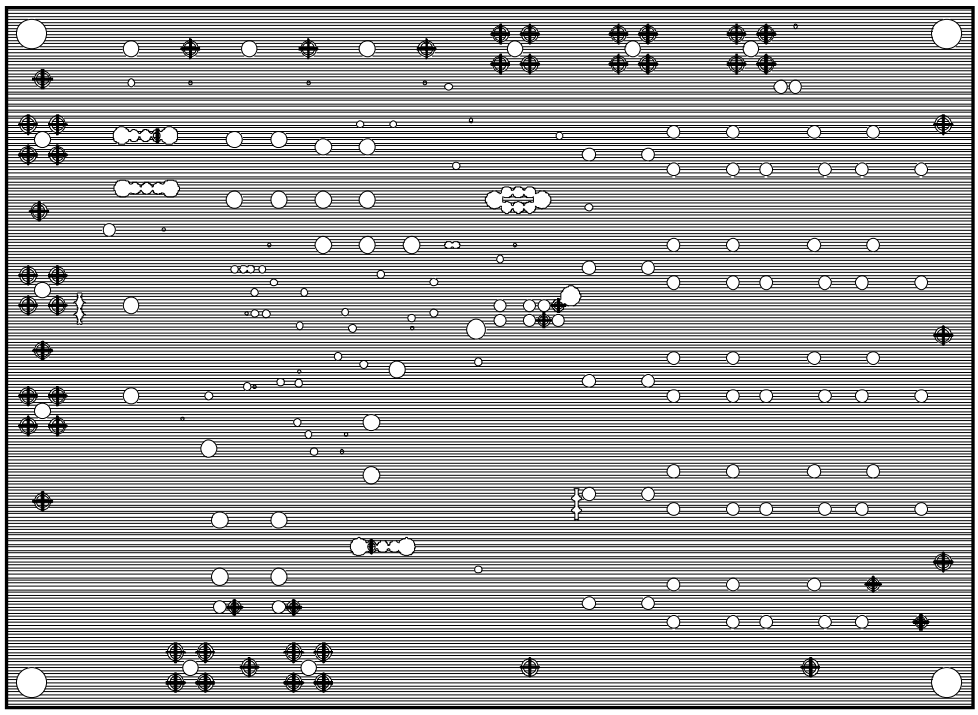
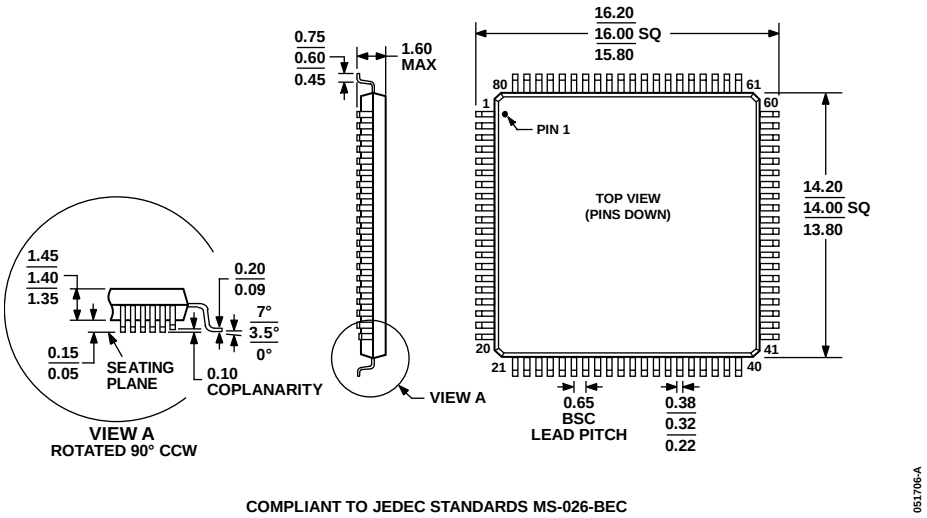


Figure 57. AD8451-EVALZ Ground Plane

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BEC

Figure 58. 80-Lead Low Profile Quad Flat Package [LQFP]
(ST-80-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8451ASTZ	−40°C to +85°C	80-Lead LQFP	ST-80-2
AD8451ASTZ-RL	−40°C to +85°C	80-Lead LQFP	ST-80-2
AD8451-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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