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Devices Connected/Referenced

ADL5356	1.2 GHz to 2.5 GHz, Dual-Balanced Mixer, LO Buffer, IF Amplifier, and RF Balun
AD8376	Ultralow Distortion IF Dual VGA
AD9258	14-Bit, 125 MSPS, 1.8 V Dual ADC
AD9517-4	12-Output Clock Generator with Integrated 1.6 GHz VCO

High Performance, Dual Channel IF Sampling Receiver

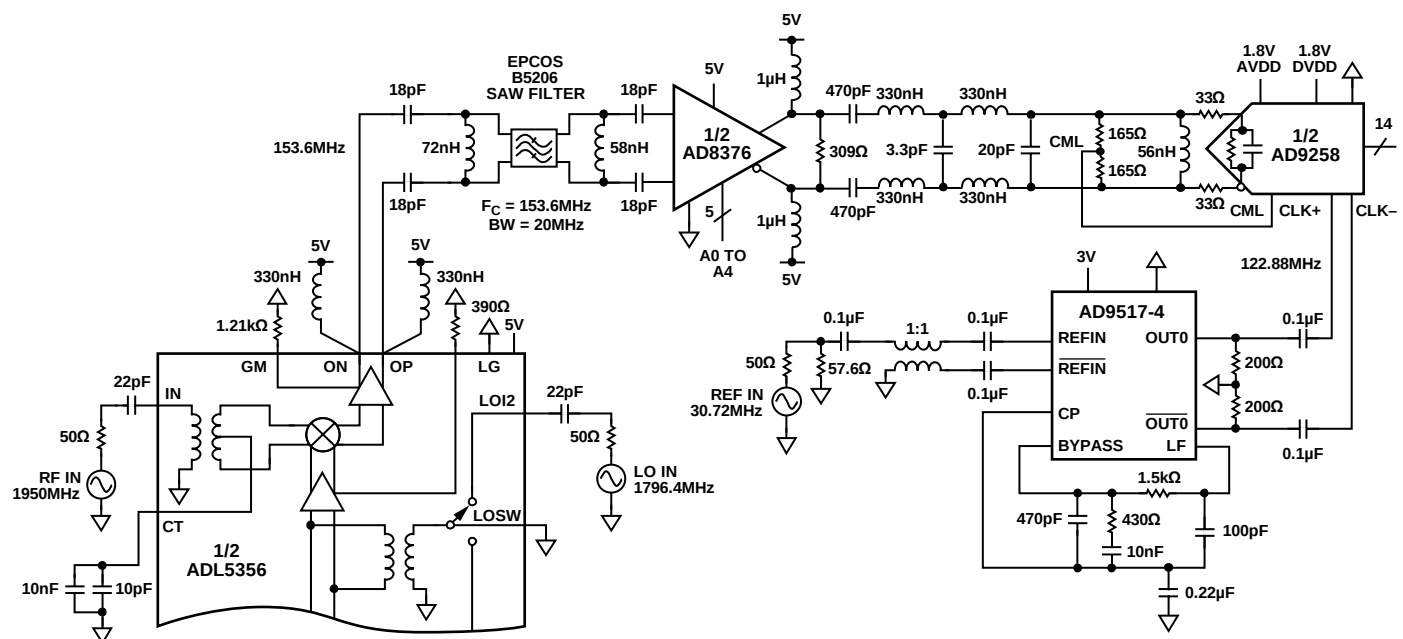
CIRCUIT FUNCTION AND BENEFITS

This circuit is a high performance, dual channel IF sampling receiver, also called a “main” and “diversity” receiver in base station terminology. The downconverting receiver uses a single IF frequency of 153.6 MHz and includes a dual downconverting mixer, digitally controlled dual VGA, dual ADC, and clock synthesizer. The circuit takes an incoming RF waveform and outputs a dual 14-bit resolution digital data stream. It is optimized for high frequency IF sampling and provides exceptional spurious-free dynamic range (SFDR) performance of 79.61 dBc with a sampling rate of 122.88 MSPS at the high gain setting.

CIRCUIT DESCRIPTION

This circuit includes the RF front end, as well as the IF sampling receiver. It is composed of a dual balanced mixer, broadband IF SAW filter, digitally controlled dual VGA, and dual ADC. The circuit also includes a synthesizer, which generates the ADC sampling clock.

The [ADL5356](#) dual balanced mixer is designed to downconvert radio frequencies (RF) primarily between 1200 MHz and 2500 MHz to lower intermediate frequencies (IF) between 30 MHz and 450 MHz.



NOTES

- ALL PINS AND CONNECTIONS TO ADL5356, AD8376, AD9258 AND AD9417 NOT SHOWN. CONSULT PRODUCT DATA SHEETS FOR DETAILED INFORMATION.

Figure 1. Broadband Dual Channel IF Sampling Receiver (Simplified Schematic: Only One-Half of the Receiver Is Shown. All Connections and Decoupling Not Shown)

Rev. 0

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The RF and LO input ports are already ac-coupled to prevent nonzero dc voltages from damaging the RF balun or LO input circuits, which are part of the ADL5356. The ADL5356 is configured for single-ended LO operation with a recommended LO drive of 0 dBm. With the LOSW pin of the mixer grounded, only one of the two LO channels (LOI2) is used in this circuit.

The mixer differential IF interface requires pull-up choke inductors to bias the open-collector outputs and to set the output impedance match. The shunting impedance of the choke inductors used to couple dc current into the IF amplifier should be selected to provide the desired output return loss. The real part of the mixer output impedance is approximately 200 Ω , which matches many commonly used SAW filters without the need for a transformer.

The receiver channel filtering is mainly performed by a 153.6 MHz, 20 MHz bandwidth Epcos model B5206 SAW filter which follows the mixer. The typical insertion loss (IL) of this filter is about 9 dB. The natural matched impedance of this SAW filter is 100 Ω differential. A simple L-C reactive network matches the SAW filter to the mixer 200 Ω differential output and the AD8376 VGA 150 Ω differential input impedance.

Table 1 highlights the cascaded performance of the dual mixer plus SAW filter. Note that IP3 is the third-order intercept point; IP1dB is the input referred -1 dB compression point; and NF is the noise figure.

A receiver gain control of 24 dB is provided by the AD8376 dual, high output linearity VGA that is optimized for ADC interfacing. Two independent 5-bit binary codes change each attenuator setting in 1 dB steps such that the gain of each amplifier can be set from +20 dB to -4 dB. The output third order intercept point (IP3) and noise floor essentially remain constant across the 24 dB available gain range. This is a valuable feature in a variable gain receiver where it is desirable to maintain a constant instantaneous dynamic range as the receiver gain is modified. The output IP3 of the AD8376 and the subsequent antialiasing filter is in excess of 50 dBm with a 2 V p-p composite signal.

The AD8376 provides a 150 Ω input impedance and is tuned to drive a 150 Ω load impedance. The open-collector output structure requires dc bias through an external bias network. A set of 1 μ H choke inductors are used on each channel output to

provide bias to the open-collector output pins. An optimized differential fourth order band-pass antialiasing filter is implemented at the DGA outputs before analog-to-digital conversion. Note that the antialiasing filter is terminated with shunt input and output resistances of about 300 Ω . The shunt resistances at either end of the filter, 309 Ω at the input and 330 Ω (through two 165 Ω bias setting resistors) at the output, combine to present the AD8376 with a nominal 150 Ω load impedance.

The band-pass antialiasing attenuates the output noise of the AD8376 outside of the intended Nyquist zone. In general, the SNR improves several dB by including a reasonable order antialiasing filter. The antialiasing filter is comprised of a fourth order Butterworth filter with a resonant tank circuit. The resonant tank helps ensure that the ADC input looks like a real resistance at the target center frequency by resonating out the capacitive portion of the ADC load (see AN-742 and AN-827 application notes). In addition, the ac-coupling capacitors and the bias chokes introduce additional zeros into the transfer function. The overall frequency response takes on a band-pass characteristic, helping to reject noise outside of the intended Nyquist zone. The filter provides a 20 MHz pass band centered at 153.6 MHz with 0.3 dB flatness and an insertion loss of about 3 dB.

The ADC utilized is the 14-bit AD9258, which samples at rates up to 125 MSPS. The AD9258's analog inputs are driven by the AD8376 through the band-pass antialiasing filter. The ADC sampling rate is set to 122.88 MSPS with a full-scale input range of 2 V p-p. The AD9258 differential clock signal is provided by the AD9517-4, a clock generation IC with on-chip VCO. The LVPECL level output, OUT0, is used for low jitter. The AD9517-4 uses its internal VCO frequency of 1474.56 MHz to derive the 122.88 MHz output clock to the ADC. A loop filter, designed with the ADISimCLK™ simulation software, provides a 60 kHz cutoff frequency and 50° of phase margin, giving timing jitter of about 160 fs rms. This jitter corresponds to a theoretical SNR of 76 dB, assuming a 153.6 MHz input, using the formula $SNR = 20 \log(1/2\pi \times f_{IN} \times t_j)$.

Using this circuit, exceptional SFDR performance of 79.61 dBc at 153.6 MHz is achieved at maximum gain, as shown in Figure 2.

Table 1. Cascaded performance of the dual mixer plus SAW filter (RF = 1950 MHz, LO = 1796.4 MHz, IF = 153.6 MHz, RF power = -10 dBm, LO power = 0 dBm)

	Gain (dB)	IP3 (dBm)	IP1dB (dBm)	NF (dB)
ADL5356	8.2	30.0	11.5	9.7
ADL5356 + SAW	-0.3	28.6	11.7	10.9

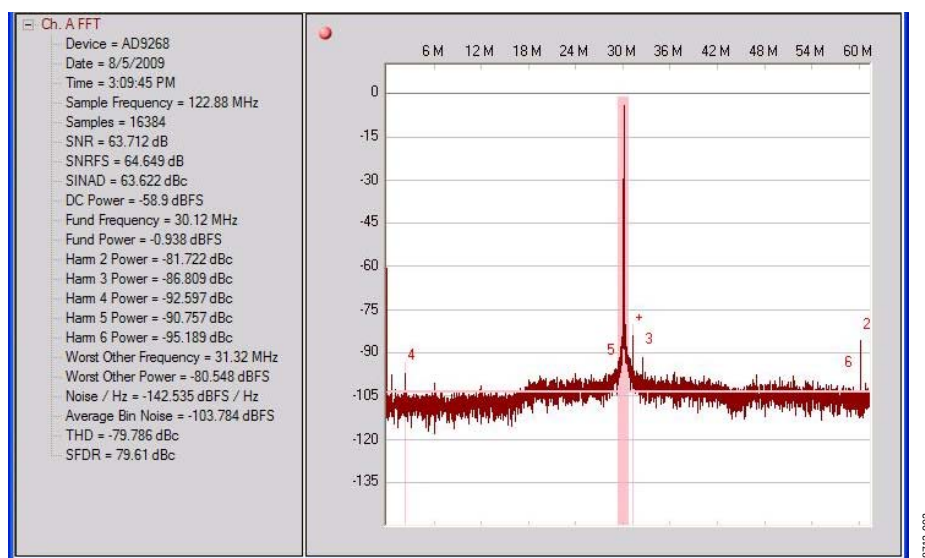


Figure 2. Measured Single-Tone Performance of the Circuit in Figure 1 for a 1950 MHz RF Input Signal. Sampling Frequency = 122.88 MSPS, IF Input = 153.6 MHz

COMMON VARIATIONS

Front-end LNAs and attenuators are not included in this circuit but can easily be interfaced to the 50 Ω single-ended RF inputs of the ADL5356 mixer. For a complete receiver design, [ADL5521/ADL5523](#) LNAs may be incorporated.

The standard configuration using the ADL5356 allows reception of RF signals from 1.2 GHz to 2.4 GHz, but it is possible to use the [ADL5358](#) mixer, which covers RF input frequencies from 500 MHz to 1700 MHz.

An Epcos (www.epcos.com) SAW filter follows the mixer and provides the necessary channel selectivity over a bandwidth ranging from 20 MHz to 40 MHz, depending on the chosen filter. The circuit shown uses a 20 MHz bandwidth, 153.6 MHz centered SAW filter (part number: B5206) but can also accommodate other pin-compatible filters.

Some empirical optimization may be needed to help compensate for actual PCB parasitics in SAW filter matching and antialias filter implementation. Details of designing the interstage filters can be found in the [AN-742](#) and [AN-827](#) application notes.

To ensure repeatability of band response, 1% capacitors are recommended for the SAW filter matching components and the antialiasing filter. In addition, Coilcraft 0603CS or similar inductors are recommended. Other resistors, capacitors, and inductors can be 10% values.

Excellent layout, grounding, and decoupling techniques must be utilized in order to achieve the desired performance from the circuits discussed in this note. As a minimum, a 4-layer PCB should be used with one ground plane layer, one power plane layer, and two signal layers.

All IC power pins must be decoupled to the ground plane with low inductance multilayer ceramic capacitors (MLCC) of 0.01 μ F to 0.1 μ F (for simplicity, not shown in the diagrams). Follow the recommendations on the individual data sheets and in [Tutorial MT-101](#).

The product evaluation boards should be consulted for recommended layout and critical component placement. These can be accessed through the product pages for the devices.

Even though the AD8376 and AD9258 (or other ADC) may be powered from different supplies, sequencing is not an issue because the input signal to the ADC is ac-coupled.

The individual data sheet for the ADC should be consulted regarding the proper sequencing of the AVDD and the DVDD power supplies (if separate supplies are used).

LEARN MORE

AN-742 Application Note, *Frequency Domain Response of Switched Capacitor ADCs*, Analog Devices.

AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*, Analog Devices.

CN-0002 Circuit Note, *Using the AD8376 VGA to Drive Wide Bandwidth ADCs for High IF AC-Coupled Applications*, Analog Devices.

CN-0046 Circuit Note, *An Ultra Low Distortion Differential RF/IF Front-End for High Speed ADCs*, Analog Devices.

Kester, Walt. *High Speed System Applications*, Chapter 2 "Optimizing Data Converter Interfaces," Analog Devices, 2006.

MT-007 Tutorial, *Aperture Time, Aperture Jitter, Aperture Delay Time—Removing the Confusion*, Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-073 Tutorial, *High Speed Variable Gain Amplifiers (VGAs)*, Analog Devices.

MT-075 Tutorial, *Differential Drivers for High Speed ADCs Overview*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Data Sheets and Evaluation Boards

AD8376 Data Sheet

AD9258 Data Sheet

AD9258 Evaluation Board

AD9517-4 Data Sheet

AD9517-4 Evaluation Board

ADL5356 Data Sheet

ADL5356 Evaluation Board

REVISION HISTORY

1/10—Revision 0: Initial Version

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