Ultralow Distortion IF VGA

Data Sheet

AD8375

FEATURES

Bandwidth of 630 MHz (−3 dB)
Gain range: −4 dB to +20 dB
Step size: 1 dB ± 0.2 dB
Differential input and output
Noise figure: 8 dB @ maximum gain
Output IP3 of ~50 dBm at 200 MHz
Output P1dB of 19 dBm at 200 MHz
Provides constant SFDR vs. gain
Parallel 5-bit control interface
Power-down feature
Single 5 V supply operation
24-lead, 4 mm × 4 mm LFCSP

APPLICATIONS

Differential ADC drivers
High IF sampling receivers
Wideband multichannel receivers
Instrumentation

FUNCTIONAL BLOCK DIAGRAM

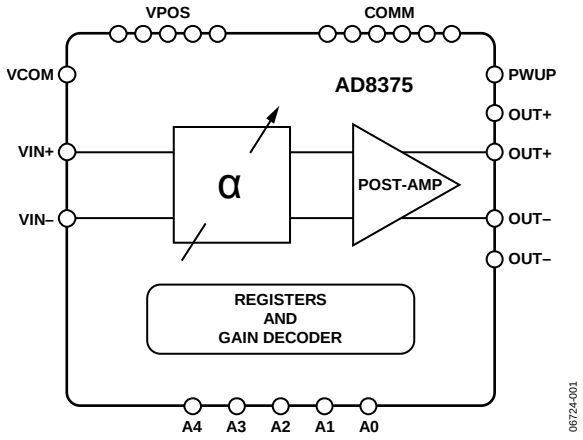


Figure 1.

GENERAL DESCRIPTION

The AD8375 is a digitally controlled, variable gain, wide bandwidth amplifier that provides precise gain control, high IP3, and low noise figure. The excellent distortion performance and high signal bandwidth make the AD8375 an excellent gain control device for a variety of receiver applications.

Using an advanced high speed SiGe process and incorporating proprietary distortion cancellation techniques, the AD8375 achieves 50 dBm output IP3 at 200 MHz.

The AD8375 provides a broad 24 dB gain range with 1 dB resolution. The gain is adjusted through a 5-pin control interface and can be driven using standard TTL levels. The open-collector outputs provide a flexible interface, allowing the overall signal gain to be set by the loading impedance. Thus, the signal voltage gain is directly proportional to the load.

The AD8375 is powered on by applying the appropriate logic level to the PWUP pin. The quiescent current of the AD8375 is typically 130 mA. When powered down, the AD8375 consumes less than 5 mA and offers excellent input-to-output isolation.

Fabricated on an Analog Devices, Inc., high speed SiGe process, the AD8375 is supplied in a compact, thermally enhanced, 4 mm × 4 mm, 24-lead LFCSP package and operates over the temperature range of −40°C to +85°C.

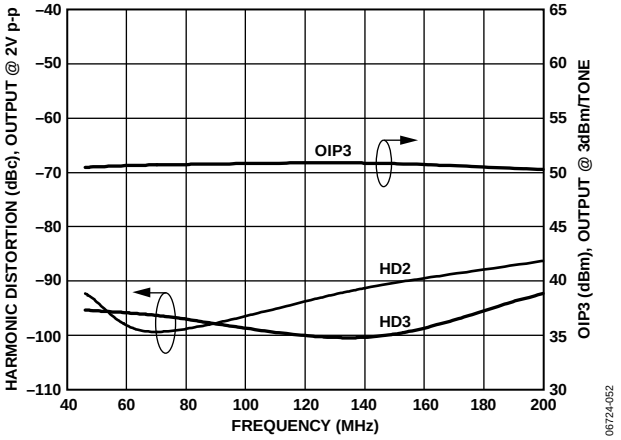


Figure 2. Harmonic Distortion and Output IP3 vs. Frequency

Rev. A **Document Feedback**

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REVISION HISTORY

10/12—Rev. 0 to Rev. A

Change to Maximum Junction Temperature Parameter, Table 3 ... 5
Added Exposed Pad Notation, Figure 3 and Exposed Pad Notation, Table 4 ... 6
Added Exposed Pad Notation to Outline Dimensions ... 22

8/07—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T = 25°C, R_S = R_L = 150 Ω at 140 MHz, 2 V p-p differential output, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} < 2 V p-p (5.2 dBm)		630		MHz
Slew Rate			5		V/ns
INPUT STAGE	Pin VIN+ and Pin VIN−				
Maximum Input Swing	For linear operation (A_V = −4 dB)		8.5		V p-p
Differential Input Resistance	Differential	125	150	165	Ω
Common-Mode Input Voltage			1.9		V
CMRR	Gain code = 00000		55		dB
GAIN					
Amplifier Transconductance	Gain code = 00000	0.060	0.067	0.074	S
Maximum Voltage Gain	Gain code = 00000		20		dB
Minimum Voltage Gain	Gain code ≥ 11000		−4		dB
Gain Step Size	From gain code = 00000 to 11000	0.89	0.98	1.01	dB
Gain Flatness	All gain codes, 20% fractional bandwidth for f_C < 200 MHz		0.12		dB
Gain Temperature Sensitivity	Gain code = 00000		8		mdB/°C
Gain Step Response	For V_{IN} = 100 mV p-p, gain code = 10100 to 00000		5		ns
OUTPUT STAGE	Pin VOUT+ and Pin VOUT−				
Output Voltage Swing	At P1dB, gain code = 00000		12.6		V p-p
Output Impedance	Differential		16||0.8		kΩ||pF
NOISE/HARMONIC PERFORMANCE					
46 MHz	Gain code = 00000				
Noise Figure			8.3		dB
Second Harmonic	V_{OUT} = 2 V p-p		−92		dBc
Third Harmonic	V_{OUT} = 2 V p-p		−94		dBc
Output IP3	2 MHz spacing, +3 dBm per tone		50		dBm
Output 1 dB Compression Point			22		dBm
70 MHz	Gain code = 00000				
Noise Figure			8.3		dB
Second Harmonic	V_{OUT} = 2 V p-p		−98		dBc
Third Harmonic	V_{OUT} = 2 V p-p		−95		dBc
Output IP3	2 MHz spacing, 3 dBm per tone		51		dBm
Output 1 dB Compression Point			22		dBm
140 MHz	Gain code = 00000				
Noise Figure			8.3		dB
Second Harmonic	V_{OUT} = 2 V p-p		−90		dBc
Third Harmonic	V_{OUT} = 2 V p-p		−100		dBc
Output IP3	2 MHz spacing, 3 dBm per tone		51		dBm
Output 1 dB Compression Point			20		dBm
200 MHz	Gain code = 00000				
Noise Figure			8.3		dB
Second Harmonic	V_{OUT} = 2 V p-p		−85		dBc
Third Harmonic	V_{OUT} = 2 V p-p		−92		dBc
Output IP3	2 MHz spacing, 3 dBm per tone		50		dBm
Output 1 dB Compression Point			19		dBm

Parameter	Conditions	Min	Typ	Max	Unit
POWER INTERFACE					
Supply Voltage		4.5	5.0	5.5	V
VPOS and Output Quiescent Current	Thermal connection made to exposed paddle under device	120	125	130	mA
vs. Temperature	$-40°C \le T_A \le +85°C$			150	mA
Power-Down Current	PWUP low		2.5		mA
vs. Temperature	$-40°C \le T_A \le +85°C$			3	mA
POWER-UP/GAIN CONTROL	Pin A0 to Pin A4, Pin PWUP				
V_{IH}	Minimum voltage for a logic high	1.6			V
V_{IL}	Maximum voltage for a logic low			0.8	V
Logic Input Bias Current			900		nA

Table 2. Gain Code vs. Voltage Gain Look-Up Table

5-Bit Binary Gain Code	Voltage Gain (dB)
00000	+20
00001	+19
00010	+18
00011	+17
00100	+16
00101	+15
00110	+14
00111	+13
01000	+12
01001	+11
01010	+10
01011	+9
01100	+8

5-Bit Binary Gain Code	Voltage Gain (dB)
01101	+7
01110	+6
01111	+5
10000	+4
10001	+3
10010	+2
10011	+1
10100	0
10101	−1
10110	−2
10111	−3
11000	−4
>11000	−4

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage, V_{POS}	5.5 V
PWUP, A0 to A4	−0.6 V to (V_{POS} + 0.6 V)
Input Voltage, V_{IN+}, V_{IN-}	−0.15 V to +4.15 V
DC Common Mode	VCOM ± 0.25 V
VCOM	±6 mA
Internal Power Dissipation	825 mW
θ_{JA} (Exposed Paddle Soldered Down)	63.6°C/W
θ_{JC} (At Exposed Paddle)	14.6°C/W
Maximum Junction Temperature	140°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

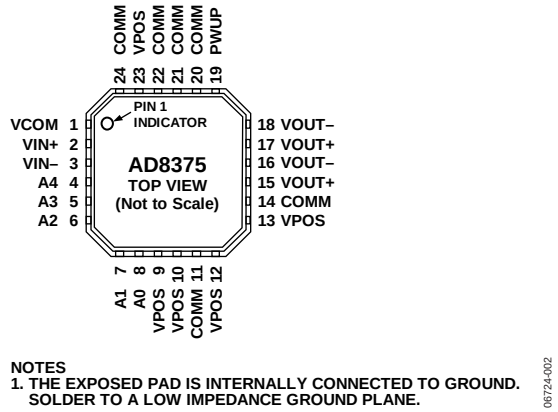


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCOM	Common-Mode Pin. Typically bypassed to ground using external capacitor.
2	VIN+	Voltage Input Positive.
3	VIN–	Voltage Input Negative.
4	A4	MSB for the 5-Bit Gain Control Interface.
5	A3	MSB – 1 for the Gain Control Interface.
6	A2	MSB – 2 for the Gain Control Interface.
7	A1	LSB + 1 for the Gain Control Interface.
8	A0	LSB for the 5-Bit Gain Control Interface.
9, 10, 12, 13, 23	VPOS	Positive Supply Pins. Should be bypassed to ground using suitable bypass capacitor.
11, 14, 20, 21, 22, 24	COMM	Device Common (DC Ground).
15, 17	VOUT+	Positive Output Pins (Open Collector). Require dc bias of +5 V nominal.
16, 18	VOUT–	Negative Output Pins (Open Collector). Require dc bias of +5 V nominal.
19	PWUP	Chip Enable Pin. Enabled with a logic high and disabled with a logic low.
	EPAD	Exposed Pad. The Exposed Pad is internally connected to ground. Solder to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T_A = 25°C, R_S = R_L = 150 Ω, 2 V p-p output, maximum gain unless otherwise noted.

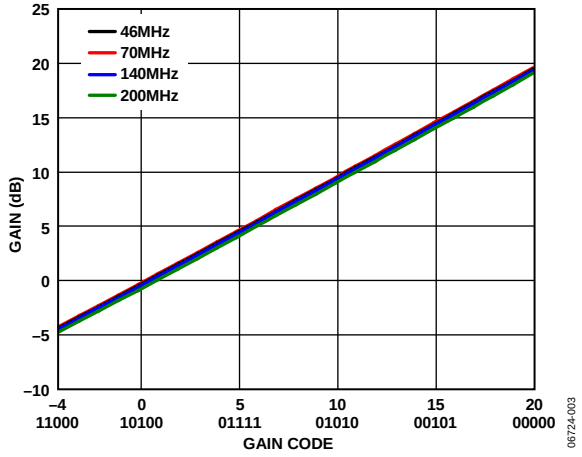


Figure 4. Gain vs. Gain Code at 46 MHz, 70 MHz, 140 MHz, and 200 MHz

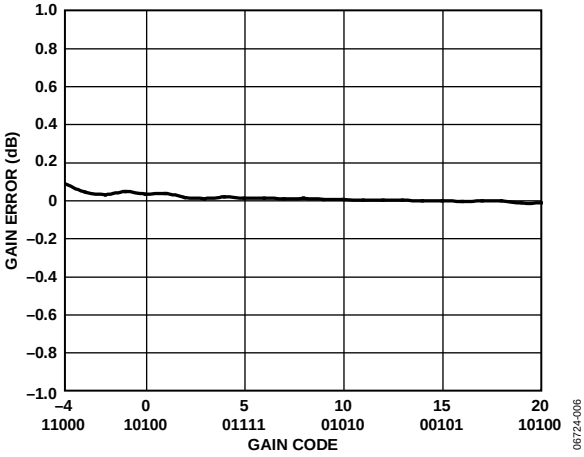


Figure 7. Gain Step Error, Frequency 140 MHz

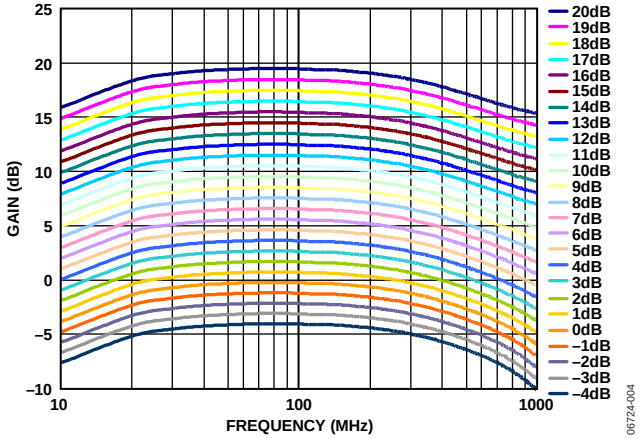


Figure 5. Gain vs. Frequency Response

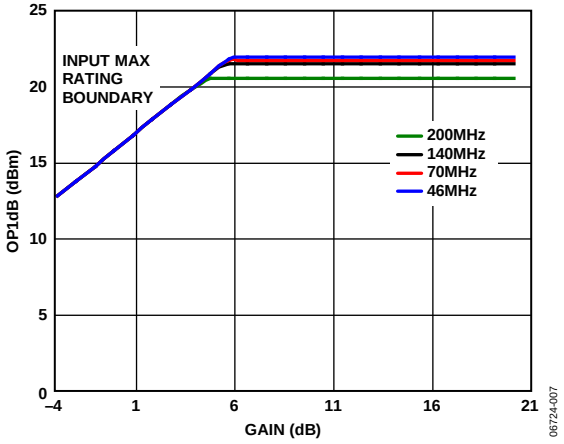


Figure 8. P1dB vs. Gain at 46 MHz, 70 MHz, 140 MHz, and 200 MHz

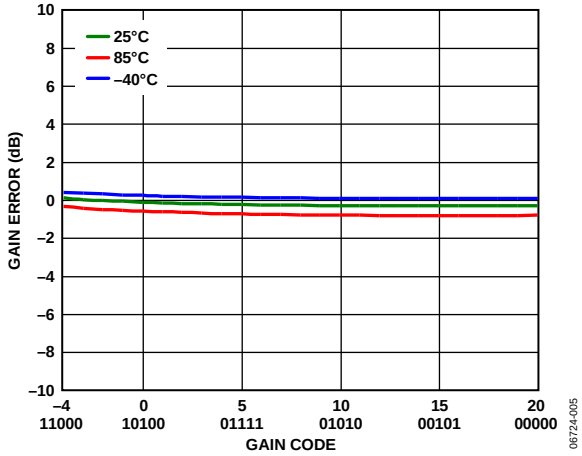


Figure 6. Gain Error over Temperature at 140 MHz

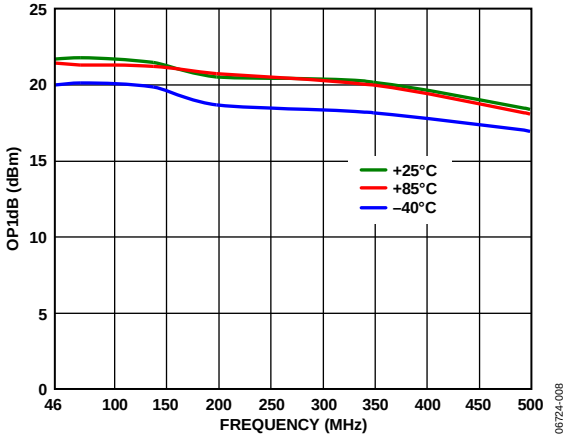


Figure 9. P1dB vs. Frequency at Maximum Gain, Three Temperatures

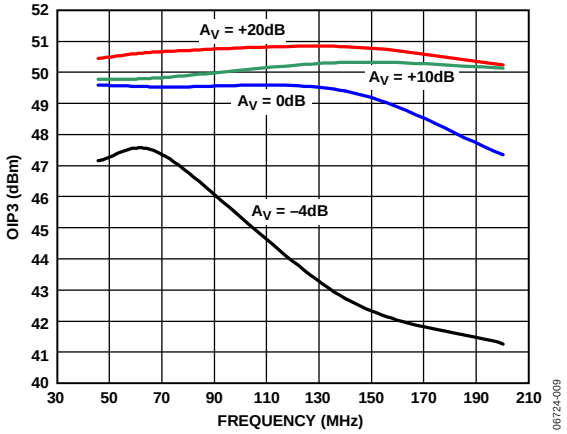


Figure 10. Output Third-Order Intercept at Four Gains, Output Level at 3 dBm/Tone

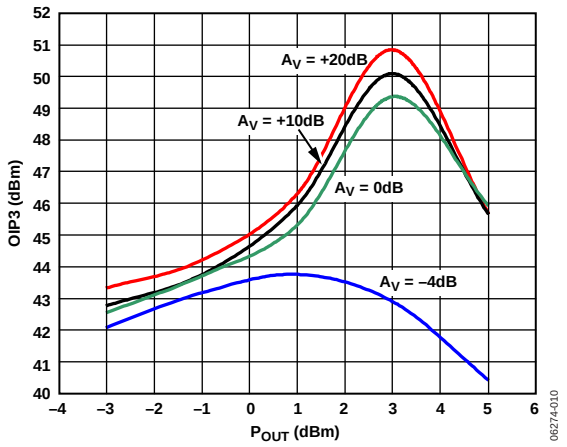


Figure 11. Output Third-Order Intercept vs. Power at Four Gains, Frequency 140 MHz

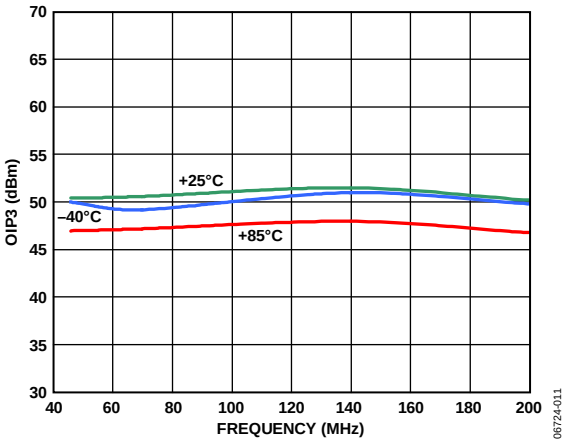


Figure 12. Output Third-Order Intercept vs. Frequency, Three Temperatures, Output Level at 3 dBm/Tone

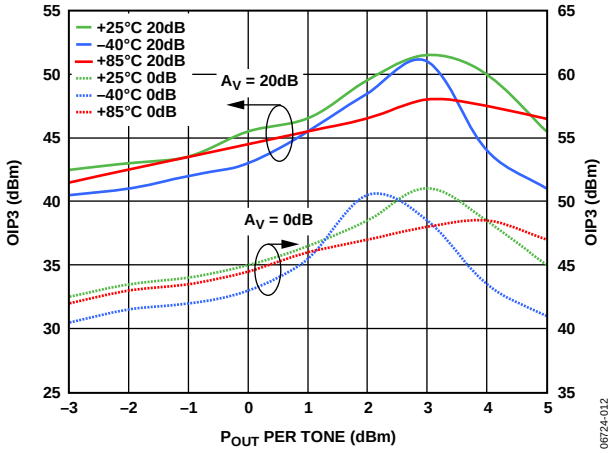


Figure 13. Output Third-Order Intercept vs. Power, Frequency 140 MHz, Three Temperatures

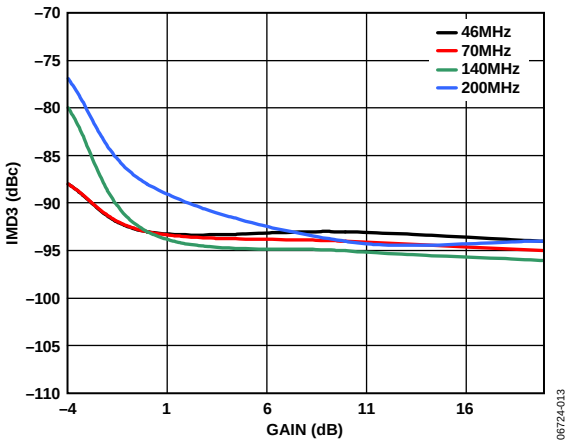


Figure 14. Two-Tone Output IMD vs. Gain at 46 MHz, 70 MHz, 140 MHz, and 200 MHz, Output Level at 3 dBm/Tone

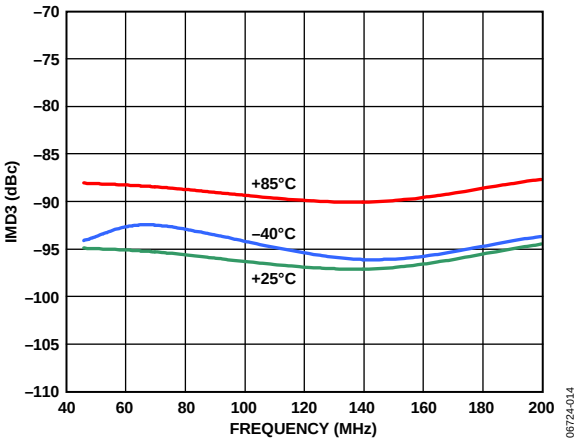


Figure 15. Two-Tone Output IMD vs. Frequency, Three Temperatures, Output Level at 3 dBm/Tone

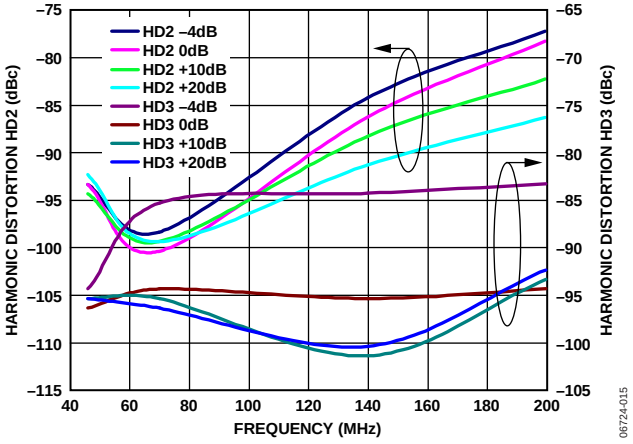


Figure 16. Harmonic Distortion vs. Frequency at Four Gain Codes, V_{OUT} = 2 V p-p

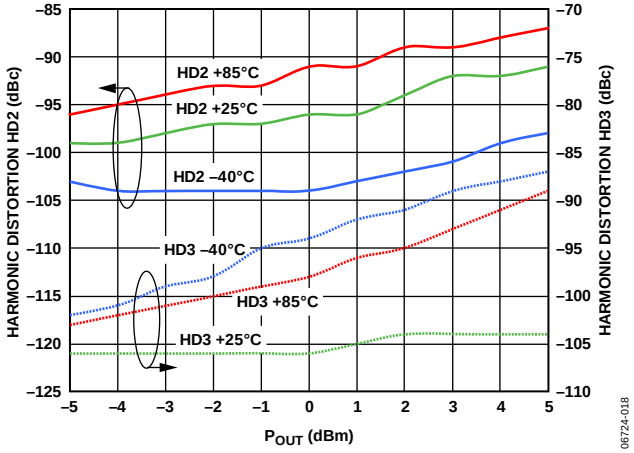


Figure 19. Harmonic Distortion vs. Power, Frequency 140 MHz, Three Temperatures

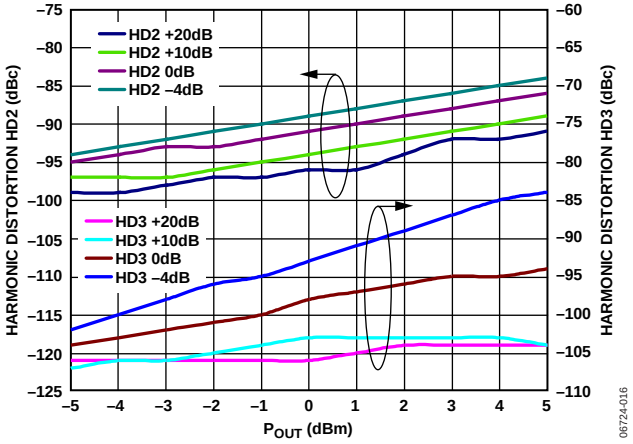


Figure 17. Harmonic Distortion vs. Power at Four Gain Codes, Frequency 140 MHz

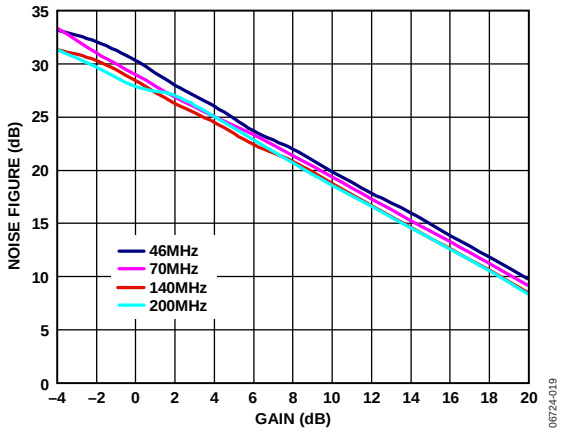


Figure 20. NF vs. Gain at 46 MHz, 70 MHz, 140 MHz, and 200 MHz

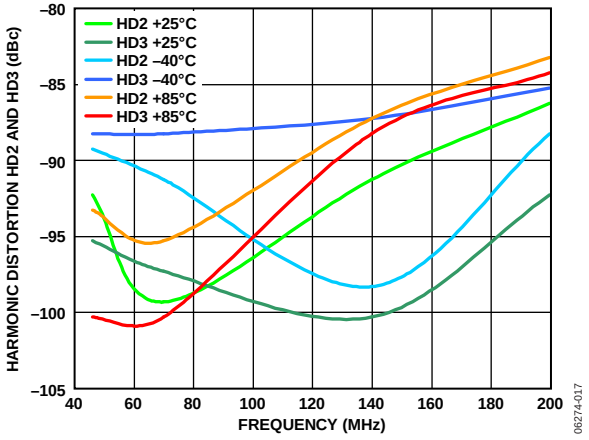


Figure 18. Harmonic Distortion vs. Frequency, Three Temperatures, V_{OUT} = 2 V p-p

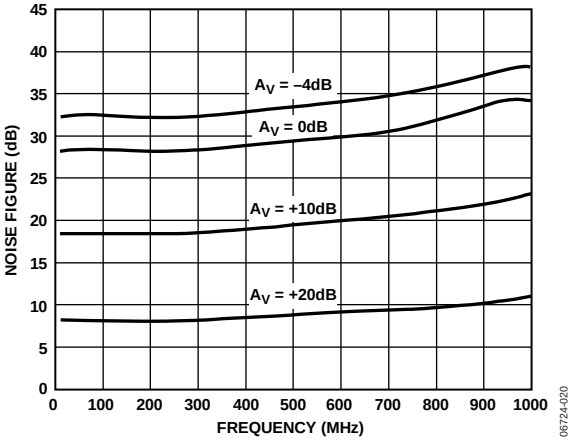


Figure 21. NF vs. Frequency

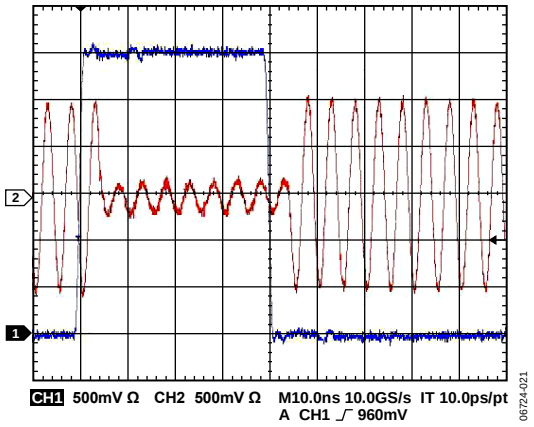


Figure 22. Gain Step Time Domain Response

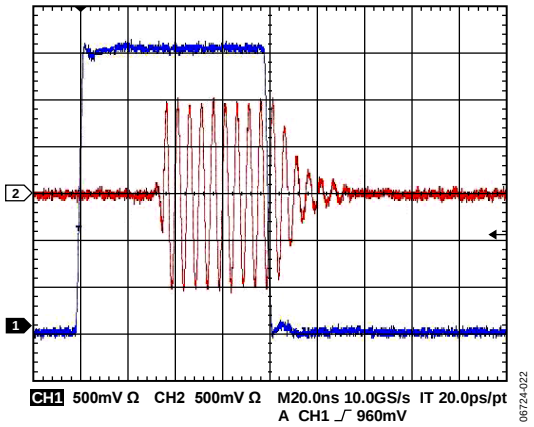


Figure 23. ENBL Time Domain Response

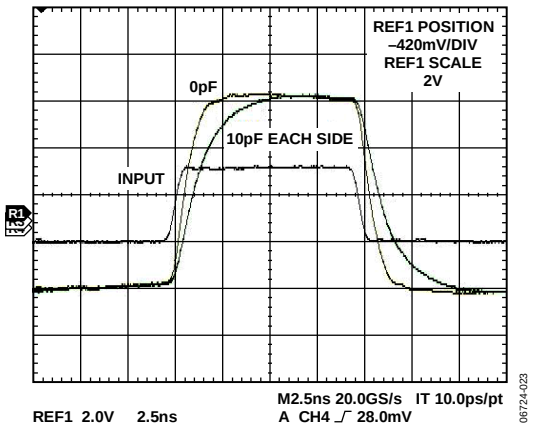


Figure 24. Pulse Response to Capacitive Loading, Gain −4 dB

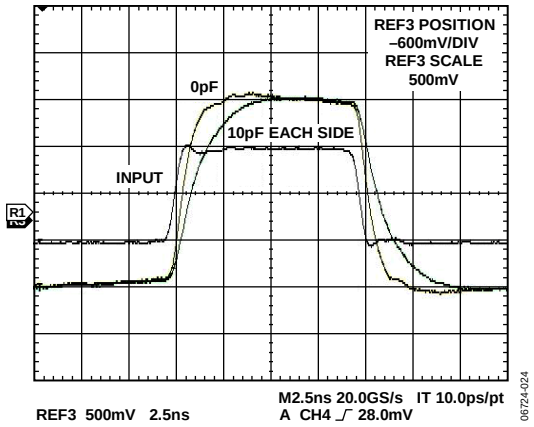


Figure 25. Pulse Response to Capacitive Loading, Gain 20 dB

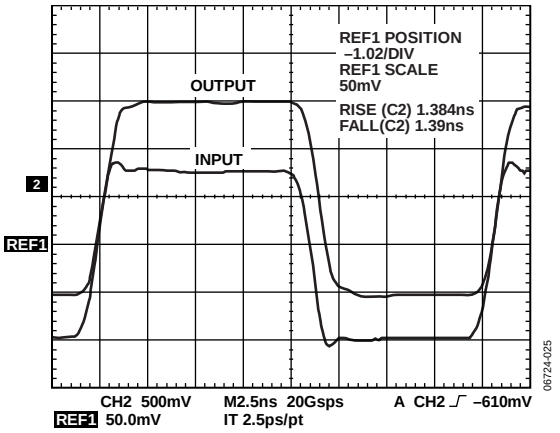


Figure 26. Large Signal Pulse Response

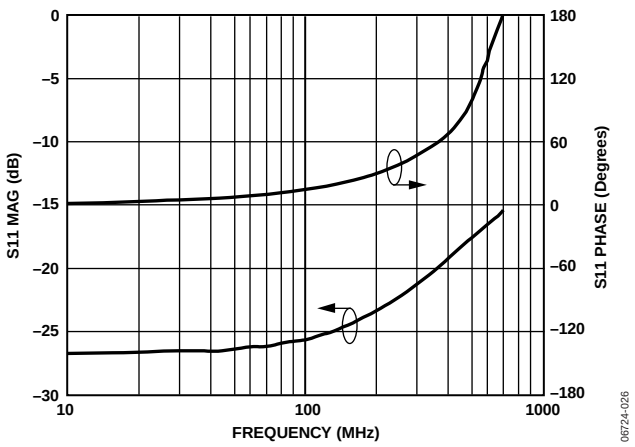


Figure 27. S11 vs. Frequency

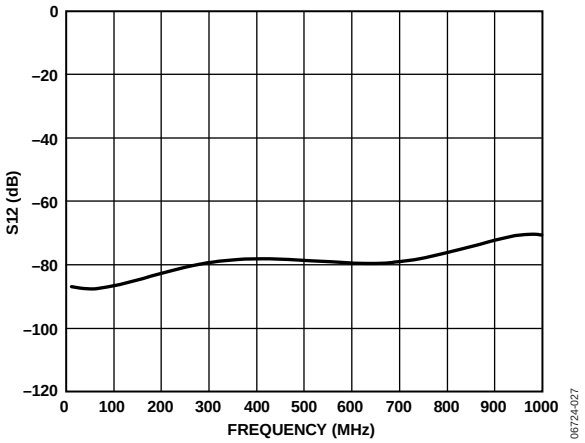


Figure 28. Reverse Isolation vs. Frequency

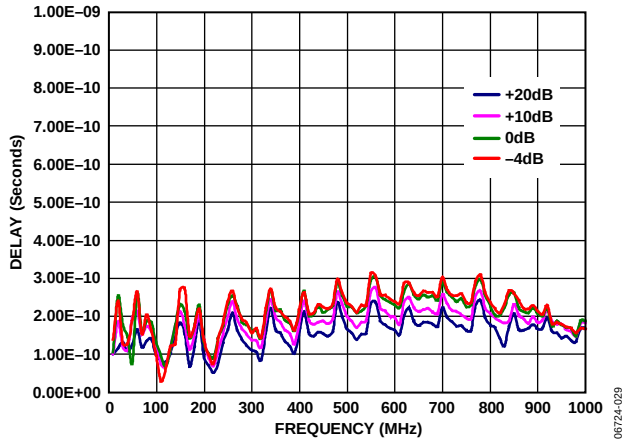


Figure 30. Group Delay vs. Frequency at Gain

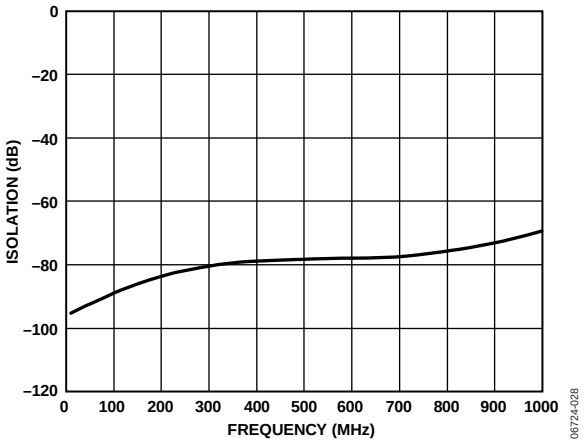


Figure 29. Off-State Isolation vs. Frequency

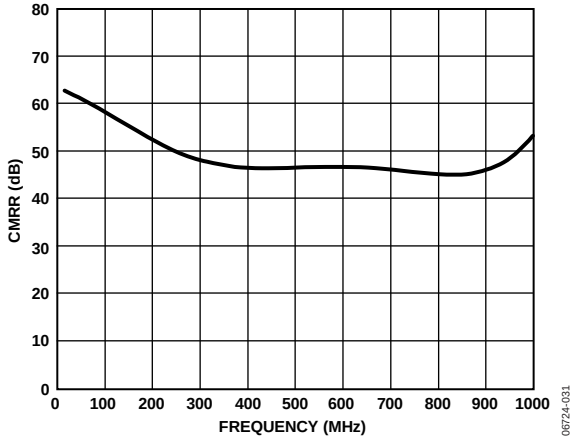


Figure 31. Common-Mode Rejection Ratio vs. Frequency

CIRCUIT DESCRIPTION

BASIC STRUCTURE

The AD8375 is a differential variable gain amplifier consisting of a 150 Ω digitally controlled passive attenuator followed by a highly linear transconductance amplifier.

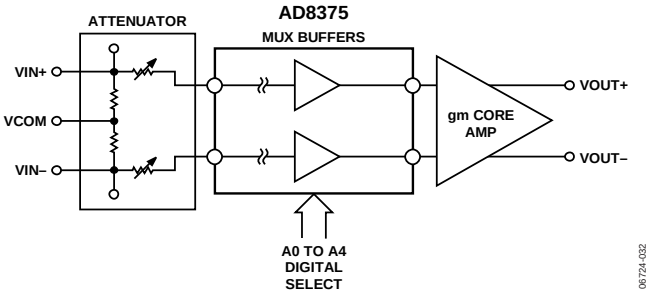


Figure 32. Simplified Schematic

Input System

The dc voltage level at the inputs of the AD8375 is set by an internal voltage reference circuit to about 2 V. This reference is accessible at VCOM and can be used to source or sink 100 μA. For cases where a common-mode signal is applied to the inputs, such as in a single-ended application, an external capacitor between VCOM and ground is required. The capacitor improves the linearity performance of the part in this mode. This capacitor should be sized to provide a reactance of 10 Ω or less at the lowest frequency of operation. If the applied common-mode signal is dc, its amplitude should be limited to 0.25 V from VCOM (VCOM ± 0.25 V).

The device can be powered down by pulling the PWUP pin down to below 0.8 V. In the powered down mode, the total current reduces to 3 mA (typical). The dc level at the inputs and at VCOM remains at about 2 V, regardless of the state of the PWUP pin.

Output Amplifier

The gain is based on a 150 Ω differential load and varies as R_L is changed per the following equations:

$$Voltage\ Gain = 20 \times (\log(R_L/150) + 1)$$

and

$$Power\ Gain = 10 \times (\log(R_L/150) + 2)$$

The dependency of the gain on the load is due to the open-collector architecture of the output stage.

The dc current to the outputs of the amplifier is supplied through two external chokes. The inductance of the chokes and the resistance of the load determine the low frequency pole of the amplifier. The parasitic capacitance of the chokes adds to the output capacitance of the part. This total capacitance in parallel with the load resistance sets the high frequency pole of the device. Generally, the larger the inductance of the choke, the higher its parasitic capacitance. Therefore, the value and type of the choke should be chosen keeping this trade-off in mind.

For operation frequency of 15 MHz to 700 MHz driving a 150 Ω load, 1 μH chokes with SRF of 160 MHz or higher are recommended (such as 0805LS-102XJBB from Coilcraft).

The supply current consists of about 50 mA through the VCC pin and 80 mA through the two chokes combined. The latter increases with temperature at about 2.5 mA per 10°C.

There are two output pins for each polarity and they are oriented in an alternating fashion. When designing the board, care should be taken to minimize the parasitic capacitance due to the routing that connects the corresponding outputs together. A good practice is to avoid any ground or power plane under this routing region and under the chokes to minimize the parasitic capacitance.

Gain Control

A 5-bit binary code changes the attenuator setting in 1 dB steps such that the gain of the device changes from 20 dB (Code 0) to −4 dB (Code 24 and higher).

The noise figure of the device is about 8 dB at maximum gain setting and it increases as the gain is reduced. The increase in noise figure is equal to the reduction in gain. The linearity of the part measured at the output is first-order independent of the gain setting. From 0 dB to 20 dB gain, OIP3 is approximately 50 dBm into 150 Ω load at 140 MHz (3 dBm per tone). At gain settings below 0 dB, it drops to approximately 45 dBm.

APPLICATIONS

BASIC CONNECTIONS

Figure 35 shows the basic connections for operating the AD8375. A voltage between 4.5 V and 5.5 V should be applied to the supply pins. Each supply pin should be decoupled with at least one low inductance, surface-mount ceramic capacitor of 0.1 µF placed as close as possible to the device.

The outputs of the AD8375 are open collectors that need to be pulled up to the positive supply with 1 µH RF chokes. The differential outputs are biased to the positive supply and require ac coupling capacitors, preferably 0.1 µF. Similarly, the input pins are at bias voltages of about 2 V above ground and should be ac-coupled as well. The ac coupling capacitors and the RF chokes are the principle limitations for operation at low frequencies.

To enable the AD8375, the PWUP pin must be pulled high. Taking PWUP low puts the AD8375 in sleep mode, reducing current consumption to 5 mA at ambient.

SINGLE-ENDED-TO-DIFFERENTIAL CONVERSION

The AD8375 can be configured as a single-ended input to differential output driver as shown in Figure 33. A 150 Ω resistor in parallel with the input impedance of input pin provides an impedance matching of 50 Ω. The voltage gain and the bandwidth of this configuration, using a 150 Ω load, remains the same as when using a differential input.

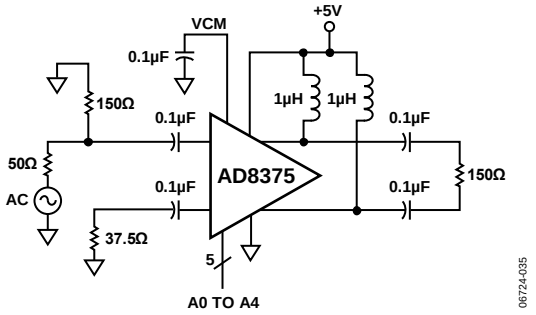


Figure 33. Single-Ended-to-Differential Conversion

Using a single-ended input decreases the power gain by 3 dB and limits distortion cancellation. Consequently, the second-order distortion is degraded. The third-order distortion remains low to 200 MHz, as shown in Figure 34.

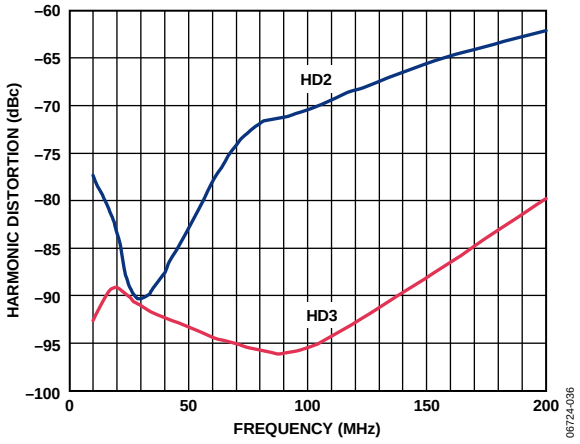


Figure 34. Harmonic Distortion vs. Frequency of Single-Ended-to-Differential Conversion

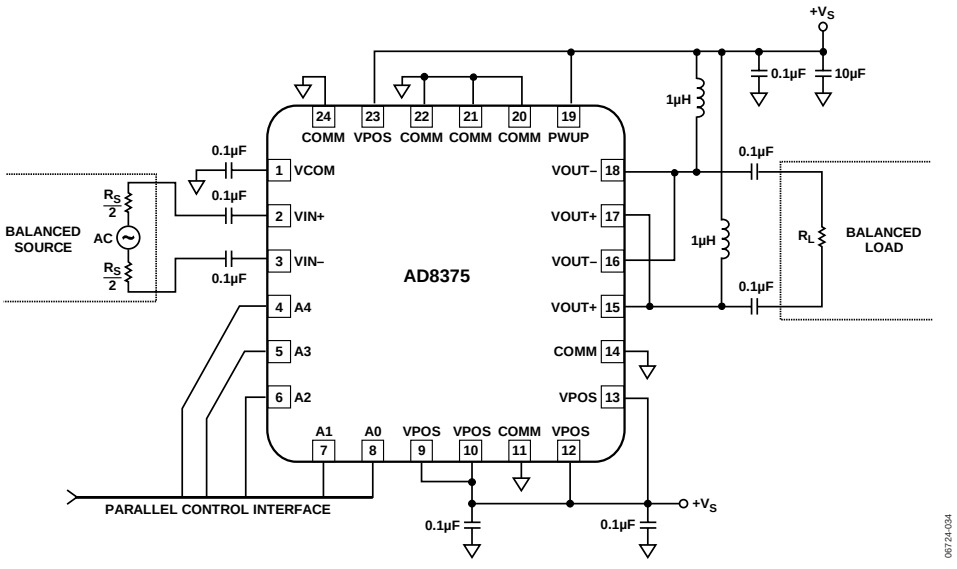


Figure 35. Basic Connections

BROADBAND OPERATION

The AD8375 uses an open-collector output structure that requires dc bias through an external bias network. Typically, choke inductors are used to provide bias to the open-collector outputs. Choke inductors work well at signal frequencies where the impedance of the choke is substantially larger than the target ac load impedance. In broadband applications, it may not be possible to find large enough choke inductors that offer enough reactance at the lowest frequency of interest while offering a high enough self resonant frequency (SRF) to support the maximum bandwidth available from the device. The circuit in Figure 36 can be used when frequency response below 10 MHz is desired. This circuit replaces the bias chokes with bias resistors. The bias resistor has the disadvantage of a greater IR drop, and requires a supply rail that is several volts above the local 5 V supply used to power the device. Additionally, it is necessary to account for the ac loading effect of the bias resistors when designing the output interface. Whereas the gain of the AD8375 is load dependent, R_L, in parallel with R1 + R2, should equal the optimum 150 Ω target load impedance to provide the expected ac performance depicted in the data sheet. Additionally, to ensure good output balance and even-order distortion performance, it is essential that R1 = R2.

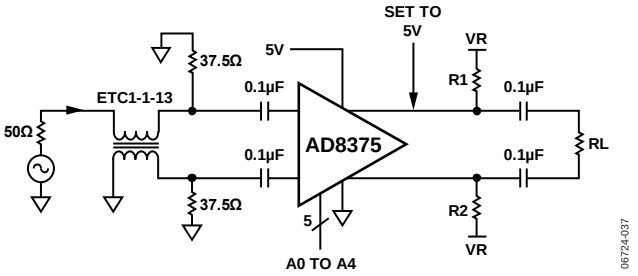


Figure 36. Single-Ended Broadband Operation with Resistive Pull-Ups

Using the formula for R1 (Equation 1), the values of R1 = R2 that provide a total presented load impedance of 150 Ω can be found. The required voltage applied to the bias resistors, VR, can be found by using the VR formula (Equation 2).

$$R1 = \frac{75 \times R_L}{R_L - 150} \quad (1)$$

and

$$VR = R1 \times 40 \times 10^{-3} + 5 \quad (2)$$

For example, in the extreme case where the load is assumed to be high impedance, $R_L = \infty$, the equation for R1 reduces to R1 = 75 Ω. Using the equation for VR, the applied voltage should be VR = 8 V. The measured single-tone low frequency harmonic distortion for a 2 V p-p output using 75 Ω resistive pull-ups is provided in Figure 37.

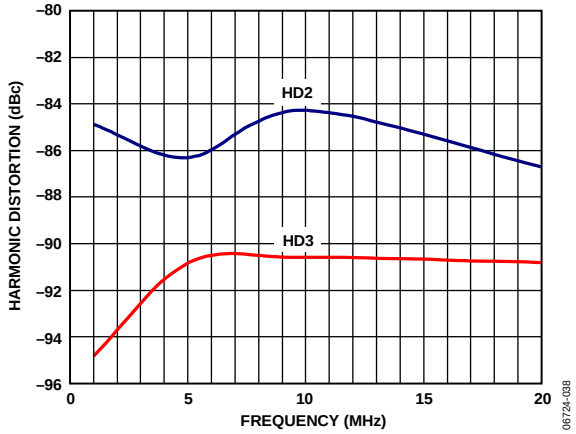


Figure 37. Harmonic Distortion vs. Frequency Using Resistive Pull-Ups

ADC INTERFACING

The AD8375 is a high output linearity variable gain amplifier that is optimized for ADC interfacing. The output IP3 and noise floor essentially remain constant vs. the 24 dB available gain range. This is a valuable feature in a variable gain receiver where it is desirable to maintain a constant instantaneous dynamic range as the receiver gain is modified. The output noise density is typically around 20 nV/√Hz, which is comparable to 14-/16-bit sensitivity limits. The two-tone IP3 performance of the AD8375 is typically around 50 dBm. This results in SFDR levels of better than 86 dB when driving the AD9445 up to 140 MHz.

There are several options available to the designer when using the AD8375. The open-collector output provides the capability of driving a variety of loads. Figure 38 shows a simplified wideband interface with the AD8375 driving a AD9445. The AD9445 is a 14-bit 125 MSPS analog-to-digital converter with a buffered wideband input, which presents a 2 kΩ differential load impedance and requires a 2 V p-p differential input swing to reach full scale.

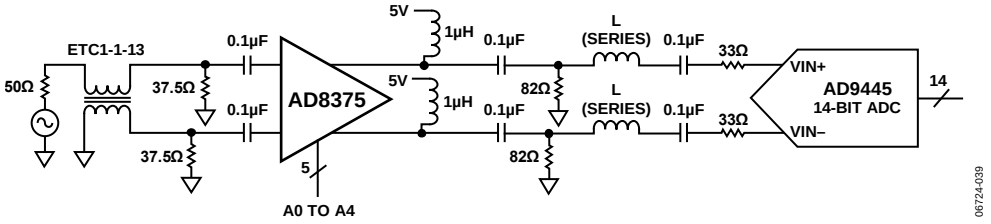


Figure 38. Wideband ADC Interfacing Example Featuring the AD9445

For optimum performance, the AD8375 should be driven differentially using an input balun or impedance transformer. Figure 38 uses a wideband 1:1 transmission line balun followed by two 37.5 Ω resistors in parallel with the 150 Ω input impedance of the AD8375 to provide a 50 Ω differential terminated input impedance. This provides a wideband match to a 50 Ω source. The open-collector outputs of the AD8375 are biased through the two 1 µH inductors and are ac-coupled to the two 82 Ω load resistors. The 82 Ω load resistors in parallel with the series-terminated ADC impedance yields the target 150 Ω differential load impedance, which is recommended to provide the specified gain accuracy of the device. The load resistors are ac-coupled from the AD9445 to avoid common-mode dc loading. The 33 Ω series resistors help to improve the isolation between the AD8375 and any switching currents present at the analog-to-digital sample and hold input circuitry.

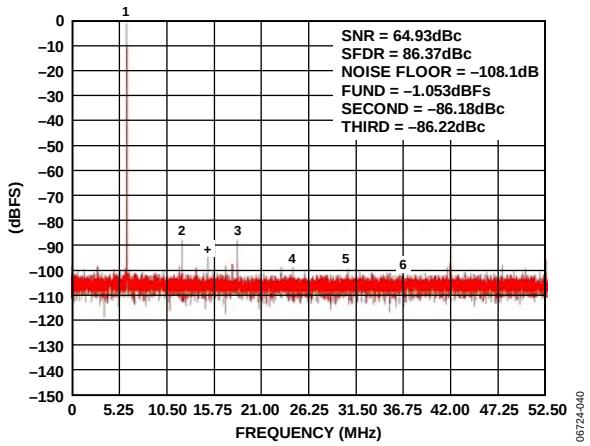


Figure 39. Measured Single-Tone Performance of the Circuit in Figure 38 for a 100 MHz Input Signal

The circuit depicted in Figure 38 provides variable gain, isolation and source matching for the AD9445. Using this circuit with the AD8375 in a gain of 20 dB (maximum gain) an SFDR performance of 86 dBc is achieved at 100 MHz, as indicated in Figure 39.

The addition of the series inductors L (series) in Figure 38 extends the bandwidth of the system and provides response flatness. Using 100 nH inductors as L (series), the wideband system response of Figure 40 is obtained. The wideband frequency response is an advantage in broadband applications such as predistortion receiver designs and instrumentation applications. However, by designing for a wide analog input frequency range, the cascaded SNR performance is somewhat degraded due to high frequency noise aliasing into the wanted Nyquist zone.

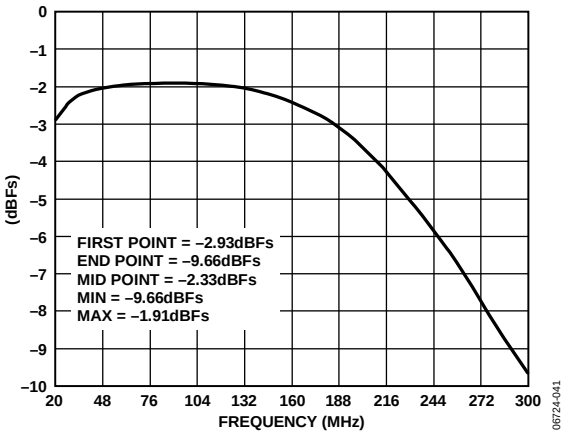


Figure 40. Measured Frequency Response of Wideband ADC Interface Depicted in Figure 38

An alternative narrow-band approach is presented in Figure 41. By designing a narrow band-pass antialiasing filter between the AD8375 and the target ADC, the output noise of the AD8375 outside of the intended Nyquist zone can be attenuated, helping to preserve the available SNR of the ADC. In general, the SNR improves several dB when including a reasonable order antialiasing filter. In this example, a low loss 1:3 input transformer is used to match the AD8375's 150 Ω balanced input to a 50 Ω unbalanced source, resulting in minimum insertion loss at the input.

Figure 41 is optimized for driving some of Analog Devices popular unbuffered ADCs, such as the AD9246, AD9640, and AD6655. Table 5 includes antialiasing filter component recommendations for popular IF sampling center frequencies. Inductor L5 works in parallel with the on-chip ADC input capacitance and a portion of the capacitance presented by C4 to form a resonant tank circuit. The resonant tank helps to ensure the ADC input looks like a real resistance at the target center frequency. Additionally, the L5 inductor shorts the ADC inputs at dc, which introduces a zero into the transfer function. In addition, the ac coupling capacitors and the bias chokes introduce additional zeros into the transfer function. The final overall frequency response takes on a band-pass characteristic, helping to reject noise outside of the intended Nyquist zone. Table 5 provides initial suggestions for prototyping purposes. Some empirical optimization may be needed to help compensate for actual PCB parasitics.

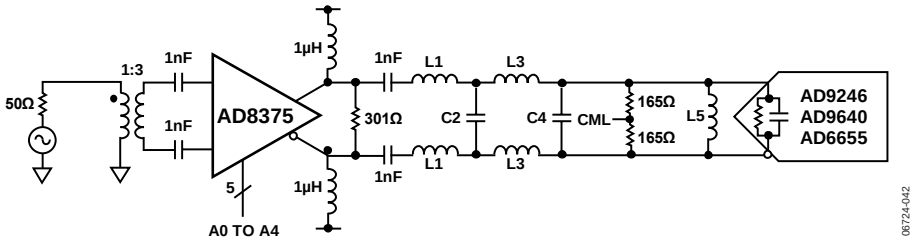


Figure 41. Narrow-Band IF Sampling Solution for Unbuffered ADC Application

Table 5. Interface Filter Recommendations for Various IF Sampling Frequencies

Center Frequency	1 dB Bandwidth	L1	C2	L3	C4	L5
96 MHz	27 MHz	390 nH	5.6 pF	390 nH	25 pF	100 nH
140 MHz	30 MHz	330 nH	3.3 pF	330 nH	20 pF	56 nH
170 MHz	32 MHz	270 nH	2.7 pF	270 nH	20 pF	39 nH
211 MHz	32 MHz	220 nH	2.2 pF	220 nH	18 pF	27 nH

LAYOUT CONSIDERATIONS

There are two output pins for each polarity, and they are oriented in an alternating fashion. When designing the board, care should be taken to minimize the parasitic capacitance due to the routing that connects the corresponding outputs together. A good practice is to avoid any ground or power plane under this routing region and under the chokes to minimize the parasitic capacitance.

CHARACTERIZATION TEST CIRCUITS

Differential-to-Differential Characterization

The S-parameter characterization for the AD8375 was performed using a dedicated differential input to differential output characterization board. Figure 44 shows the layout of characterization board. The board was designed for optimum impedance matching into a 75 Ω system. Because both the input and output impedances of the AD8375 are 150 Ω differentially, 75 Ω impedance runs were used to match 75 Ω network analyzer port impedances. On-board 1 µH inductors were used for output biasing, and the output board traces were designed for minimum capacitance.

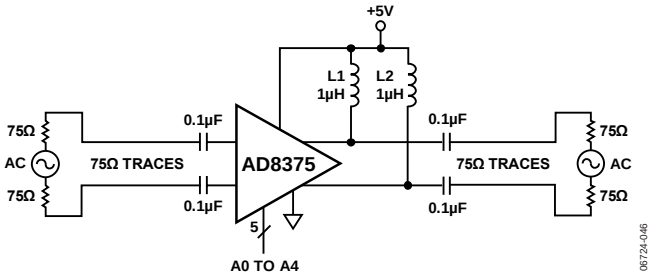


Figure 42. Test Circuit for S-Parameters on Dedicated 75 Ω Differential-to-Differential Board

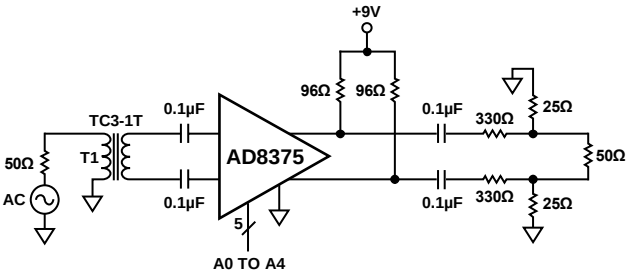


Figure 43. Test Circuit for Time Domain Measurements

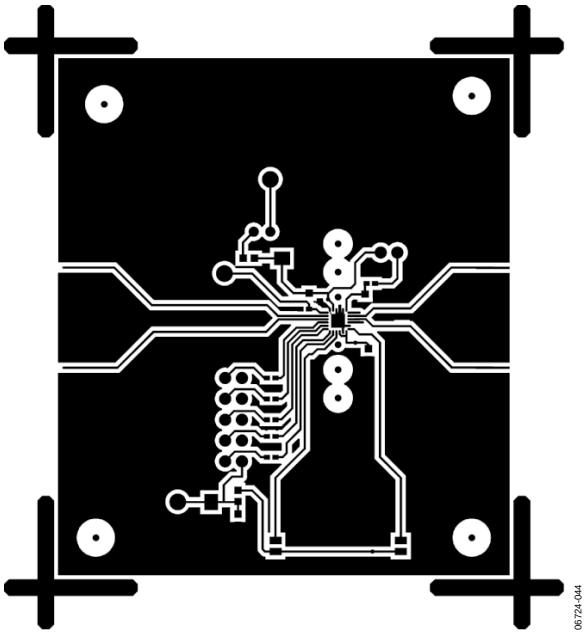


Figure 44. Differential-to-Differential Characterization Board Circuit Side Layout

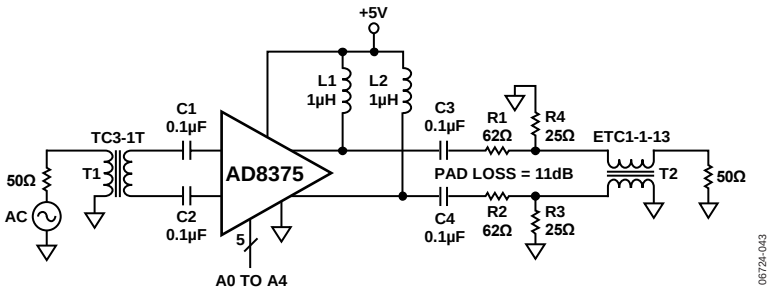


Figure 45. Test Circuit for Distortion, Gain, and Noise

EVALUATION BOARD

Figure 46 shows the schematic of the AD8375 evaluation board. The silkscreen and layout of the component and circuit sides are shown in Figure 47 through Figure 50. The board is powered by a single supply in the 4.5 V to 5.5 V range. The power supply is decoupled by 10 μF and 0.1 μF capacitors at each power supply pin. Additional decoupling, in the form of a series resistor or inductor at the supply pins, can also be added. Table 6 details the various configuration options of the evaluation board.

The output pins of the AD8375 require supply biasing with 1 μH RF chokes. Both the input and output pins must be ac-coupled. These pins are converted to single-ended with a pair of baluns (Mini-Circuits TC3-1T+ and M/A-COM ETC1-1-13). The balun at the input, T1, is used to transform a 50 Ω source impedance to the desired 150 Ω reference level. The output balun, T3, and the matching components are configured to provide a 150 Ω to 50 Ω impedance transformation with an insertion loss of about 11 dB.

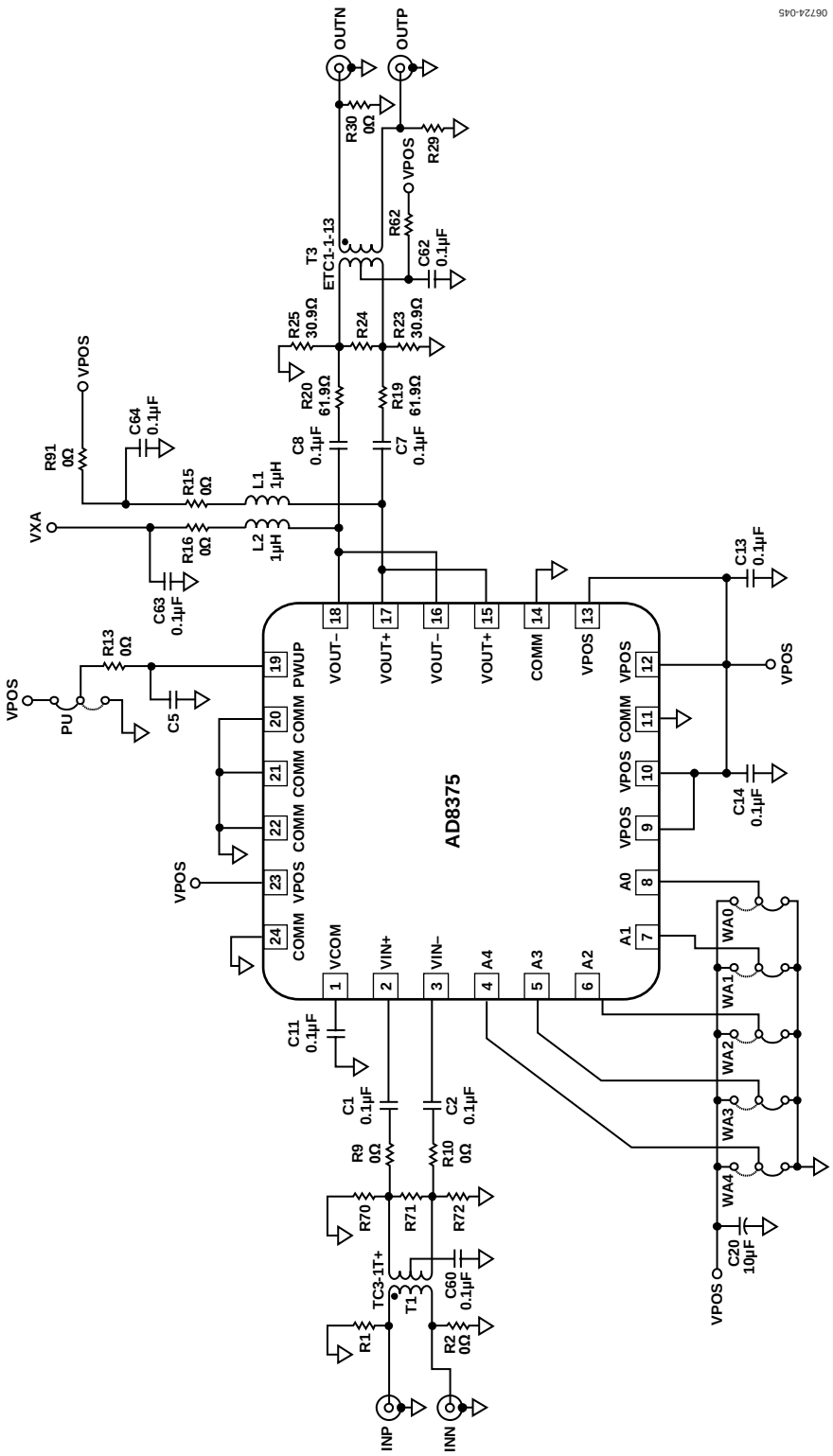


Figure 46. AD8375 Evaluation Board Schematic

Table 6. Evaluation Board Configuration Options

Components	Function	Default Conditions
C13, C14, C20, C63, C64, R91	Power Supply Decoupling. Nominal supply decoupling consists a 10 µF capacitor to ground followed by 0.1 µF capacitors to ground positioned as close to the device as possible.	C20 = 10 µF (size 3528) C13, C14, C63, C64 = 0.1 µF (size 0402) R91 = 0 Ω (size 0402)
T1, C1, C2, C60, R1, R2, R9, R10, R70 to R72	Input Interface. T1 is a 3:1 impedance ratio balun to transform a 50 Ω single-ended input into a 150 Ω balanced differential signal. R2 grounds one side of the differential drive interface for single-ended applications. R9, R10, and R70 to R72 are provided for generic placement of matching components. C1 and C2 are dc blocks.	T1 = TC3-1+ (Mini-Circuits) C1, C2, C60 = 0.1 µF (size 0402) R2, R9, R10 = 0 Ω (size 0402) R1, R70 to R72 = open (size 0402)
T3, C7, C8, C62 L1, L2, R15, R16, R19, R20, R23 to R25, R29, R30, R62	Output Interface. C7 and C8 are dc blocks. L1 and L2 provide dc biases for the output. R19, R20, and R23 to R25 are provided for generic placement of matching components. The evaluation board is configured to provide a 150 Ω to 50 Ω impedance transformation with an insertion loss of about 11 dB. T3 is a 1:1 impedance ratio balun to transform the balanced differential signal to a single-ended signal. R30 grounds one side of the differential output interface for single-ended applications.	T3 = ETC1-1-13 (M/A-COM) C7, C8, C62 = 0.1 µF (size 0402) L1, L2 = 1 µH (size 0805) R19, R20 = 61.9 Ω (size 0402) R23, R25 = 30.9 Ω (size 0402) R15, R16 = 0 Ω (size 0603) R30 = 0 Ω (size 0402) R24, R29, R62 = open (size 0402)
PU, R13, C5	Enable Interface. The AD8375 is enabled by applying a logic high voltage to the PWUP pin. The device is disabled when the PU switch is set in the position closest to the PU label, connecting the PWUP pin to ground. The device is enabled when the PU switch is set in the opposite position, connecting the PWUP to VPOS.	PU = installed R13 = 0 Ω (size 0603) C5 = open (size 0603)
WA0 to WA4	Parallel Interface Control. Used to hardwire A0 through A4 to the desired gain. The bank of switches, WA4 to WA0, set the binary gain code. WA4 represents the LSB. WA0 represents the MSB.	WA0 to WA4 = installed
C11	Voltage Reference. Input common-mode voltage ac-coupled to ground by 0.1 µF capacitor, C11.	C11 = 0.1 µF (size 0402)

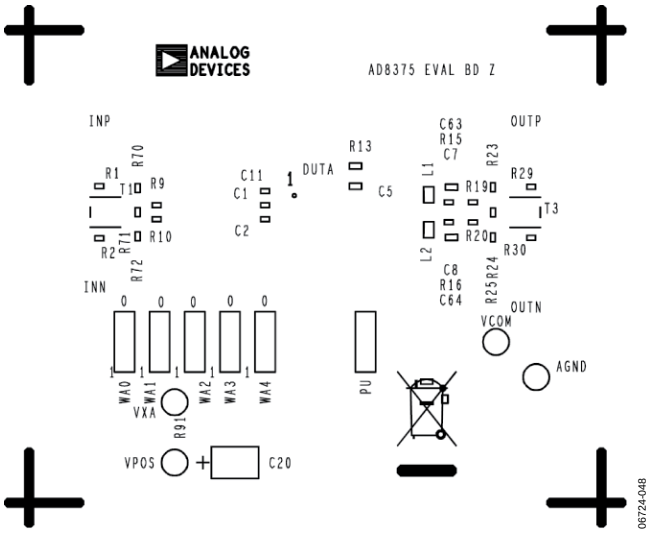


Figure 47. Component Side Silkscreen

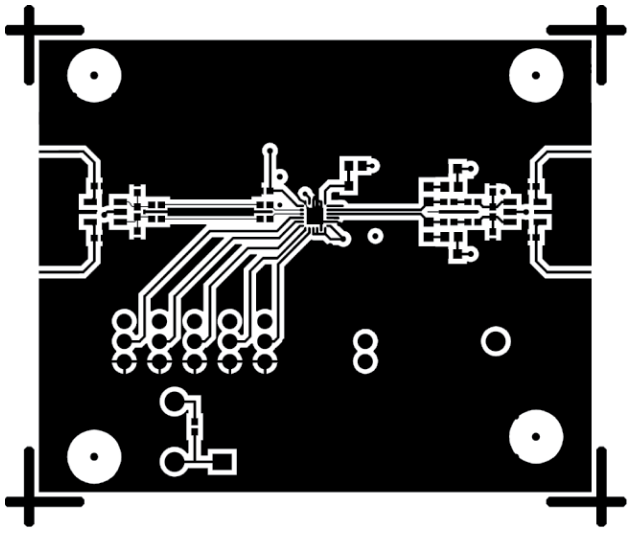


Figure 49. Component Side Layout

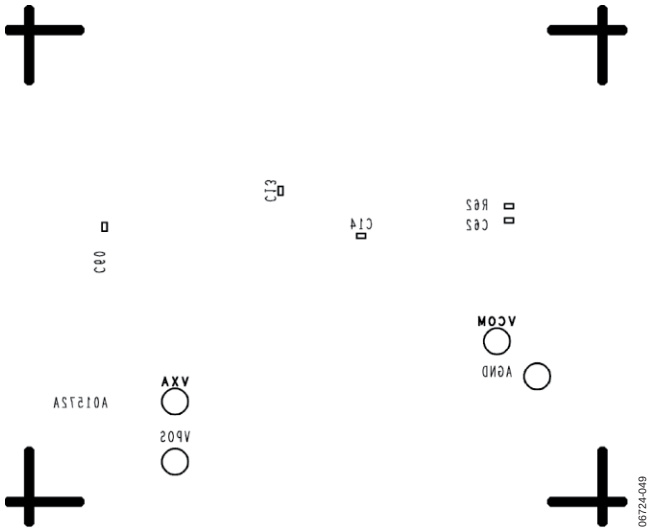


Figure 48. Circuit Side Silkscreen

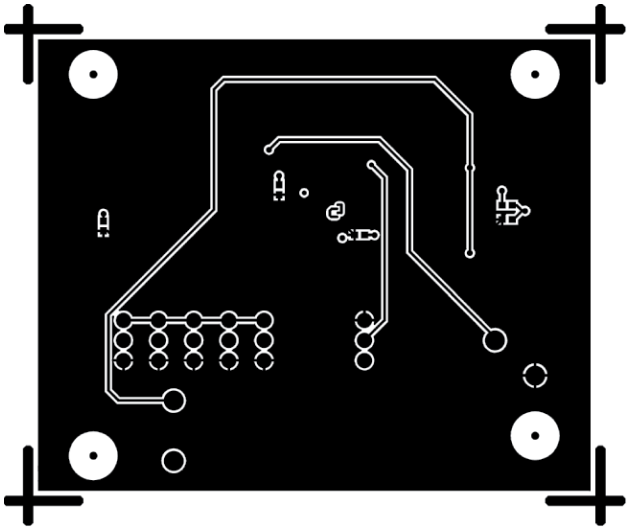


Figure 50. Circuit Side Layout

OUTLINE DIMENSIONS

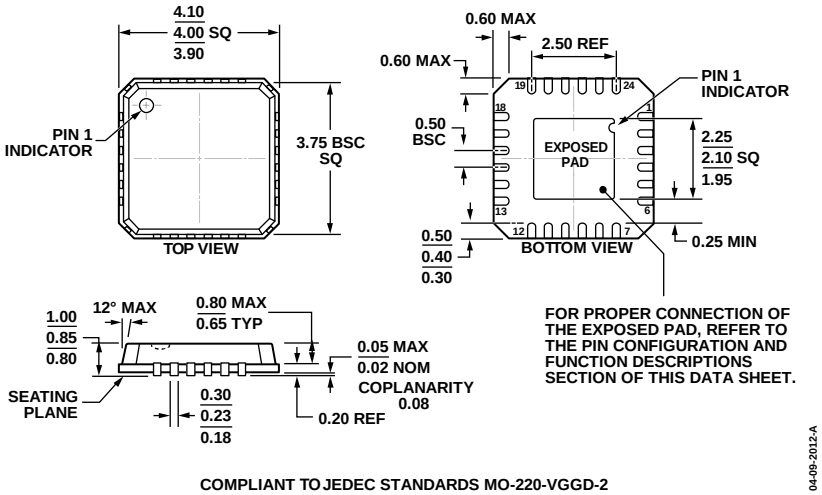


Figure 51. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-24-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8375ACPZ-WP	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_VQ], Waffle Pack	CP-24-1
AD8375ACPZ-R7	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_VQ], 7″ Tape and Reel	CP-24-1
AD8375-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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