1 MHz to 10 GHz, 55 dB Log Detector/Controller

AD8317

FEATURES

Wide bandwidth: 1 MHz to 10 GHz
High accuracy: ±1.0 dB over temperature
55 dB dynamic range up to 8 GHz ± 3 dB error
Stability over temperature: ±0.5 dB
Low noise measurement/controller output, VOUT
Pulse response time: 6 ns/10 ns (fall/rise)
Small footprint, 2 mm × 3 mm LFCSP
Supply operation: 3.0 V to 5.5 V @ 22 mA
Fabricated using high speed SiGe process

APPLICATIONS

RF transmitter PA setpoint control and level monitoring
Power monitoring in radio link transmitters
RSSI measurement in base stations, WLANs, WiMAX, and radars

FUNCTIONAL BLOCK DIAGRAM

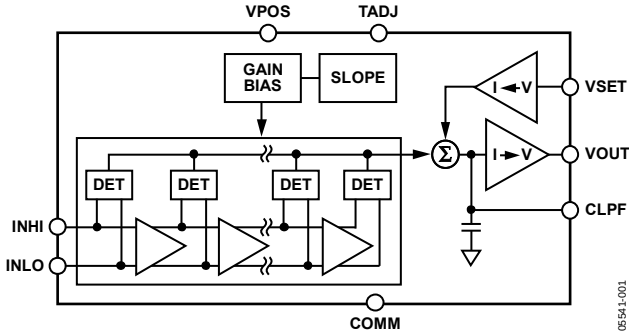


Figure 1.

GENERAL DESCRIPTION

The AD8317 is a demodulating logarithmic amplifier, capable of accurately converting an RF input signal to a corresponding decibel-scaled output. It employs the progressive compression technique over a cascaded amplifier chain, each stage of which is equipped with a detector cell. The device can be used in either measurement or controller modes. The AD8317 maintains accurate log conformance for signals of 1 MHz to 8 GHz and provides useful operation to 10 GHz. The input dynamic range is typically 55 dB (re: 50 Ω) with less than ±3 dB error. The AD8317 has 6 ns/10 ns response time (fall time/rise time) that enables RF burst detection to a pulse rate of beyond 50 MHz. The device provides unprecedented logarithmic intercept stability vs. ambient temperature conditions. A supply of 3.0 V to 5.5 V is required to power the device. Current consumption is typically 22 mA, and it decreases to 200 µA when the device is disabled.

The AD8317 can be configured to provide a control voltage to a power amplifier or a measurement output from the VOUT pin. Because the output can be used for controller applications, special attention has been paid to minimize wideband noise. In this mode, the setpoint control voltage is applied to the VSET pin.

The feedback loop through an RF amplifier is closed via VOUT, the output of which regulates the output of the amplifier to a magnitude corresponding to V_{SET}. The AD8317 provides 0 V to (V_{POS} − 0.1 V) output capability at the VOUT pin, suitable for controller applications. As a measurement device, VOUT is externally connected to VSET to produce an output voltage, V_{OUT}, that is a decreasing linear-in-dB function of the RF input signal amplitude.

The logarithmic slope is −22 mV/dB, determined by the VSET interface. The intercept is 15 dBm (re: 50 Ω, CW input) using the INHI input. These parameters are very stable against supply and temperature variations.

The AD8317 is fabricated on a SiGe bipolar IC process and is available in a 2 mm × 3 mm, 8-lead LFCSP with an operating temperature range of −40°C to +85°C.

Rev. B
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10/05—Revision 0: Initial Version

SPECIFICATIONS

V_{POS} = 3 V, C_{LPF} = 1000 pF, T_A = 25°C, 52.3 Ω termination resistor at INHI, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
SIGNAL INPUT INTERFACE	INHI (Pin 1)				
Specified Frequency Range		0.001		10	GHz
DC Common-Mode Voltage			V_{POS} − 0.6		V
MEASUREMENT MODE	VOUT (Pin 5) shorted to VSET (Pin 4), sinusoidal input signal				
f = 900 MHz	R_{TADJ} = 18 kΩ				
Input Impedance			1500||0.33		Ω||pF
±1 dB Dynamic Range	T_A = 25°C		50		dB
	−40°C < T_A < +85°C		46		dB
Maximum Input Level	±1 dB error		−3		dBm
Minimum Input Level	±1 dB error		−53		dBm
Slope[1]		−25	−22	−19.5	mV/dB
Intercept[1]		12	15	21	dBm
Output Voltage, High Power In	P_{IN} = −10 dBm	0.42	0.58	0.78	V
Output Voltage, Low Power In	P_{IN} = −40 dBm	1.00	1.27	1.40	V
f = 1.9 GHz	R_{TADJ} = 8 kΩ				
Input Impedance			950||0.38		Ω||pF
±1 dB Dynamic Range	T_A = 25°C		50		dB
	−40°C < T_A < +85°C		48		dB
Maximum Input Level	±1 dB error		−4.00		dBm
Minimum Input Level	±1 dB error		−54		dBm
Slope[1]		−25	−22	−19.5	mV/dB
Intercept[1]		10	14	20	dBm
Output Voltage, High Power In	P_{IN} = −10 dBm	0.35	0.54	0.80	V
Output Voltage, Low Power In	P_{IN} = −35 dBm	0.75	1.21	1.35	V
f = 2.2 GHz	R_{TADJ} = 8 kΩ				
Input Impedance			810||0.39		Ω||pF
±1 dB Dynamic Range	T_A = 25°C		50		dB
	−40°C < T_A < +85°C		47		dB
Maximum Input Level	±1 dB error		−5		dBm
Minimum Input Level	±1 dB error		−55		dBm
Slope[1]			−22		mV/dB
Intercept[1]			14		dBm
Output Voltage, High Power In	P_{IN} = −10 dBm		0.53		V
Output Voltage, Low Power In	P_{IN} = −40 dBm		1.20		V
f = 3.6 GHz	R_{TADJ} = 8 kΩ				
Input Impedance			300||0.33		Ω||pF
±1 dB Dynamic Range	T_A = 25°C		42		dB
	−40°C < T_A < +85°C		40		dB
Maximum Input Level	±1 dB error		−6		dBm
Minimum Input Level	±1 dB error		−48		dBm
Slope[1]			−22		mV/dB
Intercept[1]			11		dBm
Output Voltage, High Power In	P_{IN} = −10 dBm		0.47		V
Output Voltage, Low Power In	P_{IN} = −40 dBm		1.16		V

Parameter	Conditions	Min	Typ	Max	Unit
f = 5.8 GHz	R_{TADJ} = 500 Ω				
Input Impedance			110||0.05		Ω||pF
±1 dB Dynamic Range	T_A = 25°C		50		dB
	−40°C < T_A < +85°C		48		dB
Maximum Input Level	±1 dB error		−4		dBm
Minimum Input Level	±1 dB error		−54		dBm
Slope[1]			−22		mV/dB
Intercept[1]			16		dBm
Output Voltage, High Power In	P_{IN} = −10 dBm		0.59		V
Output Voltage, Low Power In	P_{IN} = −40 dBm		1.27		V
f = 8.0 GHz	R_{TADJ} = open				
Input Impedance			28||0.79		Ω||pF
±1 dB Dynamic Range	T_A = 25°C		44		dB
	−40°C < T_A < +85°C		35		dB
Maximum Input Level	±1 dB error		−2		dBm
Minimum Input Level	±1 dB error		−46		dBm
Slope[2]			−22		mV/dB
Intercept[2]			21		dBm
Output Voltage, High Power In	P_{IN} = −10 dBm		0.70		V
Output Voltage, Low Power In	P_{IN} = −40 dBm		1.39		V
OUTPUT INTERFACE	VOUT (Pin 5)				
Voltage Swing	V_{SET} = 0 V, RFIN = open		V_{POS} − 0.1		V
	V_{SET} = 1.7 V, RFIN = open		10		mV
Output Current Drive	V_{SET} = 0 V, RFIN = open		10		mA
Small Signal Bandwidth	RFIN = −10 dBm, from CLPF to VOUT		140		MHz
Output Noise	RFIN = 2.2 GHz, −10 dBm, f_{NOISE} = 100 kHz, C_{LPF} = open		90		nV/√Hz
Fall Time	Input level = no signal to −10 dBm, 90% to 10%, C_{LPF} = 8 pF		18		ns
	Input level = no signal to −10 dBm, 90% to 10%, C_{LPF} = open, R_{OUT} = 150 Ω		6		ns
Rise Time	Input level = −10 dBm to no signal, 10% to 90%, C_{LPF} = 8 pF		20		ns
	Input level = −10 dBm to no signal, 10% to 90%, C_{LPF} = open, R_{OUT} = 150 Ω		10		ns
Video Bandwidth (or Envelope Bandwidth)			50		MHz
VSET INTERFACE	VSET (Pin 4)				
Nominal Input Range	RFIN = 0 dBm, measurement mode		0.35		V
	RFIN = −50 dBm, measurement mode		1.40		V
Logarithmic Scale Factor			−45		dB/V
Input Resistance	RFIN = −20 dBm, controller mode, V_{SET} = 1 V		40		kΩ
TADJ INTERFACE	TADJ (Pin 6)				
Input Resistance	TADJ = 0.9 V, sourcing 50 µA		13		kΩ
Disable Threshold Voltage	TADJ = open		V_{POS} − 0.4		V
POWER INTERFACE	VPOS (Pin 7)				
Supply Voltage		3.0		5.5	V
Quiescent Current		18	22	30	mA
vs. Temperature	−40°C ≤ T_A ≤ +85°C		60		µA/°C
Disable Current	TADJ = V_{POS}		200		µA

[1] Slope and intercept are determined by calculating the best-fit line between the power levels of −40 dBm and −10 dBm at the specified input frequency.
[2] Slope and intercept are determined by calculating the best-fit line between the power levels of −34 dBm and −16 dBm at 8.0 GHz.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, V_{POS}	5.7 V
V_{SET} Voltage	0 V to V_{POS}
Input Power (Single-Ended, Re: 50 Ω)	12 dBm
Internal Power Dissipation	0.73 W
θ_{JA}	55°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

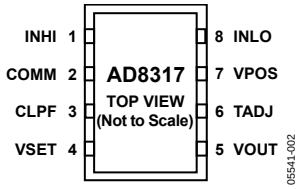


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	INHI	RF Input. Nominal input range of −50 dBm to 0 dBm, re: 50 Ω; ac-coupled RF input.
2	COMM	Device Common. Connect to a low impedance ground plane.
3	CLPF	Loop Filter Capacitor. In measurement mode, this capacitor sets the pulse response time and video bandwidth. In controller mode, the capacitance on this node sets the response time of the error amplifier/integrator.
4	VSET	Setpoint Control Input for Controller Mode or Feedback Input for Measurement Mode.
5	VOUT	Measurement and Controller Output. In measurement mode, VOUT provides a decreasing linear-in-dB representation of the RF input signal amplitude. In controller mode, VOUT is used to control the gain of a VGA or VVA with a positive gain sense (increasing voltage increases gain).
6	TADJ	Temperature Compensation Adjustment. Frequency-dependent temperature compensation is set by connecting a ground-referenced resistor to this pin.
7	VPOS	Positive Supply Voltage: 3.0 V to 5.5 V.
8	INLO	RF Common for INHI. AC-coupled RF common.
	Paddle	Internally connected to COMM; solder to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{POS} = 3 V; T_A = +25°C, −40°C, +85°C; C_{LPF} = 1000 pF, unless otherwise noted. Black: +25°C; Blue: −40°C; Red: +85°C. Error is calculated by using the best-fit line between P_{IN} = −40 dBm and P_{IN} = −10 dBm at the specified input frequency, unless otherwise noted

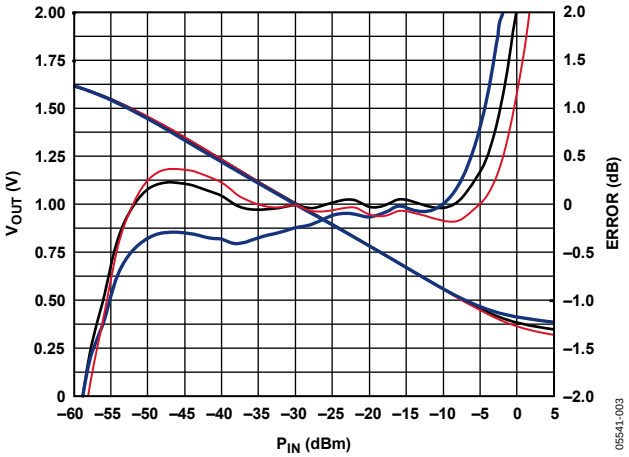


Figure 3. V_{OUT} and Log Conformance vs. Input Amplitude at 900 MHz, R_{TADJ} = 18 kΩ

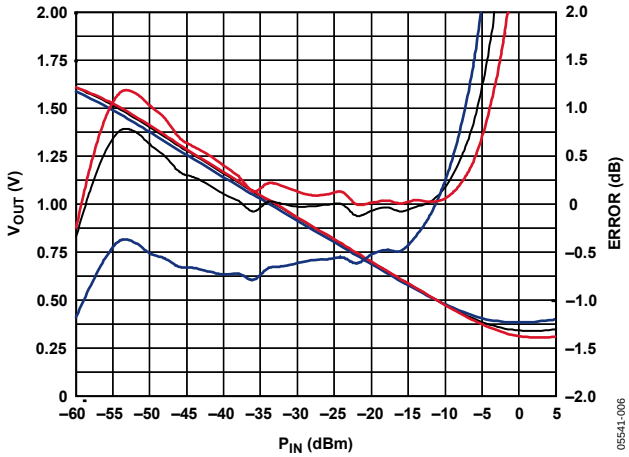


Figure 6. V_{OUT} and Log Conformance vs. Input Amplitude at 3.6 GHz, R_{TADJ} = 8 kΩ

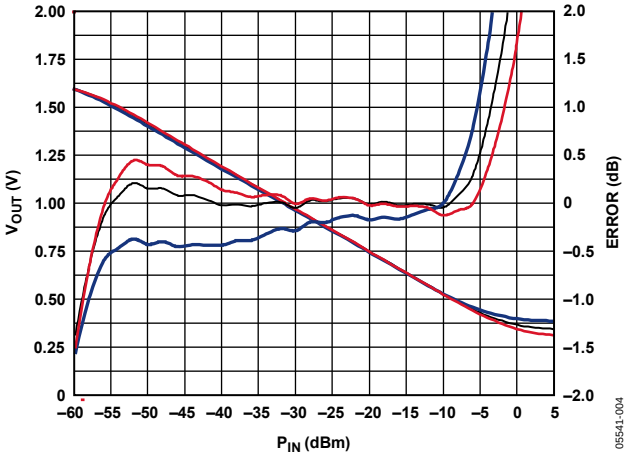


Figure 4. V_{OUT} and Log Conformance vs. Input Amplitude at 1.9 GHz, R_{TADJ} = 8 kΩ

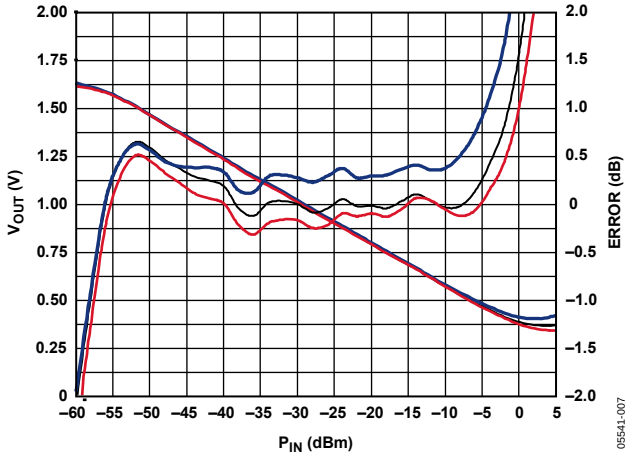


Figure 7. V_{OUT} and Log Conformance vs. Input Amplitude at 5.8 GHz, R_{TADJ} = 500 Ω

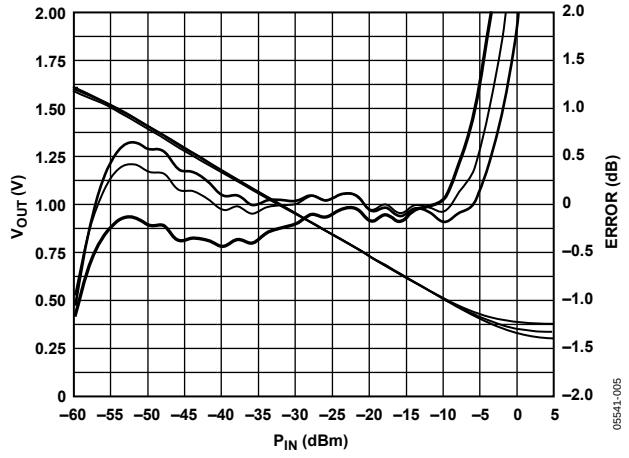


Figure 5. V_{OUT} and Log Conformance vs. Input Amplitude at 2.2 GHz, R_{TADJ} = 8 kΩ

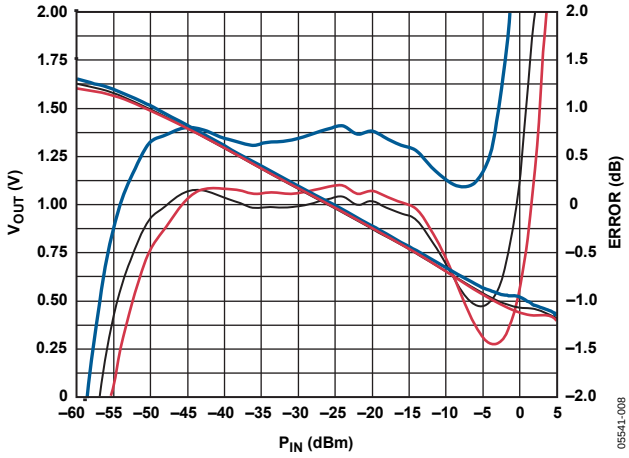


Figure 8. V_{OUT} and Log Conformance vs. Input Amplitude at 8.0 GHz, R_{TADJ} = Open, Error Calculated from P_{IN} = −34 dBm to P_{IN} = −16 dBm

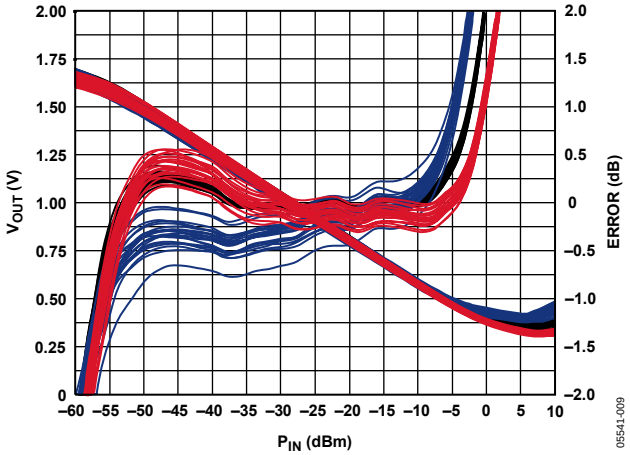


Figure 9. V_{OUT} and Log Conformance vs. Input Amplitude at 900 MHz, Multiple Devices, R_{TADJ} = 18 kΩ

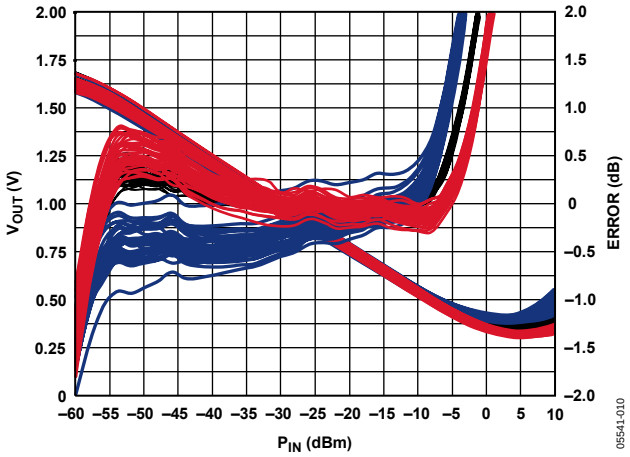


Figure 10. V_{OUT} and Log Conformance vs. Input Amplitude at 1.9 GHz, Multiple Devices, R_{TADJ} = 8 kΩ

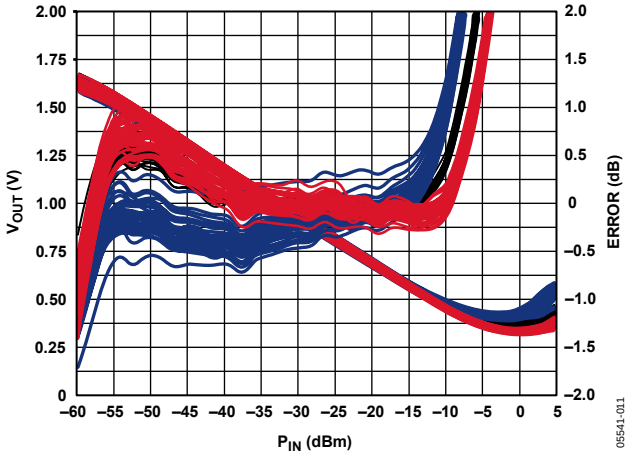


Figure 11. V_{OUT} and Log Conformance vs. Input Amplitude at 2.2 GHz, Multiple Devices, R_{TADJ} = 8 kΩ

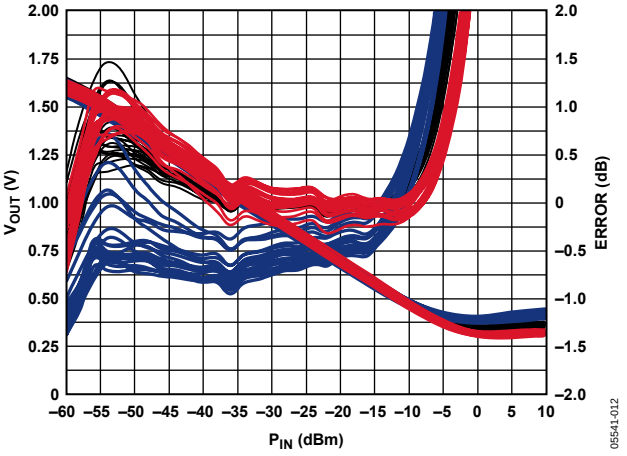


Figure 12. V_{OUT} and Log Conformance vs. Input Amplitude at 3.6 GHz, Multiple Devices, R_{TADJ} = 8 kΩ

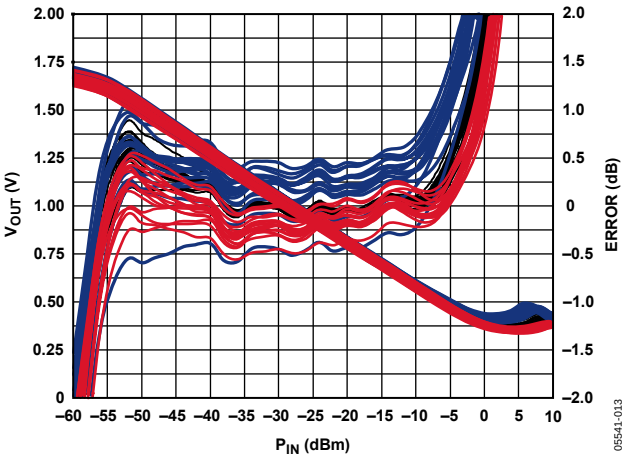


Figure 13. V_{OUT} and Log Conformance vs. Input Amplitude at 5.8 GHz, Multiple Devices, R_{TADJ} = 500 Ω

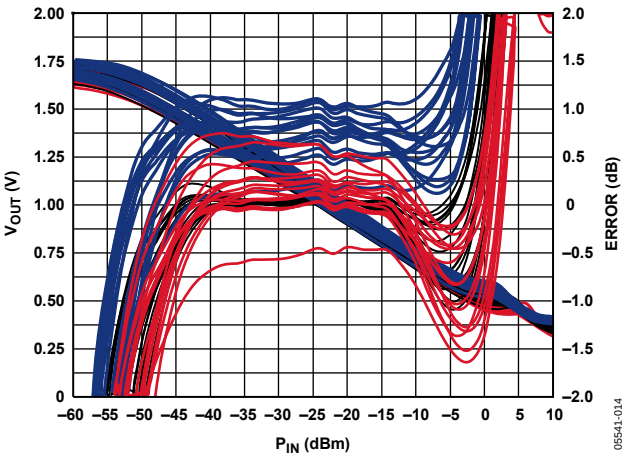


Figure 14. V_{OUT} and Log Conformance vs. Input Amplitude at 8.0 GHz, Multiple Devices, R_{TADJ} = Open, Error Calculated from P_{IN} = −34 dBm to P_{IN} = −16 dBm

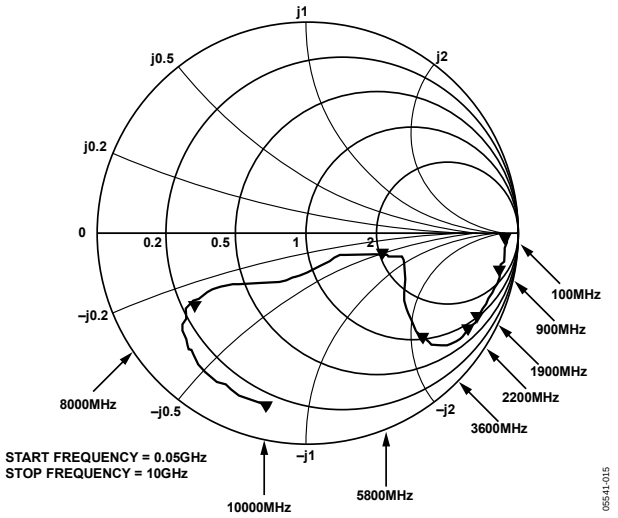


Figure 15. Input Impedance vs. Frequency; No Termination Resistor on INHI (Impedance De-Embedded to Input Pins), $Z_0 = 50\ \Omega$

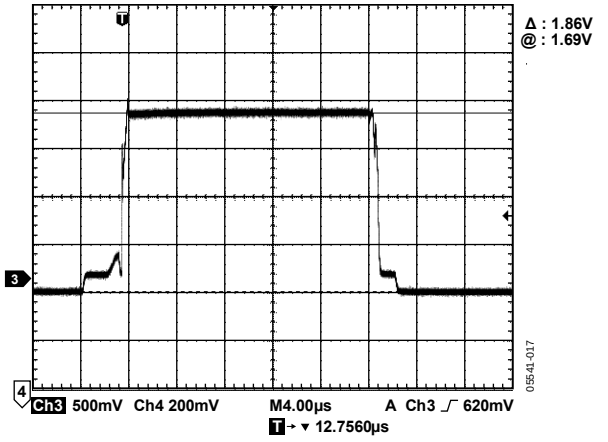


Figure 16. Power-On/Power-Off Response Time; $V_{POS} = 3.0$ V; Input AC-Coupling Capacitors = 10 pF; C_{LPF} = Open

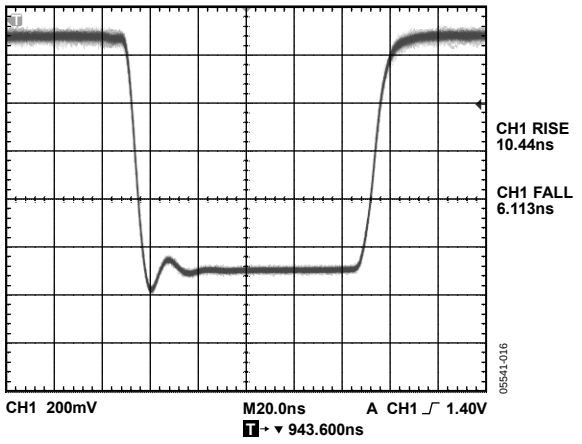


Figure 17. V_{OUT} Pulse Response Time; Pulsed RF Input 0.1 GHz, −10 dBm; C_{LPF} = Open; $R_{LOAD} = 150\ \Omega$

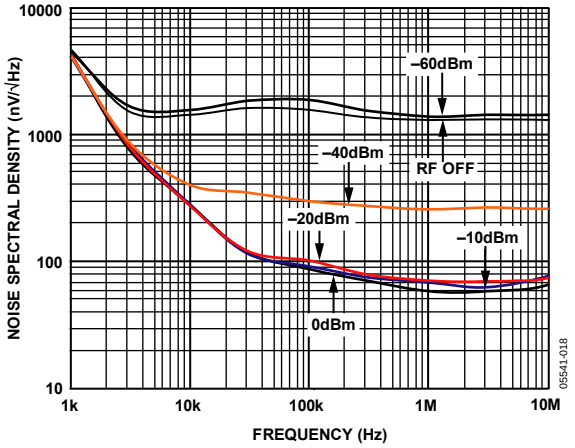


Figure 18. Noise Spectral Density of Output; C_{LPF} = Open

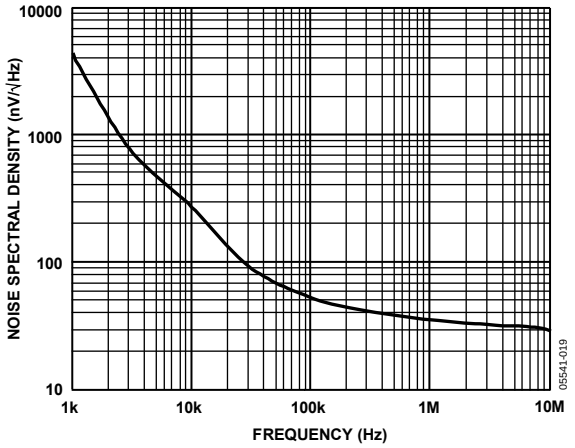


Figure 19. Noise Spectral Density of Output Buffer (from CLPF to VOUT); $C_{LPF} = 0.1\ \mu F$

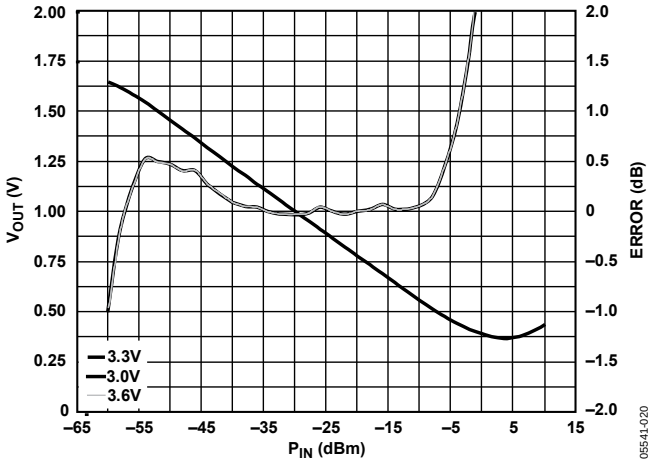


Figure 20. Output Voltage Stability vs. Supply Voltage at 1.9 GHz When V_{POS} Varies by 10%

THEORY OF OPERATION

The AD8317 is a 6-stage demodulating logarithmic amplifier, specifically designed for use in RF measurement and power control applications at frequencies up to 10 GHz. A block diagram is shown in Figure 21. Sharing much of its design with the AD8318 logarithmic detector/controller, the AD8317 maintains tight intercept variability vs. temperature over a 50 dB range. Additional enhancements over the AD8318, such as a reduced RF burst response time of 6 ns to 10 ns, 22 mA supply current, and board space requirements of only 2 mm × 3 mm, add to the low cost and high performance benefits of the AD8317.

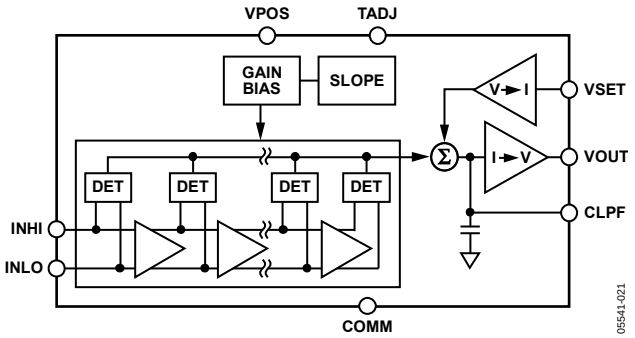


Figure 21. Block Diagram

A fully differential design, using a proprietary, high speed SiGe process, extends high frequency performance. Input INHI receives the signal with a low frequency impedance of nominally 500 Ω in parallel with 0.7 pF. The maximum input with ±1 dB log-conformance error is typically 0 dBm (re: 50 Ω). The noise spectral density referred to the input is 1.15 nV/√Hz, which is equivalent to a voltage of 118 μV rms in a 10.5 GHz bandwidth or a noise power of −66 dBm (re: 50 Ω). This noise spectral density sets the lower limit of the dynamic range. However, the low end accuracy of the AD8317 is enhanced by specially shaping the demodulating transfer characteristic to partially compensate for errors due to internal noise. The common pin, COMM, provides a quality low impedance connection to the printed circuit board (PCB) ground. The package paddle, which is internally connected to the COMM pin, should also be grounded to the PCB to reduce thermal impedance from the die to the PCB.

The logarithmic function is approximated in a piecewise fashion by six cascaded gain stages. (For a more comprehensive explanation of the logarithm approximation, see the AD8307 data sheet.) The cells have a nominal voltage gain of 9 dB each and a 3 dB bandwidth of 10.5 GHz. Using precision biasing, the gain is stabilized over temperature and supply variations. The overall dc gain is high, due to the cascaded nature of the gain stages. An offset compensation loop is included to correct for offsets within the cascaded cells. At the output of each of the gain stages, a square-law detector cell is used to rectify the signal.

The RF signal voltages are converted to a fluctuating differential current having an average value that increases with signal level. Along with the six gain stages and detector cells, an additional detector is included at the input of the AD8317, providing a 50 dB dynamic range in total. After the detector currents are summed and filtered, the following function is formed at the summing node:

$$I_D \times \log_{10}(V_{IN}/V_{INTERCEPT}) \quad (1)$$

where:
I_D is the internally set detector current.
V_{IN} is the input signal voltage.
$V_{INTERCEPT}$ is the intercept voltage (that is, when $V_{IN} = V_{INTERCEPT}$, the output voltage would be 0 V, if it were capable of going to 0 V).

USING THE AD8317

BASIC CONNECTIONS

The AD8317 is specified for operation up to 10 GHz; as a result, low impedance supply pins with adequate isolation between functions are essential. A power supply voltage of between 3.0 V and 5.5 V should be applied to VPOS. Power supply decoupling capacitors of 100 pF and 0.1 µF should be connected close to this power supply pin.

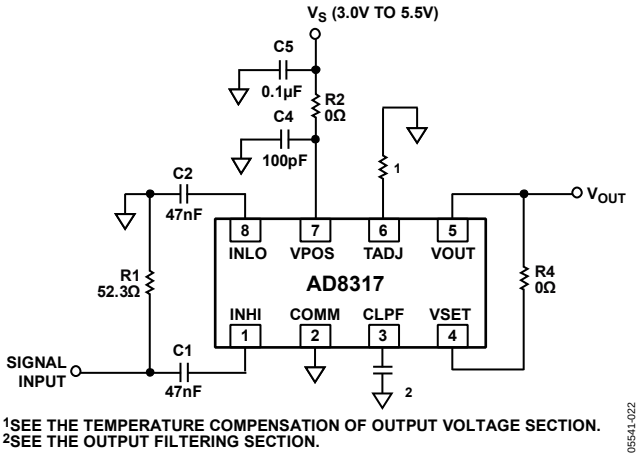


Figure 22. Basic Connections

The paddle of the LFCSP package is internally connected to COMM. For optimum thermal and electrical performance, the paddle should be soldered to a low impedance ground plane.

INPUT SIGNAL COUPLING

The RF input (INHI) is single-ended and must be ac-coupled. INLO (input common) should be ac-coupled to ground. Suggested coupling capacitors are 47 nF ceramic 0402-style capacitors for input frequencies of 1 MHz to 10 GHz. The coupling capacitors should be mounted close to the INHI and INLO pins. The coupling capacitor values can be increased to lower the high-pass cutoff frequency of the input stage. The high-pass corner is set by the input coupling capacitors and the internal 10 pF high-pass capacitor. The dc voltage on INHI and INLO is approximately one diode voltage drop below V_{POS}.

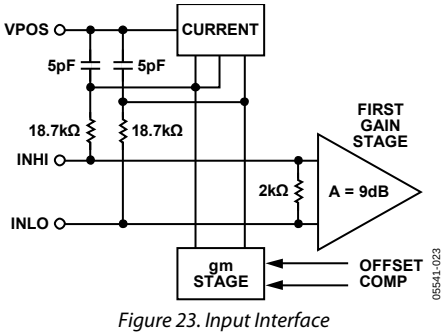


Figure 23. Input Interface

While the input can be reactively matched, in general, this is not necessary. An external 52.3 Ω shunt resistor (connected on the signal side of the input coupling capacitors, as shown in Figure 22) combines with the relatively high input impedance to give an adequate broadband 50 Ω match.

The coupling time constant, 50 × C_C/2, forms a high-pass corner with a 3 dB attenuation at $f_{HP} = 1/(2\pi \times 50 \times C_C)$, where C1 = C2 = C_C. Using the typical value of 47 nF, this high-pass corner is ~68 kHz. In high frequency applications, f_{HP} should be as large as possible to minimize the coupling of unwanted low frequency signals. In low frequency applications, a simple RC network forming a low-pass filter should be added at the input for similar reasons. This low-pass filter network should generally be placed at the generator side of the coupling capacitors, thereby lowering the required capacitance value for a given high-pass corner frequency.

OUTPUT INTERFACE

The VOUT pin is driven by a PNP output stage. An internal 10 Ω resistor is placed in series with the output and the VOUT pin. The rise time of the output is limited mainly by the slew on CLPF. The fall time is an RC-limited slew given by the load capacitance and the pull-down resistance at VOUT. There is an internal pull-down resistor of 1.6 kΩ. A resistive load at VOUT is placed in parallel with the internal pull-down resistor to provide additional discharge current.

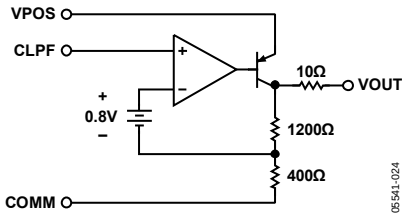


Figure 24. Output Interface

To reduce the fall time, VOUT should be loaded with a resistive load of <1.6 kΩ. For example, with an external load of 150 Ω, the AD8317 fall time is <7 ns.

SETPOINT INTERFACE

The V_{SET} input drives the high impedance (40 kΩ) input of an internal op amp. The V_{SET} voltage appears across the internal 1.5 kΩ resistor to generate I_{SET}. When a portion of V_{OUT} is applied to VSET, the feedback loop forces

$$-I_D \times \log_{10}(V_{IN}/V_{INTERCEPT}) = I_{SET} \quad (2)$$

If $V_{SET} = V_{OUT}/2x$, then $I_{SET} = V_{OUT}/(2x \times 1.5\ k\Omega)$.

The result is

$$V_{OUT} = (-I_D \times 1.5\ k\Omega \times 2x) \times \log_{10}(V_{IN}/V_{INTERCEPT})$$

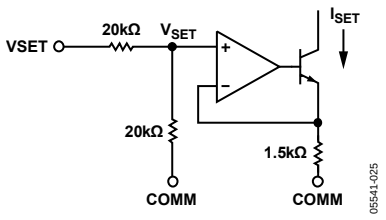


Figure 25. VSET Interface

The slope is given by

$$-I_D \times 2x \times 1.5\ \text{k}\Omega = -22\ \text{mV/dB} \times x$$

For example, if a resistor divider to ground is used to generate a V_{SET} voltage of $V_{OUT}/2$, x = 2. The slope is set to −880 V/decade or −44 mV/dB.

TEMPERATURE COMPENSATION OF OUTPUT VOLTAGE

The primary component of the variation in V_{OUT} vs. temperature, as the input signal amplitude is held constant, is the drift of the intercept. This drift is also a weak function of the input signal frequency; therefore, provision is made for the optimization of internal temperature compensation at a given frequency by providing Pin TADJ.

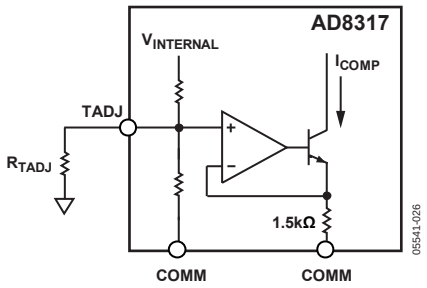


Figure 26. TADJ Interface

R_{TADJ} is connected between TADJ and ground. The value of this resistor partially determines the magnitude of an analog correction coefficient, which is used to reduce intercept drift.

The relationship between output temperature drift and frequency is not linear and cannot be easily modeled. As a result, experimentation is required to choose the correct TADJ resistor. Table 4 shows the recommended values for some commonly used frequencies.

Table 4. Recommended R_{TADJ} Values

Frequency	Recommended R_{TADJ}
50 MHz	18 kΩ
100 MHz	18 kΩ
900 MHz	18 kΩ
1.8 GHz	8 kΩ
1.9 GHz	8 kΩ
2.2 GHz	8 kΩ
3.6 GHz	8 kΩ
5.3 GHZ	500 Ω
5.8 GHz	500 Ω
8 GHz	Open

MEASUREMENT MODE

When the V_{OUT} voltage or a portion of the V_{OUT} voltage is fed back to the VSET pin, the device operates in measurement mode. As seen in Figure 27, the AD8317 has an offset voltage, a negative slope, and a V_{OUT} measurement intercept at the high end of its input signal range.

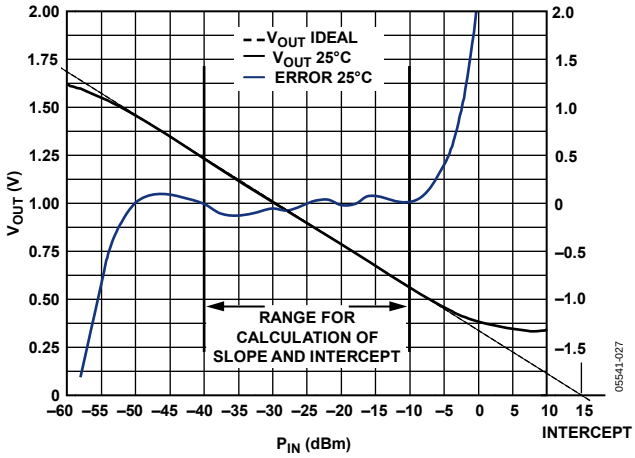


Figure 27. Typical Output Voltage vs. Input Signal

The output voltage vs. input signal voltage of the AD8317 is linear-in-dB over a multidecade range. The equation for this function is

$$V_{OUT} = X \times V_{SLOPE/DEC} \times \log_{10}(V_{IN}/V_{INTERCEPT}) \quad (3)$$

$$= X \times V_{SLOPE/dB} \times 20 \times \log_{10}(V_{IN}/V_{INTERCEPT}) \quad (4)$$

where:
X is the feedback factor in $V_{SET} = V_{OUT}/X$.
$V_{SLOPE/DEC}$ is nominally −440 mV/decade, or −22 mV/dB.
$V_{INTERCEPT}$ is the x-axis intercept of the linear-in-dB portion of the V_{OUT} vs. P_{IN} curve (see Figure 27).
$V_{INTERCEPT}$ is 2 dBV for a sinusoidal input signal.

An offset voltage, V_{OFFSET}, of 0.35 V is internally added to the detector signal, so that the minimum value for V_{OUT} is $X \times V_{OFFSET}$; therefore, for X = 1, the minimum V_{OUT} is 0.35 V.

The slope is very stable vs. process and temperature variation. When base-10 logarithms are used, $V_{SLOPE/DECADE}$ represents the volts/decade. A decade corresponds to 20 dB; $V_{SLOPE/DECADE}/20 = V_{SLOPE/dB}$ represents the slope in volts/dB.

As noted in Equation 3 and Equation 4, the V_{OUT} voltage has a negative slope. This is also the correct slope polarity to control the gain of many power amplifiers in a negative feedback configuration. Because both the slope and intercept vary slightly with frequency, it is recommended to refer to the Specifications section for application-specific values for slope and intercept.

Although demodulating log amps respond to input signal voltage, not input signal power, it is customary to discuss the amplitude of high frequency signals in terms of power. In this case, the characteristic impedance of the system, Z_0, must be known to convert voltages to their corresponding power levels. The following equations are used to perform this conversion:

$$P\ [\text{dBm}] = 10 \times \log_{10}(V_{RMS}^2/(Z_0 \times 1\ \text{mW})) \quad (5)$$

$$P\ [\text{dBV}] = 20 \times \log_{10}(V_{RMS}/1\ \text{V}_{RMS}) \quad (6)$$

$$P\ [\text{dBm}] = P\ [\text{dBV}] - 10 \times \log_{10}(Z_0 \times 1\ \text{mW}/1\ \text{V}_{RMS}^2) \quad (7)$$

For example, $P_{INTERCEPT}$ for a sinusoidal input signal expressed in terms of dBm (decibels referred to 1 mW), in a 50 Ω system is

$$P_{INTERCEPT}\ [\text{dBm}] = P_{INTERCEPT}\ [\text{dBV}] - 10 \times \log_{10}(Z_0 \times 1\ \text{mW}/1\ V_{RMS}^2) = 2\ \text{dBV} - 10 \times \log_{10}(50 \times 10^{-3}) = 15\ \text{dBm} \quad (8)$$

For a square wave input signal in a 200 Ω system,

$$P_{INTERCEPT} = -1\ \text{dBV} - 10 \times \log_{10}[(200\ \Omega \times 1\ \text{mW}/1\ V_{RMS}^2)] = 6\ \text{dBm}$$

Further information on the intercept variation dependence upon waveform can be found in the AD8313 and AD8307 data sheets.

SETTING THE OUTPUT SLOPE IN MEASUREMENT MODE

To operate in measurement mode, VOUT must be connected to VSET. Connecting VOUT directly to VSET yields the nominal logarithmic slope of approximately −22 mV/dB. The output swing corresponding to the specified input range is then approximately 0.35 V to 1.7 V. The slope and output swing can be increased by placing a resistor divider between VOUT and VSET (that is, one resistor from VOUT to VSET and one resistor from VSET to ground). The input impedance of VSET is approximately 40 kΩ. Slope-setting resistors should be kept below 20 kΩ to prevent this input impedance from affecting the resulting slope. If two equal resistors are used (for example, 10 kΩ/10 kΩ), the slope doubles to approximately −44 mV/dB.

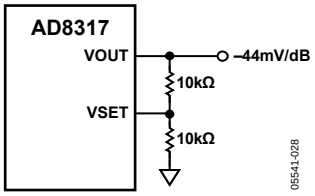


Figure 28. Increasing the Slope

CONTROLLER MODE

The AD8317 provides a controller mode feature at the VOUT pin. By using V_{SET} for the setpoint voltage, it is possible for the AD8317 to control subsystems, such as power amplifiers (PAs), variable gain amplifiers (VGAs), or variable voltage attenuators (VVAs), that have output power that increases monotonically with respect to their gain control signal.

To operate in controller mode, the link between VSET and VOUT is broken. A setpoint voltage is applied to the VSET input, VOUT is connected to the gain control terminal of the VGA, and the RF input of the detector is connected to the output of the VGA (usually using a directional coupler and some additional attenuation). Based on the defined relationship between V_{OUT} and the RF input signal when the device is in measurement mode, the AD8317 adjusts the voltage on VOUT (VOUT is now an error amplifier output) until the level at the RF input corresponds to the applied V_{SET}. When the AD8317 operates in controller mode, there is no defined relationship between the V_{SET} and the V_{OUT} voltage; V_{OUT} settles to a value that results in the correct input signal level appearing at INHI/INLO.

For this output power control loop to be stable, a ground-referenced capacitor must be connected to the CLPF pin. This capacitor, C_{FLT}, integrates the error signal (in the form of a current) to set the loop bandwidth and ensure loop stability. Further details on control loop dynamics can be found in the AD8315 data sheet.

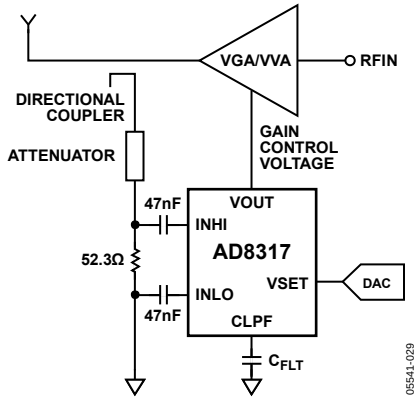


Figure 29. Controller Mode

Decreasing V_{SET}, which corresponds to demanding a higher signal from the VGA, increases V_{OUT}. The gain control voltage of the VGA must have a positive sense. A positive control voltage to the VGA increases the gain of the device.

The basic connections for operating the AD8317 in an automatic gain control (AGC) loop with the ADL5330 are shown in Figure 30. The ADL5330 is a 10 MHz to 3 GHz VGA. It offers a large gain control range of 60 dB with ±0.5 dB gain stability. This configuration is similar to Figure 29.

The gain of the ADL5330 is controlled by the output pin of the AD8317. This voltage, V_{OUT}, has a range of 0 V to near V_{POS}. To avoid overdrive recovery issues, the AD8317 output voltage can be scaled down using a resistive divider to interface with the 0 V to 1.4 V gain control range of the ADL5330.

A coupler/attenuation of 21 dB is used to match the desired maximum output power from the VGA to the top end of the linear operating range of the AD8317 (approximately −5 dBm at 900 MHz).

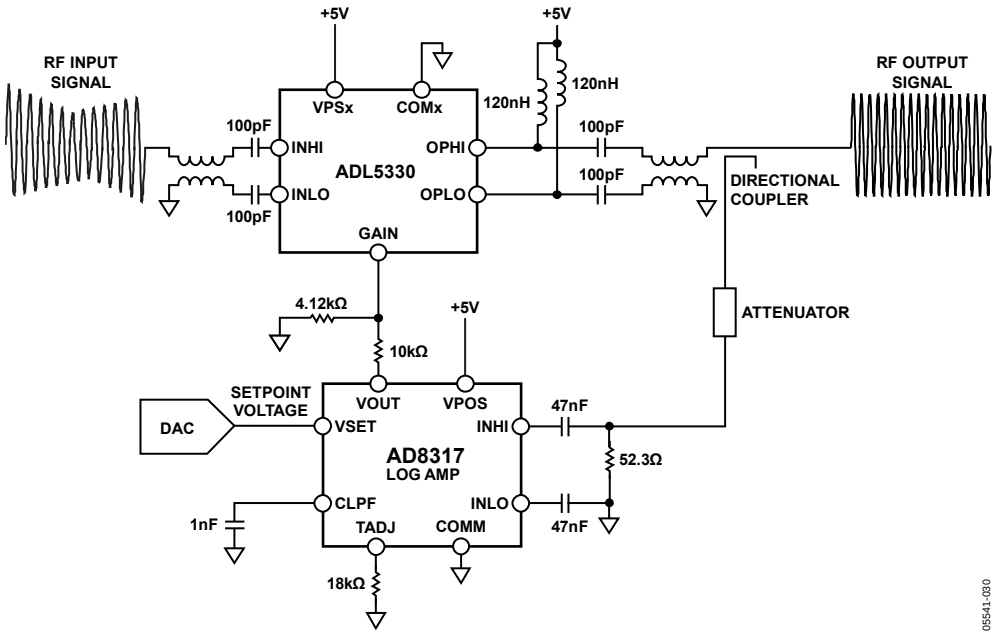


Figure 30. AD8317 Operating in Controller Mode to Provide Automatic Gain Control Functionality in Combination with the ADL5330

Figure 31 shows the transfer function of the output power vs. the setpoint voltage over temperature for a 900 MHz sine wave with an input power of −1.5 dBm. Note that the power control of the AD8317 has a negative sense. Decreasing V_{SET}, which corresponds to demanding a higher signal from the ADL5330, increases gain.

The AGC loop is capable of controlling signals just under the full 60 dB gain control range of the ADL5330. The performance over temperature is most accurate over the highest power range, where it is generally most critical. Across the top 40 dB range of output power, the linear conformance error is well within ±0.5 dB over temperature.

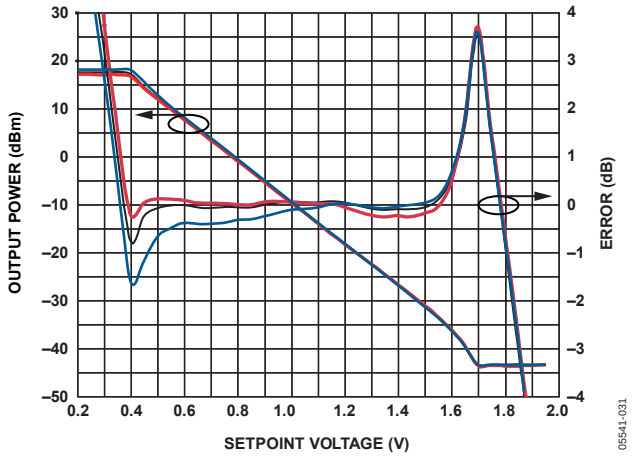


Figure 31. ADL5330 Output Power vs. AD8317 Setpoint Voltage, P_{IN} = −1.5 dBm

For the AGC loop to remain in equilibrium, the AD8317 must track the envelope of the ADL5330 output signal and provide the necessary voltage levels to the ADL5330 gain control input. Figure 32 shows an oscilloscope screenshot of the AGC loop depicted in Figure 30. A 100 MHz sine wave with 50% AM modulation is applied to the ADL5330. The output signal from the VGA is a constant envelope sine wave with amplitude corresponding to a setpoint voltage at the AD8317 of 1.5 V. Also shown is the gain control response of the AD8317 to the changing input envelope.

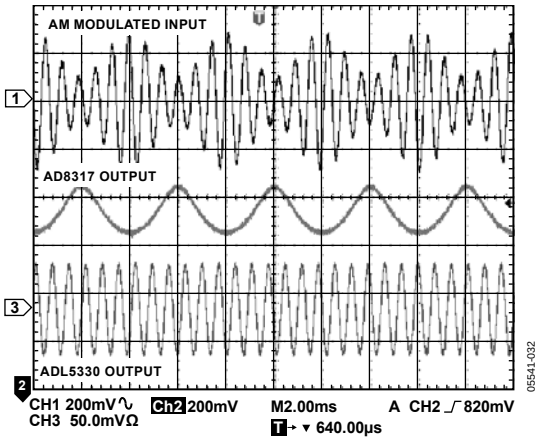


Figure 32. Oscilloscope Screenshot Showing an AM Modulated Input Signal and the Response from the AD8317

Figure 33 shows the response of the AGC RF output to a pulse on VSET. As V_{SET} decreases from 1.7 V to 0.4 V, the AGC loop responds with an RF burst. In this configuration, the input signal to the ADL5330 is a 1 GHz sine wave at a power level of −15 dBm.

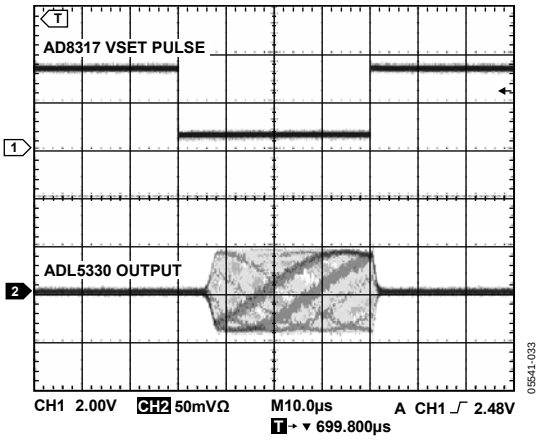


Figure 33. Oscilloscope Screenshot Showing the Response Time of the AGC Loop

Response time and the amount of signal integration are controlled by C_{FLT}. This functionality is analogous to the feedback capacitor around an integrating amplifier. Although it is possible to use large capacitors for C_{FLT}, in most applications, values under 1 nF provide sufficient filtering.

Calibration in controller mode is similar to the method used in measurement mode. A simple 2-point calibration can be done by applying two known V_{SET} voltages or DAC codes and measuring the output power from the VGA. Slope and intercept can then be calculated by:

$$Slope = (V_{SET1} - V_{SET2})/(P_{OUT1} - P_{OUT2}) \quad (9)$$

$$Intercept = P_{OUT1} - V_{SET1}/Slope \quad (10)$$

$$V_{SETx} = Slope \times (P_{OUTX} - Intercept) \quad (11)$$

More information on the use of the ADL5330 in AGC applications can be found in the ADL5330 data sheet.

OUTPUT FILTERING

For applications in which maximum video bandwidth and, consequently, fast rise time are desired, it is essential that the CLPF pin be left unconnected and free of any stray capacitance.

The nominal output video bandwidth of 50 MHz can be reduced by connecting a ground-referenced capacitor (C_{FLT}) to the CLPF pin, as shown in Figure 34. This is generally done to reduce output ripple (at twice the input frequency for a symmetric input waveform such as sinusoidal signals).

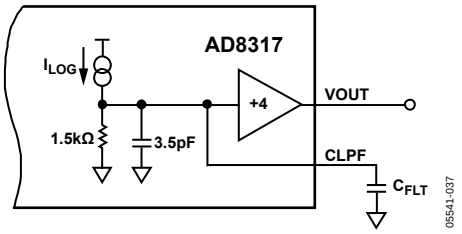


Figure 34. Lowering the Postdemodulation Bandwidth

C_{FLT} is selected by

$$C_{FLT} = \frac{1}{(2\pi \times 1.5\ \text{k}\Omega \times Video\ Bandwidth)} - 3.5\ \text{pF} \quad (12)$$

The video bandwidth should typically be set to a frequency equal to about one-tenth the minimum input frequency. This ensures that the output ripple of the demodulated log output, which is at twice the input frequency, is well filtered.

In many log amp applications, it may be necessary to lower the corner frequency of the postdemodulation filter to achieve low output ripple while maintaining a rapid response time to changes in signal level. An example of a 4-pole active filter is shown in the AD8307 data sheet.

OPERATION BEYOND 8 GHz

The AD8317 is specified for operation up to 8 GHz, but it provides useful measurement accuracy over a reduced dynamic range of up to 10 GHz. Figure 35 shows the performance of the AD8317 over temperature at 10 GHz when the device is configured as shown in Figure 22. Dynamic range is reduced at this frequency, but the AD8317 does provide 30 dB of measurement range within ±3 dB of linearity error.

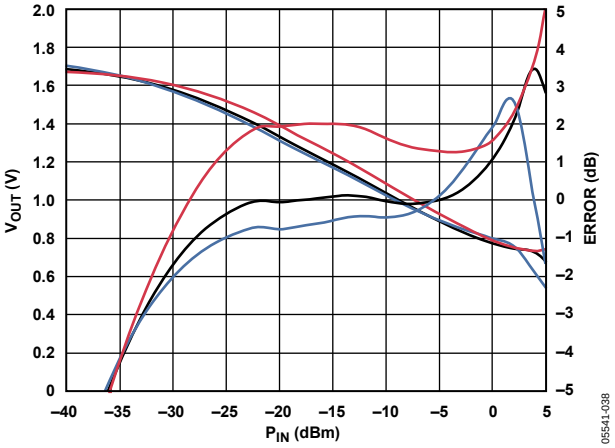


Figure 35. V_{OUT} and Log Conformance vs. Input Amplitude at 10.0 GHz, Multiple Devices, R_{TADJ} = Open, C_{LPF} = 1000 pF

Implementing an impedance match for frequencies beyond 8 GHz can improve the sensitivity of the AD8317 and measurement range.

Operation beyond 10 GHz is possible, but part-to-part variation, most notably in the intercept, becomes significant.

EVALUATION BOARD

Table 5. Evaluation Board (Rev. A) Configuration Options

Component	Function	Default Conditions
VPOS, GND	Supply and Ground Connections.	Not applicable
R1, C1, C2	Input Interface. The 52.3 Ω resistor in Position R1 combines with the internal input impedance of the AD8317 to give a broadband input impedance of about 50 Ω. C1 and C2 are dc-blocking capacitors. A reactive impedance match can be implemented by replacing R1 with an inductor and C1 and C2 with appropriately valued capacitors.	R1 = 52.3 Ω (Size 0402) C1 = 47 nF (Size 0402) C2 = 47 nF (Size 0402)
R5, R7	Temperature Compensation Interface. The internal temperature compensation network is optimized for input signals up to 3.6 GHz when R7 is 10 kΩ. This circuit can be adjusted to optimize performance for other input frequencies by changing the value of the resistor in Position R7. See Table 4 for specific R_{TADJ} resistor values.	R5 = 200 Ω (Size 0402) R7 = open (Size 0402)
R2, R3, R4, R6, RL, CL	Output Interface—Measurement Mode. In measurement mode, a portion of the output voltage is fed back to the VSET pin via R2. The magnitude of the slope of the VOUT output voltage response can be increased by reducing the portion of V_{OUT} that is fed back to VSET. R6 can be used as a back-terminating resistor or as part of a single-pole, low-pass filter.	R2 = 0 Ω (Size 0402) R3 = open (Size 0402) R4 = open (Size 0402) R6 = 1 kΩ (Size 0402) RL = CL = open (Size 0402)
R2, R3	Output Interface—Controller Mode. In this mode, R2 must be open. In controller mode, the AD8317 can control the gain of an external component. A setpoint voltage is applied to Pin VSET, the value of which corresponds to the desired RF input signal level applied to the AD8317 RF input. A sample of the RF output signal from this variable gain component is selected, typically via a directional coupler, and applied to the AD8317 RF input. The voltage at the VOUT pin is applied to the gain control of the variable gain element. A control voltage is applied to the VSET pin. The magnitude of the control voltage can optionally be attenuated via the voltage divider comprising R2 and R3, or a capacitor can be installed in Position R3 to form a low-pass filter along with R2.	R2 = open (Size 0402) R3 = open (Size 0402)
C4, C5	Power Supply Decoupling. The nominal supply decoupling consists of a 100 pF filter capacitor placed physically close to the AD8317 and a 0.1 µF capacitor placed nearer to the power supply input pin.	C4 = 0.1 µF (Size 0603) C5 = 100 pF (Size 0402)
C3	Filter Capacitor. The low-pass corner frequency of the circuit that drives the VOUT pin can be lowered by placing a capacitor between CLPF and ground. Increasing this capacitor increases the overall rise/fall time of the AD8317 for pulsed input signals. See the Output Filtering section for more details.	C3 = 8.2 pF (Size 0402)

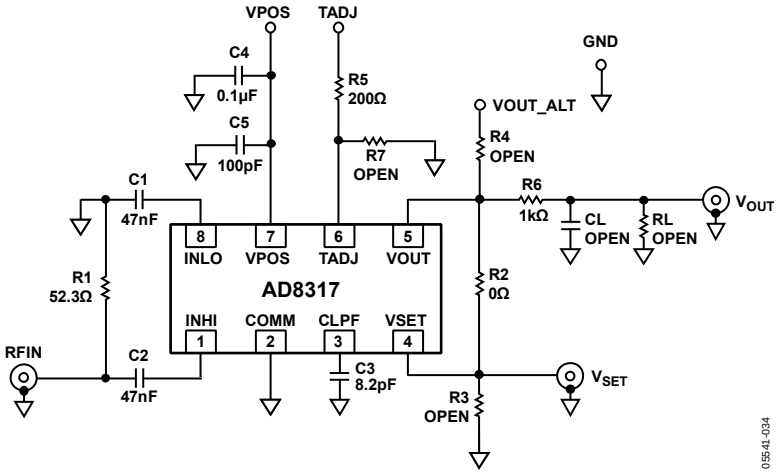


Figure 36. Evaluation Board Schematic

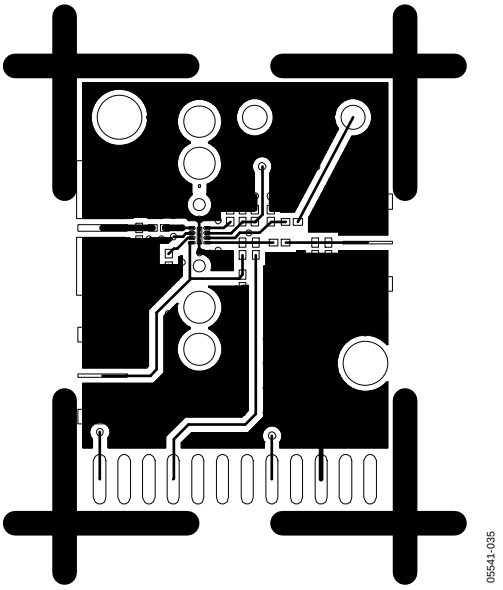


Figure 37. Component Side Layout

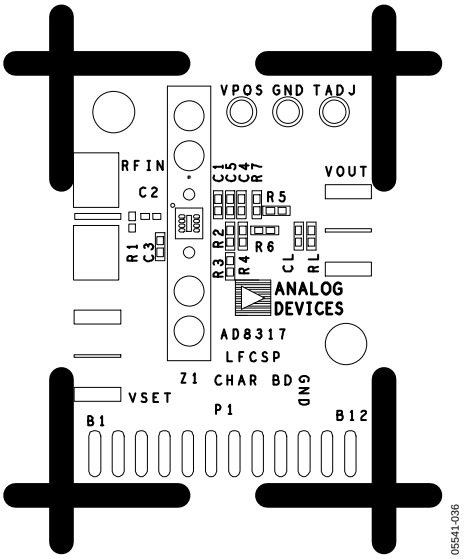
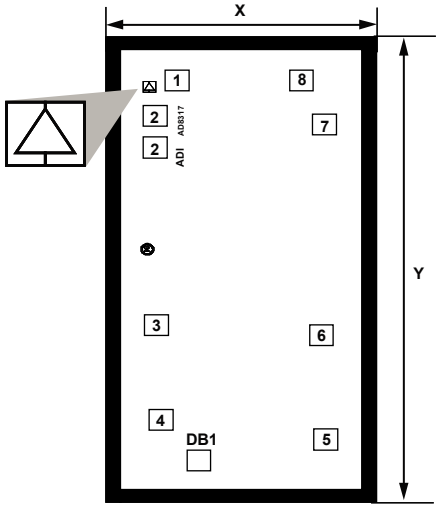


Figure 38. Component Side Silkscreen

DIE INFORMATION



BOND PAD STATISTICS
ALL MEASURMENTS IN MICRONS.
MINIMUM PASSIVATION OPENING: 59 × 59 MIN PAD PITCH: 89

DIE SIZE CALCULATION
ALL MEASURMENTS IN MICRONS.
DIEX (WIDTH OF DIE IN X DIRECTION) = 670
DIEY (WIDTH OF DIE IN Y DIRECTION) = 1325

DIE THICKNESS = 305 MICRONS

BALL BOND SHEAR STRENGTH SPECIFICATION: MINIMUM 15 GRAMS

05541-039

Figure 39. Die Outline Dimensions

Table 6. Die Pad Function Descriptions

Pin No.	Mnemonic	Description
1	INHI	RF Input. Nominal input range of −50 dBm to 0 dBm, re: 50 Ω; ac-coupled RF input.
2, 2	COMM	Device Common. Connect both pads to a low impedance ground plane.
3	CLPF	Loop Filter Capacitor. In measurement mode, this capacitor sets the pulse response time and video bandwidth. In controller mode, the capacitance on this node sets the response time of the error amplifier/integrator.
4	VSET	Setpoint Control Input for Controller Mode or Feedback Input for Measurement Mode.
5	VOUT	Measurement and Controller Output. In measurement mode, VOUT provides a decreasing linear-in dB representation of the RF input signal amplitude. In controller mode, VOUT is used to control the gain of a VGA or VVA with a positive gain sense (increasing voltage increases gain).
6	TADJ	Temperature Compensation Adjustment. Frequency-dependent temperature compensation is set by connecting a ground-referenced resistor to this pin.
7	VPOS	Positive Supply Voltage: 3.0 V to 5.5 V.
8	INLO	RF Common for INHI. AC-coupled RF common.
DB1	COMM	Device Common. Connect to a low impedance ground plane.

OUTLINE DIMENSIONS

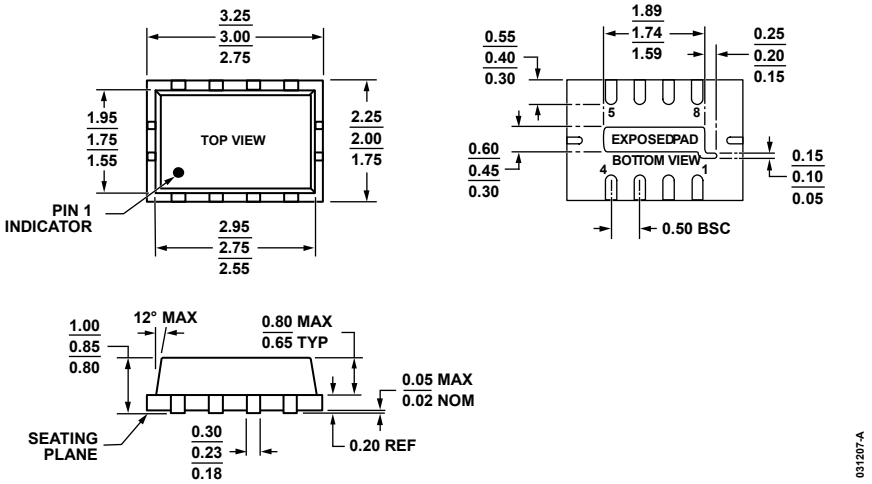


Figure 40. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
2 mm × 3 mm Body, Very Thin, Dual Lead
(CP-8-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8317ACPZ-R7[1]	−40°C to +85°C	8-Lead LFCSP_VD, 7″ Tape and Reel	CP-8-1	Q1
AD8317ACPZ-R2[1]	−40°C to +85°C	8-Lead LFCSP_VD, 7″ Tape and Reel	CP-8-1	Q1
AD8317ACPZ-WP[1]	−40°C to +85°C	8-Lead LFCSP_VD, Waffle Pack	CP-8-1	Q1
AD8317ACHIPS	−40°C to +85°C	Die		
AD8317-EVALZ[1]		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

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