50 dB GSM PA Controller

Data Sheet

AD8315

FEATURES

Complete RF detector/controller function
>50 dB range at 0.9 GHz (−49 dBm to +2 dBm, re 50 Ω)
Accurate scaling from 0.1 GHz to 2.5 GHz
Temperature-stable linear-in-dB response
Log slope of 23 mV/dB, intercept at −60 dBm at 0.9 GHz
True integration function in control loop
Low power: 20 mW at 2.7 V, 38 mW at 5 V
Power-down to 10.8 µW

APPLICATIONS

Single, dual, and triple band mobile handset (GSM, DCS, EDGE)
Transmitter power control

GENERAL DESCRIPTION

The AD8315 is a complete low cost subsystem for the precise control of RF power amplifiers operating in the frequency range 0.1 GHz to 2.5 GHz and over a typical dynamic range of 50 dB. It is intended for use in cellular handsets and other battery-operated wireless devices. The log amp technique provides a much wider measurement range and better accuracy than controllers using diode detectors. In particular, the temperature stability is excellent over a specified range of −30°C to +85°C.

Its high sensitivity allows control at low signal levels, thus reducing the amount of power that must be coupled to the detector.

For convenience, the signal is internally ac-coupled. This high-pass coupling, with a corner at approximately 0.016 GHz, determines the lowest operating frequency. Therefore, the source can be dc grounded.

The AD8315 provides a voltage output, VAPC, that has the voltage range and current drive to directly connect to most handset power amplifiers' gain control pin. VAPC can swing from 250 mV above ground to within 200 mV below the supply voltage. Load currents of up to 6 mA can be supported.

The setpoint control input is applied to the VSET pin and has an operating range of 0.25 V to 1.4 V. The associated circuit determines the slope and intercept of the linear-in-dB measurement system; these are nominally 23 mV/dB and −60 dBm for a 50 Ω termination (−73 dBV) at 0.9 GHz. Further simplifying the application of the AD8315, the input resistance of the setpoint interface is over 100 MΩ, and the bias current is typically 0.5 µA.

The AD8315 is available in MSOP and LFCSP packages and consumes 8.5 mA from a 2.7 V to 5.5 V supply. When powered down, the sleep current is 4 µA.

FUNCTIONAL BLOCK DIAGRAM

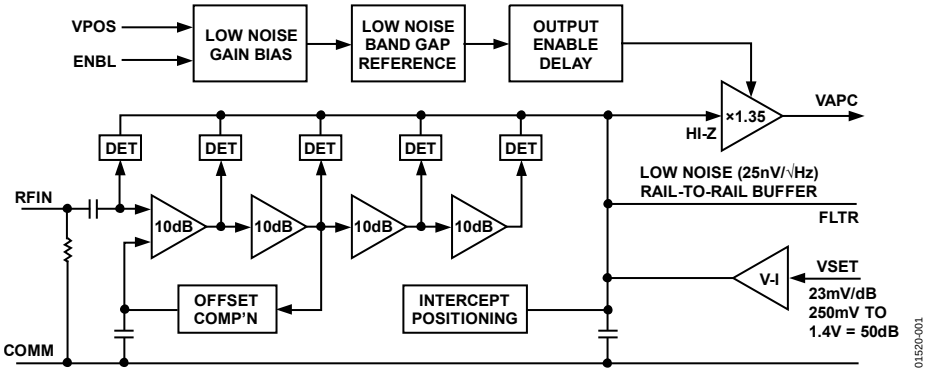


Figure 1.

Rev. D **Document Feedback**
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REVISION HISTORY

8/2016—Rev. C to Rev. D

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6/2006—Rev. B to Rev. C

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1/2003—Rev. 0 to Rev. B

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10/1999—Revision 0: Initial Version

SPECIFICATIONS

V_S = 2.7 V, T = 25°C, 52.3 Ω termination on RFIN, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range[1]	To meet all specifications	0.1		2.5	GHz
Input Voltage Range	±1 dB log conformance, 0.1 GHz	−57		−11	dBV
Equivalent dBm Range		−44		+2	dBm
Logarithmic Slope[2]	0.1 GH	21.5	24	25.5	mV/dB
Logarithmic Intercept[2]	0.1 GHz	−79	−70	−64	dBV
Equivalent dBm Level		−66	−57	−51	dBm
RF INPUT INTERFACE	Pin RFIN				
Input Resistance[3]	0.1 GHz		2.8		kΩ
Input Capacitance[3]	0.1 GHz		0.9		pF
OUTPUT	Pin VAPC				
Minimum Output Voltage	V_{SET} ≤ 200 mV, ENBL high	0.25	0.27	0.3	V
	ENBL low		0.02		V
Maximum Output Voltage	R_L ≥ 800 Ω	2.45		2.6	V
vs. Temperature[4]	85°C, V_{POS} = 3 V, I_{OUT} = 6 mA	2.54			V
General Limit	2.7 V ≤ V_{POS} ≤ 5.5 V, R_L = ∞		V_{POS} − 0.1		V
Output Current Drive	Source/Sink		5/200		mA/µA
Output Buffer Noise			25		nV√Hz
Output Noise	RF input = 2 GHz, 0 dBm, f_{NOISE} = 100 kHz, C_{FLT} = 220 pF		130		nV/√Hz
Small Signal Bandwidth	0.2 V to 2.6 V swing		30		MHz
Slew Rate	10% to 90%, 1.2 V step (V_{SET}), open loop[5]		13		V/µs
Response Time	FLTR = open, see Figure 27		150		ns
SETPOINT INTERFACE	Pin VSET				
Nominal Input Range	Corresponding to central 50 dB	0.25		1.4	V
Logarithmic Scale Factor			43.5		dB/V
Input Resistance			100		kΩ
Slew Rate			16		V/µs
ENABLE INTERFACE	Pin ENBL				
Logic Level to Enable Power		1.8		V_{POS}	V
Input Current when Enable High			20		µA
Logic Level to Disable Power				0.8	V
Enable Time	Time from ENBL high to V_{APC} within 1% of final value, V_{SET} ≤ 200 mV, refer to Figure 24		4	5	µs
Disable Time	Time from ENBL low to V_{APC} within 1% of final value, V_{SET} ≤ 200 mV, refer to Figure 24		8	9	µs
Power-On/Enable Time	Time from VPOS/ENBL high to V_{APC} within 1% of final value, V_{SET} ≤ 200 mV, refer to Figure 29		2	3	µs
	Time from VPOS/ENBL low to V_{APC} within 1% of final value, V_{SET} ≤ 200 mV, refer to Figure 29		100	200	ns

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER INTERFACE	Pin VPOS				
Supply Voltage		2.7		5.5	V
Quiescent Current	ENBL high		8.5	10.7	mA
Over Temperature	−30°C ≤ T_A ≤ +85°C			12.9	mA
Disable Current[6]	ENBL low		4	10	µA
Over Temperature	−30°C ≤ T_A ≤ +85°C			13	µA

[1] Operation down to 0.02 GHz is possible.
[2] Mean and standard deviation specifications are available in Table 2
[3] See Figure 12 for plot of input impedance vs. frequency.
[4] This parameter is guaranteed but not tested in production. Limit is −3 sigma from the mean.
[5] Response time in a closed-loop system depends on the filter capacitor (C_{FLT}) used and the response of the variable gain element.
[6] This parameter is guaranteed but not tested in production. Maximum specified limit on this parameter is the 6 sigma value.

Table 2. Typical Specifications at Selected Frequencies at 25°C (Mean and Sigma)

	Slope (mV/dB)		Intercept (dBV)		±1 dB Dynamic Range			
					Low Point (dBV)		High Point (dBV)	
Frequency (GHz)	Mean	Sigma	Mean	Sigma	Mean	Sigma	Mean	Sigma
0.1	23.8	0.3	−70.1	1.8	−57.7	1.3	−10.6	0.8
0.9	23.2	0.4	−72.6	1.8	−61.0	1.3	−11.2	0.8
1.9	22.2	0.3	−73.8	1.6	−62.9	0.9	−18.5	1.7
2.5	22.3	0.4	−75.6	1.5	−64.0	1.1	−20.0	1.7

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage VPOS	5.5 V
Temporary Overvoltage VPOS	
(100 cycles, 2 sec duration, ENBL Low)	6.3 V
VAPC, VSET, ENBL	0 V, V_{POS}
RFIN	17 dBm
Equivalent Voltage	1.6 V rms
Internal Power Dissipation	60 mW
θ_{JA} (MSOP)	200°C/W
θ_{JA} (LFCSP, Paddle Soldered)	80°C/W
θ_{JA} (LFCSP, Paddle Not Soldered)	200°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	
MSOP	300°C
LFCSP	240°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

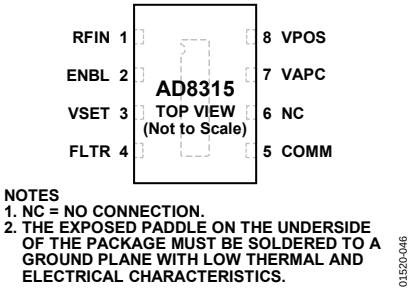


Figure 2. LFCSP Pin Configuration

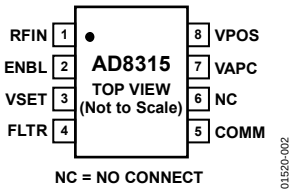


Figure 3. MSOP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RFIN	RF Input.
2	ENBL	Connect to VPOS for Normal Operation Connect Pin to Ground for Disable Mode.
3	VSET	Setpoint Input. Nominal input range 0.25 V to 1.4 V.
4	FLTR	Integrator Capacitor. Connect between FLTR and COMM.
5	COMM	Device Common (Ground).
6	NC	No Connection.
7	VAPC	Output. Control voltage for gain control element.
8	VPOS	Positive Supply Voltage: 2.7 V to 5.5 V.
	EPAD	Exposed Paddle. The exposed paddle, on the underside of the LFCSP package only, must be soldered to a ground plane with low thermal and electrical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

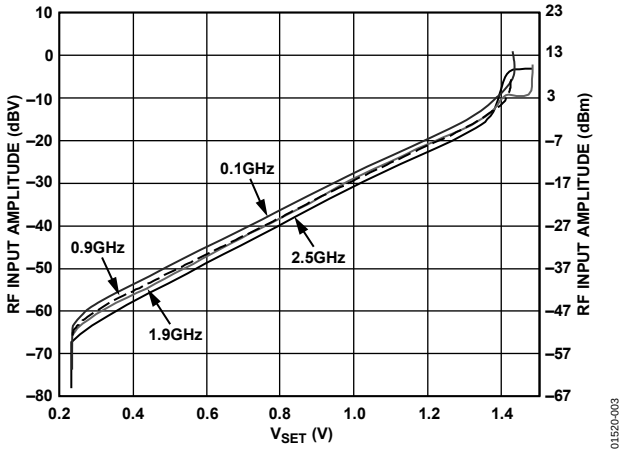


Figure 4. Input Amplitude vs. V_{SET}

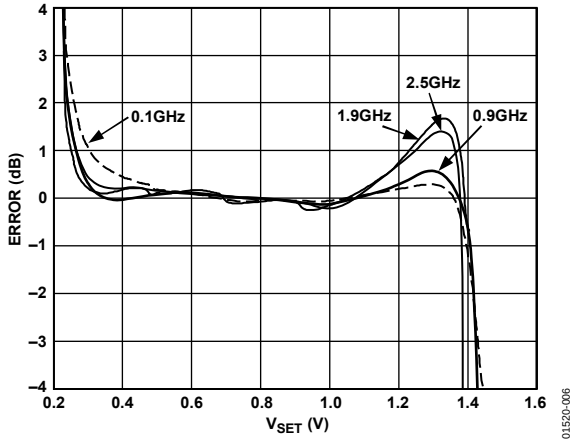


Figure 7. Log Conformance vs. V_{SET}

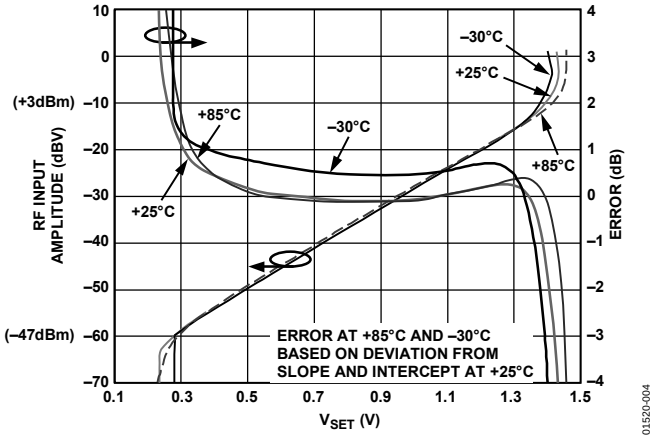


Figure 5. Input Amplitude and Log Conformance vs. V_{SET} at 0.1 GHz

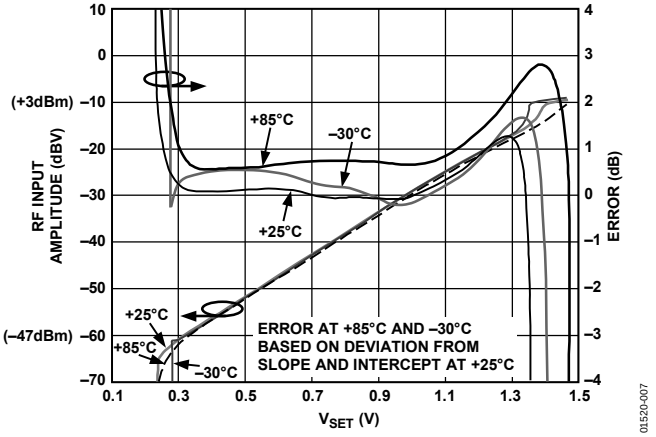


Figure 8. Input Amplitude and Log Conformance vs. V_{SET} at 1.9 GHz

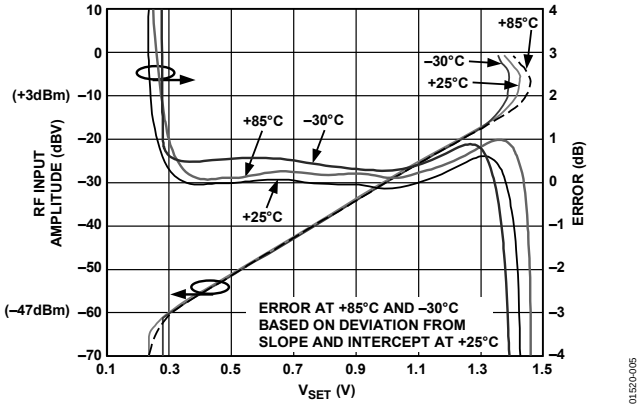


Figure 6. Input Amplitude and Log Conformance vs. V_{SET} at 0.9 GHz

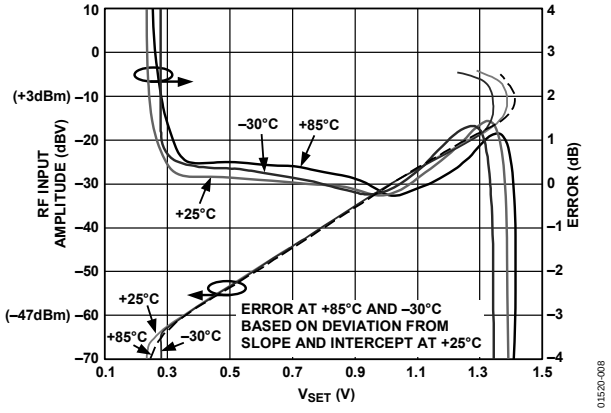


Figure 9. Input Amplitude and Log Conformance vs. V_{SET} at 2.5 GHz

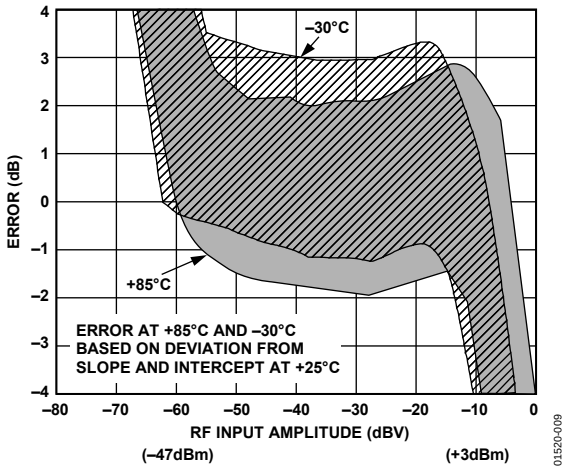


Figure 10. Distribution of Error at Temperature After Ambient Normalization vs. Input Amplitude, 3 Sigma to Either Side of Mean, 0.1 GHz

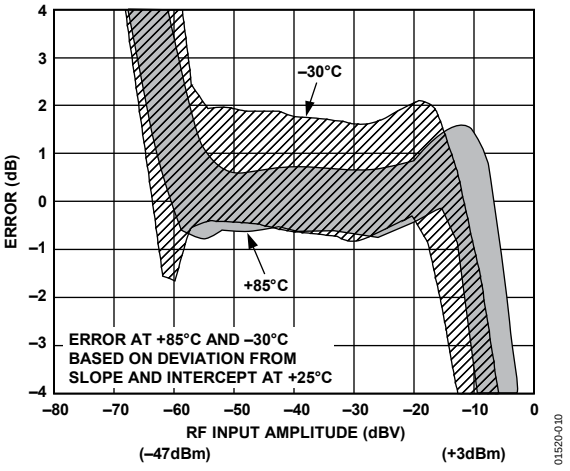


Figure 11. Distribution of Error at Temperature After Ambient Normalization vs. Input Amplitude, 3 Sigma to Either Side of Mean, 0.9 GHz

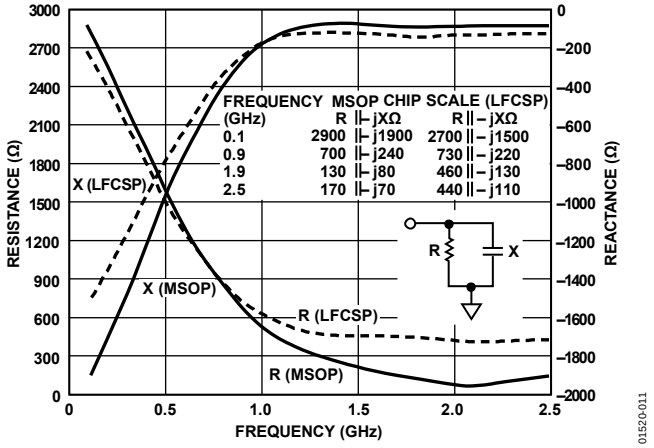


Figure 12. Input Impedance

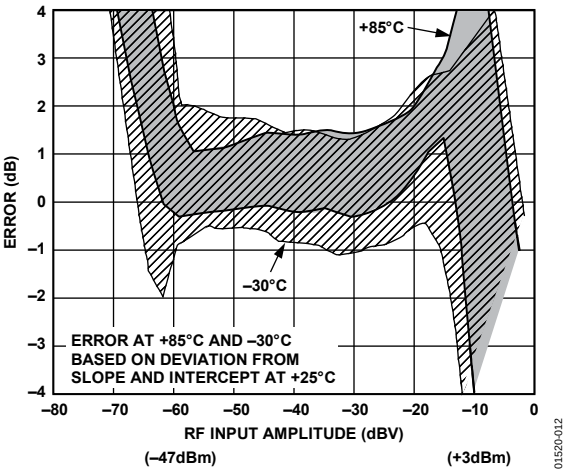


Figure 13. Distribution of Error at Temperature After Ambient Normalization vs. Input Amplitude, 3 Sigma to Either Side of Mean, 1.9 GHz

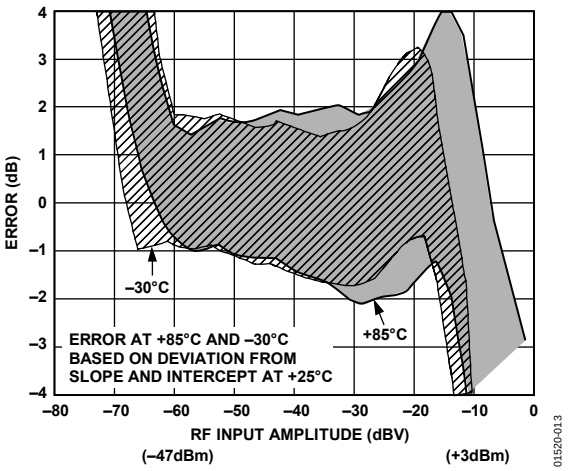


Figure 14. Distribution of Error at Temperature After Ambient Normalization vs. Input Amplitude, 3 Sigma to Either Side of Mean, 2.5 GHz

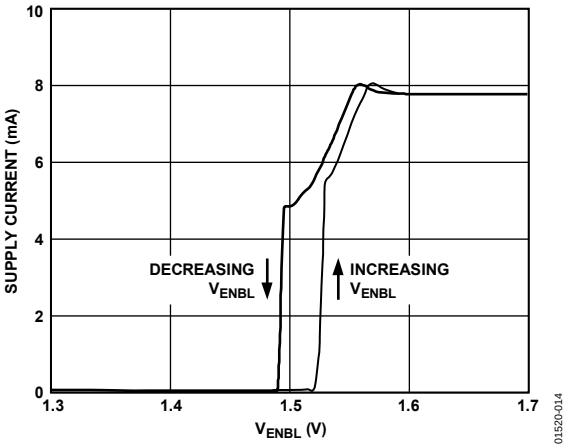


Figure 15. Supply Current vs. V_{ENBL}

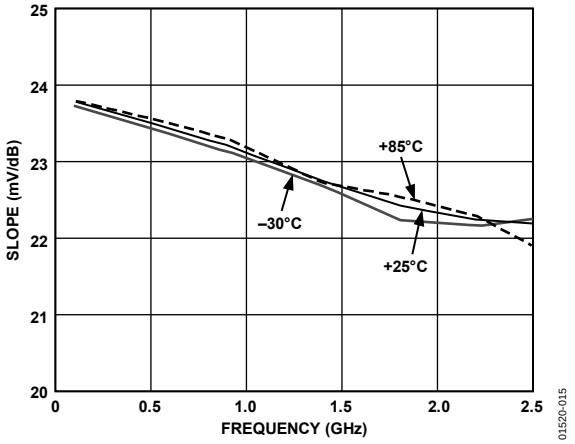


Figure 16. Slope vs. Frequency; −30°C, +25°C, and +85°C

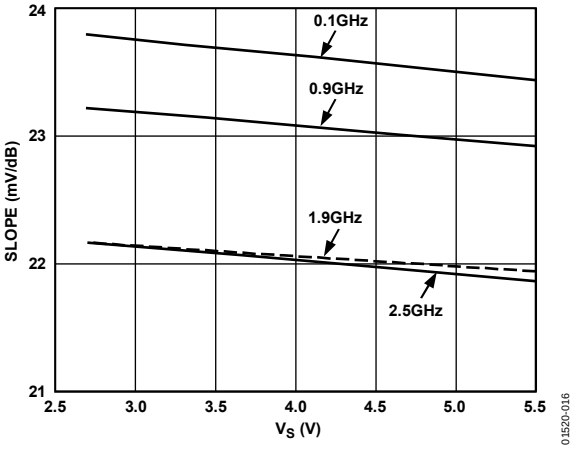


Figure 17. Slope vs. Supply Voltage

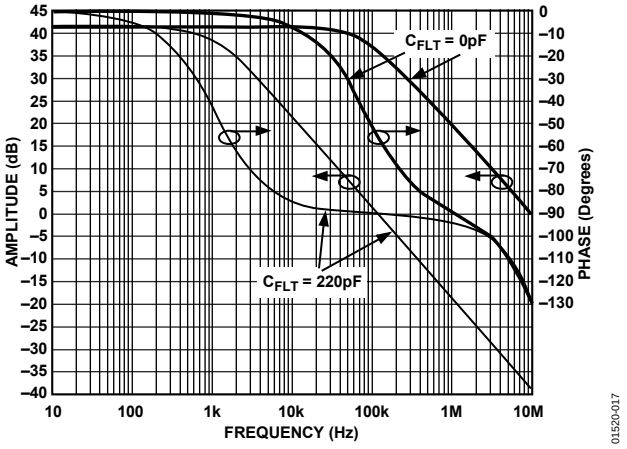


Figure 18. AC Response from VSET to VAPC

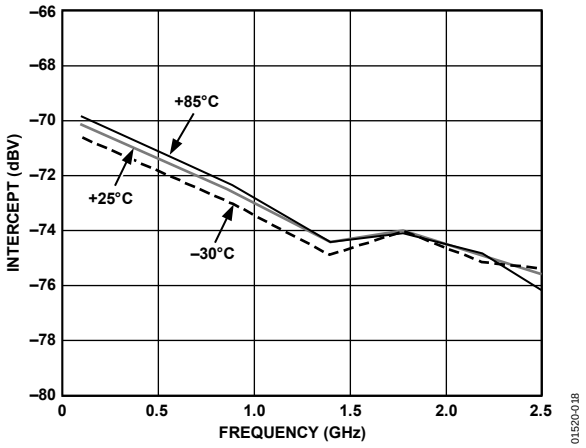


Figure 19. Intercept vs. Frequency; −30°C, +25°C, and +85°C

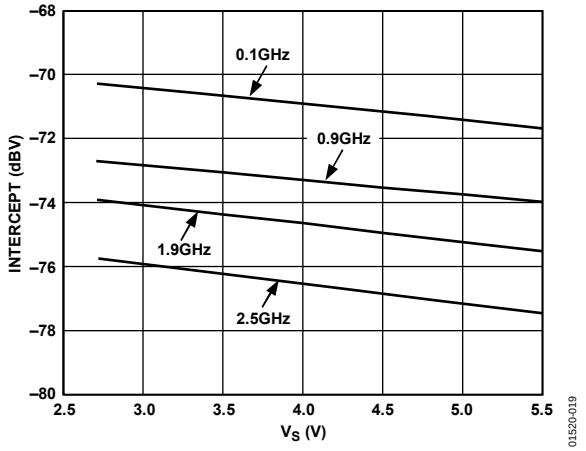


Figure 20. Intercept vs. Supply Voltage

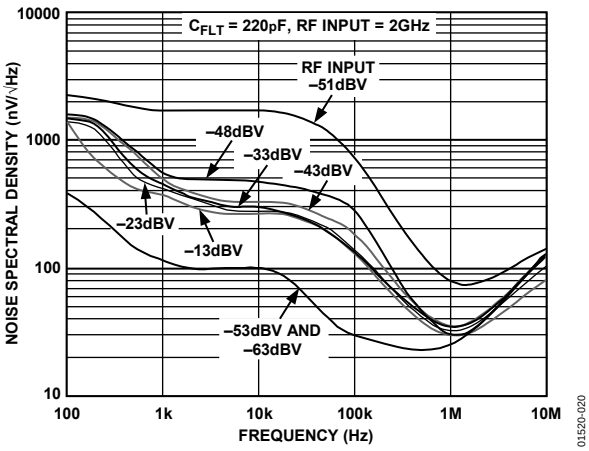


Figure 21. VAPC Noise Spectral Density

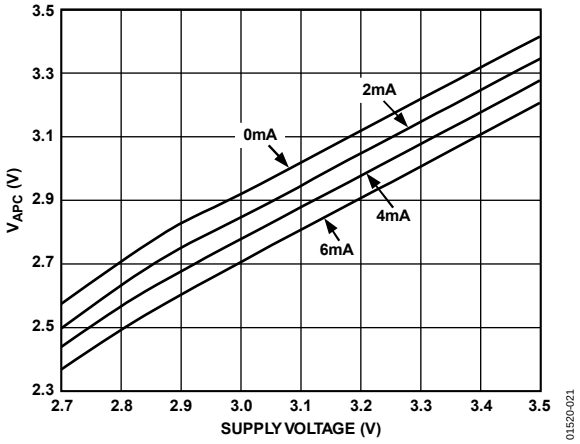


Figure 22. Maximum V_{APC} Voltage vs. Supply Voltage by Load Current

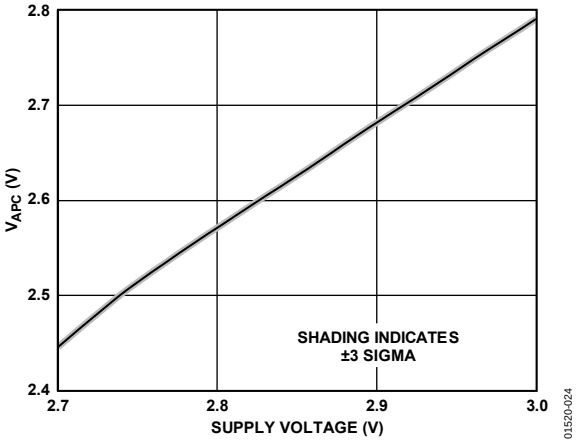


Figure 25. Maximum V_{APC} Voltage vs. Supply Voltage with 4 mA Load Current

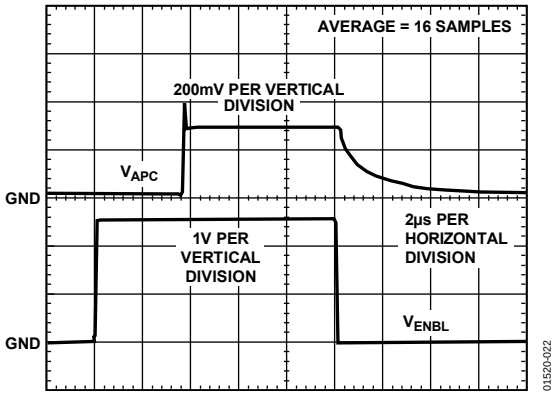


Figure 23. ENBL Response Time

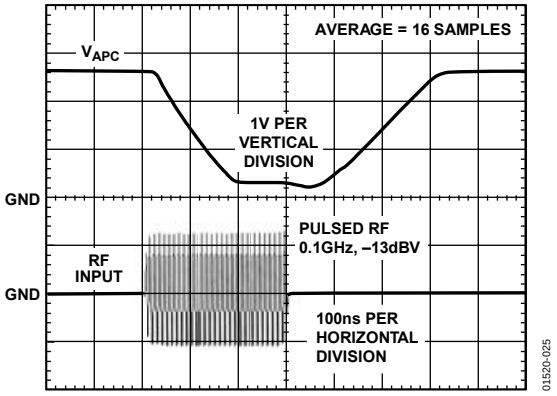


Figure 26. V_{APC} Response Time, Full-Scale Amplitude Change, Open-Loop

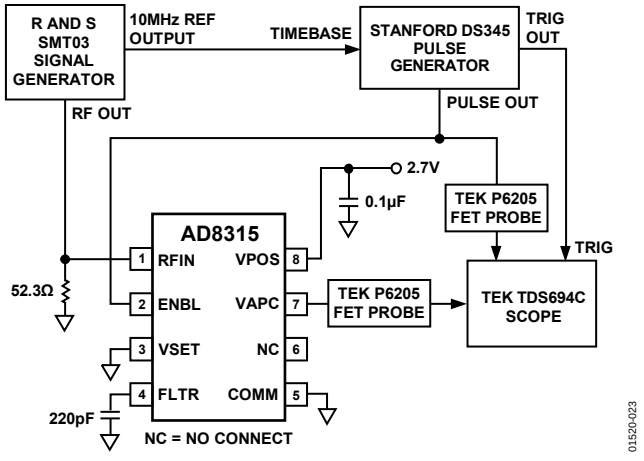


Figure 24. Test Setup for ENBL Response Time

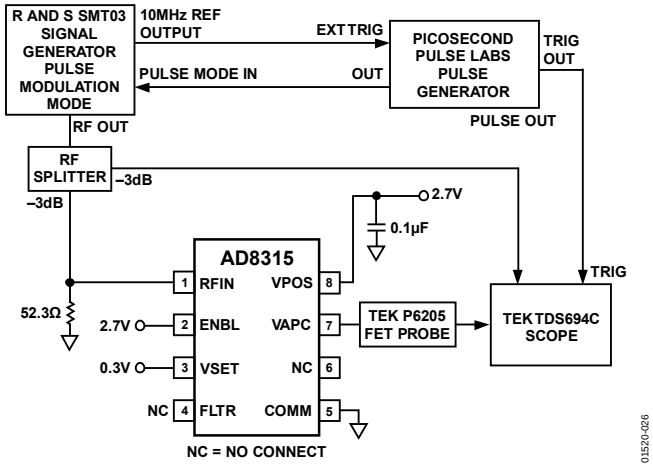


Figure 27. Test Setup for VAPC Response Time

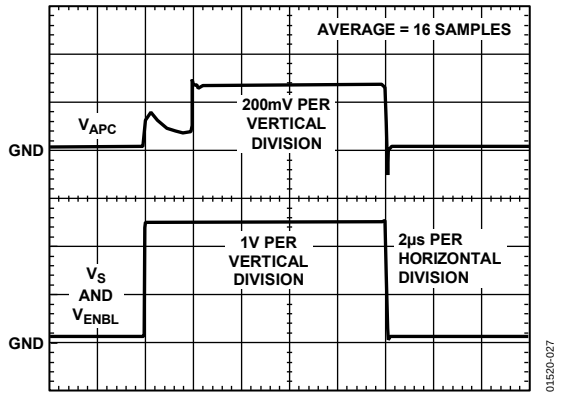


Figure 28. Power-On and Power-Off Response with VSET Grounded

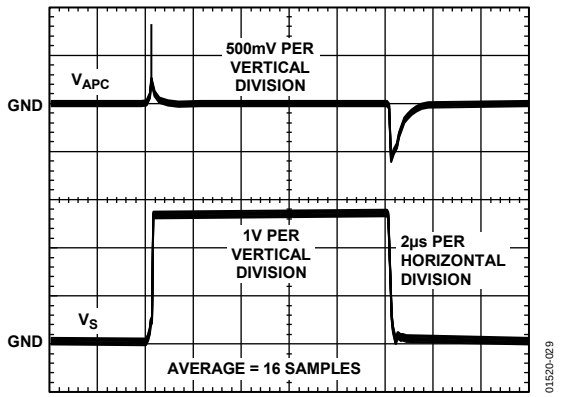


Figure 30. Power-On and Power-Off Response with VSET and ENBL Grounded

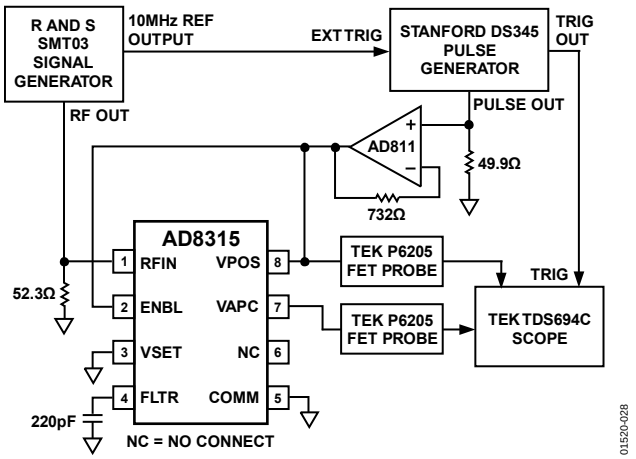


Figure 29. Test Setup for Power-On and Power-Off Response with VSET Grounded

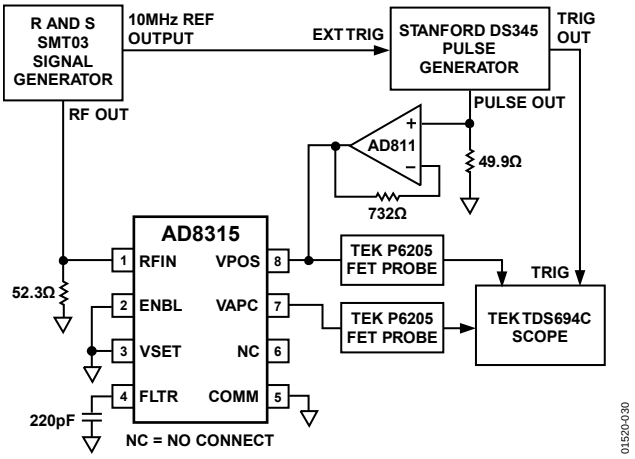


Figure 31. Test Setup for Power-On and Power-Off Response with VSET and ENBL Grounded

THEORY OF OPERATION

The AD8315 is a wideband logarithmic amplifier (log amp) similar in design to the AD8313 and AD8314. However, it is strictly optimized for use in power control applications rather than as a measurement device. Figure 32 shows the main features in block schematic form. The output (Pin 7, VAPC) is intended to be applied directly to the automatic power-control (APC) pin of a power amplifier module.

BASIC THEORY

Logarithmic amplifiers provide a type of compression in which a signal having a large range of amplitudes is converted to one of smaller range. The use of the logarithmic function uniquely results in the output representing the decibel value of the input. The fundamental mathematical form is:

$$V_{OUT} = V_{SLP} \log_{10} \frac{V_{IN}}{V_Z} \quad (1)$$

Here V_{IN} is the input voltage, V_Z is called the intercept (voltage) because when $V_{IN} = V_Z$ the argument of the logarithm is unity and thus the result is zero, and V_{SLP} is called the slope (voltage), which is the amount by which the output changes for a certain change in the ratio (V_{IN}/V_Z). When BASE-10 logarithms are used, denoted by the function $\log_{10}$, V_{SLP} represents the volts/decade, and since a decade corresponds to 20 dB, $V_{SLP}/20$ represents the volts/dB. For the AD8315, a nominal (low frequency) slope of 24 mV/dB was chosen, and the intercept V_Z was placed at the equivalent of −70 dBV for a sine wave input (316 μV rms).

This corresponds to a power level of −57 dBm when the net resistive part of the input impedance of the log amp is 50 Ω. However, both the slope and the intercept are dependent on frequency (see Figure 16 and Figure 19).

Keeping in mind that log amps do not respond to power but only to voltages and that the calibration of the intercept is waveform dependent and is only quoted for a sine wave signal, the equivalent power response can be written as

$$V_{OUT} = V_{DB} (P_{IN} - P_Z) \quad (2)$$

where:

P_{IN}, the input power, and P_Z, the equivalent intercept, are both expressed in dBm (thus, the quantity in parentheses is simply a number of decibels).

V_{DB} is the slope expressed as so many mV/dB.

For a log amp having a slope V_{DB} of 24 mV/dB and an intercept at −57 dBm, the output voltage for an input power of −30 dBm is 0.024 [−30 − (−57)] = 0.648 V.

Further details about the structure and function of log amps can be found in data sheets for other log amps produced by Analog Devices, Inc. Refer to the AD640 data sheet and AD8307 data sheet, both of which include a detailed discussion of the basic principles of operation and explain why the intercept depends on waveform, an important consideration when complex modulation is imposed on an RF carrier.

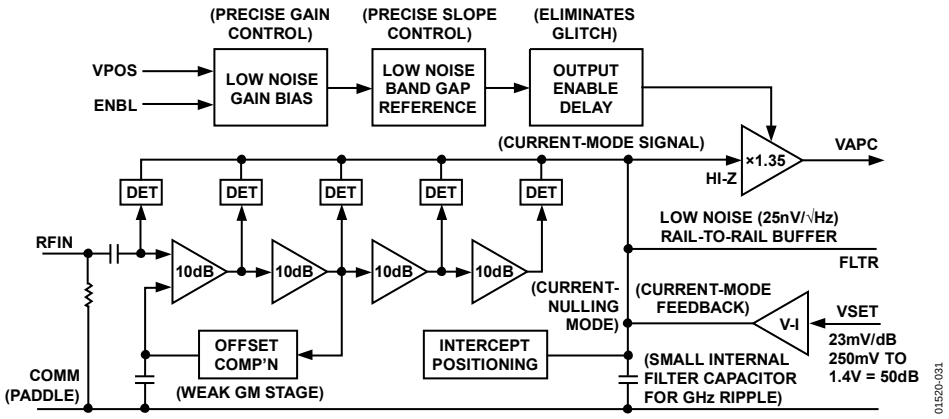


Figure 32. Block Schematic

The intercept need not correspond to a physically realizable part of the signal range for the log amp. Therefore, the specified intercept is −70 dBV, at 0.1 GHz, whereas the smallest input for accurate measurement (a +1 dB error, see Table 2) at this frequency is higher, being about −58 dBV. At 2.5 GHz, the +1 dB error point shifts to −64 dBV. This positioning of the intercept is deliberate and ensures that the V_{SET} voltage is within the capabilities of certain DACs, whose outputs cannot swing below 200 mV. Figure 33 shows the 100 MHz response of the AD8315; the vertical axis does not represent the output (at pin VAPC) but the value required at the power control pin, VSET, to null the control loop.

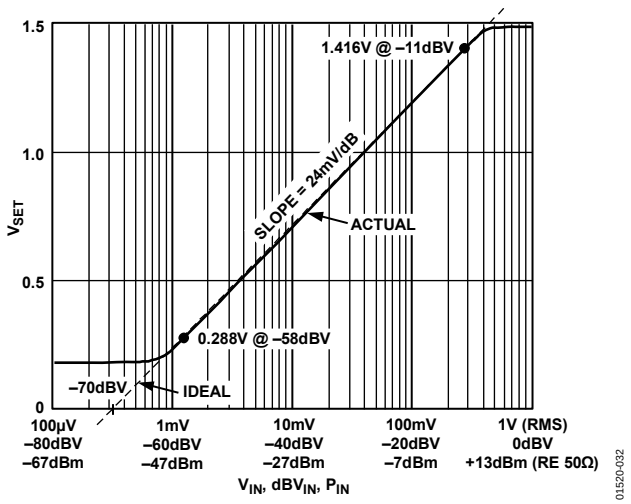


Figure 33. Basic Calibration of the AD8315 at 0.1 GHz

CONTROLLER-MODE LOG AMPS

The AD8315 combines the two key functions required for the measurement and control of the power level over a moderately wide dynamic range. First, it provides the amplification needed to respond to small signals in a chain of four amplifier/limiter cells (see Figure 32), each having a small signal gain of 10 dB and a bandwidth of approximately 3.5 GHz. At the output of each of these amplifier stages is a full-wave rectifier, essentially a square law detector cell that converts the RF signal voltages to a fluctuating current having an average value that increases with signal level. A further passive detector stage is added before the first stage. These five detectors are separated by 10 dB, spanning some 50 dB of dynamic range. Their outputs are each in the form of a differential current, making summation a simple matter. It is readily shown that the summed output can closely approximate a logarithmic function. The overall accuracy at the extremes of this total range, viewed as the deviation from an ideal logarithmic response, that is, the log conformance error, can be judged by referring to Figure 7, which shows that errors across the central 40 dB are moderate. Other performance curves show how conformance to an ideal logarithmic function varies with supply voltage, temperature, and frequency.

In a device intended for measurement applications, this current is converted to an equivalent voltage, to provide the log (V_{IN}) function shown in Equation 1. However, the design of the AD8315 differs from standard practice in that the output must be a low noise control voltage for an RF power amplifier not a direct measure of the input level. Furthermore, it is highly desirable that this voltage be proportional to the time integral of the error between the actual input V_{IN} and the dc voltage V_{SET} (applied to Pin 3, VSET) that defines the setpoint, that is, a target value for the power level, typically generated by a DAC.

This is achieved by converting the difference between the sum of the detector outputs (still in current form) and an internally generated current proportional to V_{SET} to a single-sided, current-mode signal. This, in turn, is converted to a voltage (at Pin 4, FLTR, the low-pass filter capacitor node) to provide a close approximation to an exact integration of the error between the power present in the termination at the input of the AD8315 and the setpoint voltage. Finally, the voltage developed across the ground-referenced filter capacitor C_{FLT} is buffered by a special low noise amplifier of low voltage gain (×1.35) and presented at Pin 7 (VAPC) for use as the control voltage for the RF power amplifier. This buffer can provide rail-to-rail swings and can drive a substantial load current, including large capacitors. Note that the RF power amplifier is assumed to have a positive slope with RF power increasing monotonically with an increasing APC control voltage.

CONTROL LOOP DYNAMICS

To understand how the AD8315 behaves in a complete control loop, an expression for the current in the integration capacitor as a function of the input V_{IN} and the setpoint voltage V_{SET} must be developed (see Figure 34).

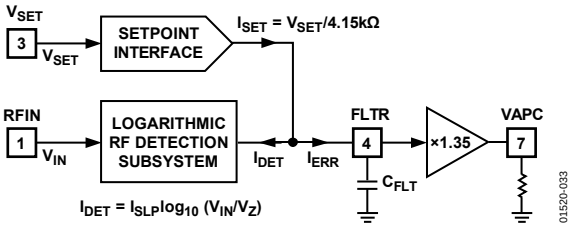


Figure 34. Behavioral Model of the AD8315

First, the summed detector currents are written as a function of the input

$$I_{DET} = I_{SLP} \log_{10} (V_{IN}/V_Z) \quad (3)$$

where:

I_{DET} is the partially filtered demodulated signal, whose exact average value is extracted through the subsequent integration step.

I_{SLP} is the current-mode slope and has a value of 115 µA per decade (that is, 5.75 µA/dB).

V_{IN} is the input in V rms.

V_Z is the effective intercept voltage, which, as previously noted, is dependent on waveform but is 316 µV rms (−70 dBV) for a sine wave input.

Now the current generated by the setpoint interface is simply

$$I_{SET(4)} = V_{SET}/415\ \text{k}\Omega \quad (4)$$

The difference between this current and I_{DET} is applied to the loop filter capacitor C_{FLT}. It follows that the voltage appearing on this capacitor, V_{FLT}, is the time integral of the difference current:

$$V_{FLT}(s) = (I_{SET} - I_{DET})/sC_{FLT} \quad (5)$$

$$= \frac{V_{SET}/4.15\ \text{k}\Omega - I_{SLP}\ \log_{10}\left(V_{IN}/V_Z\right)}{sC_{FLT}} \quad (6)$$

The control output V_{APC} is slightly greater than this, because the gain of the output buffer is ×1.35. In addition, an offset voltage is deliberately introduced in this stage; this is inconsequential because the integration function implicitly allows for an arbitrary constant to be added to the form of Equation 6. The polarity is such that V_{APC} rises to the maximum value for any value of V_{SET} greater than the equivalent value of V_{IN}. In practice, the V_{APC} output rails to the positive supply under this condition unless the control loop through the power amplifier is present. In other words, the AD8315 seeks to drive the RF power to the maximum value whenever it falls below the setpoint. The use of exact integration results in a final error that is theoretically 0, and the logarithmic detection law ideally results in a constant response time following a step change of either the setpoint or the power level, if the power-amplifier control function were likewise linear in dB. However, this latter condition is rarely true, and it follows that in practice, the loop response time depends on the power level, and this effect can strongly influence the design of the control loop.

Equation 6 can be restated as

$$V_{APC}(s) = \frac{V_{SET} - V_{SLP}\ \log_{10}\left(V_{IN}/V_Z\right)}{sT} \quad (7)$$

where V_{SLP} is the volts-per-decade slope from Equation 1, having a value of 480 mV/decade, and T is an effective time constant for the integration, being equal to 4.15 kΩ × C_{FLT}/1.35; the resistor value comes from the setpoint interface scaling Equation 4 and the factor 1.35 arises because of the voltage gain of the buffer. Therefore, the integration time constant can be written as

$$T = 3.07\ C_{FLT}\ \textit{in}\ \mu\text{s},\ \textit{when C is expressed in}\ \text{nF} \quad (8)$$

To simplify our understanding of the control loop dynamics, begin by assuming that the power amplifier gain function is actually linear in dB, and for the moment, use voltages to express the signals at the power amplifier input and output. Let the RF output voltage be V_{PA} and let the input be V_{CW}.

Furthermore, to characterize the gain control function, this form is used

$$V_{PA} = G_O V_{CW} 10^{(V_{APC}/V_{GBC})} \quad (9)$$

where:
G_O is the gain of the power amplifier when V_{APC} = 0.
V_{GBC} is the gain scaling.

While few amplifiers conform so conveniently to this law, it provides a clearer starting point for understanding the more complex situation that arises when the gain control law is less ideal.

This idealized control loop is shown in Figure 35. With some manipulation, it is found that the characteristic equation of this system is

$$V_{APC}(s) = \frac{\left(V_{SET}\ V_{GBC}\right)/V_{SLP} - V_{GBC}\ \log_{10}\left(kG_O\ V_{CW}/V_Z\right)}{1 + sT_O} \quad (10)$$

where:
k is the coupling factor from the output of the power amplifier to the input of the AD8315 (for example, ×0.1 for a 20 dB coupler).
T_O is a modified time constant (V_{GBC}/V_{SLP})T.

This is quite easy to interpret. First, it shows that a system of this sort exhibits a simple single-pole response, for any power level, with the customary exponential time domain form for either increasing or decreasing step polarities in the demand level V_{SET} or the carrier input V_{CW}. Second, it reveals that the final value of the control voltage V_{APC} is determined by several fixed factors:

$$V_{APC}\left(\tau = \infty\right) = \left(V_{SET}\ V_{GBC}\right)/V_{SLP} - \log_{10}\left(kG_O\ V_{CW}/V_Z\right) \quad (11)$$

Example

Assume that the gain magnitude of the power amplifier runs from a minimum value of ×0.316 (−10 dB) at V_{APC} = 0 to ×100 (40 dB) at V_{APC} = 2.5 V. Applying Equation 9, G_O = 0.316 and V_{GBC} = 1 V. Using a coupling factor of k = 0.0316 (that is, a 30 dB directional coupler) and recalling that the nominal value of V_{SLP} is 480 mV and V_Z = 316 µV for the AD8315, first calculate the range of values needed for V_{SET} to control an output range of +33 dBm to −17 dBm. This can be found by noting that, in the steady state, the numerator of Equation 7 must be 0, that is:

$$V_{SET} = V_{SLP} \log_{10}\left(kV_{PA}/V_Z\right) \quad (12)$$

where V_{IN} is expanded to kV_{PA}, the fractional voltage sample of the power amplifier output. For 33 dBm, V_{PA} = 10 V rms, which evaluates to

$$V_{SET}\ (max) = 0.48 \log_{10}(316\ \text{mV}/316\ \mu\text{V}) = 1.44\ \text{V} \quad (13)$$

For a delivered power of −17 dBm, V_{PA} = 31.6 mV rms

$$V_{SET}\ (min) = 0.48 \log_{10}(1\ \text{mV}/316\ \mu\text{V}) = 0.24\ \text{V} \quad (14)$$

Check that the power range is 50 dB, which must correspond to a voltage change in V_{SET} of 50 dB × 24 mV/dB = 1.2 V, which agrees.

Now, the value of V_{APC} is of interest, although it is a dependent parameter, inside the loop. It depends on the characteristics of the power amplifier, and the value of the carrier amplitude V_{CW}. Using the control values previously derived, that is, $G_O = 0.316$ and $V_{GBC} = 1$ V, and assuming the applied power is fixed at −7 dBm (so $V_{CW} = 100$ mV rms), the following is true using Equation 11

$$V_{APC}(max) = (V_{SET}V_{GBC})/V_{SLP} - \log_{10} kG_OV_{CW}/V_Z$$
$$= (1.44 \times 1)/0.48 - \log_{10}(0.0316 \times 0.316 \times 0.1/316\ \mu V)$$
$$= 3.0 - 0.5 = 2.5\ V \quad (15)$$

$$V_{APC}(min) = (V_{SET}V_{GBC})/V_{SLP} - \log_{10} kG_OV_{CW}/V_Z$$
$$= (0.24 \times 1)/0.48 - \log_{10}(0.0316 \times 0.316 \times 0.1/316\ \mu V)$$
$$= 0.5 - 0.5 = 0 \quad (16)$$

both of which results are consistent with the assumptions made about the amplifier control function. Note that the second term is independent of the delivered power and a fixed function of the drive power.

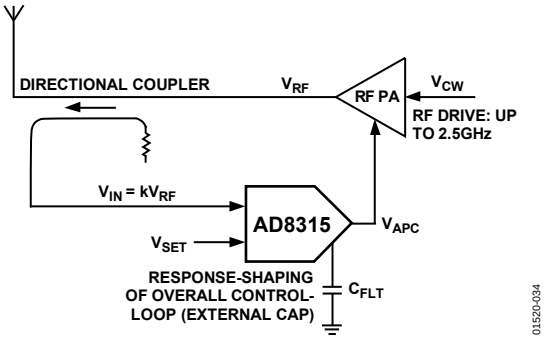


Figure 35. Idealized Control Loop for Analysis

Finally, using the loop time constant for these parameters and an illustrative value of 2 nF for the filter capacitor C_{FLT}

$$T_O = (V_{GBC}/V_{SLP})\ T$$
$$= (1/0.48)3.07\ \mu s \times 2\ (nF) = 12.8\ \mu s \quad (17)$$

PRACTICAL LOOP

At present time, power amplifiers, or VGAs preceding such amplifiers, do not provide an exponential gain characteristic. It follows that the loop dynamics (the effective time constant) varies with the setpoint because the exponential function is unique in providing constant dynamics. The procedure must therefore be as follows. Beginning with the curve usually provided for the power output vs. the APC voltage, draw a tangent at the point on this curve where the slope is highest (see Figure 36). Using this line, calculate the effective minimum value of the variable V_{GBC} and use it in Equation 17 to determine the time constant. Note that the minimum in V_{GBC} corresponds to the maximum rate of change in the output power vs. V_{APC}.

For example, suppose it is found that, for a given drive power, the amplifier generates an output power of P_1 at $V_{APC} = V_1$ and P_2 at $V_{APC} = V_2$.

Then, it is readily shown that

$$V_{GBC} = 20\ (V_2 - V_1)/(P_2 - P_1) \quad (18)$$

This must be used to calculate the filter capacitance. The response time at high and low power levels (on the shoulders of the curve shown in Figure 36) is slower. Note also that it is sometimes useful to add a 0 in the closed-loop response by placing a resistor in series with C_{FLT}. For more information on this, see the Transient Response section.

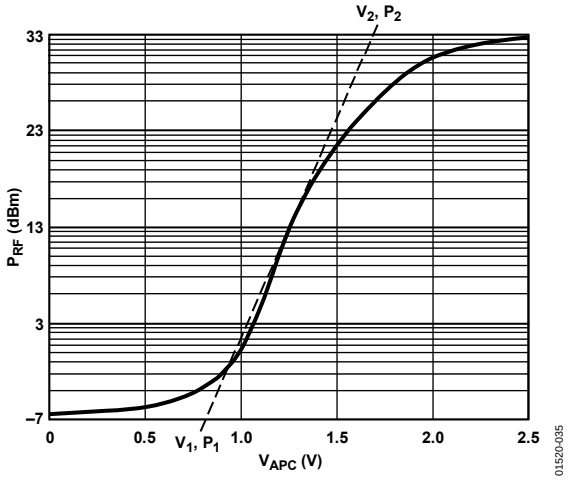


Figure 36. Typical Power-Control Curve

A NOTE ABOUT POWER EQUIVALENCY

In using the AD8315, it must be understood that log amps do not fundamentally respond to power. It is for this reason that dBV (decibels above 1 V rms) are used rather than the commonly used metric of dBm. The dBV scaling is fixed, independent of termination impedance, while the corresponding power level is not. For example, 224 mV rms is always −13 dBV (with one further condition of an assumed sinusoidal waveform; see the AD640 data sheet for more information about the effect of waveform on logarithmic intercept), and this corresponds to a power of 0 dBm when the net impedance at the input is 50 Ω. When this impedance is altered to 200 Ω, however, the same voltage corresponds to a power level that is four times smaller ($P = V^2/R$) or −6 dBm. A dBV level can be converted to dBm in the special case of a 50 Ω system and a sinusoidal signal by simply adding 13 dB (0 dBV is then, and only then, equivalent to 13 dBm).

Therefore, the external termination added ahead of the AD8315 determines the effective power scaling. This often takes the form of a simple resistor (52.3 Ω provides a net 50 Ω input), but more elaborate matching networks can be used. The choice of impedance determines the logarithmic intercept, that is, the input power for which the V_{SET} vs. P_{IN} function crosses the baseline if that relationship were continuous for all values of V_{IN}.

This is never the case for a practical log amp; the intercept (so many dBV) refers to the value obtained by the minimum error straight line fit to the actual graph of V_{SET} vs. P_{IN} (more generally, V_{IN}).

Where the modulation is complex, as in CDMA, the calibration of the power response must be adjusted; the intercept remains stable for any given arbitrary waveform. When a true power (waveform independent) response is needed, a mean-responding detector, such as the AD8361, must be considered.

The logarithmic slope, V_{SLP} in Equation 1, which is the amount by which the setpoint voltage must be changed for each decibel of input change (voltage or power), is, in principle, independent of waveform or termination impedance. In practice, it usually falls off somewhat at higher frequencies, due to the declining gain of the amplifier stages and other effects in the detector cells (see Figure 16).

BASIC CONNECTIONS

Figure 37 shows the basic connections for operating the AD8315, and Figure 38 shows a block diagram of a typical application. The AD8315 is typically used in the RF power control loop of a mobile handset.

A supply voltage of 2.7 V to 5.5 V is required for the AD8315. The supply to the VPOS pin must be decoupled with a low inductance 0.1 µF surface-mount ceramic capacitor, close to the device. The AD8315 has an internal input coupling capacitor. This negates the need for external ac coupling. This capacitor, along with the low frequency input impedance of the device of approximately 2.8 kΩ, sets the minimum usable input frequency to around 0.016 GHz. A broadband 50 Ω input match is achieved in this example by connecting a 52.3 Ω resistor between RFIN and ground. A plot of input impedance vs. frequency is shown in Figure 12. Other coupling methods are also possible (see Input Coupling Options section).

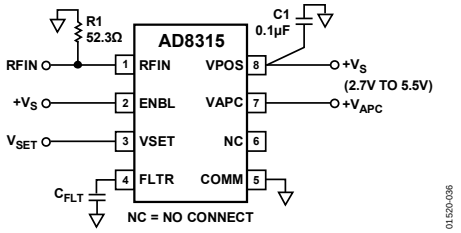


Figure 37. Basic Connections

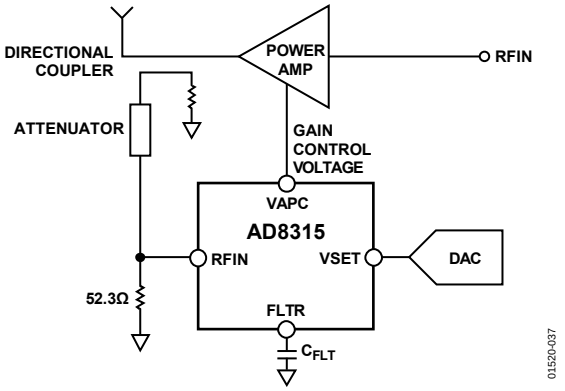


Figure 38. Typical Application

In a power control loop, the AD8315 provides both the detector and controller functions. A sample of the power amplifier (PA) output power is coupled to the RF input of the AD8315, usually via a directional coupler. In dual-mode applications, where there are two PAs and two directional couplers, the outputs of the directional couplers can be passively combined (both PAs will never be turned on simultaneously) before being applied to the AD8315.

A setpoint voltage is applied to VSET from the controlling source (generally, this is a DAC). Any imbalance between the RF input level and the level corresponding to the setpoint voltage is corrected by the AD8315 VAPC output that drives the gain control terminal of the PA. This restores a balance between the actual power level sensed at the input of the AD8315 and the value determined by the setpoint. This assumes that the gain control sense of the variable gain element is positive, that is, an increasing voltage from VAPC tends to increase gain.

V_{APC} can swing from 250 mV to within 100 mV of the supply rail and can source up to 6 mA. If the control input of the PA must source current, a suitable load resistor can be connected between VAPC and COMM. The output swing and current sourcing capability of VAPC is shown in Figure 22.

RANGE ON VSET AND RFIN

The relationship between the RF input level and the setpoint voltage follows from the nominal transfer function of the device (see Figure 5, Figure 6, Figure 8, and Figure 9). At 0.9 GHz, for example, a voltage of 1 V on VSET indicates a demand for −30 dBV (−17 dBm, re 50 Ω) at RFIN. The corresponding power level at the output of the power amplifier is greater than this amount due to the attenuation through the directional coupler.

For setpoint voltages of less than approximately 250 mV, V_{APC} remains unconditionally at the minimum level of approximately 250 mV. This feature can prevent any spurious emissions during power-up and power-down phases.

Above 250 mV, V_{SET} has a linear control range up to 1.4 V, corresponding to a dynamic range of 50 dB. This results in a slope of 23 mV/dB or approximately 43.5 dB/V.

TRANSIENT RESPONSE

The time domain response of power amplifier control loops, using any kind of controller, is only partially determined by the choice of filter, which, in the case of the AD8315, has a true integrator form 1/sT, as shown in Equation 7, with a time constant given by Equation 8. The large signal step response is also strongly dependent on the form of the gain-control law. Nevertheless, some simple rules can be applied. When the filter capacitor C_{FLT} is very large, it dominates the time domain response, but the incremental bandwidth of this loop still varies as V_{APC} traverses the nonlinear gain-control function of the PA, as shown in Figure 36.

This bandwidth is highest at the point where the slope of the tangent drawn on this curve is greatest, that is, for power outputs near the center of the PA range, and is much reduced at both the minimum and the maximum power levels, where the slope of the gain control curve is lowest due to the S-shaped form.

Using smaller values of C_{FLT}, the loop bandwidth generally increases in inverse proportion to the value. Eventually, however, a secondary effect appears due to the inherent phase lag in the power amplifier control path, some of which can be due to parasitic or deliberately added capacitance at the VAPC pin. This results in the characteristic poles in the ac loop equation moving off the real axis and thus becoming complex (and somewhat resonant). This is a classic aspect of control loop design. The lowest permissible value of C_{FLT} must be determined experimentally for a particular amplifier. For GSM and DCS power amplifiers, C_{FLT} typically ranges from 150 pF to 300 pF.

In many cases, some improvement in the worst-case response time can be achieved by including a small resistance in series with C_{FLT}; this generates an additional 0 in the closed-loop transfer function, that serves to cancel some of the higher order poles in the overall loop. A combination of main capacitor C_{FLT} shunted by a second capacitor and resistor in series is also useful in minimizing the settling time of the loop.

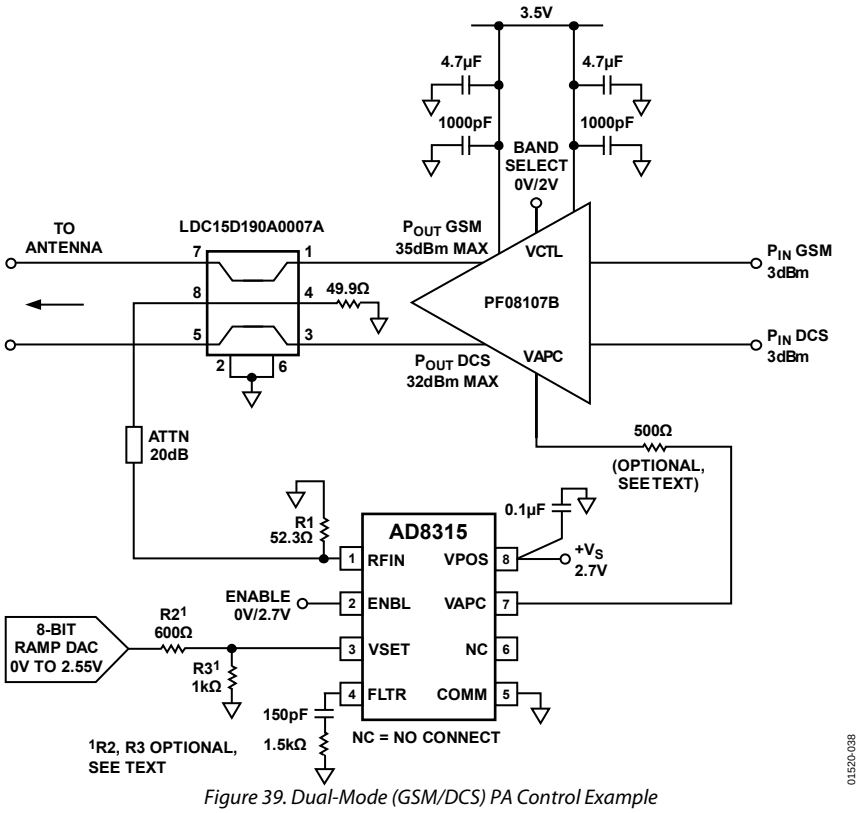


Figure 39. Dual-Mode (GSM/DCS) PA Control Example

MOBILE HANDSET POWER CONTROL EXAMPLE

Figure 39 shows a complete power amplifier control circuit for a dual-mode handset. The PF08107B (Hitachi), a dual mode (GSM, DCS) PA, is driven by a nominal power level of 3 dBm. The PA has a single gain control line; the band to be used is selected by applying either 0 V or 2 V to the PA VCTL input.

Some of the output power from the PA is coupled off using a dual-band directional coupler (Murata LDC15D190A0007A). This has a coupling factor of approximately 19 dB for the GSM band and 14 dB for DCS and an insertion loss of 0.38 dB and 0.45 dB, respectively. Because the PF08107B transmits a maximum power level of 35 dBm for GSM and 32 dBm for DCS, additional attenuation of 20 dB is required before the coupled signal is applied to the AD8315. This results in peak input levels to the AD8315 of −4 dBm (GSM) and −2 dBm (DCS). While the AD8315 gives a linear response for input levels up to 2 dBm, for highly temperature-stable performance at maximum PA output power, the maximum input level must be limited to approximately −2 dBm (see Figure 6 and Figure 8). This does, however, reduce the sensitivity of the circuit at the low end.

The operational setpoint voltage, in the range 250 mV to 1.4 V, is applied to the VSET pin of the AD8315. This is typically supplied by a DAC. The AD8315 VAPC output drives the level control pin of the power amplifier directly. V_{APC} reaches a maximum value of approximately 2.5 V on a 2.7 V supply while delivering the 3 mA required by the level control input of the PA. This is more than sufficient to exercise the gain control range of the PA.

During initialization and completion of the transmit sequence, V_{APC} must be held at the minimum level of 250 mV by keeping V_{SET} below 200 mV.

In this example, V_{SET} is supplied by an 8-bit DAC that has an output range from 0 V to 2.55 V or 10 mV per bit. This sets the control resolution of VSET to 0.4 dB/bit (0.04 dB/mV times 10 mV). If finer resolution is required, the DAC output voltage can be scaled using two resistors, as shown in Figure 39. This converts the DAC maximum voltage of 2.55 V down to 1.6 V and increases the control resolution to 0.25 dB/bit.

A filter capacitor (C_{FLT}) must stabilize the loop. The choice of CFLT depends to a large degree on the gain control dynamics of the power amplifier, something that is frequently poorly characterized, so some trial and error can be necessary.

In this example, a 150 pF capacitor is used and a 1.5 kΩ series resistor is included. This adds a zero to the control loop and increases the phase margin, which helps to make the step response of the circuit more stable when the PA output power is low and the slope of the PA power control function is the steepest.

A smaller filter capacitor can be used by inserting a series resistor between VAPC and the control input of the PA. A series resistor works with the input impedance of the PA to create a resistor divider and reduces the loop gain. The size of the resistor divider ratio depends upon the available output swing of V_{APC} and the required control voltage on the PA.

This technique can also be used to limit the control voltage in situations where the PA cannot deliver the power level being demanded by VAPC. Overdrive of the control input of some PAs causes increased distortion. It must be noted, however, that if the control loop opens (that is, V_{APC} goes to the maximum value in an effort to balance the loop), the quiescent current of the AD8315 increases somewhat, particularly at supply voltages greater than 3 V.

Figure 40 shows the relationship between V_{SET} and output power (P_{OUT}) at 0.9 GHz . The overall gain control function is linear in dB for a dynamic range of over 40 dB. Note that for V_{SET} voltages below 300 mV, the output power drops off steeply as V_{APC} drops toward the minimum level of 250 mV.

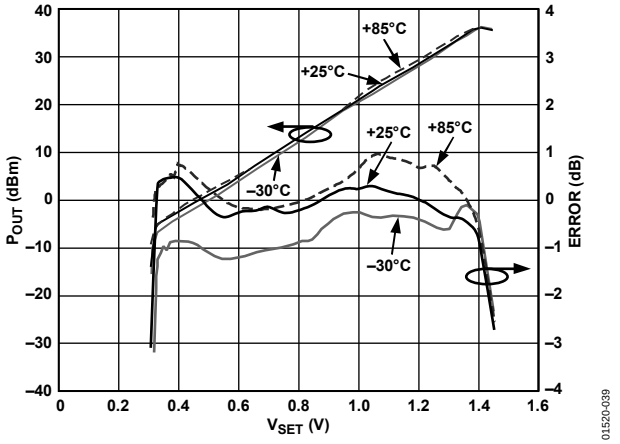


Figure 40. P_{OUT} vs. V_{SET} at 0.9 GHz for Dual-Mode Handset Power Amplifier Application, −30°C, +25°C, and +85°C

ENABLE AND POWER-ON

The AD8315 can be disabled by pulling the ENBL pin to ground. This reduces the supply current from the nominal level of 7.4 mA to 4 μA. The logic threshold for turning on the device is at 1.5 V with 2.7 V supply voltage. A plot of the enable glitch is shown in Figure 23. Alternatively, the device can be completely disabled by pulling the supply voltage to ground. To minimize glitch in this mode, ENBL and VPOS must be tied together. If VPOS is applied before the device is enabled, a narrow 750 mV glitch results (see Figure 30).

In both situations, the voltage on VSET must be kept below 200 mV during power-on and power-off to prevent any unwanted transients on VAPC.

INPUT COUPLING OPTIONS

The internal 5 pF coupling capacitor of the AD8315, along with the low frequency input impedance of 2.8 kΩ, give a high-pass input corner frequency of approximately 16 MHz. This sets the minimum operating frequency. Figure 41, Figure 42, and Figure 43 show three options for input coupling. A broadband resistive match can be implemented by connecting a shunt resistor to ground at RFIN (see Figure 41). This 52.3 Ω resistor (other values can also be used to select different overall input impedances) combines with the input impedance of the AD8315 to give a broadband input impedance of 50 Ω. While the input resistance and capacitance (C_{IN} and R_{IN}) of the AD8315 varies from device to device by approximately ±20%, and over frequency (see Figure 12), the dominance of the external shunt resistor means that the variation in the overall input impedance is close to the tolerance of the external resistor. This method of matching is most useful in wideband applications or in multiband systems where there is more than one operating frequency.

A reactive match can also be implemented as shown in Figure 42. This is not recommended at low frequencies as device tolerances dramatically vary the quality of the match because of the large input resistance. For low frequencies, Figure 41 or Figure 43 is recommended.

In Figure 42, the matching components are drawn as generic reactances. Depending on the frequency, the input impedance and the availability of standard value components, either a capacitor or an inductor is used. As in the previous case, the input impedance at a particular frequency is plotted on a Smith Chart and matching components are chosen (shunt or series L, shunt or series C) to move the impedance to the center of the chart.

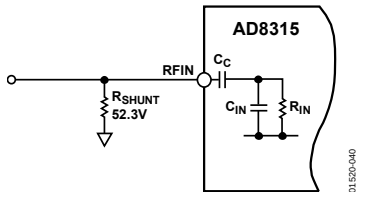


Figure 41. Broadband Resistive Input Coupling Option

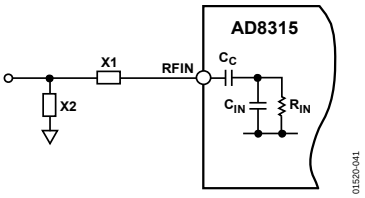


Figure 42. Narrow-Band Reactive Input Coupling Option

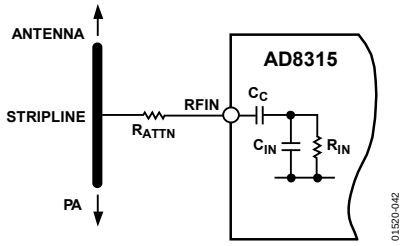


Figure 43. Series Attention Input Coupling Option

Figure 43 shows a third method for coupling the input signal into the AD8315. A series resistor, connected to the RF source, combines with the input impedance of the AD8315 to resistively divide the input signal being applied to the input. This has the advantage of very little power being tapped off in RF power transmission applications.

USING THE CHIP SCALE PACKAGE

On the underside of the chip scale package, there is an exposed paddle. This paddle is internally connected to the chip ground. There is no thermal requirement to solder the paddle down to the printed circuit board ground plane. However, soldering down the paddle has been shown to increase the stability over frequency of the AD8315 ACP response at low input power levels (that is, at around −45 dBm) in the DCS and PCS bands.

EVALUATION BOARD

Figure 44 shows the schematic of the AD8315 MSOP evaluation board. The layout and silkscreen of the component side are shown in Figure 45 and Figure 46. An evaluation board is also available for the LFCSP package (see the Ordering Guide for exact device numbers). Apart from the slightly smaller device footprint, the LFCSP evaluation board is identical to the MSOP board. The board is powered by a single supply in the 2.7 V to 5.5 V range. The power supply is decoupled by a single 0.1 µF capacitor.

Table 5 details the various configuration options of the evaluation board.

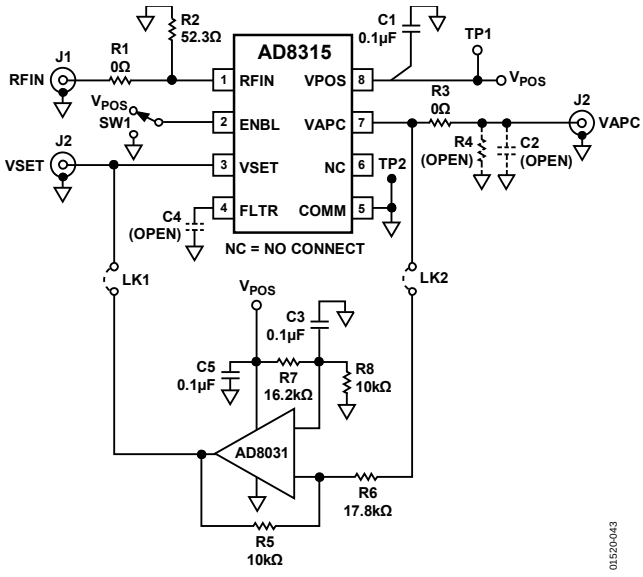


Figure 44. Evaluation Board Schematic (MSOP)

Table 5. Evaluation Board Configuration Options

Component	Function	Default Condition
TP1, TP2	Supply and Ground Vector Pins.	Not Applicable
SW1	Device Enable. When in Position A, the ENBL pin is connected to VPOS and the AD8315 is in operating mode. In Position B, the ENBL pin is grounded putting the device in power-down mode.	SW1 = A
R1, R2	Input Interface. The 52.3 Ω resistor in Position R2 combines with the AD8315 internal input impedance to give a broadband input impedance of around 50 Ω. A reactive match can be implemented by replacing R2 with an inductor and R1 (0 Ω) with a capacitor. Note that the AD8315 RF input is internally ac-coupled.	R2 = 52.3 Ω (Size 0603) R1 = 0 Ω (Size 0402)
R3, R4, C2	Output Interface. R4 and C2 can be used to check the response of VAPC to capacitive and resistive loading. R3/R4 can be used to reduce the slope of VAPC.	R4 = C2 = Open (Size 0603) R3 = 0 Ω (Size 0603)
C1	Power Supply Decoupling. The nominal supply decoupling consists of a 0.1 µF capacitor.	C1 = 0.1 µF (Size 0603)
C4	Filter Capacitor. The response time of VAPC can be modified by placing a capacitor between FLTR (Pin 4) and ground.	C4 = Open (Size 0603)
LK1, LK2	Measurement Mode. A quasimeasurement mode can be implemented by installing LK1 and LK2 (connecting an inverted VAPC to VSET) to yield the nominal relationship between RFIN and VSET. In this mode, a large capacitor (0.01 µF or greater) must be installed in C4.	LK1, LK2 = Installed

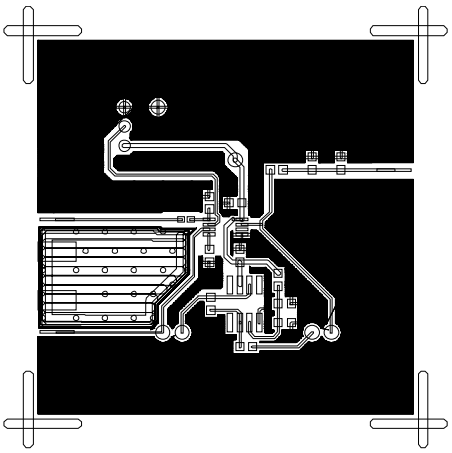


Figure 45. Layout of Component Side (MSOP)

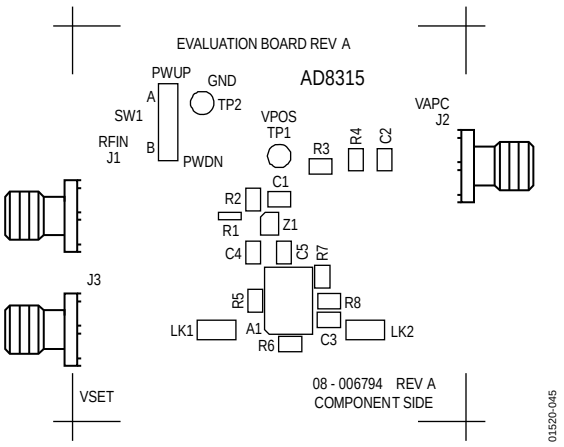


Figure 46. Silkscreen of Component Side (MSOP)

For operation in controller mode, both jumpers, LK1 and LK2, must be removed. The setpoint voltage is applied to VSET, RFIN is connected to the RF source (PA output or directional coupler), and VAPC is connected to the gain control pin of the PA. When used in controller mode, a capacitor must be installed in C4 for loop stability. For GSM/DCS handset power amplifiers, this capacitor must typically range from 150 pF to 300 pF.

A quasimeasurement mode (where the AD8315 delivers an output voltage that is proportional to the log of the input signal) can be implemented, to establish the relationship between VSET and RFIN, by installing the two jumpers, LK1 and LK2. This mimics an AGC loop. To establish the transfer function of the log amp, the RF input must be swept while the voltage on VSET is measured, that is, the SMA connector labeled VSET now acts as an output. This is the simplest method to validate operation of the evaluation board. When operated in this mode, a large capacitor (0.01 µF or greater) must be installed in C4 (filter capacitor) to ensure loop stability.

OUTLINE DIMENSIONS

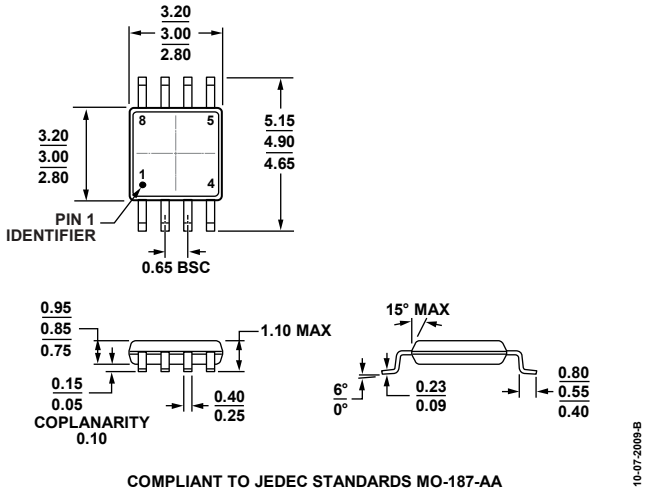


Figure 47. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

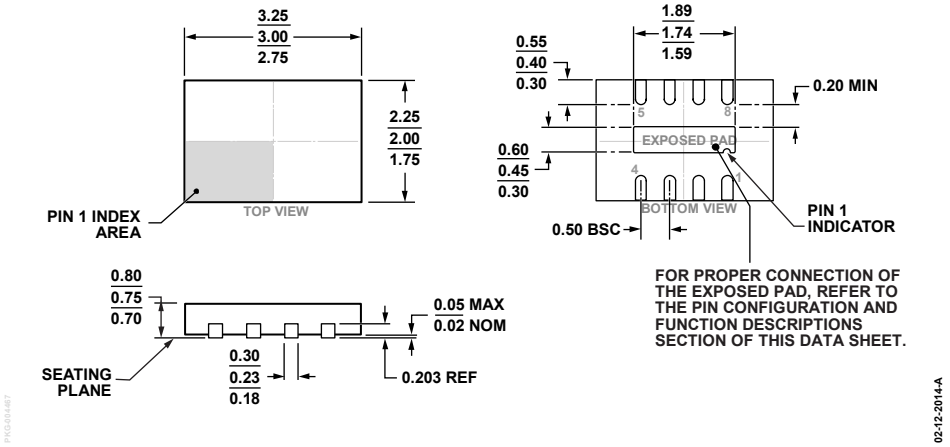


Figure 48. 8-Lead Lead Frame Chip Scale Package [LFCSP]
2 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-23)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
AD8315ARMZ	−30°C to +85°C	8-Lead MSOP, Tube	RM-8	50	Q0S
AD8315ARMZ-RL	−30°C to +85°C	8-Lead MSOP, 13" Tape and Reel	RM-8	3,000	Q0S
AD8315ACPZ-REEL7	−30°C to +85°C	8-Lead LFCSP, 7" Tape and Reel	CP-8-23	3,000	0J
AD8315ACP-EVALZ		LFCSP Evaluation Board			

[1] Z = RoHS Compliant Part.

NOTES

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