LF–2.7 GHz RF/IF Gain and Phase Detector

AD8302

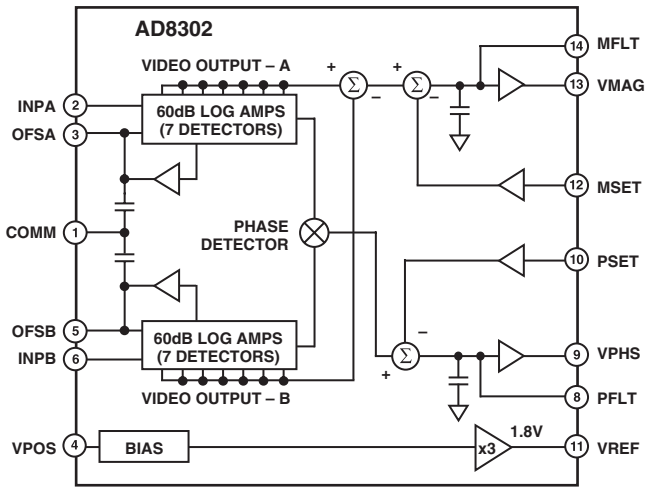
FEATURES

- Measures Gain/Loss and Phase up to 2.7 GHz
- Dual Demodulating Log Amps and Phase Detector
- Input Range –60 dBm to 0 dBm in a 50 Ω System
- Accurate Gain Measurement Scaling (30 mV/dB)
  - Typical Nonlinearity < 0.5 dB
- Accurate Phase Measurement Scaling (10 mV/Degree)
  - Typical Nonlinearity < 1 Degree
- Measurement/Controller/Level Comparator Modes
- Operates from Supply Voltages of 2.7 V–5.5 V
- Stable 1.8 V Reference Voltage Output
- Small Signal Envelope Bandwidth from DC to 30 MHz

APPLICATIONS

- RF/IF PA Linearization
- Precise RF Power Control
- Remote System Monitoring and Diagnostics
- Return Loss/VSWR Measurements
- Log Ratio Function for AC Signals

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD8302 is a fully integrated system for measuring gain/loss and phase in numerous receive, transmit, and instrumentation applications. It requires few external components and a single supply of 2.7 V–5.5 V. The ac-coupled input signals can range from –60 dBm to 0 dBm in a 50 Ω system, from low frequencies up to 2.7 GHz. The outputs provide an accurate measurement of either gain or loss over a ±30 dB range scaled to 30 mV/dB, and of phase over a 0°–180° range scaled to 10 mV/degree. Both subsystems have an output bandwidth of 30 MHz, which may optionally be reduced by the addition of external filter capacitors. The AD8302 can be used in controller mode to force the gain and phase of a signal chain toward predetermined setpoints.

The AD8302 comprises a closely matched pair of demodulating logarithmic amplifiers, each having a 60 dB measurement range. By taking the difference of their outputs, a measurement of the magnitude ratio or gain between the two input signals is available. These signals may even be at different frequencies, allowing the measurement of conversion gain or loss. The AD8302 may be used to determine absolute signal level by applying the unknown signal to one input and a calibrated ac reference signal to the other. With the output stage feedback connection disabled, a comparator may be realized, using the setpoint pins MSET and PSET to program the thresholds.

The signal inputs are single-ended, allowing them to be matched and connected directly to a directional coupler. Their input impedance is nominally 3 kΩ at low frequencies.

The AD8302 includes a phase detector of the multiplier type, but with precise phase balance driven by the fully limited signals appearing at the outputs of the two logarithmic amplifiers. Thus, the phase accuracy measurement is independent of signal level over a wide range.

The phase and gain output voltages are simultaneously available at loadable ground referenced outputs over the standard output range of 0 V to 1.8 V. The output drivers can source or sink up to 8 mA. A loadable, stable reference voltage of 1.8 V is available for precise repositioning of the output range by the user.

In controller applications, the connection between the gain output pin VMAG and the setpoint control pin MSET is broken. The desired setpoint is presented to MSET and the VMAG control signal drives an appropriate external variable gain device. Likewise, the feedback path between the phase output pin VPHS and its setpoint control pin PSET may be broken to allow operation as a phase controller.

The AD8302 is fabricated on Analog Devices' proprietary, high performance 25 GHz SOI complementary bipolar IC process. It is available in a 14-lead TSSOP package and operates over a –40°C to +85°C temperature range. An evaluation board is available.

REV. B

Document Feedback

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AD8302–SPECIFICATIONS (T_A = 25°C, V_S = 5 V, VMAG shorted to MSET, VPHS shorted to PSET, 52.3 Ω shunt resistors connected to INPA and INPB, for Phase measurement $P_{INPA} = P_{INPB}$, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Input Frequency Range		>0		2700	MHz
Gain Measurement Range	P_{IN} at INPA, P_{IN} at INPB = –30 dBm		±30		dB
Phase Measurement Range	ϕ_{IN} at INPA > ϕ_{IN} at INPB		±90		Degree
Reference Voltage Output	Pin VREF, –40°C ≤ T_A ≤ +85°C	1.72	1.8	1.88	V
INPUT INTERFACE	Pins INPA and INPB				
Input Simplified Equivalent Circuit	To AC Ground, f ≤ 500 MHz		3‖2		kΩ‖pF
Input Voltage Range	AC-Coupled (0 dBV = 1 V rms)	–73		–13	dBV
	re: 50 Ω	–60		0	dBm
Center of Input Dynamic Range			–43		dBV
			–30		dBm
MAGNITUDE OUTPUT	Pin VMAG				
Output Voltage Minimum	20 × Log (V_{INPA}/V_{INPB}) = –30 dB		30		mV
Output Voltage Maximum	20 × Log (V_{INPA}/V_{INPB}) = +30 dB		1.8		V
Center Point of Output (MCP)	$V_{INPA} = V_{INPB}$		900		mV
Output Current	Source/Sink		8		mA
Small Signal Envelope Bandwidth	Pin MFLT Open		30		MHz
Slew Rate	40 dB Change, Load 20 pF‖10 kΩ		25		V/µs
Response Time					
Rise Time	Any 20 dB Change, 10%–90%		50		ns
Fall Time	Any 20 dB Change, 90%–10%		60		ns
Settling Time	Full-Scale 60 dB Change, to 1% Settling		300		ns
PHASE OUTPUT	Pin VPHS				
Output Voltage Minimum	Phase Difference 180 Degrees		30		mV
Output Voltage Maximum	Phase Difference 0 Degrees		1.8		V
Phase Center Point	When $\phi_{INPA} = \phi_{INPB} \pm 90°$		900		mV
Output Current Drive	Source/Sink		8		mA
Slew Rate			25		V/µs
Small Signal Envelope Bandwidth			30		MHz
Response Time	Any 15 Degree Change, 10%–90%		40		ns
	120 Degree Change C_{FILT} = 1 pF, to 1% Settling		500		ns
100 MHz	MAGNITUDE OUTPUT				
Dynamic Range	±1 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		58		dB
	±0.5 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		55		dB
	±0.2 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		42		dB
Slope	From Linear Regression		29		mV/dB
Deviation vs. Temperature	Deviation from Output at 25°C				
	–40°C ≤ T_A ≤ +85°C, $P_{INPA} = P_{INPB}$ = –30 dBm		0.25		dB
	Deviation from Best Fit Curve at 25°C				
	–40°C ≤ T_A ≤ +85°C, P_{INPA} = ±25 dB, P_{INPB} = –30 dBm		0.25		dB
Gain Measurement Balance	$P_{INPA} = P_{INPB}$ = –5 dBm to –50 dBm		0.2		dB
	PHASE OUTPUT				
Dynamic Range	Less than ±1 Degree Deviation from Best Fit Line		145		Degree
	Less than 10% Deviation in Instantaneous Slope		143		Degree
Slope (Absolute Value)	From Linear Regression about –90° or +90°		10		mV/Degree
Deviation vs. Temperature	Deviation from Output at 25°C				
	–40°C ≤ T_A ≤ +85°C, Delta Phase = 90 Degrees		0.7		Degree
	Deviation from Best Fit Curve at 25°C				
	–40°C ≤ T_A ≤ +85°C, Delta Phase = ±30 Degrees		0.7		Degree

Parameter	Conditions	Min	Typ	Max	Unit
900 MHz	MAGNITUDE OUTPUT				
Dynamic Range	±1 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		58		dB
	±0.5 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		54		dB
	±0.2 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		42		dB
Slope	From Linear Regression		28.7		mV/dB
Deviation vs. Temperature	Deviation from Output at 25°C				
	–40°C ≤ T_A ≤ +85°C, P_{INPA} = P_{INPB} = –30 dBm		0.25		dB
	Deviation from Best Fit Curve at 25°C				
	–40°C ≤ T_A ≤ +85°C, P_{INPA} = ±25 dB, P_{INPB} = –30 dBm		0.25		dB
Gain Measurement Balance	P_{INPA} = P_{INPB} = –5 dBm to –50 dBm		0.2		dB
	PHASE OUTPUT				
Dynamic Range	Less than ± 1 Degree Deviation from Best Fit Line		143		Degree
	Less than 10% Deviation in Instantaneous Slope		143		Degree
Slope (Absolute Value)	From Linear Regression about –90° or +90°		10.1		mV/Degree
Deviation	Linear Deviation from Best Fit Curve at 25°C				
	–40°C ≤ T_A ≤ +85°C, Delta Phase = 90 Degrees		0.75		Degree
	–40°C ≤ T_A ≤ +85°C, Delta Phase = ±30 Degrees		0.75		Degree
Phase Measurement Balance	Phase @ INPA = Phase @ INPB, P_{IN} = –5 dBm to –50 dBm		0.8		Degree
1900 MHz	MAGNITUDE OUTPUT				
Dynamic Range	±1 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		57		dB
	±0.5 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		54		dB
	±0.2 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		42		dB
Slope	From Linear Regression		27.5		mV/dB
Deviation vs. Temperature	Deviation from Output at 25°C				
	–40°C ≤ T_A ≤ +85°C, P_{INPA} = P_{INPB} = –30 dBm		0.27		dB
	Deviation from Best Fit Curve at 25°C				
	–40°C ≤ T_A ≤ +85°C, P_{INPA} = ±25 dB, P_{INPB} = –30 dBm		0.33		dB
Gain Measurement Balance	P_{INPA} = P_{INPB} = –5 dBm to –50 dBm		0.2		dB
	PHASE OUTPUT				
Dynamic Range	Less than ±1 Degree Deviation from Best Fit Line		128		Degree
	Less than 10% Deviation in Instantaneous Slope		120		Degree
Slope (Absolute Value)	From Linear Regression about –90° or +90°		10.2		mV/Degree
Deviation	Linear Deviation from Best Fit Curve at 25°C				
	–40°C ≤ T_A ≤ +85°C, Delta Phase = 90 Degrees		0.8		Degree
	–40°C ≤ T_A ≤ +85°C, Delta Phase = ±30 Degrees		0.8		Degree
Phase Measurement Balance	Phase @ INPA = Phase @ INPB, P_{IN} = –5 dBm to –50 dBm		1		Degree
2200 MHz	MAGNITUDE OUTPUT				
Dynamic Range	±1 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		53		dB
	±0.5 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		51		dB
	±0.2 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		38		dB
Slope	From Linear Regression		27.5		mV/dB
Deviation vs. Temperature	Deviation from Output at 25°C				
	–40°C ≤ T_A ≤ +85°C, P_{INPA} = P_{INPB} = –30 dBm		0.28		dB
	Deviation from Best Fit Curve at 25°C				
	–40°C ≤ T_A ≤ +85°C, P_{INPA} = ±25 dB, P_{INPB} = –30 dBm		0.4		dB
Gain Measurement Balance	P_{INPA} = P_{INPB} = –5 dBm to –50 dBm		0.2		dB
	PHASE OUTPUT				
Dynamic Range	Less than ±1 Degree Deviation from Best Fit Line		115		Degree
	Less than 10% Deviation in Instantaneous Slope		110		Degree
Slope (Absolute Value)	From Linear Regression about –90° or +90°		10		mV/Degree
Deviation	Linear Deviation from Best Fit Curve at 25°C				
	–40°C ≤ T_A ≤ +85°C, Delta Phase = 90 Degrees		0.85		Degree
	–40°C ≤ T_A ≤ +85°C, Delta Phase = ±30 Degrees		0.9		Degree
REFERENCE VOLTAGE	Pin VREF				
Output Voltage	Load = 2 kΩ	1.7	1.8	1.9	V
PSRR	V_S = 2.7 V to 5.5 V		0.25		mV/V
Output Current	Source/Sink (Less than 1% Change)		5		mA
POWER SUPPLY	Pin VPOS				
Supply		2.7	5.0	5.5	V
Operating Current (Quiescent)	V_S = 5 V		19	25	mA
	–40°C ≤ T_A ≤ +85°C		21	27	mA

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

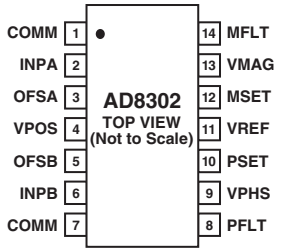
Supply Voltage V_S . . . . . 5.5 V
PSET, MSET Voltage . . . . . V_S + 0.3 V
INPA, INPB Maximum Input . . . . . –3 dBV
Equivalent Power Re. 50 Ω . . . . . 10 dBm
θ_{JA}[2] . . . . . 150°C/W
Maximum Junction Temperature . . . . . 125°C
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]JEDEC 1S Standard (2-layer) board data.

PIN CONFIGURATION



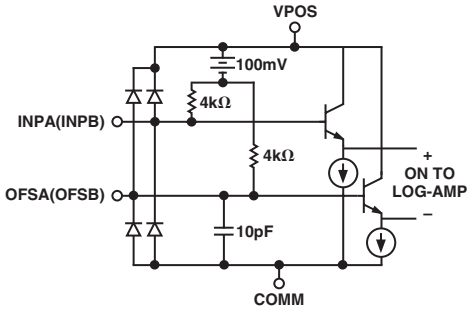
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function	Equivalent Circuit
1, 7	COMM	Device Common. Connect to low impedance ground.	
2	INPA	High Input Impedance to Channel A. Must be ac-coupled.	Circuit A
3	OFSA	A capacitor to ground at this pin sets the offset compensation filter corner and provides input decoupling.	Circuit A
4	VPOS	Voltage Supply (V_S), 2.7 V to 5.5 V	
5	OFSB	A capacitor to ground at this pin sets the offset compensation filter corner and provides input decoupling.	Circuit A
6	INPB	Input to Channel B. Same structure as INPA.	Circuit A
8	PFLT	Low Pass Filter Terminal for the Phase Output	Circuit E
9	VPHS	Single-Ended Output Proportional to the Phase Difference between INPA and INPB.	Circuit B
10	PSET	Feedback Pin for Scaling of VPHS Output Voltage in Measurement Mode. Apply a setpoint voltage for controller mode.	Circuit D
11	VREF	Internally Generated Reference Voltage (1.8 V Nominal)	Circuit C
12	MSET	Feedback Pin for Scaling of VMAG Output Voltage Measurement Mode. Accepts a set point voltage in controller mode.	Circuit D
13	VMAG	Single-Ended Output. Output voltage proportional to the decibel ratio of signals applied to INPA and INPB.	Circuit B
14	MFLT	Low Pass Filter Terminal for the Magnitude Output	Circuit E

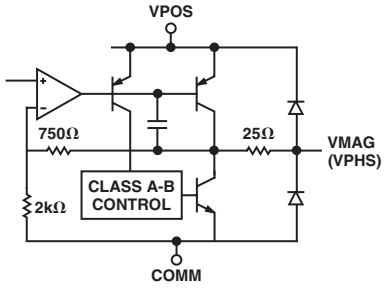
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8302 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

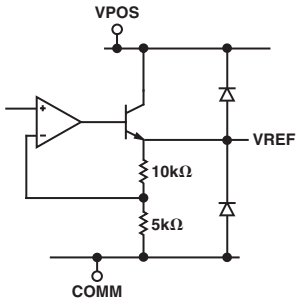




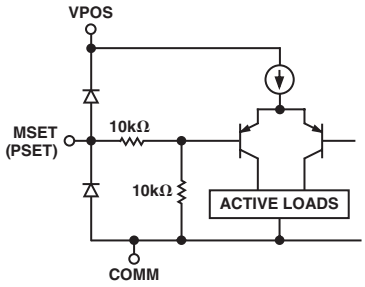
Circuit A



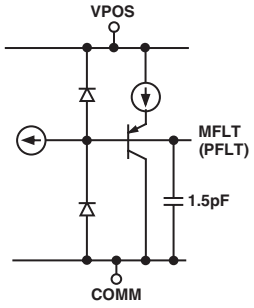
Circuit B



Circuit C



Circuit D

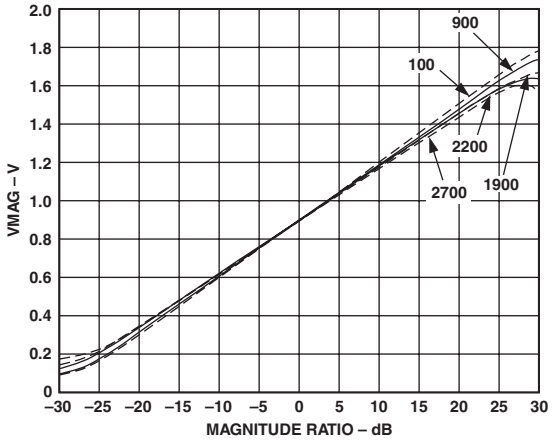


Circuit E

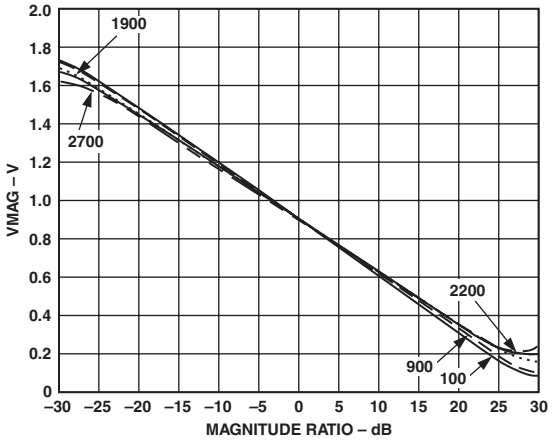
Figure 1. Equivalent Circuits

AD8302–Typical Performance Characteristics

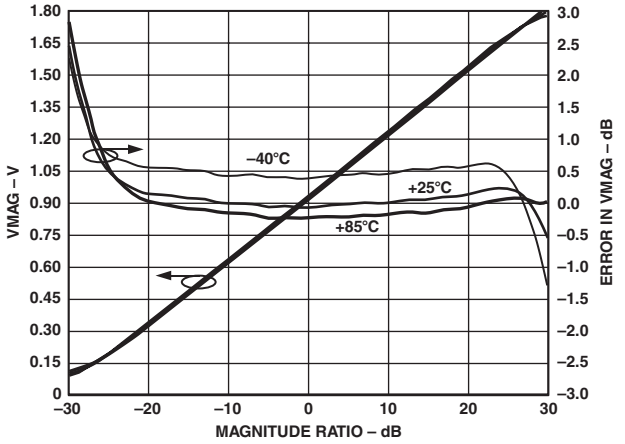
(V_S = 5 V, V_{INPB} is the reference input and V_{INPA} is swept, unless otherwise noted. All references to dBm are referred to 50 Ω. For the phase output curves, the input signal levels are equal, unless otherwise noted.)



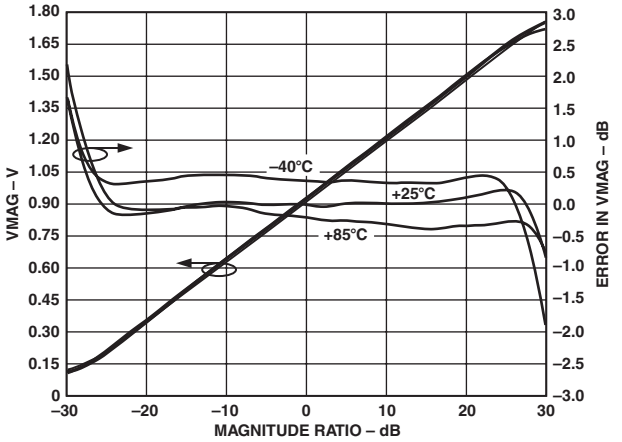
TPC 1. Magnitude Output (VMAG) vs. Input Level Ratio (Gain) V_{INPA}/V_{INPB}, Frequencies 100 MHz, 900 MHz, 1900 MHz, 2200 MHz, 2700 MHz, 25°C, P_{INPB} = –30 dBm, (Re: 50 Ω)



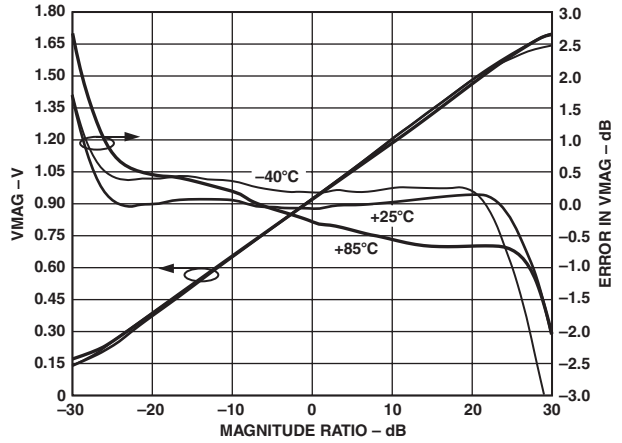
TPC 2. VMAG vs. Input Level Ratio (Gain) V_{INPA}/V_{INPB}, Frequencies 100 MHz, 900 MHz, 1900 MHz, 2200 MHz, 2700 MHz, P_{INPA} = –30 dBm



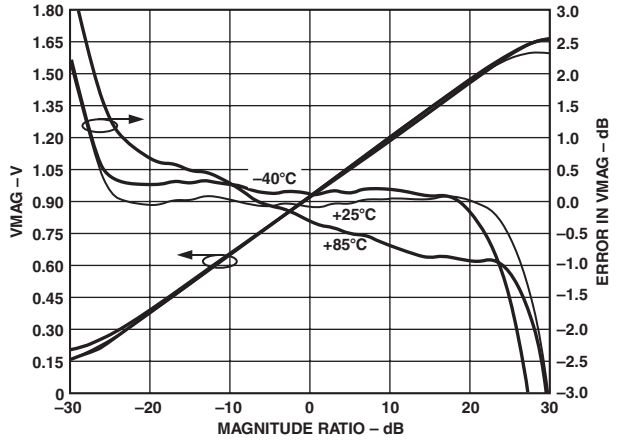
TPC 3. VMAG Output and Log Conformance vs. Input Level Ratio (Gain), Frequency 100 MHz, –40°C, +25°C, and +85°C, Reference Level = –30 dBm



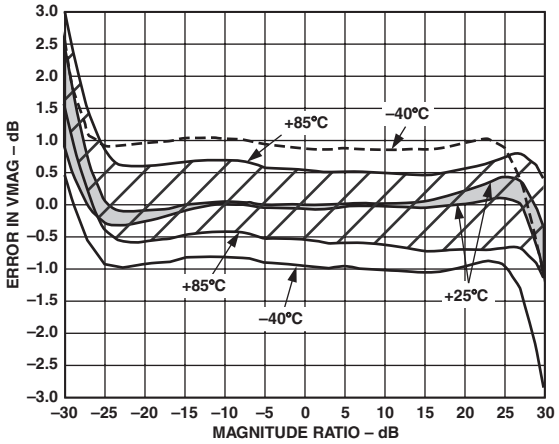
TPC 4. VMAG and Log Conformance vs. Input Level Ratio (Gain), Frequency 900 MHz, –40°C, +25°C, and +85°C, Reference Level = –30 dBm



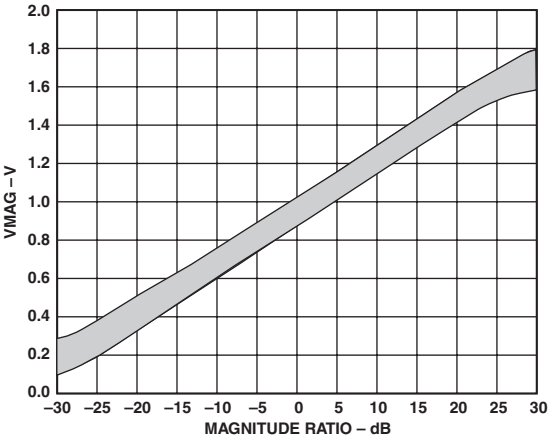
TPC 5. VMAG and Log Conformance vs. Input Level Ratio (Gain), Frequency 1900 MHz, –40°C, +25°C, and +85°C, Reference Level = –30 dBm



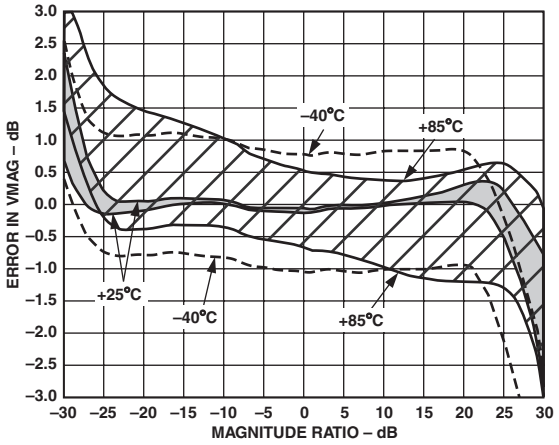
TPC 6. VMAG Output and Log Conformance vs. Input Level Ratio (Gain), Frequency 2200 MHz, –40°C, +25°C, and +85°C, Reference Level = –30 dBm



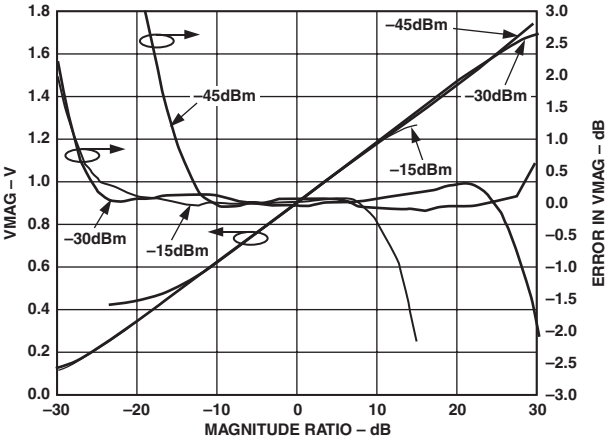
TPC 7. Distribution of Magnitude Error vs. Input Level Ratio (Gain), Three Sigma to Either Side of Mean, Frequency 900 MHz, –40°C, +25°C, and +85°C, Reference Level = –30 dBm



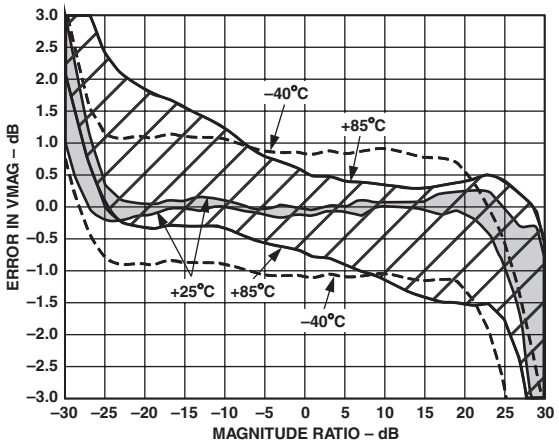
TPC 10. Distribution of VMAG vs. Input Level Ratio (Gain), Three Sigma to Either Side of Mean, Frequency 1900 MHz, Temperatures Between –40°C and +85°C, Reference Level = –30 dBm



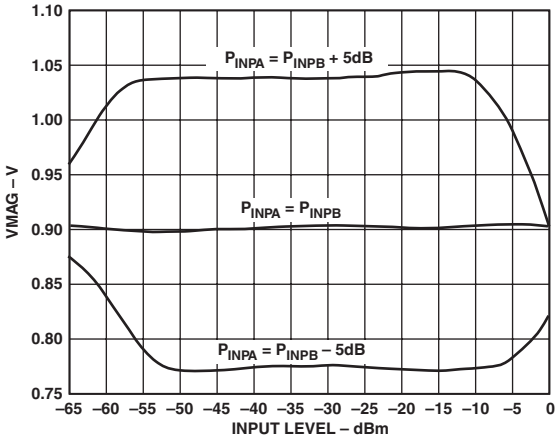
TPC 8. Distribution of Error vs. Input Level Ratio (Gain), Three Sigma to Either Side of Mean, Frequency 1900 MHz, –40°C, +25°C, and +85°C, Reference Level = –30 dBm



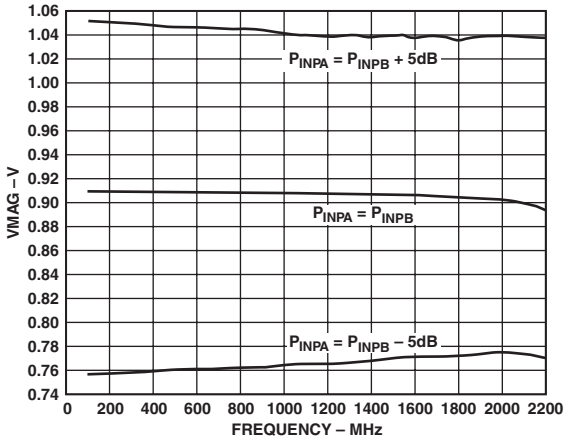
TPC 11. VMAG Output and Log Conformance vs. Input Level Ratio (Gain), Reference Level = –15 dBm, –30 dBm, and –45 dBm, Frequency 1900 MHz



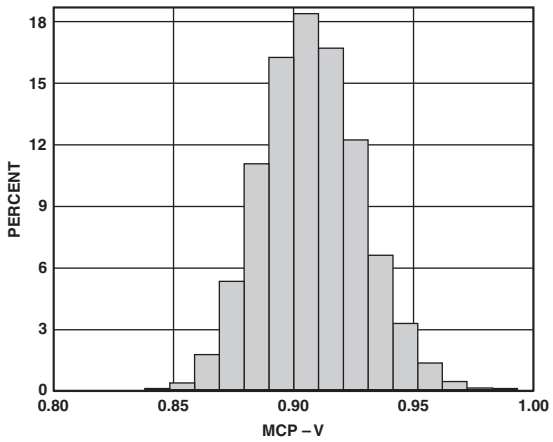
TPC 9. Distribution of Magnitude Error vs. Input Level Ratio (Gain), Three Sigma to Either Side of Mean, Frequency 2200 MHz, Temperatures –40°C, +25°C, and +85°C, Reference Level = –30 dBm



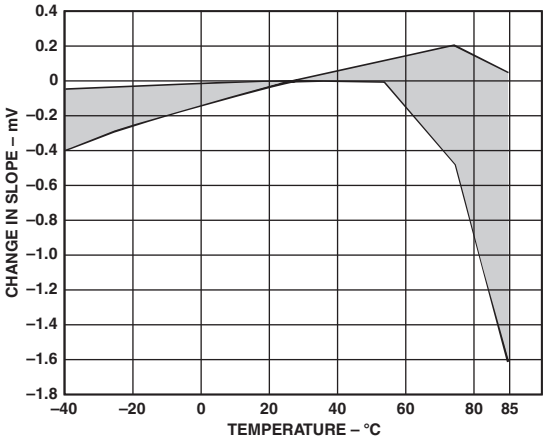
TPC 12. VMAG Output vs. Input Level for $P_{INPA} = P_{INPB}$, $P_{INPA} = P_{INPB} + 5$ dB, $P_{INPA} = P_{INPB} – 5$ dB, Frequency 1900 MHz



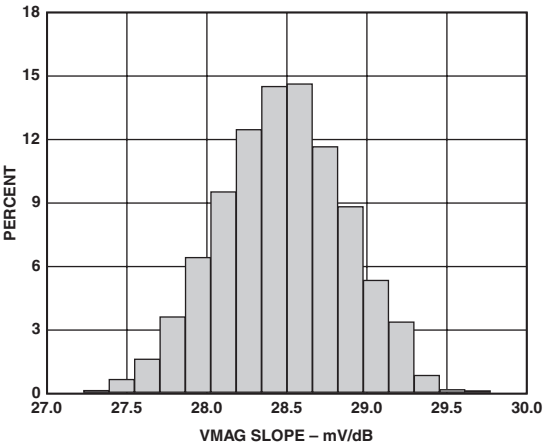
TPC 13. VMAG Output vs. Frequency, for $P_{INPA} = P_{INPB}$, $P_{INPA} = P_{INPB}$ + 5 dB, and $P_{INPA} = P_{INPB}$ – 5 dB, P_{INPB} = –30 dBm



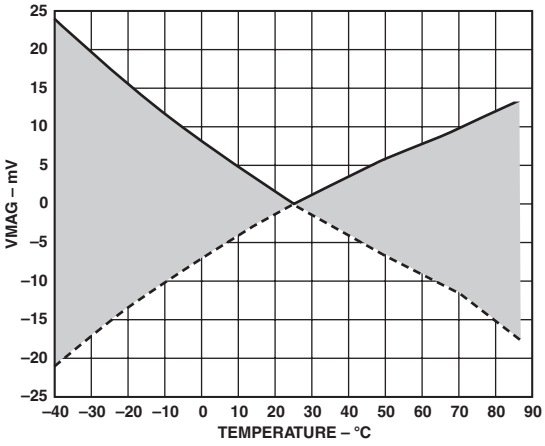
TPC 16. Center Point of Magnitude Output (MCP) Distribution Frequencies 900 MHz, 17,000 Units



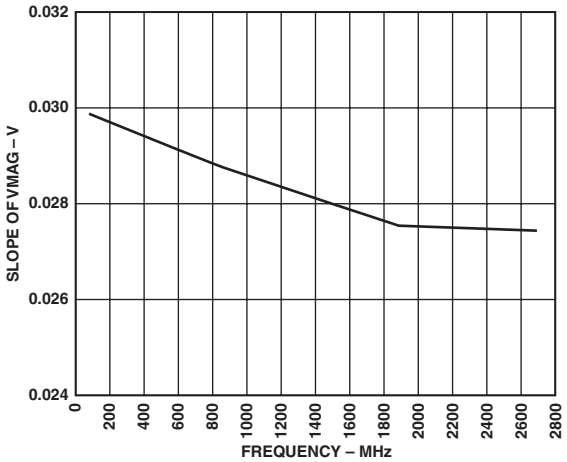
TPC 14. Change in VMAG Slope vs. Temperature, Three Sigma to Either Side of Mean, Frequencies 1900 MHz



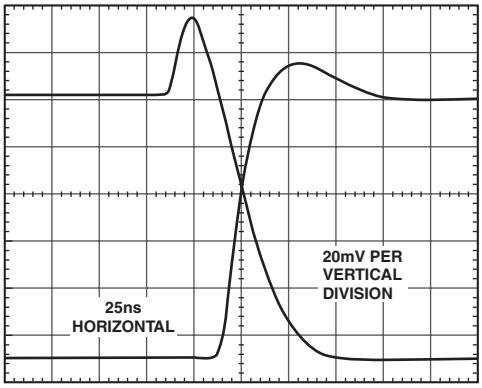
TPC 17. VMAG Slope, Frequency 900 MHz, 17,000 Units



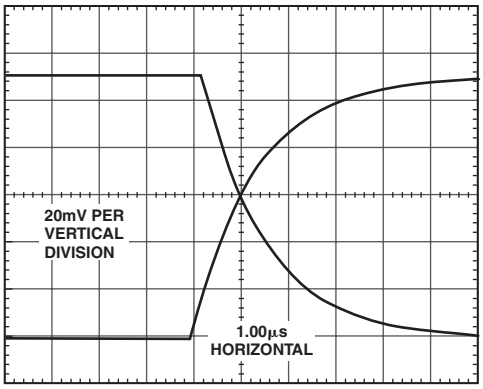
TPC 15. Change in Center Point of Magnitude Output (MCP) vs. Temperature, Three Sigma to Either Side of Mean, Frequencies 1900 MHz



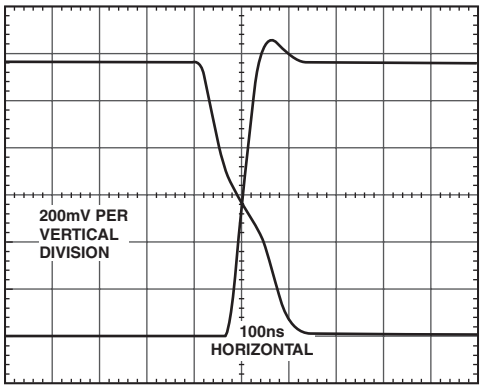
TPC 18. VMAG Slope vs. Frequency



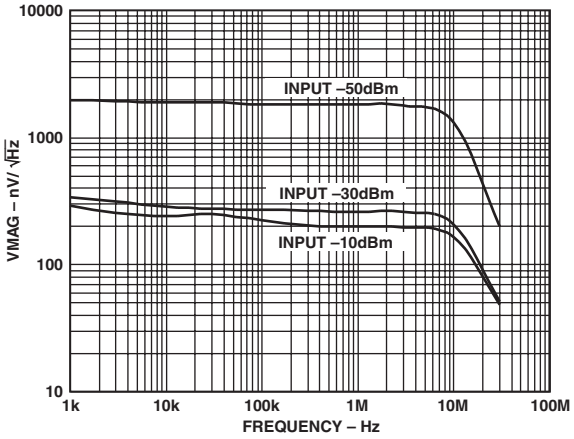
TPC 19. Magnitude Output Response to 4 dB Step, for P_{INPB} = –30 dBm, P_{INPA} = –32 dBm to –28 dBm, Frequency 1900 MHz, No Filter Capacitor



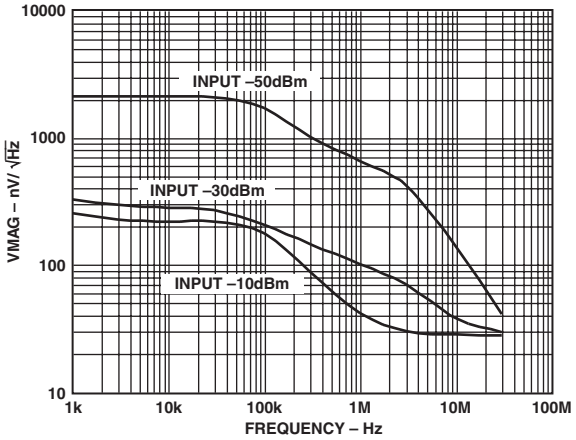
TPC 20. Magnitude Output Response to 4 dB Step, for P_{INPB} = –30 dBm, P_{INPA} = –32 dBm to –28 dBm, Frequency 1900 MHz, 1 nF Filter Capacitor



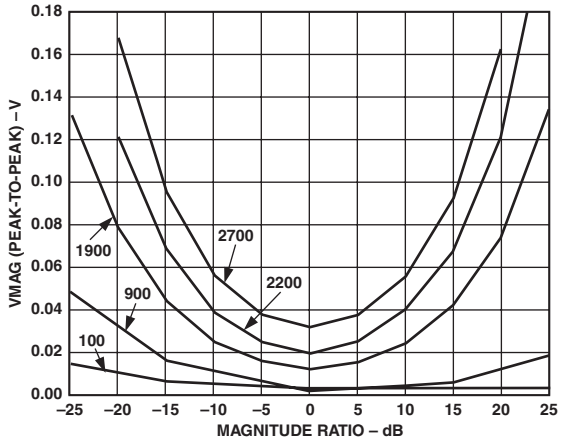
TPC 21. Magnitude Output Response to 40 dB Step, for P_{INPB} = –30 dBm, P_{INPA} = –50 dBm to –10 dBm, Supply 5 V, Frequency 1900 MHz, No Filter Capacitor



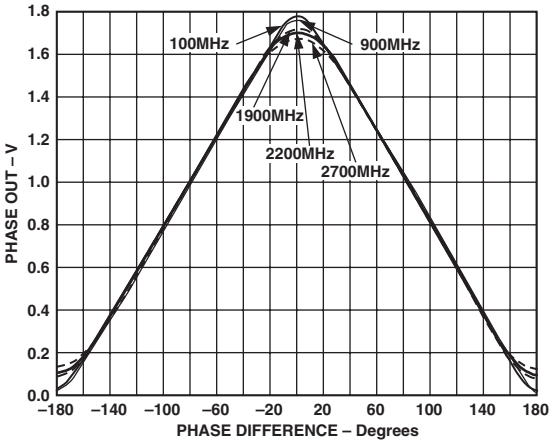
TPC 22. Magnitude Output Noise Spectral Density, P_{INPA} = P_{INPB} = –10 dBm, –30 dBm, –50 dBm, No Filter Capacitor



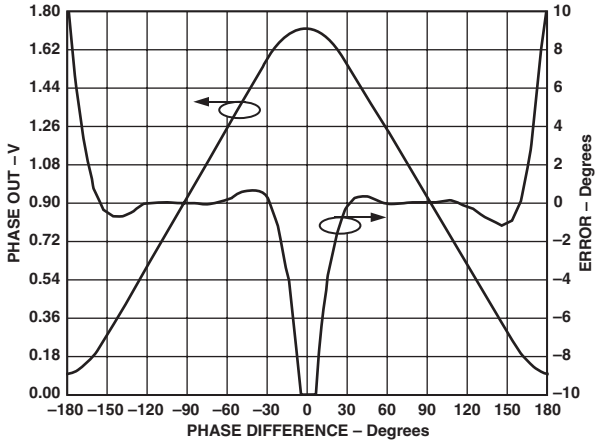
TPC 23. Magnitude Output Noise Spectral Density, P_{INPA} = P_{INPB} = –10 dBm, –30 dBm, –50 dBm, with Filter Capacitor, C = 1 nF



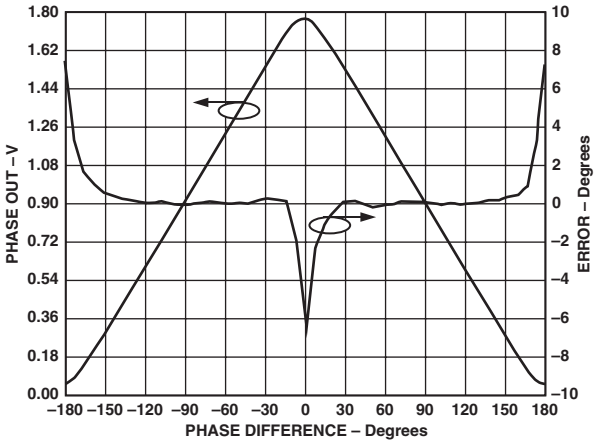
TPC 24. VMAG Peak-to-Peak Output Induced by Sweeping Phase Difference through 360 Degrees vs. Magnitude Ratio, Frequencies 100 MHz, 900 MHz, 1900 MHz, 2200 MHz, and 2700 MHz



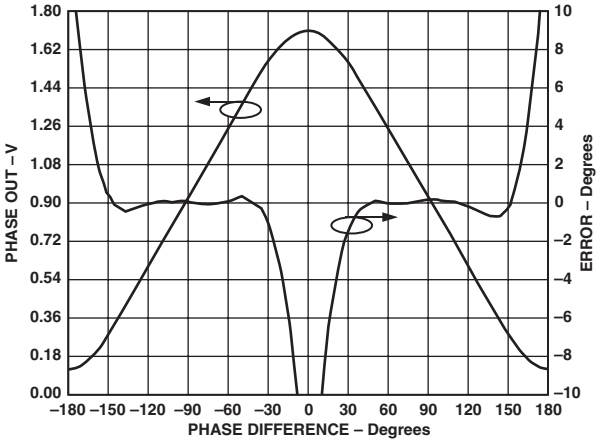
TPC 25. Phase Output (VPHS) vs. Input Phase Difference, Input Levels –30 dBm, Frequencies 100 MHz, 900 MHz, 1900 MHz, 2200 MHz, Supply 5 V, 2700 MHz



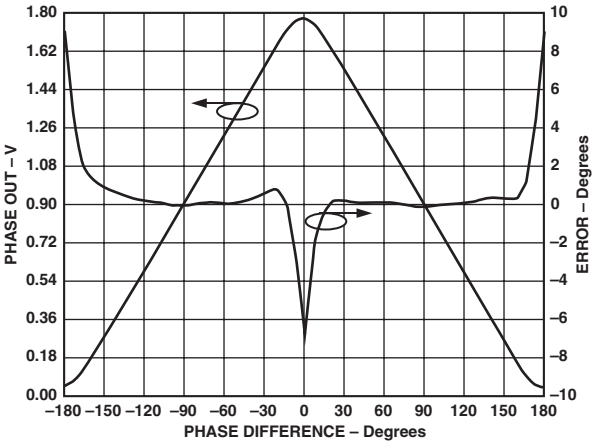
TPC 28. VPHS Output and Nonlinearity vs. Input Phase Difference, Input Levels –30 dBm, Frequency 1900 MHz



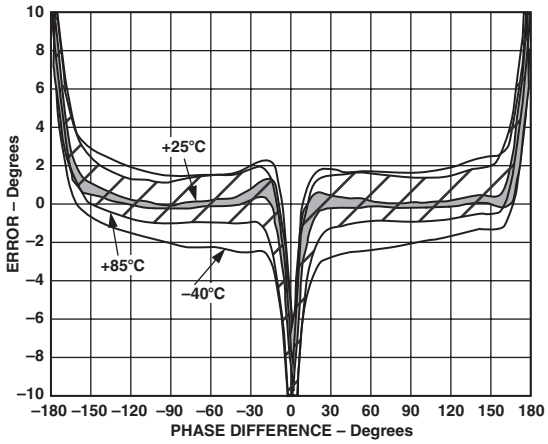
TPC 26. VPHS Output and Nonlinearity vs. Input Phase Difference, Input Levels –30 dBm, Frequency 100 MHz



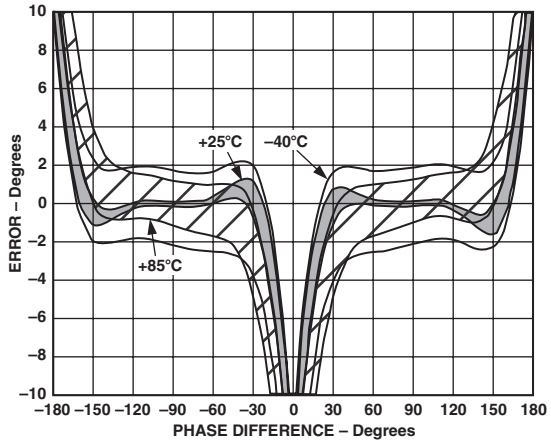
TPC 29. VPHS Output and Nonlinearity vs. Input Phase Difference, Input Levels –30 dBm, Frequency 2200 MHz



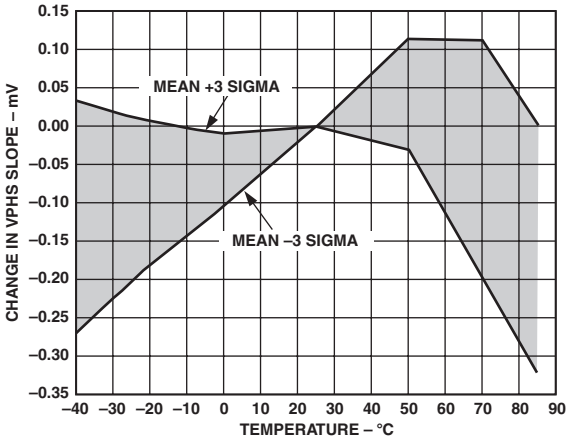
TPC 27. VPHS Output and Nonlinearity vs. Input Phase Difference, Input Levels –30 dBm, Frequency 900 MHz



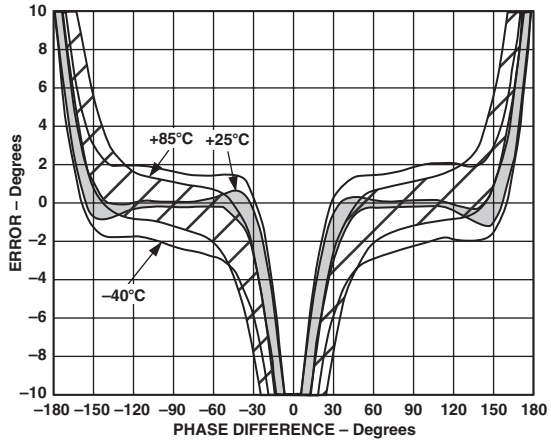
TPC 30. Distribution of VPHS Error vs. Input Phase Difference, Three Sigma to Either Side of Mean, Frequency 900 MHz, –40°C, +25°C, and +85°C, Input Levels –30 dBm



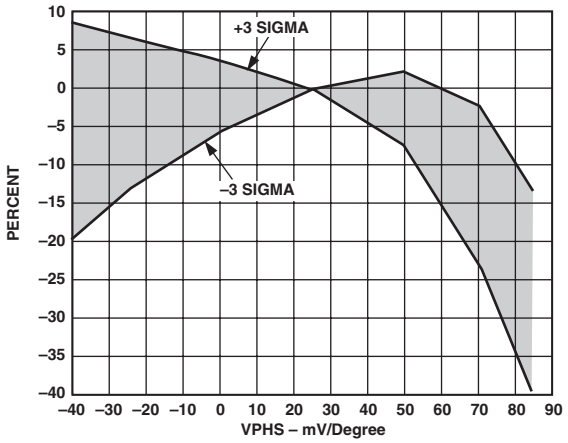
TPC 31. Distribution of VPHS Error vs. Input Phase Difference, Three Sigma to Either Side of Mean, Frequency 1900 MHz, –40°C, +25°C, and +85°C, Supply 5 V, Input Levels $P_{INPA} = P_{INPB} = –30$ dBm



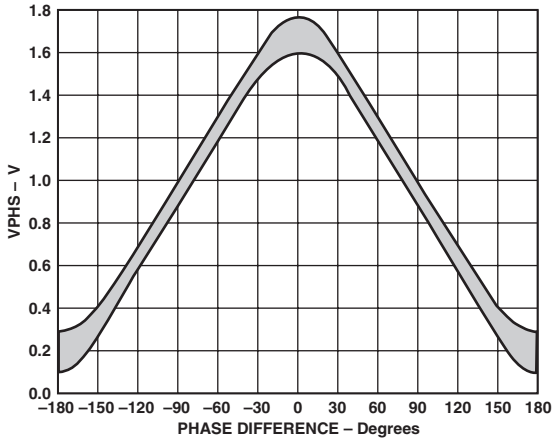
TPC 34. Change in VPHS Slope vs. Temperature, Three Sigma to Either Side of Mean, Frequency 1900 MHz



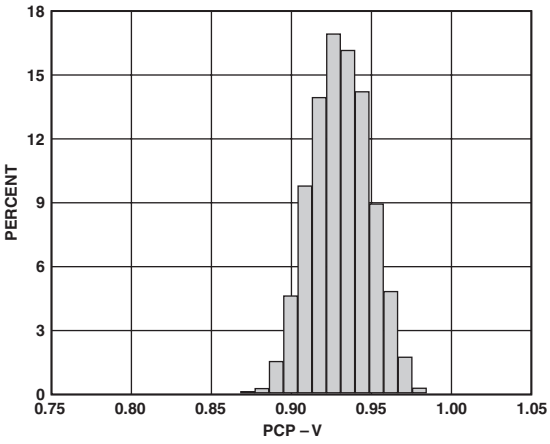
TPC 32. Distribution of VPHS Error vs. Input Phase Difference, Three Sigma to Either Side of Mean, Frequency 2200 MHz, –40°C, +25°C, and +85°C, Input Levels –30 dBm



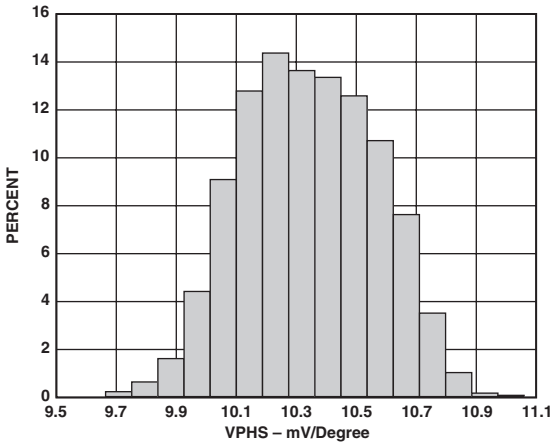
TPC 35. Change in Phase Center Point (PCP) vs. Temperature, Three Sigma to Either Side of Mean, Frequency 1900 MHz



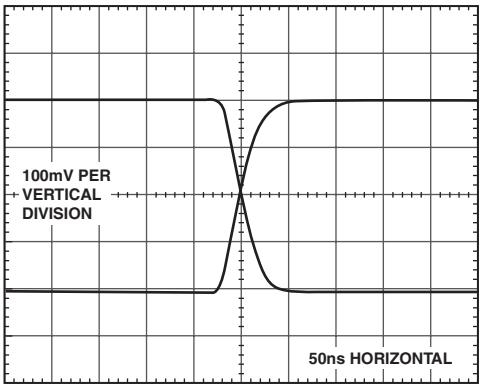
TPC 33. Distribution of VPHS vs. Input Phase Difference, Three Sigma to Either Side of Mean, Frequency 900 MHz, Temperature between –40°C and +85°C, Input Levels –30 dBm



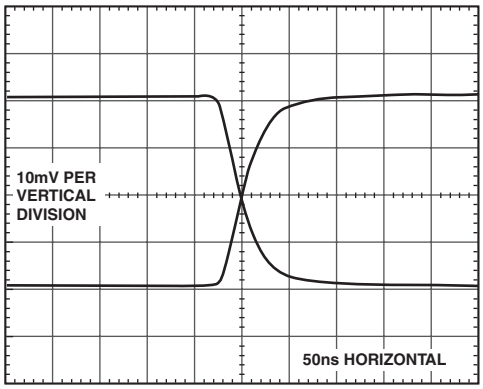
TPC 36. Phase Center Point (PCP) Distribution, Frequency 900 MHz, 17,000 Units



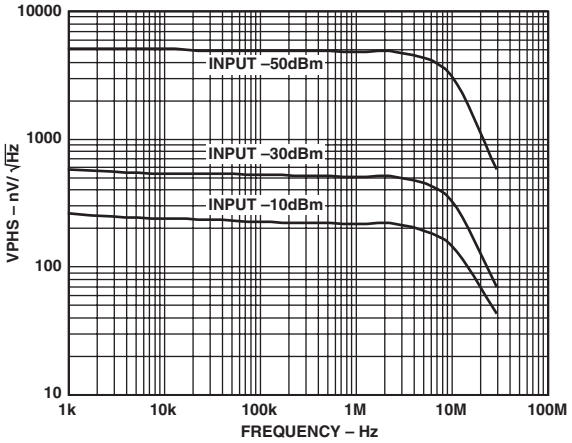
TPC 37. VPHS Slope Distribution, Frequency 900 MHz



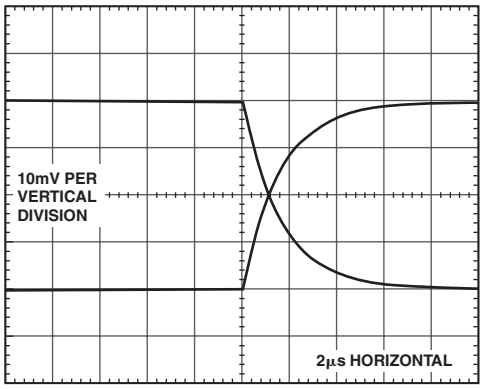
TPC 40. VPHS Output Response to 40° Step with Nominal Phase Shift of 90°, Input Levels $P_{INPA} = P_{INPB} = –30$ dBm, Frequency 1900 MHz,1 pF Filter Capacitor



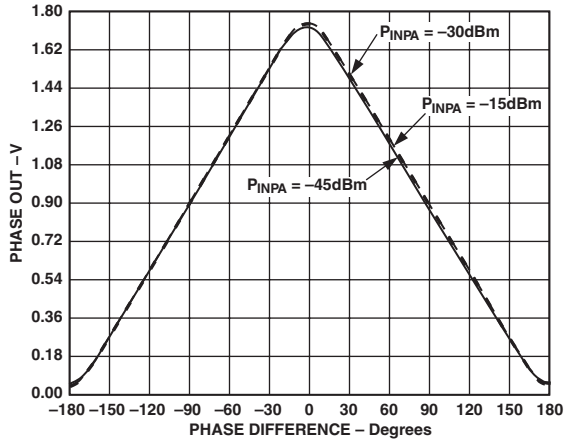
TPC 38. VPHS Output Response to 4° Step with Nominal Phase Shift of 90°, Input Levels –30 dBm, Frequency 1900 MHz, 25°C, 1 pF Filter Capacitor



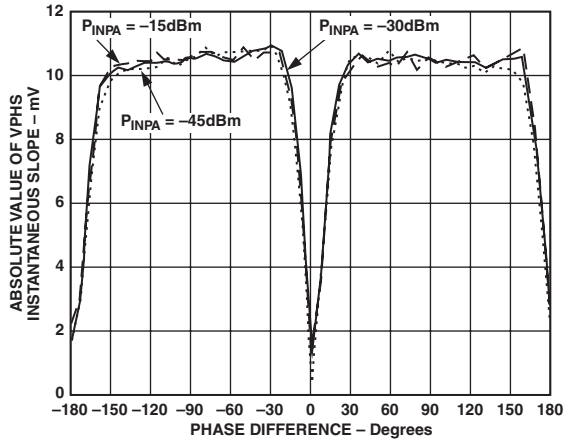
TPC 41. VPHS Output Noise Spectral Density vs. Frequency, $P_{INPA} = –30$ dBm, $P_{INPB} = –10$ dBm, –30 dBm, –50 dBm, and 90° Input Phase Difference



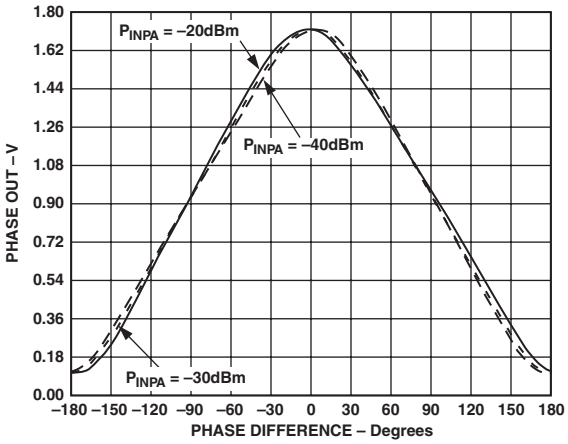
TPC 39. VPHS Output Response to 4° Step with Nominal Phase Shift of 90°, Input Levels $P_{INPA} = P_{INPB} = –30$ dBm, Supply 5 V, Frequency 1900 MHz, 25°C, with 100 pF Filter Capacitor



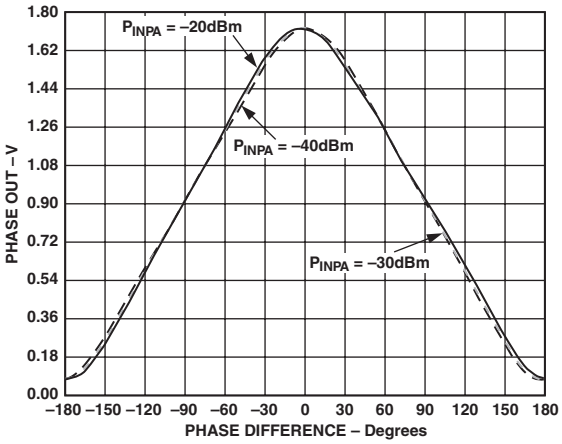
TPC 42. Phase Output vs. Input Phase Difference, $P_{INPA} = P_{INPB}$, $P_{INPA} = P_{INPB} + 15$ dB, $P_{INPA} = P_{INPB} – 15$ dB, Frequency 900 MHz



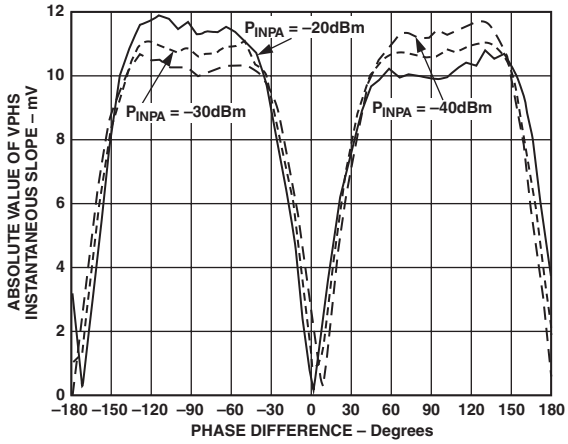
TPC 43. Phase Output Instantaneous Slope, $P_{INPA} = P_{INPB}$, $P_{INPA} = P_{INPB}$ + 15 dB, $P_{INPA} = P_{INPB}$ – 15 dB, Frequency 900 MHz



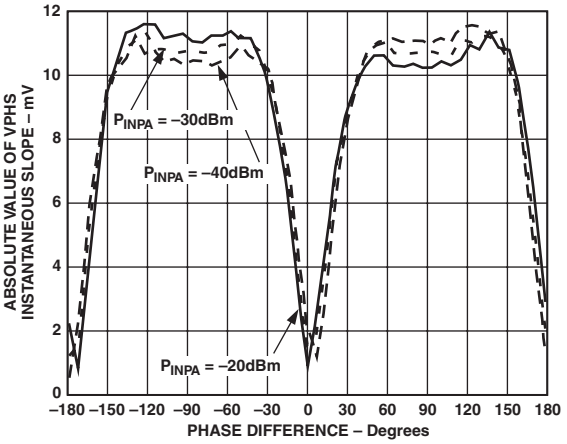
TPC 46. Phase Output vs. Input Phase Difference, $P_{INPA} = P_{INPB}$, $P_{INPA} = P_{INPB}$ + 10 dB, $P_{INPA} = P_{INPB}$ – 10 dB, Frequency 2200 MHz



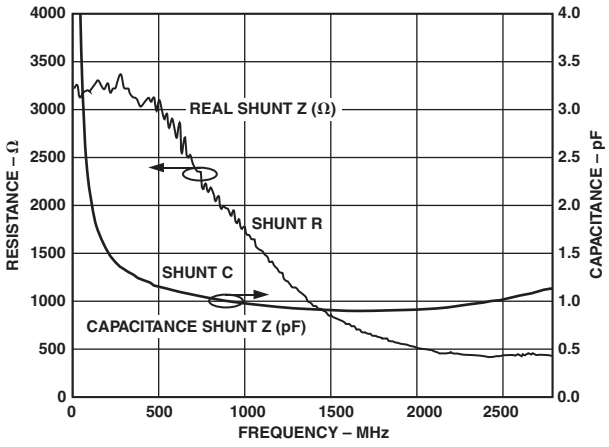
TPC 44. Phase Output vs. Input Phase Difference, $P_{INPA} = P_{INPB}$, $P_{INPA} = P_{INPB}$ + 10 dB, $P_{INPA} = P_{INPB}$ – 10 dB, Frequency 1900 MHz, Supply 5 V



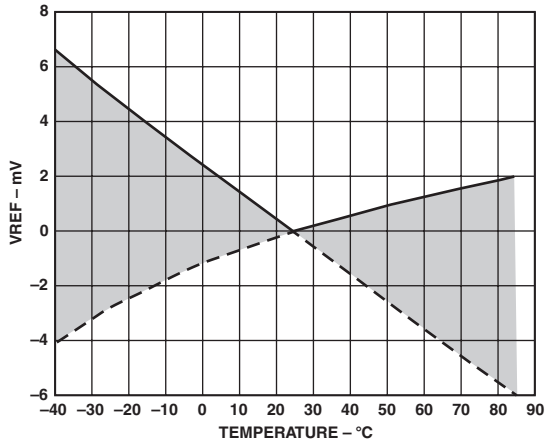
TPC 47. Phase Output Instantaneous Slope, $P_{INPA} = P_{INPB}$, $P_{INPA} = P_{INPB}$ + 10 dB, $P_{INPA} = P_{INPB}$ – 10 dB, Frequency 2200 MHz



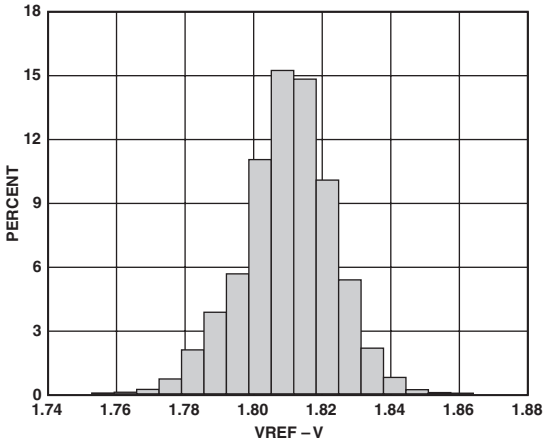
TPC 45. Phase Output Instantaneous Slope, $P_{INPA} = P_{INPB}$, $P_{INPA} = P_{INPB}$ + 10 dB, $P_{INPA} = P_{INPB}$ – 10 dB, Frequency 1900 MHz, Supply 5 V



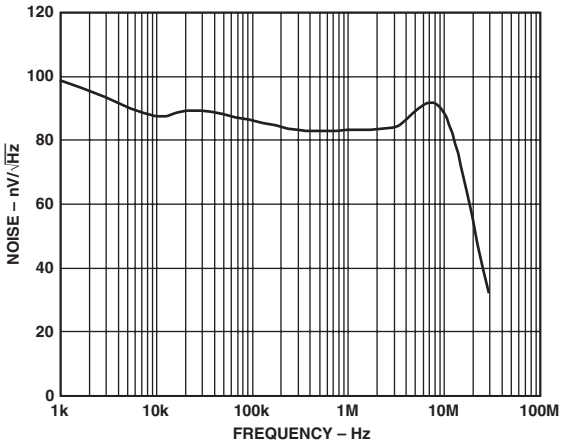
TPC 48. Input Impedance, Modeled as Shunt R in Parallel with Shunt C



TPC 49. Change in VREF vs. Temperature, Three Sigma to Either Side of Mean



TPC 51. VREF Distribution, 17,000 Units



TPC 50. VREF Output Noise Spectral Density vs. Frequency

GENERAL DESCRIPTION AND THEORY

The AD8302 measures the magnitude ratio, defined here as gain, and phase difference between two signals. A pair of matched logarithmic amplifiers provide the measurement, and their hard-limited outputs drive the phase detector.

Basic Theory

Logarithmic amplifiers (log amps) provide a logarithmic compression function that converts a large range of input signal levels to a compact decibel-scaled output. The general mathematical form is:

$$V_{OUT} = V_{SLP} \log\left(V_{IN} / V_Z\right) \quad (1)$$

where V_{IN} is the input voltage, V_Z is called the intercept (voltage), and V_{SLP} is called the slope (voltage). It is assumed throughout that log(x) represents the log10(x) function. V_{SLP} is thus the volts/decade, and since a decade of voltage corresponds to 20 dB, V_{SLP}/20 is the volts/dB. V_Z is the value of input signal that results in an output of zero and need not correspond to a physically realizable part of the log amp signal range. While the slope is fundamentally a characteristic of the log amp, the intercept is a function of the input waveform as well.[1] Furthermore, the intercept is typically more sensitive to temperature and frequency than the slope. When single log amps are used for power measurement, this variability introduces errors into the absolute accuracy of the measurement since the intercept represents a reference level.

The AD8302 takes the difference in the output of two identical log amps, each driven by signals of similar waveforms but at different levels. Since subtraction in the logarithmic domain corresponds to a ratio in the linear domain, the resulting output becomes:

$$V_{MAG} = V_{SLP} \log\left(V_{INA} / V_{INB}\right) \quad (2)$$

where V_{INA} and V_{INB} are the input voltages, V_{MAG} is the output corresponding to the magnitude of the signal level difference, and V_{SLP} is the slope. Note that the intercept, V_Z, has dropped out. Unlike the measurement of power, when measuring a dimensionless quantity such as relative signal level, no independent reference or intercept need be invoked. In essence, one signal serves as the intercept for the other. Variations in intercept due to frequency, process, temperature, and supply voltage affect both channels identically and hence do not affect the difference. This technique depends on the two log amps being well matched in slope and intercept to ensure cancellation. This is the case for an integrated pair of log amps. Note that if the two signals have different waveforms (e.g., different peak-to-average ratios) or different frequencies, an intercept difference may appear, introducing a systematic offset.

The log amp structure consists of a cascade of linear/limiting gain stages with demodulating detectors. Further details about the structure and function of log amps can be found in data sheets for other log amps produced by Analog Devices.[2] The output of the final stage of a log amp is a fully limited signal over most of the input dynamic range. The limited outputs from both log amps drive an exclusive-OR style digital phase detector. Operating strictly on the relative zero-crossings of the limited signals, the extracted phase difference is independent of the original input signal levels. The phase output has the general form:

$$V_{PHS} = V_\Phi \left[\Phi\left(V_{INA}\right) - \Phi\left(V_{INB}\right)\right] \quad (3)$$

where V_Φ is the phase slope in mV/degree and Φ is each signal's relative phase in degrees.

Structure

The general form of the AD8302 is shown in Figure 2. The major blocks consist of two demodulating log amps, a phase detector, output amplifiers, a biasing cell, and an output reference voltage buffer. The log amps and phase detector process the high frequency signals and deliver the gain and phase information in current form to the output amplifiers. The output amplifiers determine the final gain and phase scaling. External filter capacitors set the averaging time constants for the respective outputs. The reference buffer provides a 1.80 V reference voltage that tracks the internal scaling constants.

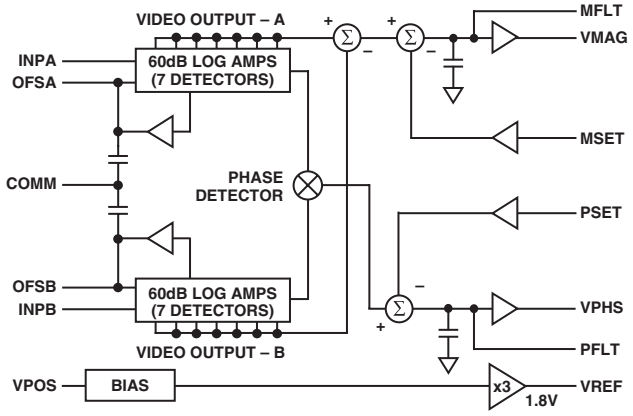


Figure 2. General Structure

Each log amp consists of a cascade of six 10 dB gain stages with seven associated detectors. The individual gain stages have 3 dB bandwidths in excess of 5 GHz. The signal path is fully differential to minimize the effect of common-mode signals and noise. Since there is a total of 60 dB of cascaded gain, slight dc offsets can cause limiting of the latter stages, which may cause measurement errors for small signals. This is corrected by a feedback loop. The nominal high-pass corner frequency, f_{HP}, of this loop is set internally at 200 MHz but can be lowered by adding external capacitance to the OFSA and OFSB pins. Signals at frequencies well below the high-pass corner are indistinguishable from dc offsets and are also nulled. The difference in the log amp outputs is performed in the current domain, yielding by analogy to Equation 2:

$$I_{LA} = I_{SLP} \log\left(V_{INA} / V_{INB}\right) \quad (4)$$

where I_{LA} and I_{SLP} are the output current difference and the characteristic slope (current) of the log amps, respectively. The slope is derived from an accurate reference designed to be insensitive to temperature and supply voltage.

The phase detector uses a fully symmetric structure with respect to its two inputs to maintain balanced delays along both signal paths. Fully differential signaling again minimizes the sensitivity to common-mode perturbations. The current-mode equivalent to Equation 3 is:

$$I_{PD} = I_\Phi \left[\Phi\left(V_{INA}\right) - \Phi\left(V_{INB}\right) - 90°\right] \quad (5)$$

where I_{PD} and I_Φ are the output current and characteristic slope associated with the phase detector, respectively. The slope is derived from the same reference as the log amp slope.

NOTES

[1]See the data sheet for the AD640 for a description of the effect of waveform on the intercept of log amps.

[2]For example, see the data sheet for the AD8307.

Note that by convention, the phase difference is taken in the range from –180° to +180°. Since this style of phase detector does not distinguish between ±90°, it is considered to have an unambiguous 180° phase difference range that can be either 0° to +180° centered at +90° or 0° to –180° centered at –90°.

The basic structure of both output interfaces is shown in Figure 3. It accepts a setpoint input and includes an internal integrating/averaging capacitor and a buffer amplifier with gain K. External access to these setpoints provides for several modes of operation and enables flexible tailoring of the gain and phase transfer characteristics. The setpoint interface block, characterized by a transresistance R_F, generates a current proportional to the voltage presented to its input pin, MSET or PSET. A precise offset voltage of 900 mV is introduced internally to establish the center-point (V_{CP}) for the gain and phase functions, i.e., the setpoint voltage that corresponds to a gain of 0 dB and a phase difference of 90°. This setpoint current is subtracted from the signal current, I_{IN}, coming from the log amps in the gain channel or from the phase detector in the phase channel. The resulting difference is integrated on the averaging capacitors at either pin MFLT or PFLT and then buffered by the output amplifier to the respective output pins, VMAG and VPHS. With this open-loop arrangement, the output voltage is a simple integration of the difference between the measured gain/phase and the desired setpoint:

$$V_{OUT} = R_F\left(I_{IN} - I_{FB}\right) / \left(sT\right) \tag{6}$$

where I_{FB} is the feedback current equal to $(V_{SET} - V_{CP})/R_F$, V_{SET} is the setpoint input, and T is the integration time constant equal to $R_F C_{AVE}/K$, where C_{AVE} is the parallel combination of the internal 1.5 pF and the external capacitor C_{FLT}.

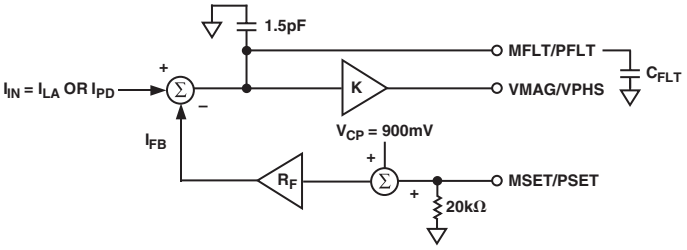


Figure 3. Simplified Block Diagram of the Output Interface

BASIC CONNECTIONS

Measurement Mode

The basic function of the AD8302 is the direct measurement of gain and phase. When the output pins, VMAG and VPHS, are connected directly to the feedback setpoint input pins, MSET and PSET, the default slopes and center points are invoked. This basic connection shown in Figure 4 is termed the measurement mode. The current from the setpoint interface is forced by the integrator to be equal to the signal currents coming from the log amps and phase detector. The closed loop transfer function is thus given by:

$$V_{OUT} = \left(I_{IN} R_F + V_{CP}\right) / \left(1 + sT\right) \tag{7}$$

The time constant T represents the single-pole response to the envelope of the dB-scaled gain and the degree-scaled phase functions. A small internal capacitor sets the maximum envelope bandwidth to approximately 30 MHz. If no external C_{FLT} is used, the AD8302 can follow the gain and phase envelopes within this bandwidth. If longer averaging is desired, C_{FLT} can be added as necessary according to T (ns) = 3.3 × C_{AVE} (pF). For best transient response with minimal overshoot, it is recommended that 1 pF minimum value external capacitors be added to the MFLT and PFLT pins.

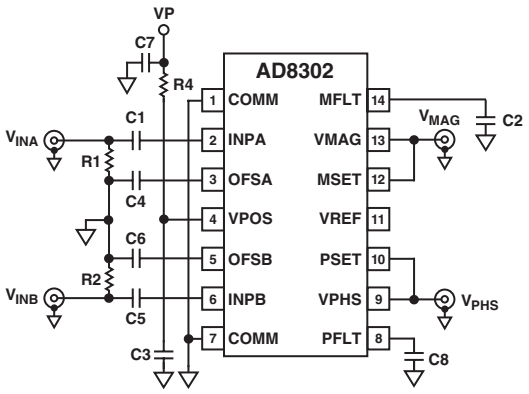


Figure 4. Basic Connections in Measurement Mode with 30 mV/dB and 10 mV/Degree Scaling

In the low frequency limit, the gain and phase transfer functions given in Equations 4 and 5 become:

$$V_{MAG} = R_F I_{SLP} \log\left(V_{INA} / V_{INB}\right) + V_{CP} \text{ or} \tag{8a}$$

$$V_{MAG} = \left(R_F I_{SLP} / 20\right)\left(P_{INA} - P_{INB}\right) + V_{CP} \tag{8b}$$

$$V_{PHS} = -R_F I_\Phi \left(\left|\Phi\left(V_{INA}\right) - \Phi\left(V_{INB}\right)\right| - 90°\right) + V_{CP} \tag{9}$$

which are illustrated in Figure 5. In Equation 8b, P_{INA} and P_{INB} are the power in dBm equivalent to V_{INA} and V_{INB} at a specified reference impedance. For the gain function, the slope represented by $R_F I_{SLP}$ is 600 mV/decade or, dividing by 20 dB/decade, 30 mV/dB. With a center point of 900 mV for 0 dB gain, a range of –30 dB to +30 dB covers the full-scale swing from 0 V to 1.8 V. For the phase function, the slope represented by $R_F I_\Phi$ is 10 mV/degree. With a center point of 900 mV for 90°, a range of 0° to 180° covers the full-scale swing from 1.8 V to 0 V. The range of 0° to –180° covers the same full-scale swing but with the opposite slope.

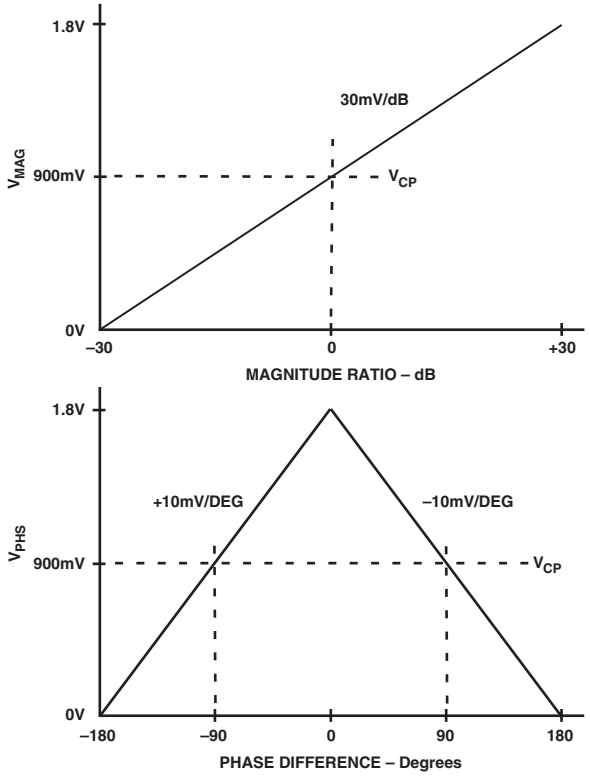


Figure 5. Idealized Transfer Characteristics for the Gain and Phase Measurement Mode

Interfacing to the Input Channels

The single-ended input interfaces for both channels are identical. Each consists of a driving pin, INPA and INPB, and an ac-grounding pin, OFSA and OFSB. All four pins are internally dc-biased at about 100 mV from the positive supply and should be externally ac-coupled to the input signals and to ground. For the signal pins, the coupling capacitor should offer negligible impedance at the signal frequency. For the grounding pins, the coupling capacitor has two functions: It provides ac grounding and sets the high-pass corner frequency for the internal offset compensation loop. There is an internal 10 pF capacitor to ground that sets the maximum corner to approximately 200 MHz. The corner can be lowered according the formula f_{HP} (MHz) = $2/C_C$(nF), where C_C is the total capacitance from OFSA or OFSB to ground, including the internal 10 pF.

The input impedance to INPA and INPB is a function of frequency, the offset compensation capacitor, and package parasitics. At moderate frequencies above f_{HP}, the input network can be approximated by a shunt 3 kΩ resistor in parallel with a 2 pF capacitor. At higher frequencies, the shunt resistance decreases to approximately 500 Ω. The Smith Chart in Figure 6 shows the input impedance over the frequency range 100 MHz to 3 GHz.

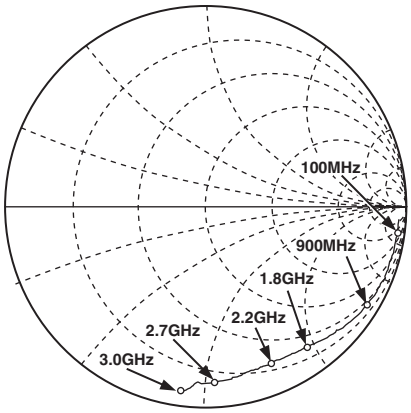


Figure 6. Smith Chart Showing the Input Impedance of a Single Channel from 100 MHz to 3 GHz

A broadband resistive termination on the signal side of the coupling capacitors can be used to match to a given source impedance. The value of the termination resistor, R_T, is determined by:

$$R_T = R_{IN}R_S / \left(R_{IN} - R_S\right) \quad (10)$$

where R_{IN} is the input resistance and R_S the source impedance. At higher frequencies, a reactive, narrow-band match might be desirable to tune out the reactive portion of the input impedance. An important attribute of the two-log-amp architecture is that if both channels are at the same frequency and have the same input network, then impedance mismatches and reflection losses become essentially common-mode and hence do not impact the relative gain and phase measurement. However, mismatches in these external components can result in measurement errors.

Dynamic Range

The maximum measurement range for the gain subsystem is limited to a total of 60 dB distributed from –30 dB to +30 dB. This means that both gain and attenuation can be measured. The limits are determined by the minimum and maximum levels that each individual log amp can detect. In the AD8302, each log amp can detect inputs ranging from –73 dBV [(223 μV, –60 dBm re: 50 Ω to –13 dBV (223 mV, 0 dBm re: 50 Ω)]. Note that log amps respond to voltages and not power. An equivalent power can be inferred given an impedance level, e.g., to convert from dBV to dBm in a 50 Ω system, simply add 13 dB. To cover the entire range, it is necessary to apply a reference level to one log amp that corresponds precisely to its midrange. In the AD8302, this level is at –43 dBV, which corresponds to –30 dBm in a 50 Ω environment. The other channel can now sweep from its low end, 30 dB below midrange, to its high end, 30 dB above midrange. If the reference is displaced from midrange, some measurement range will be lost at the extremes. This can occur either if the log amps run out of range or if the rails at ground or 1.8 V are reached. Figure 7 illustrates the effect of the reference channel level placement. If the reference is chosen lower than midrange by 10 dB, then the lower limit will be at –20 dB rather than –30 dB. If the reference chosen is higher by 10 dB, the upper limit will be 20 dB rather than 30 dB.

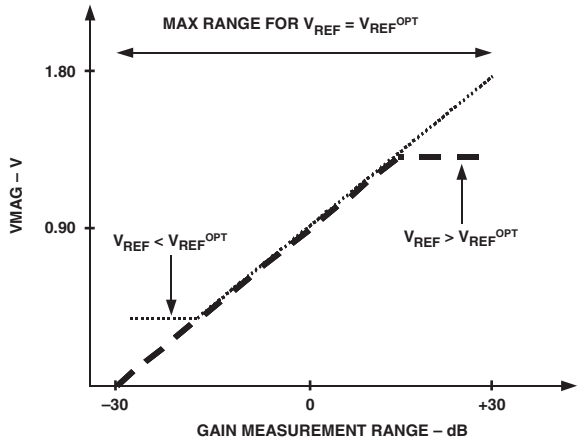


Figure 7. The Effect of Offsetting the Reference Level Is to Reduce the Maximum Dynamic Range

The phase measurement range is of 0° to 180°. For phase differences of 0° to –180°, the transfer characteristics are mirrored as shown in Figure 5, with a slope of the opposite sign. The phase detector responds to the relative position of the zero crossings between the two input channels. At higher frequencies, the finite rise and fall times of the amplitude limited inputs create an ambiguous situation that leads to inaccessible dead zones at the 0° and 180° limits. For maximum phase difference coverage, the reference phase difference should be set to 90°.

Cross Modulation of Magnitude and Phase

At high frequencies, unintentional cross coupling between signals in Channels A and B inevitably occurs due to on-chip and board-level parasitics. When the two signals presented to the AD8302 inputs are at very different levels, the cross coupling introduces cross modulation of the phase and magnitude responses. If the two signals are held at the same relative levels and the phase between them is modulated then only the phase output should respond. Due to phase-to-amplitude cross modulation, the magnitude output shows a residual response. A similar effect occurs when the relative phase is held constant while the magnitude difference is modulated, i.e., an expected magnitude response and a residual phase response are observed due to amplitude-to-phase cross modulation. The point where these effects are noticeable depends on the signal frequency and the magnitude of the difference. Typically, for differences <20 dB, the effects of cross modulation are negligible at 900 MHz.

Modifying the Slope and Center Point

The default slope and center point values can be modified with the addition of external resistors. Since the output interface blocks are generalized for both magnitude and phase functions, the scaling modification techniques are equally valid for both outputs. Figure 8 demonstrates how a simple voltage divider from the VMAG and VPHS pins to the MSET and PSET pins can be used to modify the slope. The increase in slope is given by 1 + R1/(R2‖20 kΩ). Note that it may be necessary to account for the MSET and PSET input impedance of 20 kΩ which has a ±20% manufacturing tolerance. As is generally true in such feedback systems, envelope bandwidth is decreased and the output noise transferred from the input is increased by the same factor. For example, by selecting R1 and R2 to be 10 kΩ and 20 kΩ, respectively, gain slope increases from the nominal 30 mV/dB by a factor of 2 to 60 mV/dB. The range is reduced by a factor of 2 and the new center point is at –15 dB, i.e., the range now extends from –30 dB, corresponding to V_{MAG} = 0 V, to 0 dB, corresponding to V_{MAG} = 1.8 V.

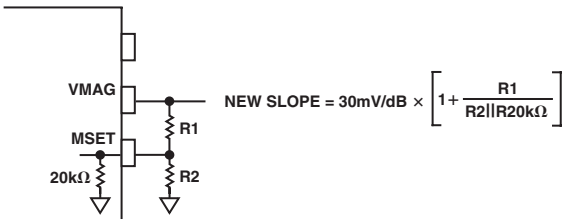


Figure 8. Increasing the Slope Requires the Inclusion of a Voltage Divider

Repositioning the center point back to its original value of 0 dB simply requires that an appropriate voltage be applied to the grounded side of the lower resistor in the voltage divider. This voltage may be provided externally or derived from the internal reference voltage on pin VREF. For the specific choice of R2 = 20 kΩ, the center point is easily readjusted to 0 dB by connecting the VREF pin directly to the lower pin of R2 as shown in Figure 9. The increase in slope is now simplified to 1 + R1/10 kΩ. Since this 1.80 V reference voltage is derived from the same band gap reference that determines the nominal center point, their tracking with temperature, supply, and part-to-part variations should be better in comparison to a fixed external voltage. If the center point is shifted to 0 dB in the previous example where the slope was doubled, then the range spans from –15 dB at V_{MAG} = 0 V to 15 dB at V_{MAG} = 1.8 V.

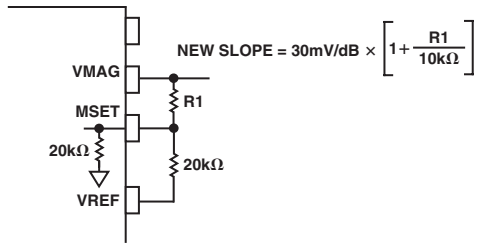


Figure 9. The Center Point Is Repositioned with the Help of the Internal Reference Voltage of 1.80 V

Comparator and Controller Modes

The AD8302 can also operate in a comparator mode if used in the arrangement shown in Figure 10 where the DUT is the element to be evaluated. The VMAG and VPHS pins are no longer connected to MSET and PSET. The trip-point thresholds for the gain and phase difference comparison are determined by the voltages applied to pins MSET and PSET according to:

$$V_{MSET}(V) = 30\ mV/dB \times Gain^{SP}(dB) + 900\ mV \quad (11)$$

$$V_{PSET}(V) = -10\ mV/^\circ \times \left(\left| Phase^{SP}(^\circ) \right| - 90^\circ \right) + 900\ mV \quad (12)$$

where $Gain^{SP}$ (dB) and $Phase^{SP}$ (°) are the desired gain and phase thresholds. If the actual gain and phase between the two input channels differ from these thresholds, the V_{MAG} and V_{PHS} outputs toggle like comparators, i.e.,

$$V_{MAG} = \begin{cases} 1.8\,V \text{ if } Gain > Gain^{SP} \\ 0\,V \text{ if } Gain < Gain^{SP} \end{cases} \quad (13)$$

$$V_{PHS} = \begin{cases} 1.8\,V \text{ if } Phase > Phase^{SP} \\ 0\,V \text{ if } Phase < Phase^{SP} \end{cases} \quad (14)$$

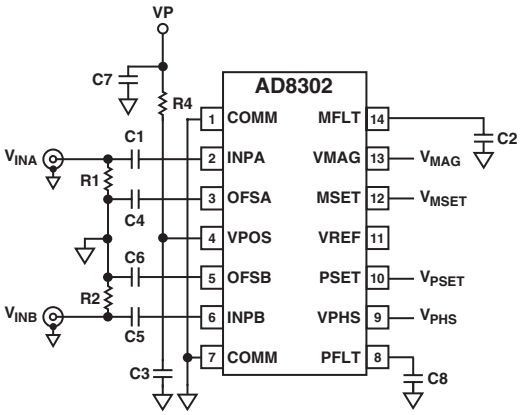


Figure 10. Disconnecting the Feedback to the Setpoint Controls, the AD8302 Operates in Comparator Mode

The comparator mode can be turned into a controller mode by closing the loop around the VMAG and VPHS outputs. Figure 11 illustrates a closed loop controller that stabilizes the gain and phase of a DUT with gain and phase adjustment elements. If VMAG and VPHS are properly conditioned to drive gain and phase adjustment blocks preceding the DUT, the actual gain and phase of the DUT will be forced toward the prescribed setpoint gain and phase given in Equations 11 and 12. These are essentially AGC and APC loops. Note that as with all control loops of this kind, loop dynamics and appropriate interfaces all must be considered in more detail.

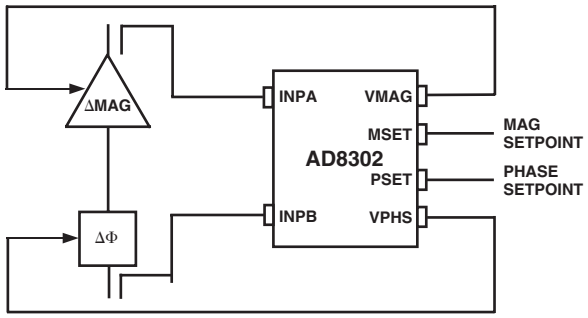


Figure 11. By Applying Overall Feedback to a DUT Via External Gain and Phase Adjusters, the AD8302 Acts as a Controller

APPLICATIONS

Measuring Amplifier Gain and Compression

The most fundamental application of AD8302 is the monitoring of the gain and phase response of a functional circuit block such as an amplifier or a mixer. As illustrated in Figure 12, directional couplers, DC_B and DC_A, sample the input and output signals of the "Black Box" DUT. The attenuators ensure that the signal levels presented to the AD8302 fall within its dynamic range. From the discussion in the Dynamic Range section, the optimal choice places both channels at P_{OPT} = –30 dBm referenced to 50 Ω, which corresponds to –43 dBV. To achieve this, the combination of coupling factor and attenuation are given by:

$$C_B + L_B = P_{IN} - P_{OPT} \quad (15)$$

$$C_A + L_A = P_{IN} + GAIN_{NOM} - P_{OPT} \quad (16)$$

where C_B and C_A are the coupling coefficients, L_B and L_A are the attenuation factors, and $GAIN_{NOM}$ is the nominal DUT gain. If identical couplers are used for both ports, then the difference in the two attenuators compensates for the nominal DUT gain. When the actual gain is nominal, the VMAG output is 900 mV, corresponding to 0 dB. Variations from nominal gain appear as a deviation from 900 mV or 0 dB with a 30 mV/dB scaling. Depending on the nominal insertion phase associated with DUT, the phase measurement may require a fixed phase shift in series with one of the channels to bring the nominal phase difference presented to the AD8302 near the optimal 90° point.

When the insertion phase is nominal, the VPHS output is 900 mV. Deviations from the nominal are reported with a 10 mV/degree scaling. Table I gives suggested component values for the measurement of an amplifier with a nominal gain of 10 dB and an input power of –10 dBm.

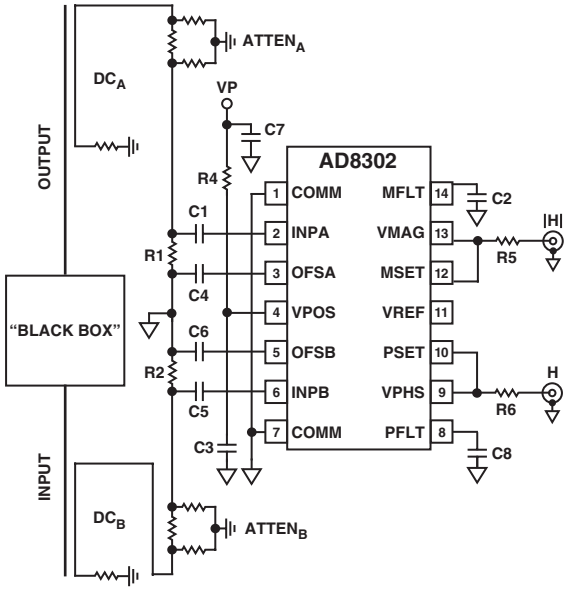


Figure 12. Using the AD8302 to Measure the Gain and Insertion Phase of an Amplifier or Mixer

Table I. Component Values for Measuring a 10 dB Amplifier with an Input Power of –10 dBm

Component	Value	Quantity
R1, R2	52.3 Ω	2
R5, R6	100 Ω	2
C1, C4, C5, C6	0.001 μF	4
C2, C8	Open	
C3	100 pF	1
C7	0.1 μF	1
AttenA	10 dB (See Text)	1
AttenB	1 dB (See Text)	1
DC_A, DC_B	20 dB	2

The gain measurement application can also monitor gain and phase distortion in the form of AM-AM (gain compression) and AM-PM conversion. In this case, the nominal gain and phase corresponds to those at low input signal levels. As the input level is increased, output compression and excess phase shifts are measured as deviations from the low level case. Note that the signal levels over which the input is swept must remain within the dynamic range of the AD8302 for proper operation.

Reflectometer

The AD8302 can be configured to measure the magnitude ratio and phase difference of signals that are incident on and reflected from a load. The vector reflection coefficient, Γ, is defined as,

$$\Gamma = \textit{Reflected Voltage} / \textit{Incident Voltage} = \left(Z_L - Z_O\right) / \left(Z_L + Z_O\right) \quad (17)$$

where Z_L is the complex load impedance and Z_O is the characteristic system impedance.

The measured reflection coefficient can be used to calculate the level of impedance mismatch or standing wave ratio (SWR) of a particular load condition. This proves particularly useful in diagnosing varying load impedances such as antennas that can degrade performance and even cause physical damage. The vector reflectometer arrangement given in Figure 13 consists of a pair of directional couplers that sample the incident and reflected signals. The attenuators reposition the two signal levels within the dynamic range of the AD8302. In analogy to Equations 15 and 16, the attenuation factors and coupling coefficients are given by:

$$C_B + L_B = P_{IN} - P_{OPT} \quad (18)$$

$$C_A + L_A = P_{IN} + \Gamma_{NOM} - P_{OPT} \quad (19)$$

where Γ_{NOM} is the nominal reflection coefficient in dB and is negative for passive loads. Consider the case where the incident signal is 10 dBm and the nominal reflection coefficient is –19 dB. As shown in Figure 13, using 20 dB couplers on both sides and –30 dBm for P_{OPT}, the attenuators for Channel A and B paths are 1 dB and 20 dB, respectively. The magnitude and phase of the reflection coefficient are available at the VMAG and VPHS pins scaled to 30 mV/dB and 10 mV/degree. When Γ is –19 dB, the VMAG output is 900 mV.

The measurement accuracy can be compromised if board level details are not addressed. Minimize the physical distance between the series connected couplers since the extra path length adds phase error to Γ. Keep the paths from the couplers to the AD8302 as well matched as possible since any differences introduce measurement errors. The finite directivity, D, of the couplers sets the minimum detectable reflection coefficient, i.e., $|\Gamma_{MIN}(\text{dB})| < |\text{D}(\text{dB})|$.

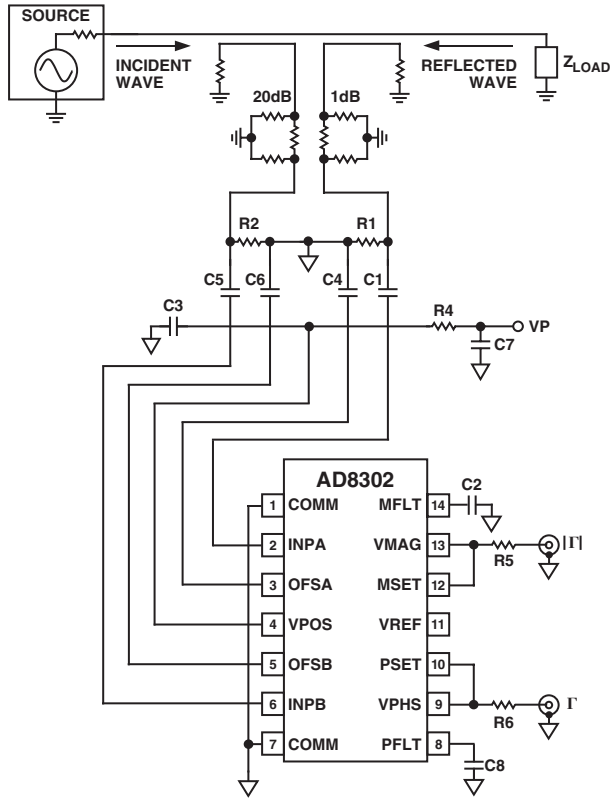


Figure 13. Using the AD8302 to Measure the Vector Reflection Coefficient Off an Arbitrary Load

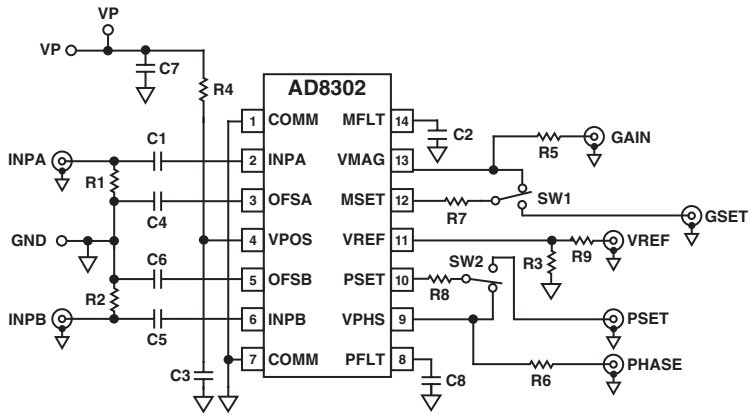


Figure 14. Evaluation Board Schematic

Table II. P1 Pin Allocations

1	Common
2	VPOS
3	Common

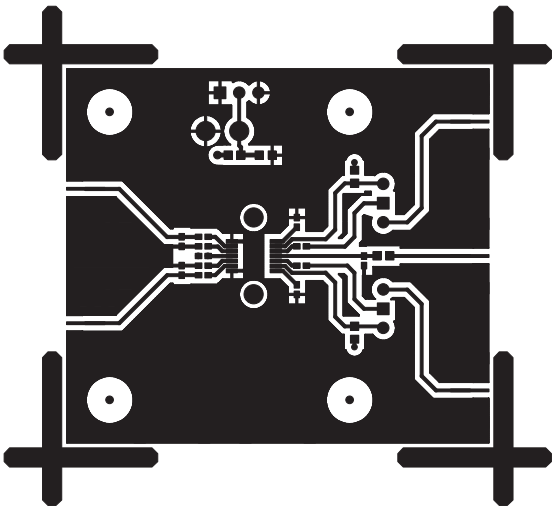


Figure 15a. Component Side Metal of Evaluation Board

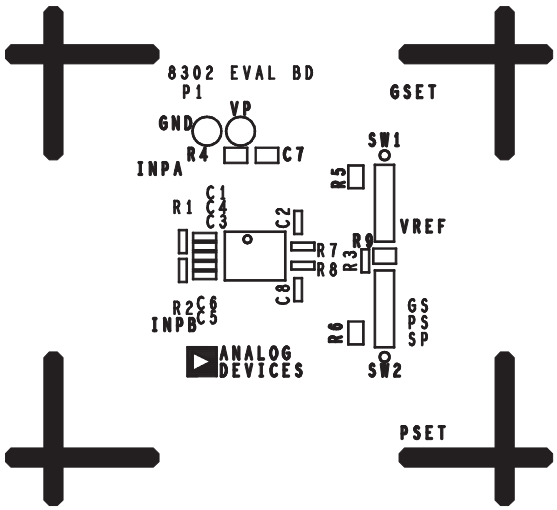


Figure 15b. Component Side Silkscreen of Evaluation Board

Table III. Evaluation Board Configuration Options

Component	Function	Default Condition
P1	Power Supply and Ground Connector: Pin 2 VPOS and Pins 1 and 3 Ground.	Not Applicable
R1, R2	Input Termination. Provide termination for input sources.	R1 = R2 = 52.3 Ω (Size 0402)
R3	VREF Output Load. This load is optional and is meant to allow the user to simulate their circuit loading of the device.	R3 = 1 kΩ (Size 0603)
R5, R6, R9	Snubbing Resistor	R5 = R6 = 0 Ω (Size 0603) R9 = 0 Ω (Size 0603)
C3, C7, R4	Supply Decoupling	C3 = 100 pF (Size 0603) C7 = 0.1 µF (Size 0603) R4 = 0 Ω (Size 0603)
C1, C5	Input AC-Coupling Capacitors	C1 = C5 = 1 nF (Size 0603)
C2, C8	Video Filtering. C2 and C8 limit the video bandwidth of the gain and phase output respectively.	C2 = C8 = Open (Size 0603)
C4, C6	Offset Feedback. These set the high-pass corner of the offset cancellation loop and thus with the input ac-coupling capacitors the minimum operating frequency.	C4 = C6 = 1 nF (Size 0603)
SW1	GSET Signal Source. When SW1 is in the position shown, the device is in gain measure mode; when switched, it operates in comparator mode and a signal must be applied to GSET.	SW1 = Installed
SW2	PSET Signal Source. When SW2 is in the position shown, the device is in phase measure mode; when switched, it operates in comparator mode and a signal must be applied to PSET.	SW1 = Installed

CHARACTERIZATION SETUPS AND METHODS

The general hardware configuration used for most of the AD8302 characterization is shown in Figure 16. The characterization board is similar to the Customer Evaluation Board. Two reference-locked R and S SMT03 signal generators are used as the inputs to INPA and INPB, while the gain and phase outputs are monitored using both a TDS 744A oscilloscope with 10× high impedance probes and Agilent 34401A multimeters.

Gain

The basic technique used to evaluate the static gain (VMAG) performance was to set one source to a fixed level and sweep the amplitude of the other source, while measuring the VMAG output with the DMM. In practice, the two sources were run at 100 kHz frequency offset and average output measured with the DMM to alleviate errors that might be induced by gain/phase modulation due to phase jitter between the two sources.

The errors stated are the difference between a best fit line calculated by a linear regression and the actual measured data divided by the slope of the line to give an error in V/dB. The referred to 25°C error uses this same method while always using the slope and intercept calculated for that device at 25°C.

Response measurement made of the VMAG output used the configuration shown in Figure 17. The variable attenuator, Alpha AD260, is driven with a HP8112A pulse generator producing a change in RF level within 10 ns.

Noise spectral density measurements were made using a HP3589A with the inputs delivered through a Narda 4032C 90° phase splitter.

To measure the modulation of VMAG due to phase variation again the sources were run at a frequency offset, f_{OS}, effectively creating a continuous linear change in phase going through 360° once every $1/f_{OS}$ seconds. The VMAG output is then measured with a DSO. When perceivable, only at high frequencies and large input magnitude differences, the linearly ramping phase creates a near sinusoid output riding on the expected VMAG dc output level. The curves in TPC 24 show the peak-to-peak output level measured with averaging.

Phase

The majority of the VPHS output data was collected by generating phase change, again by operating the two input sources with a small frequency offset (normally 100 kHz) using the same configuration shown in Figure 16. Although this method gives excellent linear phase change, good for measurement of slope and linearity, it lacks an absolute phase reference point. In the curves showing swept phase, the phase at which the VPHS is the same as VPHS with no input signal is taken to be –90° and all other angles are references to there. Typical Performance Curves show two figures of merit; instantaneous slope and error. Instantaneous slope, as shown in TPCs 43, 44, 45, and 47, was calculated simply by taking the delta in VPHS over angular change for adjacent measurement points.

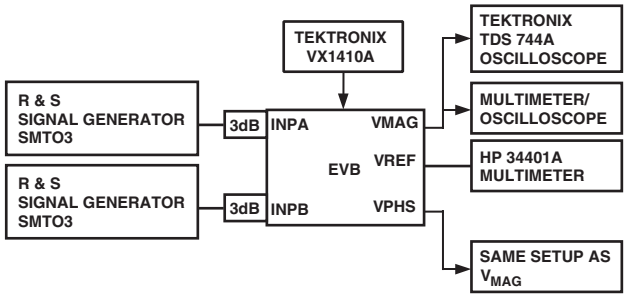


Figure 16. Primary Characterization Setup

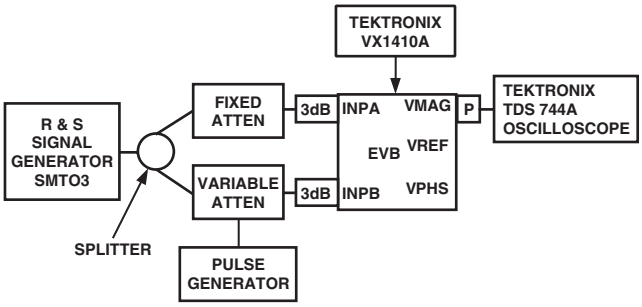


Figure 17. VMAG Dynamic Performance Measurement Setup

OUTLINE DIMENSIONS

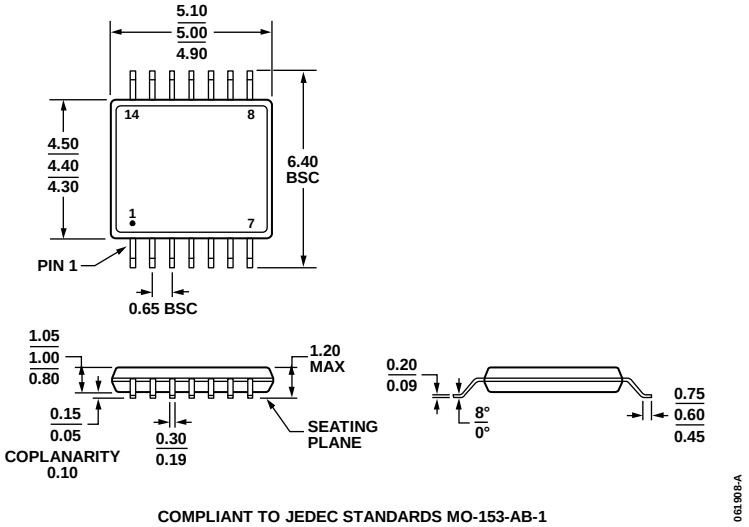


Figure 18. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8302ARUZ	−40°C to +85°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
AD8302ARUZ-REEL	−40°C to +85°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
AD8302ARUZ-RL7	−40°C to +85°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
AD8302-EVALZ			

[1] Z = RoHS Compliant Part.

REVISION HISTORY

4/2018—Rev. A to Rev. B

Updated Outline Dimensions.....23
Moved Ordering Guide 23
Changes to Ordering Guide.....23

7/2002—Rev. 0 to Rev. A.

TPC 3 Through TPC 6 Replaced 6

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D02492-0-4/18(B)