

FEATURES

True single-supply operation

Input voltage range extends below ground

Output swings rail-to-rail

Single-supply capability from 5 V to 30 V

Dual-supply capability from ± 2.5 V to ± 15 V

High load drive

Capacitive load drive of 350 pF, $G = +1$

Minimum output current of 15 mA

Excellent ac performance for low power

800 μ A maximum quiescent current per amplifier

Unity-gain bandwidth: 1.8 MHz

Slew rate of 3 V/ μ s

Good dc performance

800 μ V maximum input offset voltage

2 μ V/ $^{\circ}$ C typical offset voltage drift

25 pA maximum input bias current

Low noise

13 nV/ $\sqrt{\text{Hz}}$ @ 10 kHz

No phase inversion

ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications (AQEC standard)

Military temperature range (-55°C to $+125^{\circ}\text{C}$)

Controlled manufacturing baseline

One assembly/test site

One fabrication site

Enhanced product change notification

Qualification data available on request

APPLICATIONS

Photodiode preamps

Active filters

12-bit to 14-bit data acquisition systems

Low power references and regulators

CONNECTION DIAGRAM

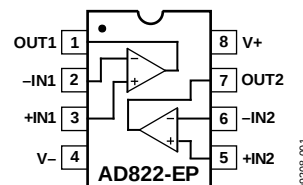


Figure 1. 8-Lead SOIC_N (R Suffix)

GENERAL DESCRIPTION

The AD822-EP is a dual precision, low power FET input op amp that can operate from a single supply of 5 V to 30 V or dual supplies of ± 2.5 V to ± 15 V. It has true single-supply capability with an input voltage range extending below the negative rail, allowing the AD822 to accommodate input signals below ground in the single-supply mode. Output voltage swing extends to within 10 mV of each rail, providing the maximum output dynamic range.

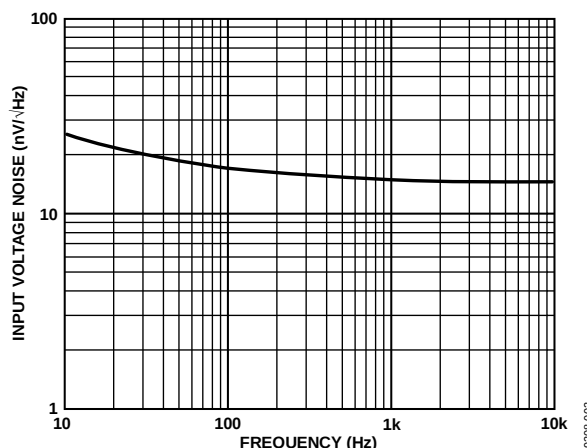


Figure 2. Input Voltage Noise vs. Frequency

Offset voltage of 800 μ V maximum, offset voltage drift of 2 μ V/ $^{\circ}$ C, input bias currents below 25 pA, and low input voltage noise provide dc precision with source impedances up to a gigaohm. The 1.8 MHz unity-gain bandwidth, -93 dB THD at 10 kHz, and 3 V/ μ s slew rate are provided with a low supply current of 800 μ A per amplifier.

Rev. 0

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REVISION HISTORY

6/10—Revision 0: Initial Version

The AD822-EP drives up to 350 pF of direct capacitive load as a follower and provides a minimum output current of 15 mA. This allows the amplifier to handle a wide range of load conditions. Its combination of ac and dc performance, plus the outstanding load drive capability, results in an exceptionally versatile amplifier for the single-supply user.

The AD822-EP operates over the military temperature range of -55°C to $+125^{\circ}\text{C}$.

The AD822-EP is offered in an 8-lead SOIC_N package.

Full details about this enhanced product are available in the [AD822](#) data sheet, which should be consulted in conjunction with this data sheet.

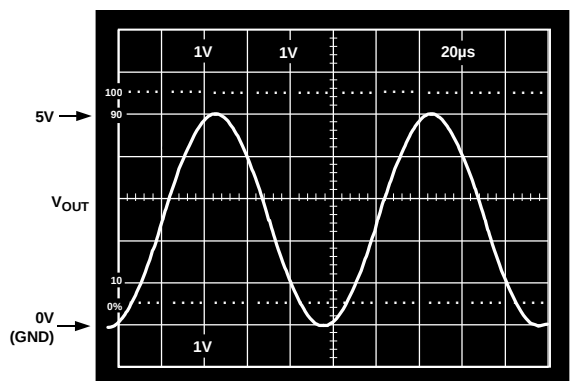


Figure 3. Gain-of-2 Amplifier; $V_S = 5\text{ V}$, 0 V , $V_{IN} = 2.5\text{ V}$ Sine Centered at 1.25 V , $R_L = 100\ \Omega$

SPECIFICATIONS

$V_S = 0\text{ V}$, 5 V @ $T_A = 25^\circ\text{C}$, $V_{CM} = 0\text{ V}$, $V_{OUT} = 0.2\text{ V}$, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	T Grade			Unit	
		Min	Typ	Max		
DC PERFORMANCE						
Initial Offset	$V_{CM} = 0\text{ V to }4\text{ V}$		0.1	0.8	mV	
Maximum Offset Over Temperature			0.5	1.2	mV	
Offset Drift			2		$\mu\text{V}/^{\circ}\text{C}$	
Input Bias Current			2	25	pA	
At T_{MAX}			0.5	6	nA	
Input Offset Current			2	20	pA	
At T_{MAX}			0.5		nA	
Open-Loop Gain	$V_{OUT} = 0.2\text{ V to }4\text{ V}$					
	$R_L = 100\text{ k}\Omega$	500	1000		V/mV	
T_{MIN} to T_{MAX}		400			V/mV	
	$R_L = 10\text{ k}\Omega$	80	150		V/mV	
T_{MIN} to T_{MAX}		80			V/mV	
	$R_L = 1\text{ k}\Omega$	15	30		V/mV	
T_{MIN} to T_{MAX}		10			V/mV	
NOISE/HARMONIC PERFORMANCE						
Input Voltage Noise	$R_L = 10\text{ k}\Omega$ to 2.5 V $V_{OUT} = 0.25\text{ V to }4.75\text{ V}$					
f = 0.1 Hz to 10 Hz			2		$\mu\text{V p-p}$	
f = 10 Hz			25		$\text{nV}/\sqrt{\text{Hz}}$	
f = 100 Hz			21		$\text{nV}/\sqrt{\text{Hz}}$	
f = 1 kHz			16		$\text{nV}/\sqrt{\text{Hz}}$	
f = 10 kHz			13		$\text{nV}/\sqrt{\text{Hz}}$	
Input Current Noise						
f = 0.1 Hz to 10 Hz				18		fA p-p
f = 1 kHz				0.8		$\text{fA}/\sqrt{\text{Hz}}$
Harmonic Distortion						
f = 10 kHz			-93		dB	
DYNAMIC PERFORMANCE						
Unity-Gain Frequency	$V_{OUT}\text{ p-p} = 4.5\text{ V}$		1.8		MHz	
Full Power Response			210		kHz	
Slew Rate			3		V/ μs	
Settling Time						
To 0.1%	$V_{OUT} = 0.2\text{ V to }4.5\text{ V}$		1.4		μs	
To 0.01%	$V_{OUT} = 0.2\text{ V to }4.5\text{ V}$		1.8		μs	
MATCHING CHARACTERISTICS						
Initial Offset	$R_L = 5\text{ k}\Omega$ $R_L = 5\text{ k}\Omega$			1.0	mV	
Maximum Offset Over Temperature				1.6	mV	
Offset Drift			3		$\mu\text{V}/^{\circ}\text{C}$	
Input Bias Current				20	pA	
Crosstalk @ f = 1 kHz			-130		dB	
Crosstalk @ f = 100 kHz			-93		dB	

Parameter	Test Conditions/Comments	T Grade			Unit
		Min	Typ	Max	
INPUT CHARACTERISTICS					
Input Voltage Range ¹ , T _{MIN} to T _{MAX}		−0.2		+4	V
Common-Mode Rejection Ratio (CMRR)	V _{CM} = 0 V to 2 V	66	80		dB
T _{MIN} to T _{MAX}	V _{CM} = 0 V to 2 V	66			dB
Input Impedance					
Differential			10 ¹³ 0.5		Ω pF
Common Mode			10 ¹³ 2.8		Ω pF
OUTPUT CHARACTERISTICS					
Output Saturation Voltage ²					
V _{OL} − V _{EE}	I _{SINK} = 20 μA		5	7	mV
T _{MIN} to T _{MAX}				10	mV
V _{CC} − V _{OH}	I _{SOURCE} = 20 μA		10	14	mV
T _{MIN} to T _{MAX}				20	mV
V _{OL} − V _{EE}	I _{SINK} = 2 mA		40	55	mV
T _{MIN} to T _{MAX}				80	mV
V _{CC} − V _{OH}	I _{SOURCE} = 2 mA		80	110	mV
T _{MIN} to T _{MAX}				160	mV
V _{OL} − V _{EE}	I _{SINK} = 15 mA		300	500	mV
T _{MIN} to T _{MAX}				1000	mV
V _{CC} − V _{OH}	I _{SOURCE} = 15 mA		800	1500	mV
T _{MIN} to T _{MAX}				1900	mV
Operating Output Current		15			mA
T _{MIN} to T _{MAX}		12			mA
Capacitive Load Drive			350		pF
POWER SUPPLY					
Quiescent Current, T _{MIN} to T _{MAX}			1.24	1.6	mA
Power Supply Rejection	V+ = 5 V to 15 V	66	80		dB
T _{MIN} to T _{MAX}		66			dB

¹ This is a functional specification. Amplifier bandwidth decreases when the input common-mode voltage is driven in the range $(V_{+} - 1\text{ V})$ to V_{+} . Common-mode error voltage is typically less than 5 mV with the common-mode voltage set at 1 V below the positive supply.

² $V_{OL} - V_{EE}$ is defined as the difference between the lowest possible output voltage (V_{OL}) and the negative voltage supply rail (V_{EE}). $V_{CC} - V_{OH}$ is defined as the difference between the highest possible output voltage (V_{OH}) and the positive supply voltage (V_{CC}).

AD822-EP

$V_S = \pm 5\text{ V}$ @ $T_A = 25^\circ\text{C}$, $V_{CM} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	T Grade			Unit
		Min	Typ	Max	
DC PERFORMANCE					
Initial Offset	$V_{CM} = -5\text{ V to }+4\text{ V}$		0.1	0.8	mV
Maximum Offset Over Temperature			0.5	1.5	mV
Offset Drift			2		$\mu\text{V}/^{\circ}\text{C}$
Input Bias Current			2	25	pA
At T_{MAX}			0.5	6	nA
Input Offset Current			2	20	pA
At T_{MAX}			0.5	nA	
Open-Loop Gain	$V_{OUT} = -4\text{ V to }+4\text{ V}$				
	$R_L = 100\text{ k}\Omega$	400	1000		V/mV
T_{MIN} to T_{MAX}		400			V/mV
	$R_L = 10\text{ k}\Omega$	80	150		V/mV
T_{MIN} to T_{MAX}		80			V/mV
	$R_L = 1\text{ k}\Omega$	20	30		V/mV
T_{MIN} to T_{MAX}		10			V/mV
NOISE/HARMONIC PERFORMANCE					
Input Voltage Noise	$R_L = 10\text{ k}\Omega$ $V_{OUT} = \pm 4.5\text{ V}$				
f = 0.1 Hz to 10 Hz			2		$\mu\text{V p-p}$
f = 10 Hz			25		$\text{nV}/\sqrt{\text{Hz}}$
f = 100 Hz			21		$\text{nV}/\sqrt{\text{Hz}}$
f = 1 kHz			16		$\text{nV}/\sqrt{\text{Hz}}$
f = 10 kHz			13		$\text{nV}/\sqrt{\text{Hz}}$
Input Current Noise					
f = 0.1 Hz to 10 Hz			18		fA p-p
f = 1 kHz			0.8		fA/ $\sqrt{\text{Hz}}$
Harmonic Distortion					
f = 10 kHz			-93		dB
DYNAMIC PERFORMANCE					
Unity-Gain Frequency	$V_{OUT\text{ p-p}} = 9\text{ V}$		1.9		MHz
Full Power Response			105		kHz
Slew Rate			3		V/ μs
Settling Time	$V_{OUT} = 0\text{ V to } \pm 4.5\text{ V}$ $V_{OUT} = 0\text{ V to } \pm 4.5\text{ V}$				
to 0.1%			1.4		μs
to 0.01%			1.8		μs
MATCHING CHARACTERISTICS					
Initial Offset	$R_L = 5\text{ k}\Omega$ $R_L = 5\text{ k}\Omega$			1.0	mV
Maximum Offset Over Temperature				3	mV
Offset Drift			3		$\mu\text{V}/^{\circ}\text{C}$
Input Bias Current				25	pA
Crosstalk @ f = 1 kHz			-130		dB
Crosstalk @ f = 100 kHz			-93		dB
INPUT CHARACTERISTICS					
Input Voltage Range ¹ , T_{MIN} to T_{MAX}	$V_{CM} = -5\text{ V to }+2\text{ V}$ $V_{CM} = -5\text{ V to }+2\text{ V}$	-5.2		+4	V
Common-Mode Rejection Ratio (CMRR)		66	80		dB
T_{MIN} to T_{MAX}		66			dB
Input Impedance					
Differential			$10^{13} 0.5$		ΩpF
Common Mode			$10^{13} 2.8$	ΩpF	

Parameter	Test Conditions/Comments	T Grade			Unit
		Min	Typ	Max	
OUTPUT CHARACTERISTICS					
Output Saturation Voltage ²					
$V_{OL} - V_{EE}$ T_{MIN} to T_{MAX}	$I_{SINK} = 20\ \mu A$		5	7	mV
$V_{CC} - V_{OH}$ T_{MIN} to T_{MAX}	$I_{SOURCE} = 20\ \mu A$		10	14	mV
$V_{OL} - V_{EE}$ T_{MIN} to T_{MAX}	$I_{SINK} = 2\ mA$		40	55	mV
$V_{CC} - V_{OH}$ T_{MIN} to T_{MAX}	$I_{SOURCE} = 2\ mA$		80	110	mV
$V_{OL} - V_{EE}$ T_{MIN} to T_{MAX}	$I_{SINK} = 15\ mA$		300	500	mV
$V_{CC} - V_{OH}$ T_{MIN} to T_{MAX}	$I_{SOURCE} = 15\ mA$		800	1500	mV
Operating Output Current T_{MIN} to T_{MAX}		15 12			mA mA
Capacitive Load Drive			350	1900	pF
POWER SUPPLY					
Quiescent Current, T_{MIN} to T_{MAX}			1.3	1.6	mA
Power Supply Rejection T_{MIN} to T_{MAX}	$V_{SY} = \pm 5\ V$ to $\pm 15\ V$	66 66	80		dB dB

¹ This is a functional specification. Amplifier bandwidth decreases when the input common-mode voltage is driven in the range ($V_+ - 1 V$) to V_+ . Common-mode error voltage is typically less than 5 mV with the common-mode voltage set at 1 V below the positive supply.

² $V_{OL} - V_{EE}$ is defined as the difference between the lowest possible output voltage (V_{OL}) and the negative voltage supply rail (V_{EE}). $V_{CC} - V_{OH}$ is defined as the difference between the highest possible output voltage (V_{OH}) and the positive supply voltage (V_{CC}).

AD822-EP

$V_S = \pm 15\text{ V}$ @ $T_A = 25^\circ\text{C}$, $V_{CM} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	T Grade			Unit
		Min	Typ	Max	
DC PERFORMANCE					
Initial Offset			0.4	2	mV
Maximum Offset Over Temperature			0.5	3	mV
Offset Drift			2		μV/°C
Input Bias Current	V _{CM} = 0 V		2	25	pA
	V _{CM} = −10 V		40		pA
At T _{MAX}	V _{CM} = 0 V		0.5	6	nA
Input Offset Current			2	20	pA
At T _{MAX}			0.5		nA
Open-Loop Gain	V _{OUT} = −10 V to +10 V				
	R _L = 100 kΩ	500	2000		V/mV
T _{MIN} to T _{MAX}		500			V/mV
	R _L = 10 kΩ	100	500		V/mV
T _{MIN} to T _{MAX}		100			V/mV
	R _L = 1 kΩ	30	45		V/mV
T _{MIN} to T _{MAX}		20			V/mV
NOISE/HARMONIC PERFORMANCE					
Input Voltage Noise					
f = 0.1 Hz to 10 Hz			2		μV p-p
f = 10 Hz			25		nV/√Hz
f = 100 Hz			21		nV/√Hz
f = 1 kHz			16		nV/√Hz
f = 10 kHz			13		nV/√Hz
Input Current Noise					
f = 0.1 Hz to 10 Hz			18		fA p-p
f = 1 kHz			0.8		fA/√Hz
Harmonic Distortion	R _L = 10 kΩ				
f = 10 kHz	V _{OUT} = ±10 V		−85		dB
DYNAMIC PERFORMANCE					
Unity-Gain Frequency			1.9		MHz
Full Power Response	V _{OUT} p-p = 20 V		45		kHz
Slew Rate			3		V/μs
Settling Time					
to 0.1%	V _{OUT} = 0 V to ±10 V		4.1		μs
to 0.01%	V _{OUT} = 0 V to ±10 V		4.5		μs
MATCHING CHARACTERISTICS					
Initial Offset				3	mV
Maximum Offset Over Temperature				4	mV
Offset Drift			3		μV/°C
Input Bias Current				25	pA
Crosstalk @ f = 1 kHz	R _L = 5 kΩ		−130		dB
Crosstalk @ f = 100 kHz	R _L = 5 kΩ		−93		dB
INPUT CHARACTERISTICS					
Input Voltage Range ¹ , T _{MIN} to T _{MAX}		−15.2		+14	V
Common-Mode Rejection Ratio (CMRR)	V _{CM} = −15 V to +12 V	70	80		dB
T _{MIN} to T _{MAX}	V _{CM} = −15 V to +12 V	70			dB
Input Impedance					
Differential			10 ¹³ 0.5		Ω pF
Common Mode			10 ¹³ 2.8		Ω pF

Parameter	Test Conditions/Comments	Min	T Grade Typ	Max	Unit
OUTPUT CHARACTERISTICS					
Output Saturation Voltage ²					
V _{OL} – V _{EE}	I _{SINK} = 20 μA		5	7	mV
T _{MIN} to T _{MAX}				10	mV
V _{CC} – V _{OH}	I _{SOURCE} = 20 μA		10	14	mV
T _{MIN} to T _{MAX}				20	mV
V _{OL} – V _{EE}	I _{SINK} = 2 mA		40	55	mV
T _{MIN} to T _{MAX}				80	mV
V _{CC} – V _{OH}	I _{SOURCE} = 2 mA		80	110	mV
T _{MIN} to T _{MAX}				160	mV
V _{OL} – V _{EE}	I _{SINK} = 15 mA		300	500	mV
T _{MIN} to T _{MAX}				1000	mV
V _{CC} – V _{OH}	I _{SOURCE} = 15 mA		800	1500	mV
T _{MIN} to T _{MAX}				1900	mV
Operating Output Current		20			mA
T _{MIN} to T _{MAX}		15			mA
Capacitive Load Drive			350		pF
POWER SUPPLY					
Quiescent Current, T _{MIN} to T _{MAX}			1.4	1.8	mA
Power Supply Rejection	V _{SY} = ±5 V to ±15 V	70	80		dB
T _{MIN} to T _{MAX}		70			dB

¹ This is a functional specification. Amplifier bandwidth decreases when the input common-mode voltage is driven in the range ($V_+ - 1 \text{ V}$) to V_+ . Common-mode error voltage is typically less than 5 mV with the common-mode voltage set at 1 V below the positive supply.

² $V_{OL} - V_{EE}$ is defined as the difference between the lowest possible output voltage (V_{OL}) and the negative voltage supply rail (V_{EE}). $V_{CC} - V_{OH}$ is defined as the difference between the highest possible output voltage (V_{OH}) and the positive supply voltage (V_{CC}).

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	$\pm 18\text{ V}$
Internal Power Dissipation 8-Lead SOIC_N (R)	Observe Maximum Junction Temperature
Input Voltage	$((V+) + 0.2\text{ V})$ to $((V-) - 20\text{ V})$
Output Short-Circuit Duration	Indefinite
Differential Input Voltage	$\pm 30\text{ V}$
Storage Temperature Range (R)	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	-55°C to $+125^{\circ}\text{C}$
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 60 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-lead SOIC_N (R)	160	43	$^{\circ}\text{C}/\text{W}$

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

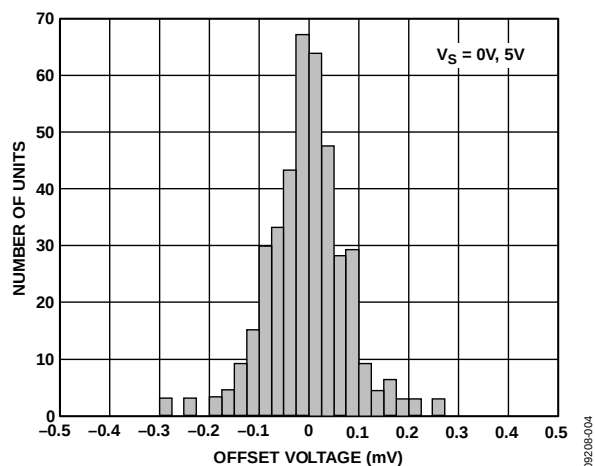


Figure 4. Typical Distribution of Offset Voltage (390 Units)

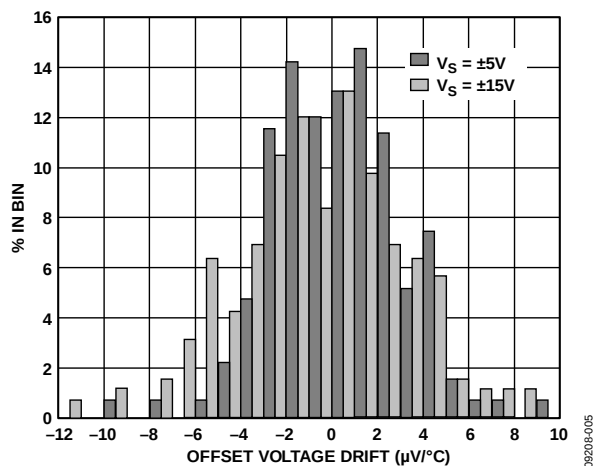


Figure 5. Typical Distribution of Offset Voltage Drift (100 Units)

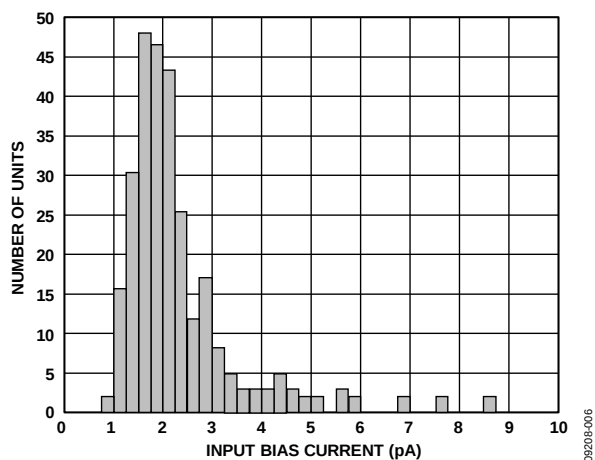


Figure 6. Typical Distribution of Input Bias Current (213 Units)

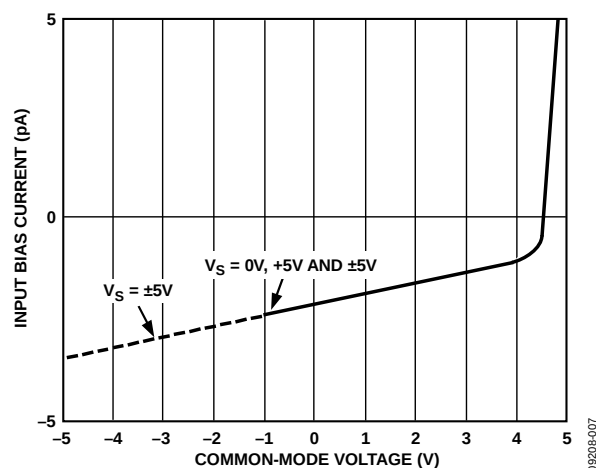


Figure 7. Input Bias Current vs. Common-Mode Voltage; $V_S = 5V, 0V$, and $V_S = \pm 5V$

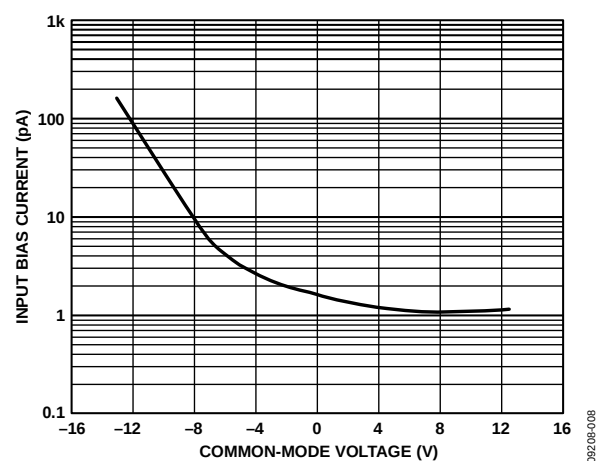


Figure 8. Input Bias Current vs. Common-Mode Voltage; $V_S = \pm 15V$

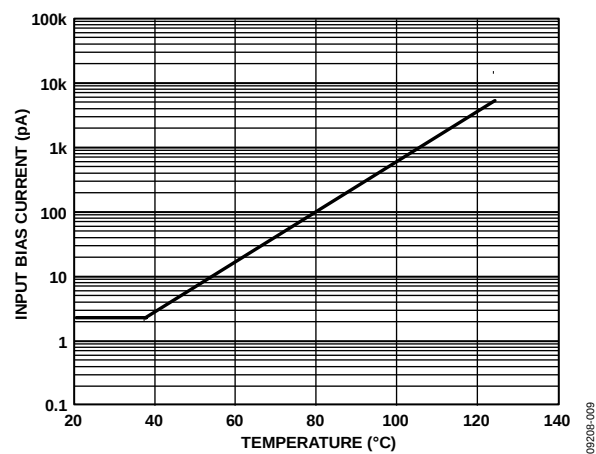


Figure 9. Input Bias Current vs. Temperature; $V_S = 5V, V_{CM} = 0V$

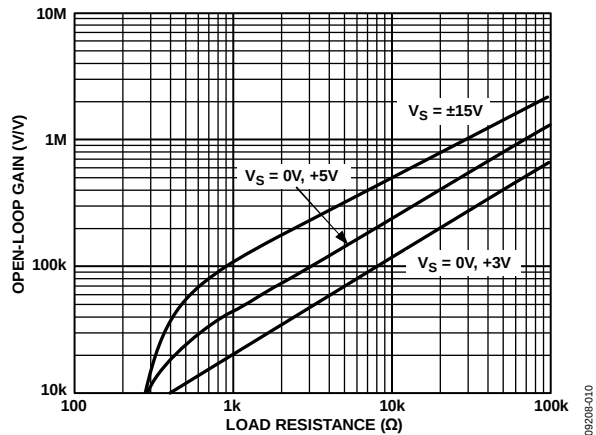


Figure 10. Open-Loop Gain vs. Load Resistance

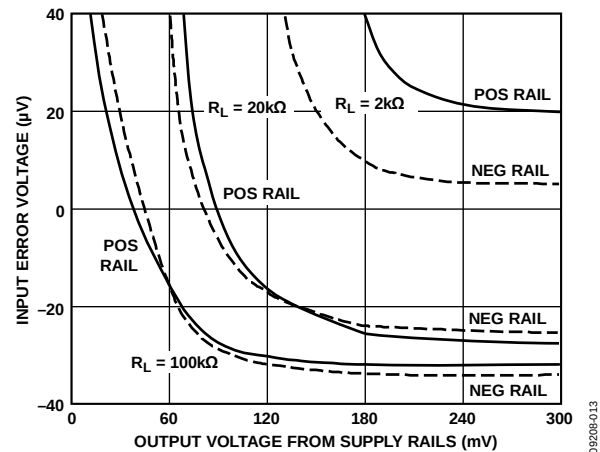


Figure 13. Input Error Voltage with Output Voltage Within 300 mV of Either Supply Rail for Various Resistive Loads; $V_S = \pm 5\text{ V}$

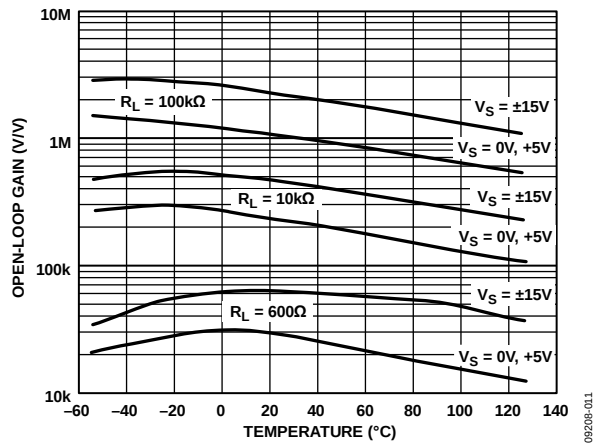


Figure 11. Open-Loop Gain vs. Temperature

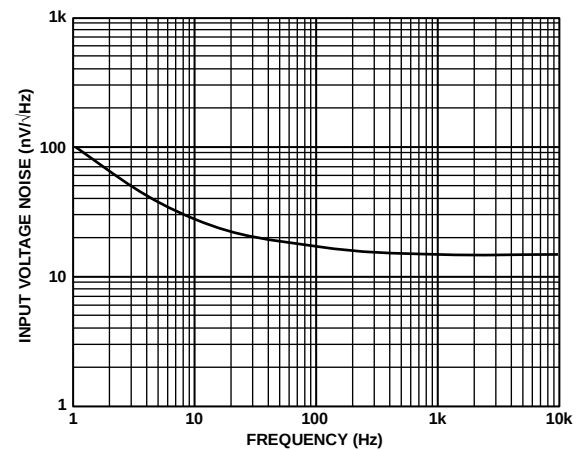


Figure 14. Input Voltage Noise vs. Frequency

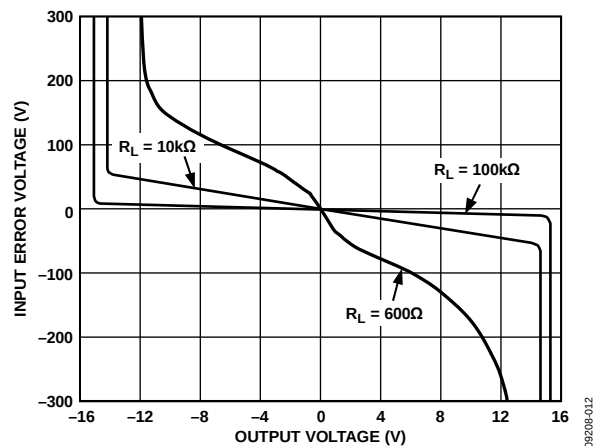


Figure 12. Input Error Voltage vs. Output Voltage for Resistive Loads

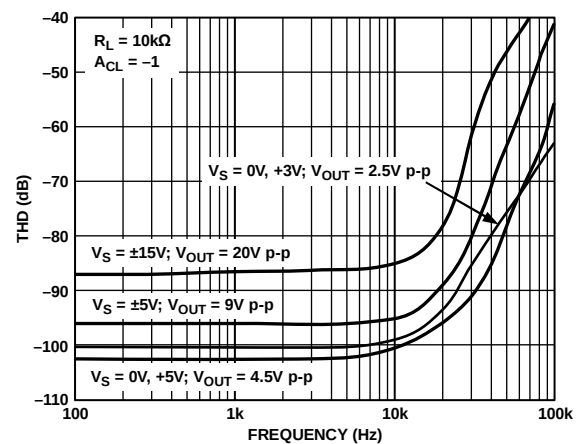


Figure 15. Total Harmonic Distortion (THD) vs. Frequency

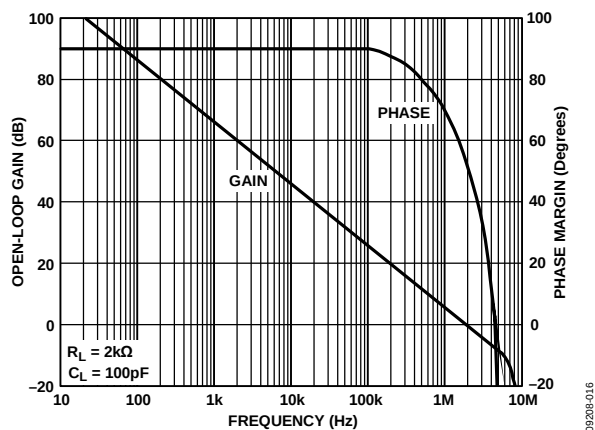


Figure 16. Open-Loop Gain and Phase Margin vs. Frequency

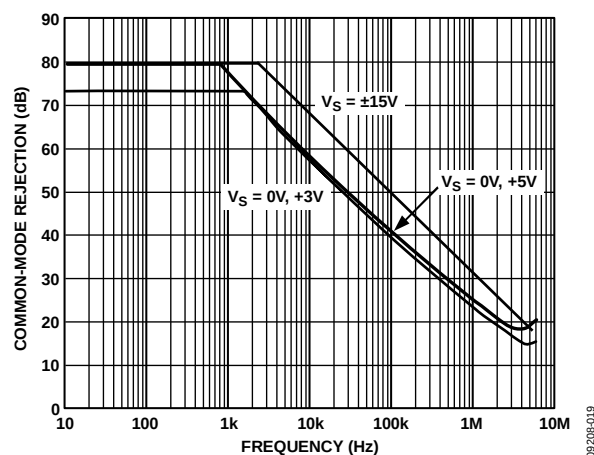


Figure 19. Common-Mode Rejection vs. Frequency

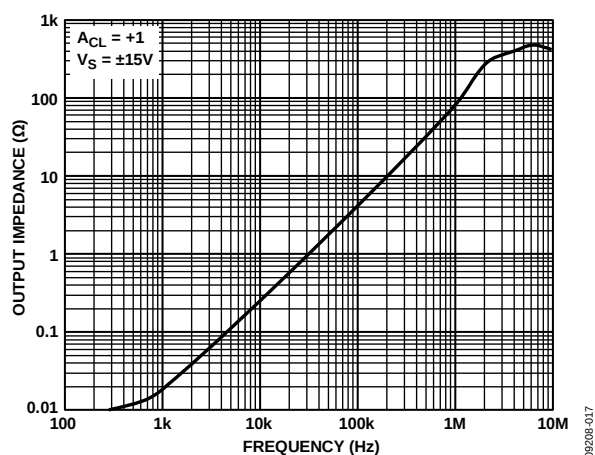


Figure 17. Output Impedance vs. Frequency

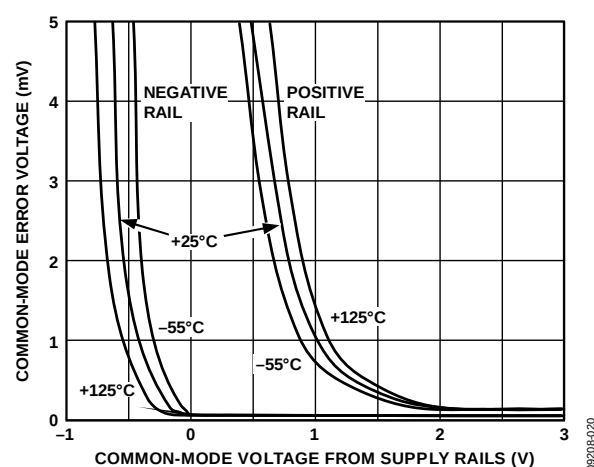


Figure 20. Absolute Common-Mode Error vs. Common-Mode Voltage from Supply Rails ($V_S - V_{CM}$)

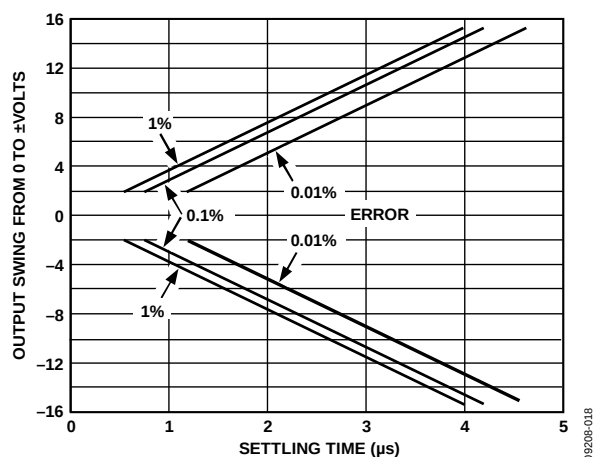


Figure 18. Output Swing and Error vs. Settling Time

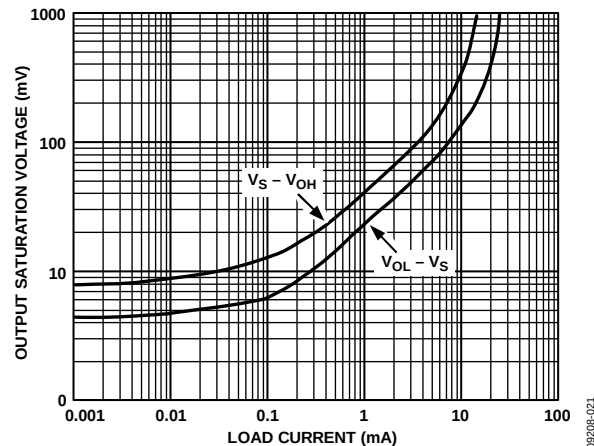


Figure 21. Output Saturation Voltage vs. Load Current

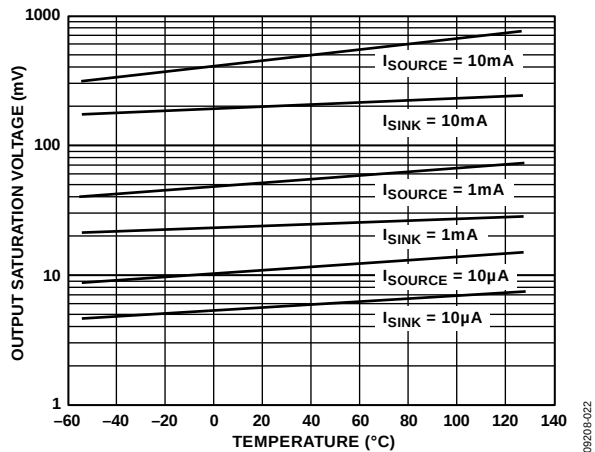


Figure 22. Output Saturation Voltage vs. Temperature

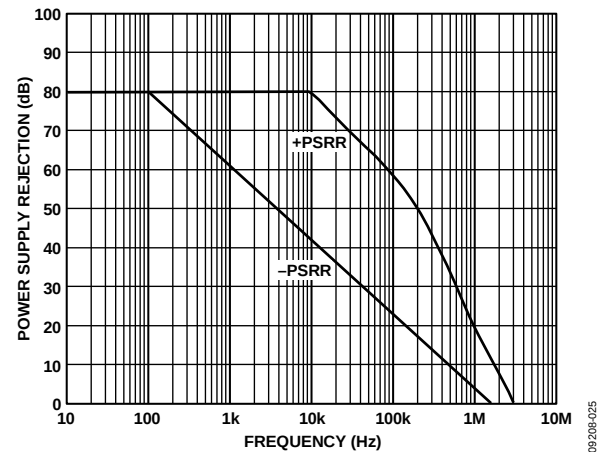


Figure 25. Power Supply Rejection vs. Frequency

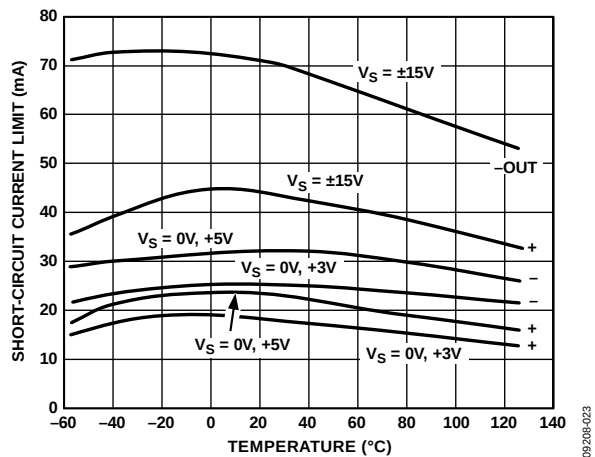


Figure 23. Short-Circuit Current Limit vs. Temperature

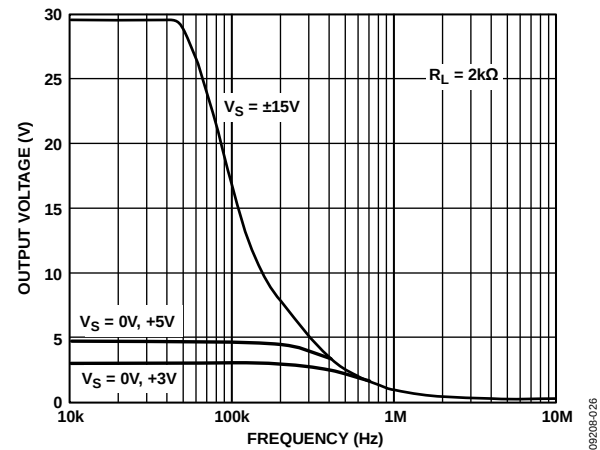


Figure 26. Large Signal Frequency Response

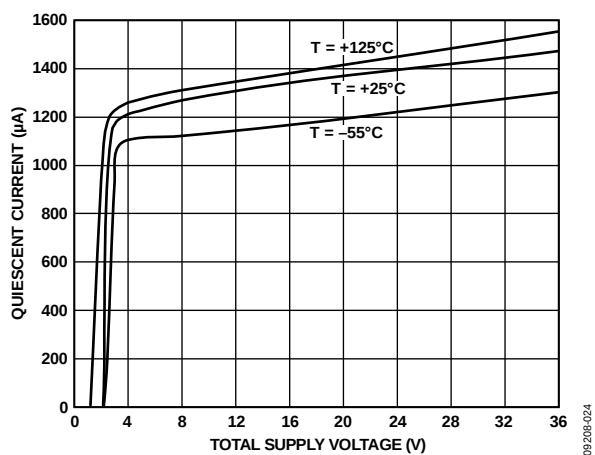


Figure 24. Quiescent Current vs. Supply Voltage vs. Temperature

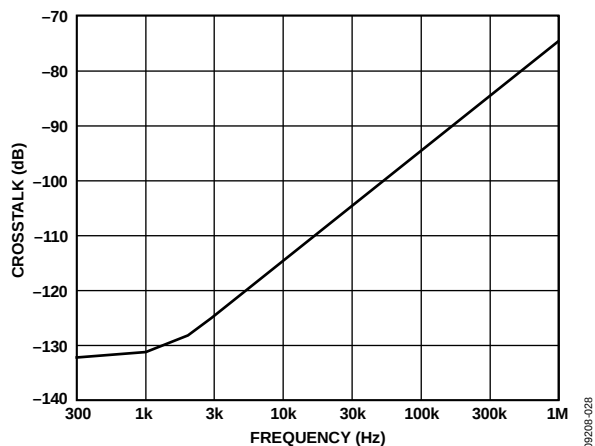


Figure 27. Crosstalk vs. Frequency

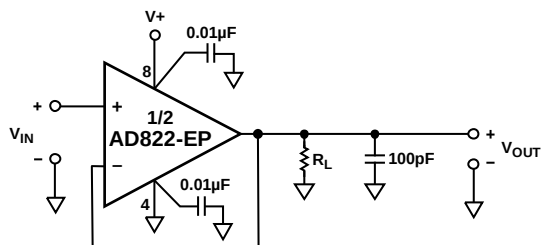


Figure 28. Unity-Gain Follower

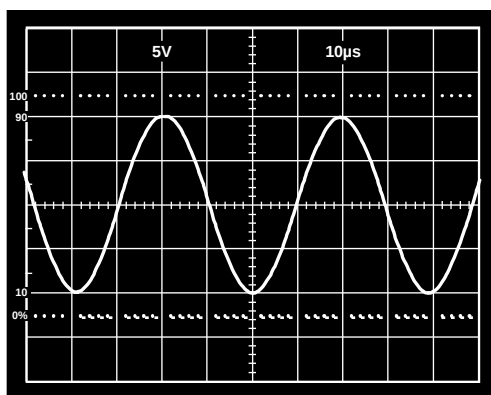


Figure 29. 20 V p-p, 25 kHz Sine Wave Input; Unity-Gain Follower; $V_S = \pm 15\text{ V}$, $R_L = 600\ \Omega$

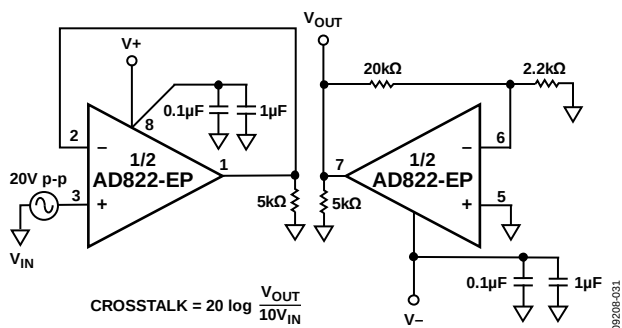


Figure 30. Crosstalk Test Circuit

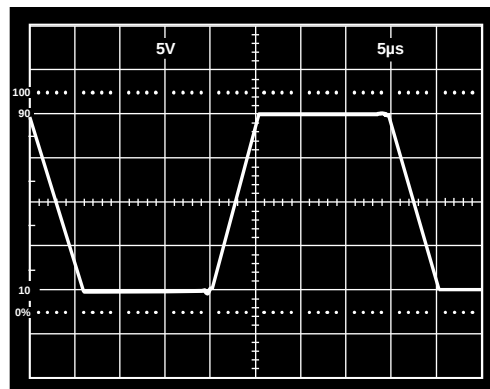


Figure 31. Large Signal Response Unity-Gain Follower; $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$

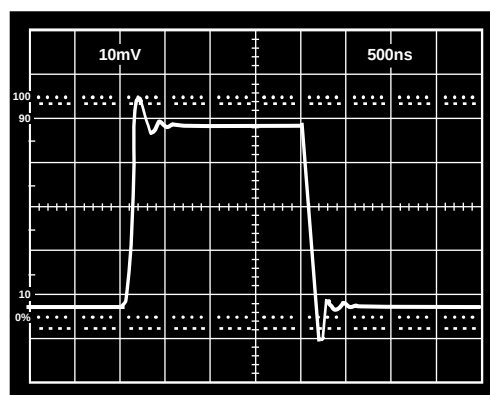


Figure 32. Small Signal Response Unity-Gain Follower; $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$

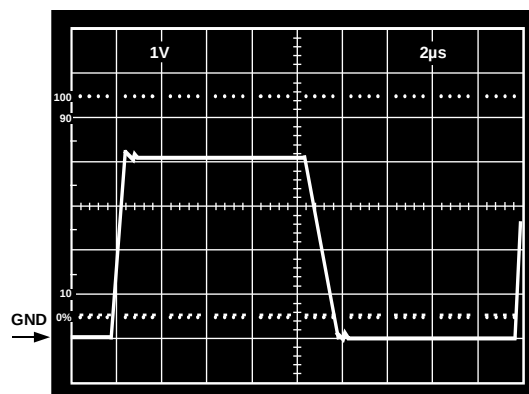


Figure 33. $V_S = 5\text{ V}$, 0 V ; Unity-Gain Follower Response to 0 V to 4 V Step

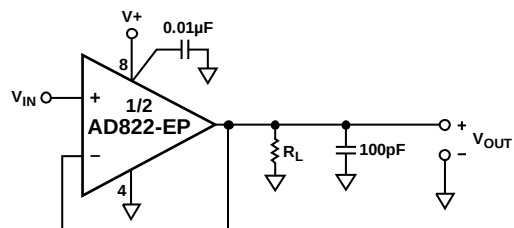


Figure 34. Unity-Gain Follower

AD822-EP

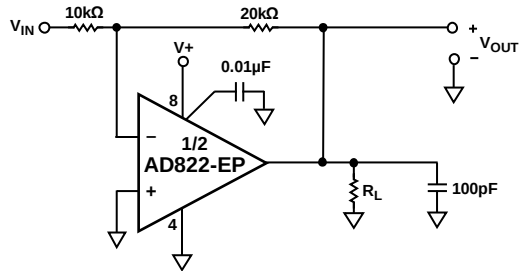


Figure 35. Gain-of-Two Inverter

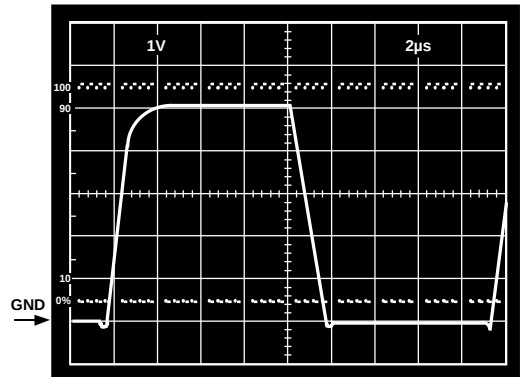


Figure 36. $V_S = 5\text{ V}$, 0 V ; Unity-Gain Follower Response to 0 V to 5 V Step

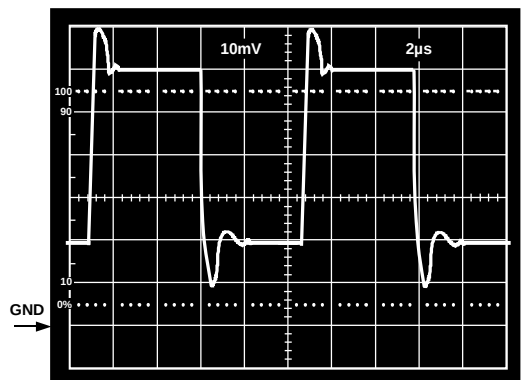


Figure 37. $V_S = 5\text{ V}$, 0 V ; Unity-Gain Follower Response to 40 mV Step, Centered 40 mV above Ground, $R_L = 10\text{ k}\Omega$

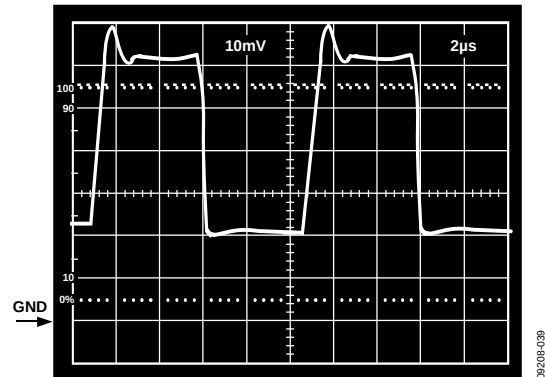


Figure 38. $V_S = 5\text{ V}$, 0 V ; Gain-of-2 Inverter Response to 20 mV Step, Centered 20 mV Below Ground, $R_L = 10\text{ k}\Omega$

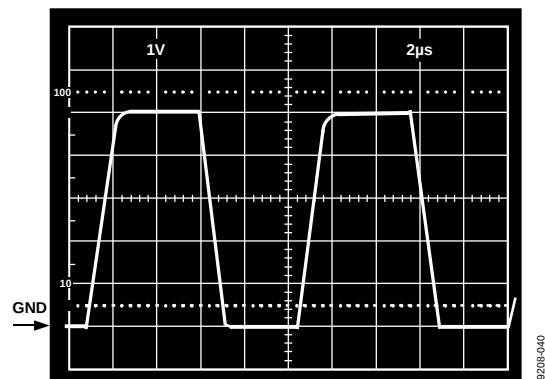


Figure 39. $V_S = 5\text{ V}$, 0 V ; Gain-of-2 Inverter Response to 2.5 V Step, Centered -1.25 V Below Ground, $R_L = 10\text{ k}\Omega$

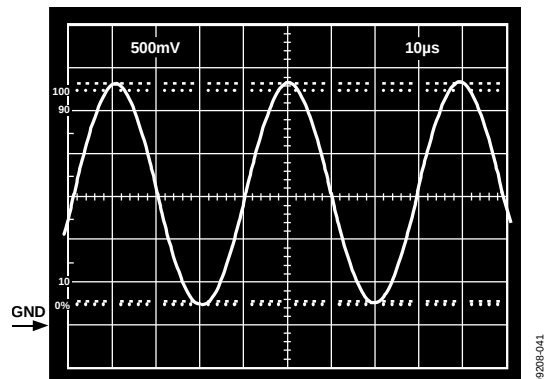
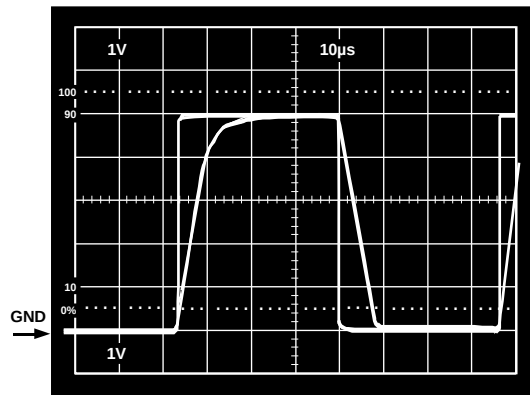
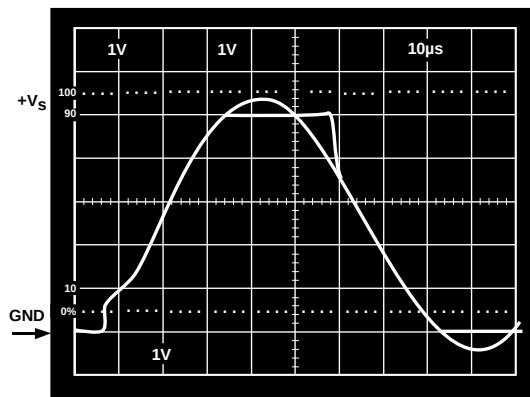


Figure 40. $V_S = 3\text{ V}$, 0 V ; Gain-of-2 Inverter, $V_{IN} = 1.25\text{ V}$, 25 kHz , Sine Wave Centered at -0.75 V , $R_L = 600\text{ }\Omega$



(a)



(b)

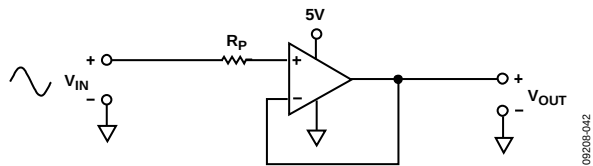
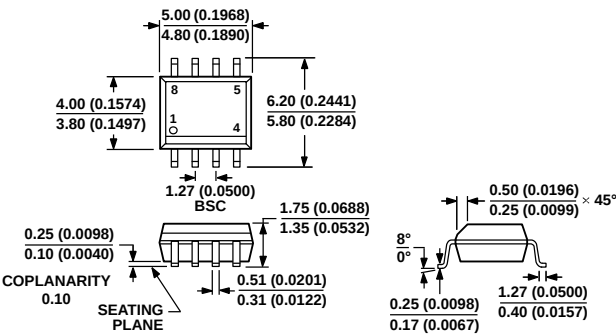


Figure 41. (a) Response with $R_P = 0$; V_{IN} from 0 V to $+V_S$
 (b) $V_{IN} = 0$ V to $+V_S + 200$ mV
 $V_{OUT} = 0$ V to $+V_S$
 $R_P = 49.9$ k Ω

09203-042

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 42. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)

Dimensions shown in millimeters and (inches)

012407-A

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
AD822TRZ-EP	–55°C to +125°C	8-Lead SOIC_N	R-8
AD822TRZ-EP-R7	–55°C to +125°C	8-Lead SOIC_N	R-8

¹ Z = RoHS Compliant Part.

SPIICE model is available at www.analog.com.

NOTES

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