HDMI/DVI Buffer with Equalization

Data Sheet **AD8195**

FEATURES

- 1 input, 1 output HDMI/DVI link
- Enables HDMI 1.3a-compliant front panel input
  - 4 TMDS channels per link
    - Supports 250 Mbps to 2.25 Gbps data rates
    - Supports 25 MHz to 225 MHz pixel clocks
    - Equalized inputs for operation with long HDMI cables (20 m at 2.25 Gbps)
    - Preemphasized outputs
    - Fully buffered unidirectional inputs/outputs
    - 50 Ω on-chip terminations
    - Low added jitter
    - Transmitter disable feature
      - Reduces power dissipation
      - Disables input termination
  - 3 auxiliary buffered channels per link
    - Bidirectional buffered DDC lines (SDA and SCL)
    - Bidirectional buffered CEC line with integrated pull-up resistors (27 kΩ)
    - Independently powered from 5 V of HDMI input connector
    - Logic level translation (3.3 V, 5 V)
    - Input/output capacitance isolation
- Standards compatible: HDMI, DVI, HDCP, DDC, CEC
- 40-lead LFCSP_VQ package (6 mm × 6 mm)

APPLICATIONS

- Front panel buffer for advanced television (HDTV) sets

GENERAL DESCRIPTION

The AD8195 is an HDMI/DVI buffer featuring equalized TMDS inputs and preemphasized TMDS outputs, ideal for systems with long cable runs. The AD8195 includes bidirectional buffering for the DDC bus and bidirectional buffering with integrated pull-up resistors for the CEC bus. The DDC and CEC buffers are powered independently of the TMDS buffers so that DDC/CEC functionality can be maintained when the system is powered off. The AD8195 meets all the requirements for sink tests as defined in Section 8 of the HDMI Compliance Test 1.3c.

The AD8195 is specified to operate over the −40°C to +85°C temperature range.

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FUNCTIONAL BLOCK DIAGRAM

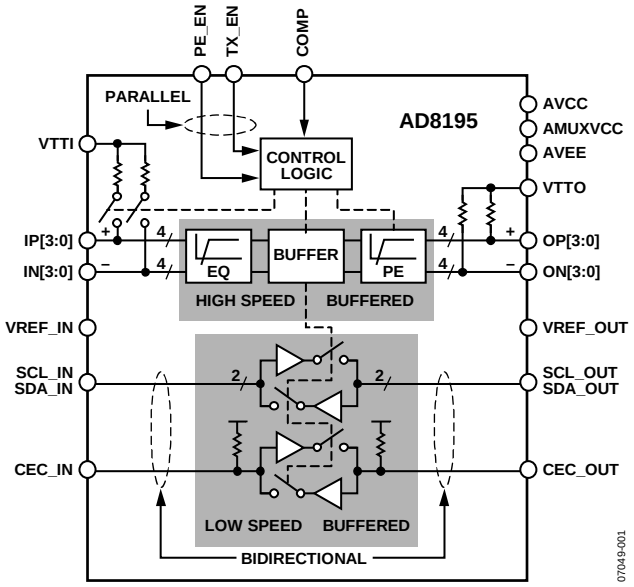


Figure 1.

TYPICAL APPLICATION

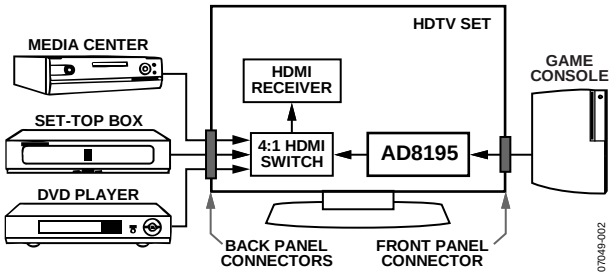


Figure 2. Typical AD8195 Application for HDTV Sets

PRODUCT HIGHLIGHTS

1. Enables a fully HDMI 1.3a-compliant front panel input.
2. Supports data rates of up to 2.25 Gbps, enabling 1080p deep color (12-bit color) HDMI formats and greater than UXGA (1600 × 1200) DVI resolutions.
3. Input cable equalizer enables use of long cables; more than 20 meters (24 AWG) at data rates of up to 2.25 Gbps.
4. Auxiliary buffer isolates and buffers the DDC bus and CEC line for a single chip, fully HDMI 1.3a-compliant solution.
5. Auxiliary buffer is powered independently from the TMDS link so that DDC/CEC functionality can be maintained when the system is powered off.

Rev. B
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REVISION HISTORY

8/12—Rev. A to Rev. B

Changed Data Rate = 3 Gbps to Data Rate = 2.25 Gbps ... Throughout
Changes to Features Section, General Description Section, and Product Highlights Section ... 1
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8/11—Rev. 0 to Rev. A

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8/08—Revision 0: Initial Version

SPECIFICATIONS

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, AMUXVCC = 5 V, VREF_IN = 5 V, VREF_OUT = 5 V, AVEE = 0 V, differential input swing = 1000 mV, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, unless otherwise noted.

TMDS PERFORMANCE SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
TMDS DYNAMIC PERFORMANCE					
Maximum Data Rate (DR) per Channel	NRZ	2.25			Gbps
Bit Error Rate (BER)	PRBS $2^{23} - 1$			10^{-9}	
Added Data Jitter	DR ≤ 2.25 Gbps, PRBS $2^7 - 1$		31		ps p-p
Added Clock Jitter			1		ps rms
Differential Intrapair Skew	At output		1		ps
Differential Interpair Skew	At output		30		ps
TMDS EQUALIZATION PERFORMANCE					
Receiver[1]	Boost frequency = 1.5 GHz		12		dB
Transmitter[2]	Boost frequency = 1.5 GHz		6		dB
TMDS INPUT CHARACTERISTICS					
Input Voltage Swing	Differential	150		1200	mV
Input Common-Mode Voltage (V_{ICM})		AVCC − 800		AVCC	mV
TMDS OUTPUT CHARACTERISTICS					
High Voltage Level	Single-ended, high speed channel	AVCC − 200		AVCC + 10	mV
Low Voltage Level	Single-ended, high speed channel	AVCC − 600		AVCC − 400	mV
Rise/Fall Time (20% to 80%)[3]	DR = 2.25 Gbps	50	90	150	ps
TMDS TERMINATION					
Input Termination Resistance	Single-ended		50		Ω
Output Termination Resistance	Single-ended		50		Ω

[1] Output meets transmitter eye diagram as defined in the DVI Standard Revision 1.0 and HDMI Standard.
[2] Cable output meets receiver eye diagram mask as defined in the DVI Standard Revision 1.0 and HDMI Standard.
[3] Output rise/fall time measurement excludes external components, such as HDMI connector or external ESD protection diodes. See the Applications Information section for more information.

AUXILIARY CHANNEL PERFORMANCE SPECIFICATIONS

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DDC CHANNELS					
Input Capacitance, C_{AUX}	DC bias = 2.5 V, ac voltage = 3.5 V p-p, f = 100 kHz		10	15	pF
Input Low Voltage, V_{IL}				0.5	V
Input High Voltage, V_{IH}		0.7 × VREF[1]		VREF[1]	V
Output Low Voltage, V_{OL}	I_{OL} = 5 mA		0.25	0.4	V
Output High Voltage, V_{OH}			VREF[1]		V
Rise Time	10% to 90%, no load		140		ns
Fall Time	90% to 10%, C_{LOAD} = 400 pF		100	200	ns
Leakage	Input voltage = 5.0 V			10	µA
CEC CHANNEL					
Input Capacitance, C_{AUX}	DC bias = 1.65 V, ac voltage = 2.5 V p-p, f = 100 kHz, 2 kΩ pull-up resistor from CEC_OUT to 3.3 V		5	25	pF
Input Low Voltage, V_{IL}				0.8	V
Input High Voltage, V_{IH}		2.0			V
Output Low Voltage, V_{OL}			0.25	0.6	V
Output High Voltage, V_{OH}		2.5	3.3		V
Rise Time	10% to 90%, C_{LOAD} = 1500 pF, $R_{PULL-UP}$ = 27 kΩ; or C_{LOAD} = 7200 pF, $R_{PULL-UP}$ = 3 kΩ		50	100	µs
Fall Time	90% to 10%, C_{LOAD} = 1500pF, $R_{PULL-UP}$ = 27 kΩ; or C_{LOAD} = 7200 pF, $R_{PULL-UP}$ = 3 kΩ		5	10	µs
Pull-Up Resistance			27		kΩ
Leakage	Off leakage test conditions[2]			1.8	µA

[1] VREF is the voltage at the reference pin (VREF_IN for SCL_IN and SDA_IN, or VREF_OUT for SCL_OUT and SDA_OUT); nominally 5.0 V.
[2] Off leakage test conditions are described in the HDMI Compliance Test Specification 1.3b Section 8, Test ID 8-14: "Remove power (mains) from DUT. Connect CEC line to 3.63 V via 27 kΩ ± 5% resistor with ammeter in series. Measure CEC line leakage."

POWER SUPPLY AND CONTROL LOGIC SPECIFICATIONS

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
AVCC	Operating range (3.3 V ± 10%)	3	3.3	3.6	V
AMUXVCC	Operating range (5 V ± 10%)	4.5	5	5.5	V
VREF_IN, VREF_OUT		3		5.5	V
QUIESCENT CURRENT					
AVCC	Output disabled		20	40	mA
	Output enabled, no preemphasis (0 dB)		32	50	mA
	Output enabled, maximum preemphasis (6 dB)		66	80	mA
VTTI	Input termination on		40	54	mA
VTTO	Output termination on, no preemphasis		40	50	mA
	Output termination on, maximum preemphasis		80	100	mA
VREF_IN			120	200	µA
VREF_OUT			120	200	µA
AMUXVCC			10	20	mA
POWER DISSIPATION					
	Output disabled		116	254	mW
	Output enabled, no preemphasis (0 dB)		180	663	mW
	Output enabled, maximum preemphasis (6 dB)		736	1047	mW
PARALLEL CONTROL INTERFACE	TX_EN, PE_EN				
Input High Voltage, V_{IH}		2.4			V
Input Low Voltage, V_{IL}				0.8	V

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
AVCC to AVEE	3.7 V
VTTI	AVCC + 0.6 V
VTTO	AVCC + 0.6 V
AMUXVCC	5.5 V
VREF_IN	5.5 V
VREF_OUT	5.5 V
Internal Power Dissipation	1.81 W
High Speed Input Voltage	AVCC − 1.4 V < V_{IN} < AVCC + 0.6 V
High Speed Differential Input Voltage	2.0 V
Parallel Control Input Voltage	AVEE − 0.3 V < V_{IN} < AVCC + 0.6 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature	150°C
ESD, Human Body Model	
Input Pins Only	±5 kV
All Other Pins	±3 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 5.

Package	θ_{JA}	θ_{JC}	Unit
40-Lead LFCSP_VQ	36	5.0	°C/W

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8195 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure. To ensure proper operation, it is necessary to observe the maximum power derating as determined by the thermal resistance coefficients.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

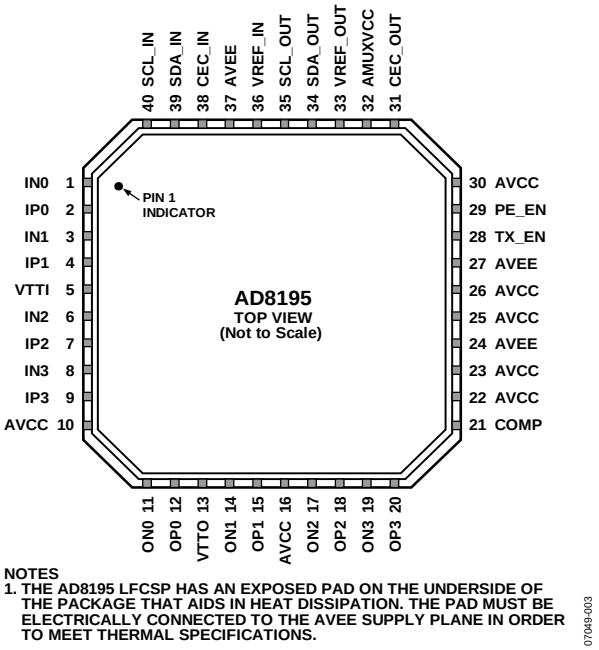


Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	IN0	HS I	High Speed Input Complement.
2	IP0	HS I	High Speed Input.
3	IN1	HS I	High Speed Input Complement.
4	IP1	HS I	High Speed Input.
5	VTTI	Power	Input Termination Supply. Nominally connected to AVCC.
6	IN2	HS I	High Speed Input Complement.
7	IP2	HS I	High Speed Input.
8	IN3	HS I	High Speed Input Complement.
9	IP3	HS I	High Speed Input.
10, 16, 22, 23, 25, 26, 30	AVCC	Power	Positive Analog Supply. 3.3 V nominal.
11	ON0	HS O	High Speed Output Complement.
12	OP0	HS O	High Speed Output.
13	VTTO	Power	Output Termination Supply. Nominally connected to AVCC.
14	ON1	HS O	High Speed Output Complement.
15	OP1	HS O	High Speed Output.
17	ON2	HS O	High Speed Output Complement.
18	OP2	HS O	High Speed Output.
19	ON3	HS O	High Speed Output Complement.
20	OP3	HS O	High Speed Output.
21	COMP	Control	Power-On Compensation Pin. Bypass to ground through a 10 µF capacitor.
24, 27, 37, Exposed Pad	AVEE	Power	Negative Analog Supply. 0 V nominal.
28	TX_EN	Control	High Speed Output Enable Parallel Interface.
29	PE_EN	Control	High Speed Preemphasis Enable Parallel Interface.

Pin No.	Mnemonic	Type[1]	Description
31	CEC_OUT	LS I/O	CEC Output Side.
32	AMUXVCC	Power	Positive Auxiliary Buffer Supply. 5 V nominal.
33	VREF_OUT	Reference	DDC Output Side Pull-Up Reference Voltage.
34	SDA_OUT	LS I/O	DDC Output Side Data Line Input/Output.
35	SCL_OUT	LS I/O	DDC Output Side Clock Line Input/Output.
36	VREF_IN	Reference	DDC Input Side Pull-Up Reference Voltage.
38	CEC_IN	LS I/O	CEC Input Side.
39	SDA_IN	LS I/O	DDC Input Side Data Line.
40	SCL_IN	LS I/O	DDC Input Side Clock Line

[1] HS = high speed, LS = low speed, I = input, and O = output.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, AVEE = 0 V, differential input swing = 1000 mV, pattern = PRBS $2^7 - 1$, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, unless otherwise noted.

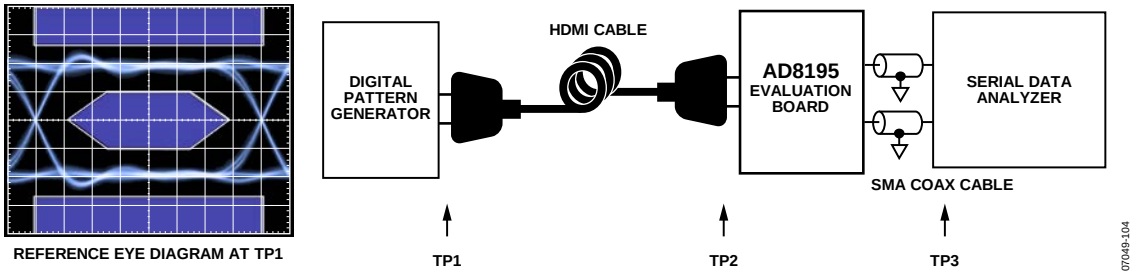


Figure 4. Test Circuit Diagram for Rx Eye Diagrams

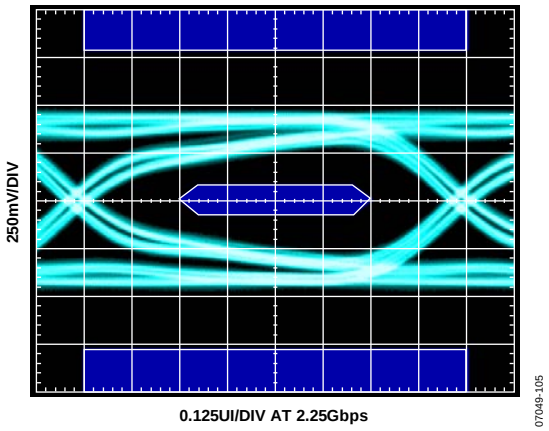


Figure 5. Rx Eye Diagram at TP2
(Cable = 2 Meters, 24 AWG, Data Rate = 2.25 Gbps)

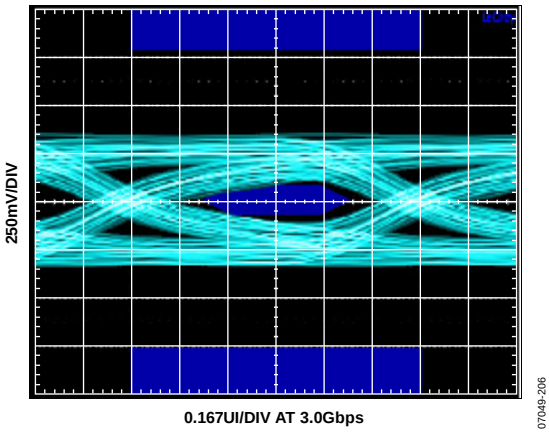


Figure 6. Rx Eye Diagram at TP2
(Cable = 2 Meters, 24 AWG, Data Rate = 3 Gbps)

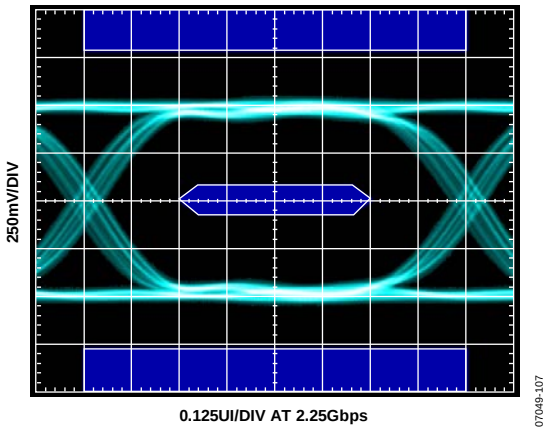


Figure 7. Rx Eye Diagram at TP3, EQ = 12 dB
(Cable = 2 Meters, 24 AWG, Data Rate = 2.25 Gbps)

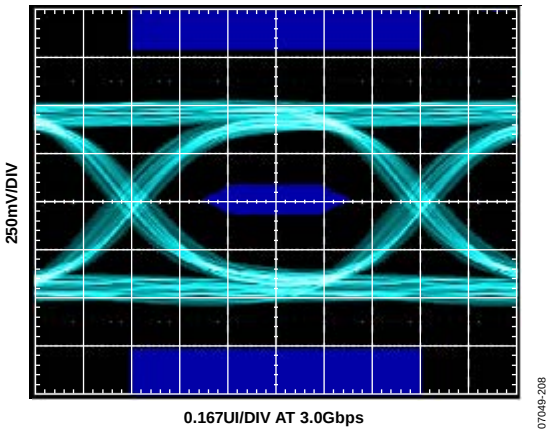


Figure 8. Rx Eye Diagram at TP3, EQ = 12 dB
(Cable = 2 Meters, 24 AWG, Data Rate = 3 Gbps)

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, AVEE = 0 V, differential input swing = 1000 mV, pattern = PRBS $2^7 - 1$, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, unless otherwise noted.

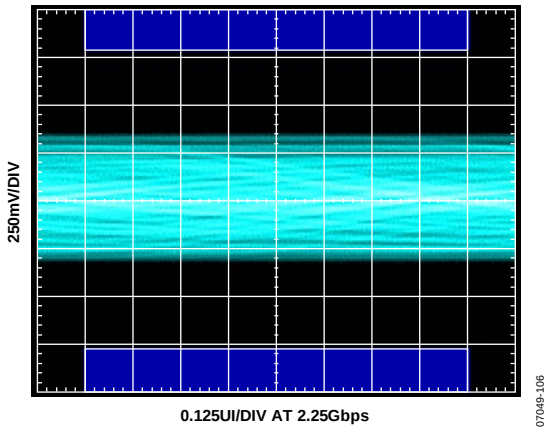


Figure 9 Rx Eye Diagram at TP2
(Cable = 20 Meters, 24 AWG, Data Rate = 2.25 Gbps)

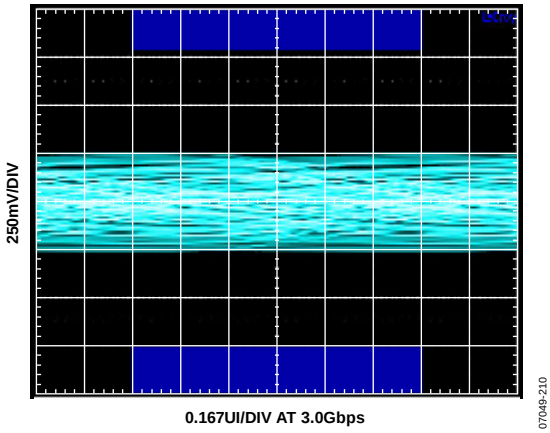


Figure 10 Rx Eye Diagram at TP2
(Cable = 15 Meters, 24 AWG, Data Rate = 3 Gbps)

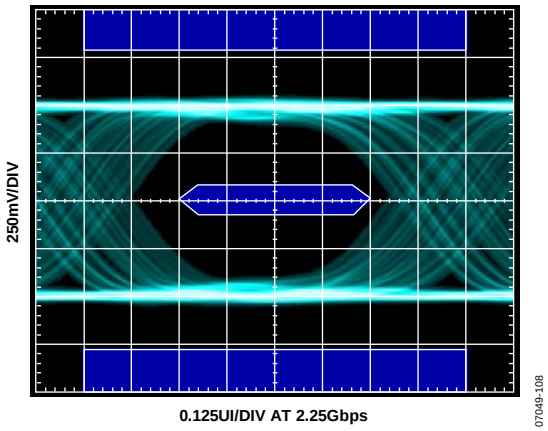


Figure 11. Rx Eye Diagram at TP3, EQ = 12 dB
(Cable = 20 Meters, 24 AWG, Data Rate = 2.25 Gbps)

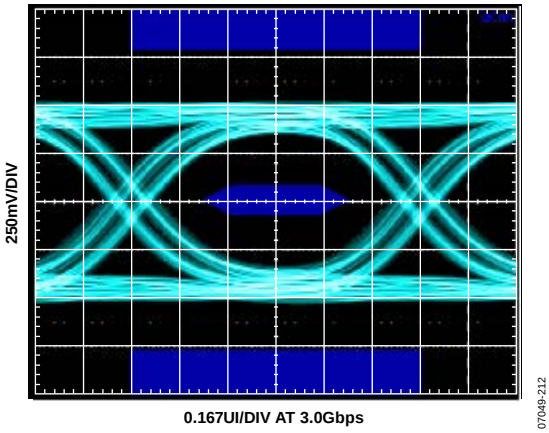


Figure 12. Rx Eye Diagram at TP3, EQ = 12 dB
(Cable = 15 Meters, 24 AWG, Data Rate = 3 Gbps)

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, AVEE = 0 V, differential input swing = 1000 mV, pattern = PRBS $2^7 - 1$, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, unless otherwise noted.

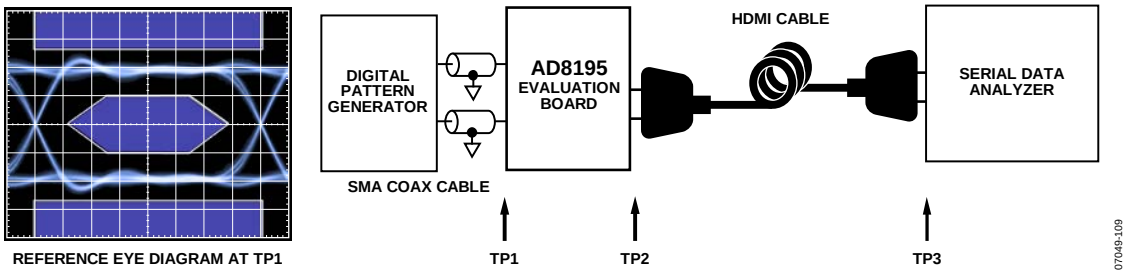


Figure 13. Test Circuit Diagram for Tx Eye Diagrams

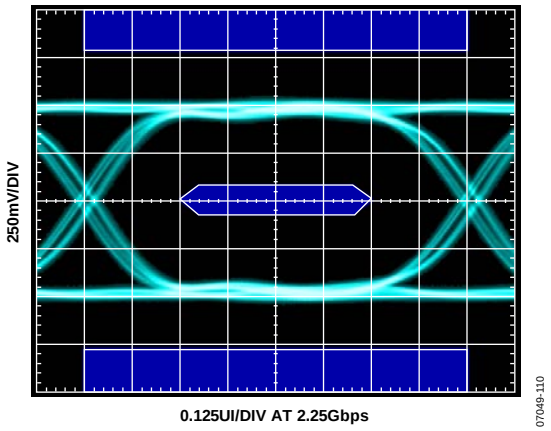


Figure 14. Tx Eye Diagram at TP2, PE = 0 dB, Data Rate = 2.25 Gbps

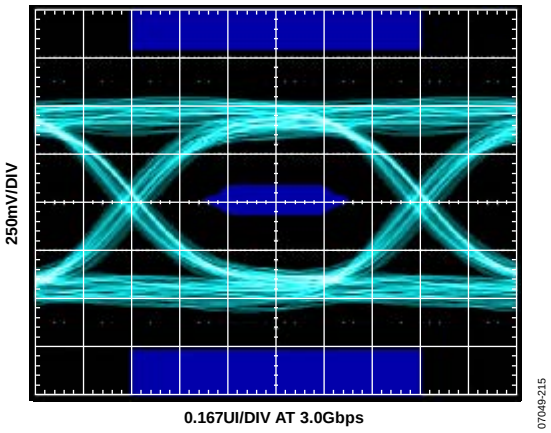


Figure 15. Tx Eye Diagram at TP2, PE = 0 dB, Data Rate = 3.0 Gbps

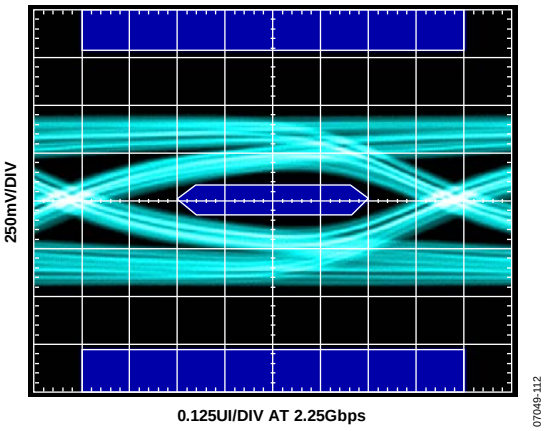


Figure 16. Tx Eye Diagram at TP3, PE = 0 dB, Data Rate = 2.25 Gbps (Cable = 6 Meters, 24 AWG)

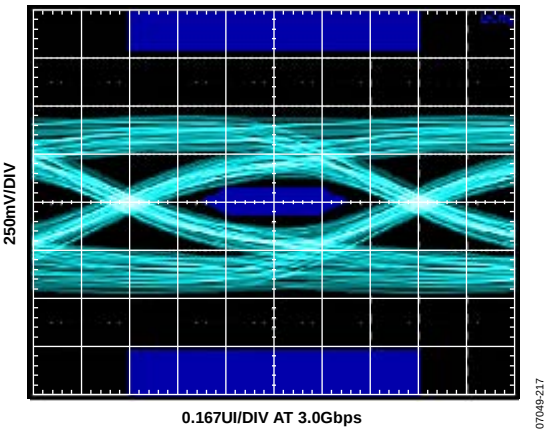


Figure 17. Tx Eye Diagram at TP3, PE = 0 dB, Data Rate = 3.0 Gbps (Cable = 6 Meters, 24 AWG)

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, AVEE = 0 V, differential input swing = 1000 mV, pattern = PRBS $2^7 - 1$, data rate = 2.25 Gbps, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, unless otherwise noted.

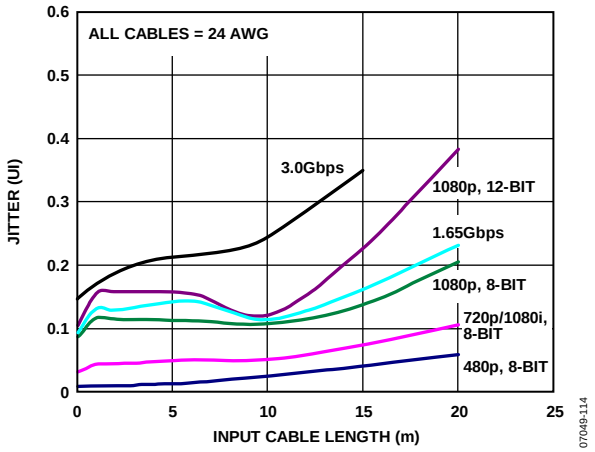


Figure 18. Jitter vs. Input Cable Length (See Figure 4 for Test Setup)

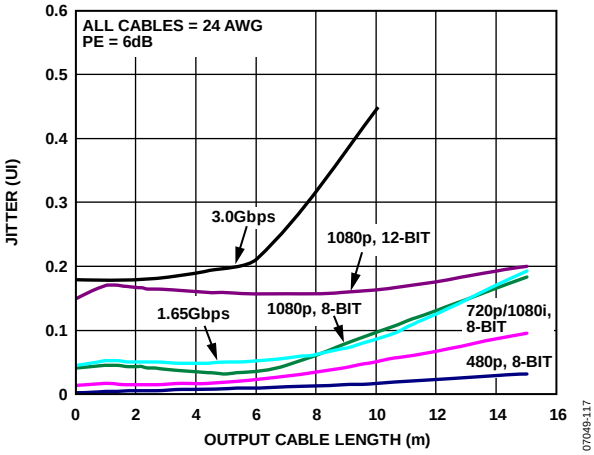


Figure 21. Jitter vs. Output Cable Length (See Figure 13 for Test Setup)

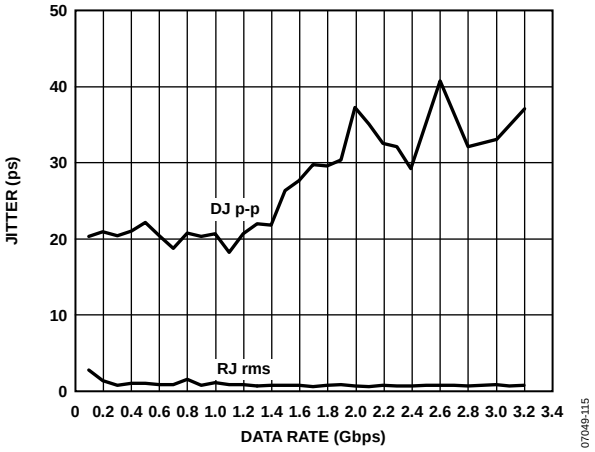


Figure 19. Jitter vs. Data Rate

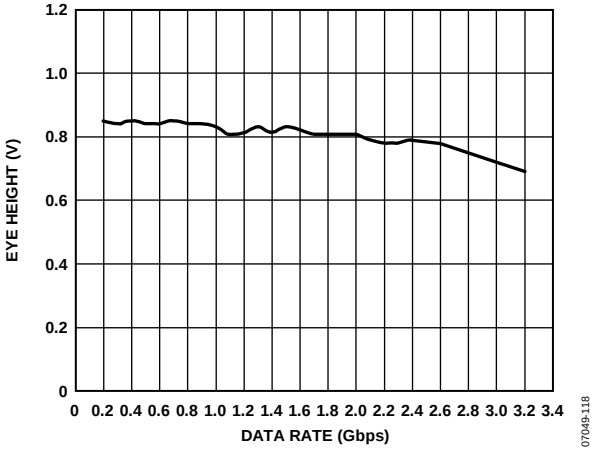


Figure 22. Eye Height vs. Data Rate

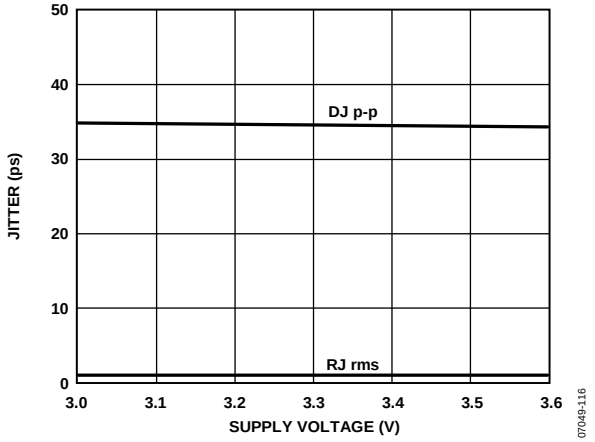


Figure 20. Jitter vs. Supply Voltage

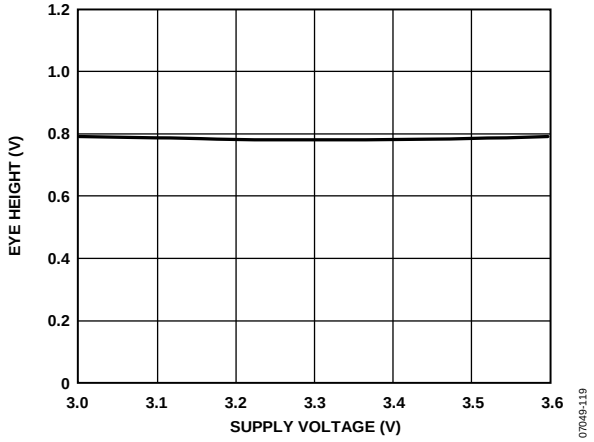


Figure 23. Eye Height vs. Supply Voltage

T_A = 27°C, AVCC = 3.3 V, VTTI = 3.3 V, VTTO = 3.3 V, AVEE = 0 V, differential input swing = 1000 mV, pattern = PRBS $2^7 - 1$, data rate = 3 Gbps, TMDS outputs terminated with external 50 Ω resistors to 3.3 V, unless otherwise noted.

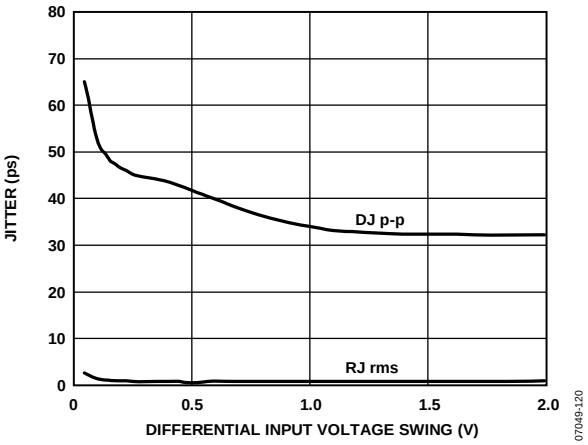


Figure 24. Jitter vs. Differential Input Voltage Swing

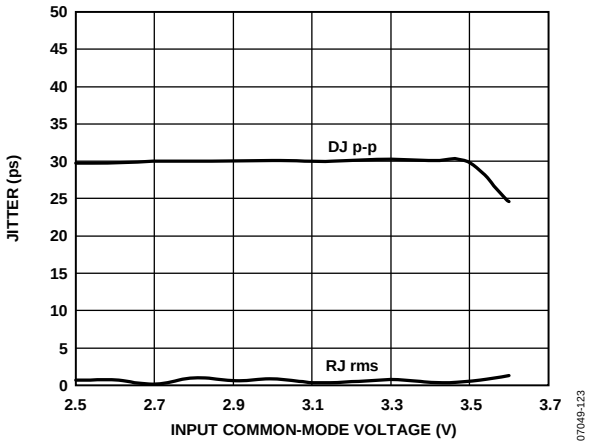


Figure 27. Jitter vs. Input Common-Mode Voltage

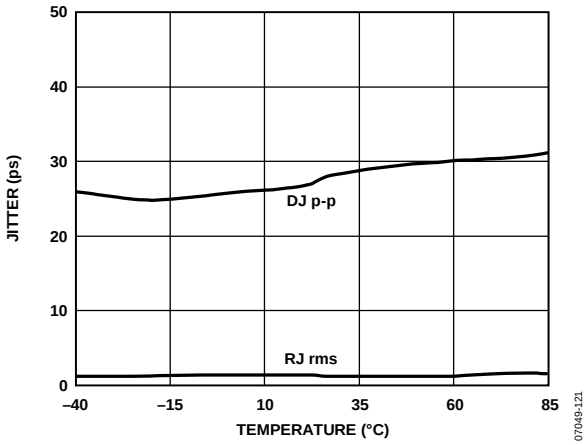


Figure 25. Jitter vs. Temperature

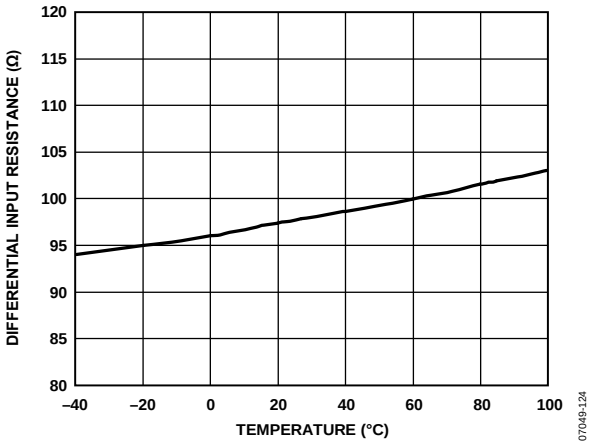


Figure 28. Differential Input Resistance vs. Temperature

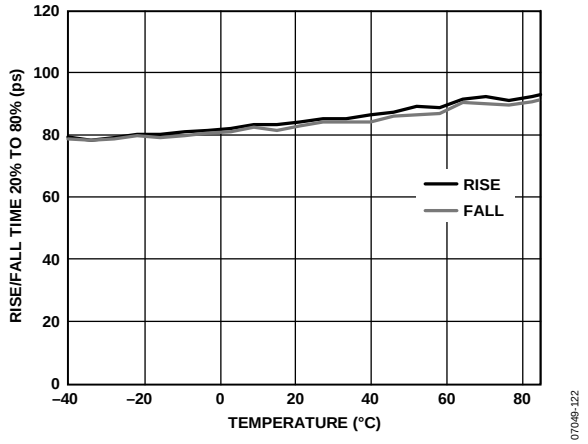


Figure 26. Rise and Fall Time vs. Temperature

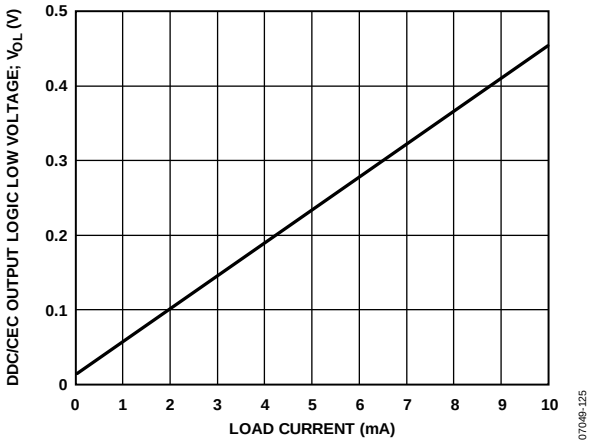


Figure 29.DDC/CEC Output Logic Low Voltage (V_{OL}) vs. Load Current

THEORY OF OPERATION

The primary function of the AD8195 is to buffer a single (HDMI or DVI) link. The HDMI or DVI link consists of four differential, high speed channels and three auxiliary single-ended, low speed control signals. The high speed channels include a data-word clock and three transition minimized differential signaling (TMDS) data channels running at 10× the data-word clock frequency for data rates up to 2.25 Gbps. The three low speed control signals consist of the display data channel (DDC) bus (SDA and SCL) and the consumer electronics control (CEC) line.

All four high speed TMDS channels are identical; that is, the pixel clock can be run on any of the four TMDS channels. Receive channel compensation is provided for the high speed channels to support long input cables. The AD8195 also includes selectable preemphasis for driving high loss output cables.

In the intended application, the AD8195 is placed between a source and a sink, with long cable runs on the input and output.

INPUT CHANNELS

Each high speed input differential pair terminates to the 3.3 V VTTI power supply through a pair of single-ended 50 Ω on-chip resistors, as shown in Figure 30. When the transmitter of the AD8195 is disabled by setting the TX_EN control pin, the input termination resistors are also disabled to provide a high impedance node at the TMDS inputs.

The input equalizer provides 12 dB of high frequency boost. No specific cable length is suggested for this equalization level because cable performance varies widely between manufacturers; however, in general, the AD8195 does not degrade or over-equalize input signals, even for short input cables. The AD8195 can equalize more than 20 meters of 24 AWG cable at 2.25 Gbps, over reference cables that exhibit an insertion loss of −15 dB.

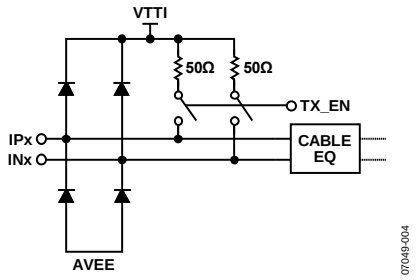


Figure 30. High Speed Input Simplified Schematic

OUTPUT CHANNELS

Each high speed output differential pair is terminated to the 3.3 V VTTO power supply through two single-ended 50 Ω on-chip resistors (see Figure 31).

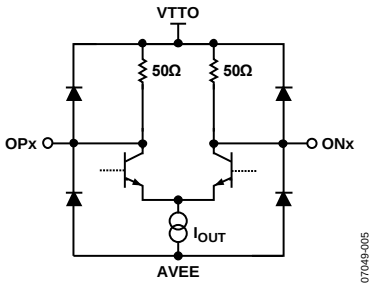


Figure 31. High Speed Output Simplified Schematic

The output termination resistors of the AD8195 back terminate the output TMDS transmission lines. These back terminations, as `recommended in the HDMI specification, act to absorb reflections from impedance discontinuities on the output traces, improving the signal integrity of the output traces and adding flexibility to how the output traces can be routed. For example, interlayer vias can be used to route the AD8195 TMDS outputs on multiple layers of the PCB without severely degrading the quality of the output signal. Note that the arrangement of the ESD structures cause current to flow into the TMDS outputs when in the off state. The AD8195 outputs will not meet the requirements of Test ID 7-3 (TMDS-VOFF) of the HDMI Compliance Test Specification 1.3c. These outputs should only interface to an internal system node and should not be interfaced to an HDMI output connector.

The AD8195 has an external control pin, TX_EN, that disables the transmitter, reducing power when the transmitter is not in use. Additionally, when the transmitter is disabled, the input termination resistors are also disabled to present a high impedance state at the input and indicate to any connected HDMI sources that the link through the AD8195 is inactive.

Table 7. Transmitter Enable Setting

TX_EN	Function
0	Tx/input termination disabled
1	Tx/input termination enabled

The AD8195 also includes two levels of programmable output preemphasis, 0 dB and 6 dB. The output preemphasis level can be manually configured by setting the PE_EN pin. No specific cable length is suggested for use with either preemphasis setting, as cable performance varies widely among manufacturers.

Table 8. Preemphasis Setting

PE_EN	PE Boost
0	0 dB
1	6 dB

PREEMPHASIS

The preemphasized TMDS outputs precompensate the transmitted signal to account for losses in systems with long cable runs. These long cable runs selectively attenuate the high frequency energy of the signal, leading to degraded transition times and eye closure. Similar to a receive equalizer, the goal of the preemphasis filter is to boost the high frequency energy in the signal. However, unlike the receive equalizer, the preemphasis filter is applied before the channel, thus predistorting the transmitted signal to account for the loss of the channel. The series connection of the preemphasis filter and the channel results in a flatter frequency response than that of the channel, thus leading to improved high frequency energy, improved transition times, and improved eye opening on the far end of the channel. Using a preemphasis filter to compensate for channel losses allows for longer cable runs with or without a receiver equalizer on the far end of the channel.

When there is no receive equalizer on the far end of the channel, the preemphasis filter should allow longer cable runs than would be acceptable with no preemphasis. When there is both a preemphasis filter on the near end and a receive equalizer on the far end of the channel, the allowable cable run should be longer than either compensation could achieve alone. The pulse response of a preemphasized waveform is shown in Figure 32. The output voltage levels and symbol descriptions are listed in Table 9 and Table 10, respectively. The preemphasis circuit is designed to work up to 2.25 Gbps and does not perform suitably at higher data rates.

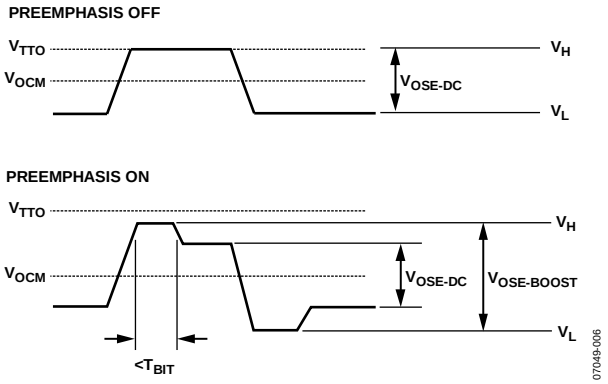


Figure 32. Preemphasis Pulse Response

AUXILIARY LINES

The auxiliary (low speed) lines provide buffering for the DDC and CEC signals. The auxiliary lines are powered independently from the TMDS link; therefore, their functionality can be maintained even when the system is powered off. In an application, these lines can be powered by connecting AMUXVCC to the 5 V supply provided from the video source through the input HDMI connector.

DDC Buffers

The DDC buffers are 5 V tolerant bidirectional lines that can carry extended display identification data (EDID), HDCP encryption, and other information, depending on the specific application. The DDC buffers are bidirectional and fully support arbitration, clock synchronization, clock stretching, slave acknowledgement, and other relevant features of a standard mode I^2C bus.

The DDC buffers also have separate voltage references for the input side and the output side, allowing the sink to use internal bus voltages (3.3 V), alleviating the need for 5 V tolerant I/Os for system ASICs. The logic level for the DDC_IN bus is set by the voltage on VREF_IN, and the logic level for the DDC_OUT bus is set by the voltage on VREF_OUT. For example, if the DDC_IN bus is using 5 V I^2C, the VREF_IN power supply pin should be connected to a 5 V power supply. If the DDC_OUT bus is using 3.3 V I^2C, the VREF_OUT power supply pin should be connected to a 3.3 V power supply.

CEC Buffer

The CEC buffer is a 3.3 V tolerant bidirectional buffer with integrated pull-up resistors. This buffer enables full compliance with all CEC specifications, including but not limited to input capacitance, logic levels, transition times, and leakage (both with the system power on and off). This allows the CEC functionality to be implemented in a standard microcontroller that may not have CEC compliant I/Os. The CEC buffer is powered from the AMUXVCC supply.

Table 9. Output Voltage Levels

PE Setting	Boost (dB)	I_T (mA)	V_{OSE-DC} (mV p-p)	$V_{OSE-BOOST}$ (mV p-p)	V_{OCM} (V)	V_H (V)	V_L (V)
0	0	20	500	500	3.050	3.3	2.8
1	6	40	500	1000	2.8	3.3	2.3

Table 10. Symbol Definitions

Symbol	Formula	Definition
V_{OSE-DC}	$I_T\|_{PE=0} \times 25\ \Omega$	Single-ended output voltage swing after settling
$V_{OSE-BOOST}$	$I_T \times 25\ \Omega$	Boosted single-ended output voltage swing
V_{OCM} (DC-Coupled)	$V_{TTO} - I_T/2 \times 25\ \Omega$	Common-mode voltage when the output is dc-coupled
V_H	$V_{OCM} + V_{OSE-BOOST}/2$	High single-ended output voltage excursion
V_L	$V_{OCM} - V_{OSE-BOOST}/2$	Low single-ended output voltage excursion

APPLICATIONS INFORMATION

FRONT PANEL BUFFER FOR ADVANCED TV

A front panel input provides easy access to an HDMI connector for connecting devices, such as an HD camcorder or video game console, to an HDTV. In designs where the main PCB is not near the side or front of the HDTV, a front panel HDMI input must be connected to the main board through a cable. The AD8195 enables the implementation of a front or side panel HDMI input for an HDTV by buffering the HDMI signals and compensating for the cable interconnect to the main board.

A simplified typical front panel buffer circuit is shown in Figure 33. The AD8195 is designed to have an HDMI/DVI receiver pinout at its input and a transmitter pinout at its output. This makes the AD8195 ideal for use in television set front panel connectors and AVR-type applications where a designer routes both the inputs and the outputs directly to HDMI/DVI connectors.

One advantage of the AD8195 in a television set front panel connector is that all of the high speed signals can be routed on one side (the topside) of the board. The AD8195 provides 12 dB of input equalization so it can compensate for the signal degradation of long input cables. In addition, the AD8195 can also provide up to 6 dB of output preemphasis that boosts the output TMDS signals and allows the AD8195 to precompensate when driving long PCB traces or high loss output cables. The net effect of the input equalization and output preemphasis of the AD8195 is that the AD8195 can compensate for the signal degradation of both the input and output cables; it acts to reopen a closed input data eye and transmit a full swing HDMI signal to an end receiver.

Placement of a shunt resistor from the negative terminal of the input TMDS clock differential pair to ground is recommended to prevent amplification of ambient noise resulting in a large swing signal at the input of the HDMI receiver.

For the CEC and DDC buffer circuits to be active when the local supply is off, power must be provided to the AD8195 AMUXVCC supply pin from the HDMI source. The 5 V from the HDMI connector and the local 5 V supply should be isolated with diodes to prevent contention. Additionally, the diodes should be selected such that the forward voltage drop from the local supply is less than from the HDMI source so that current is not drawn from the HDMI source when the local supply is on.

The rise time of the CEC buffer output is set by the time constant of the pull-up resistance and the capacitance on the output node. An additional external pull-up resistance is recommended at the CEC output to allow for optimal rise times. A Thevenin equivalent 2 kΩ pull-up to 3.3 V is shown in Figure 34.

The VREF_IN and VREF_OUT pins are voltage references for the input and output pins of DDC buffer. The external pull-up resistors for the DDC bus should be connected to the same voltage as applied to the respective VREF pin.

Typically, an EDID EEPROM is placed prior to the AD8195, as shown in Figure 34. If desired, the EDID EEPROM can be downstream of the AD8195. This optional configuration is also illustrated in Figure 34. Regardless of the configuration, the pull-up voltage at the DDC output should be on even when the local system power supply is off.

To ensure that the AD8195 operates properly, Pin 21 (COMP) should be tied to ground through a 10 µF bypass capacitor. A 34 kΩ pull-up resistor from COMP to AMUXVCC is integrated on chip.

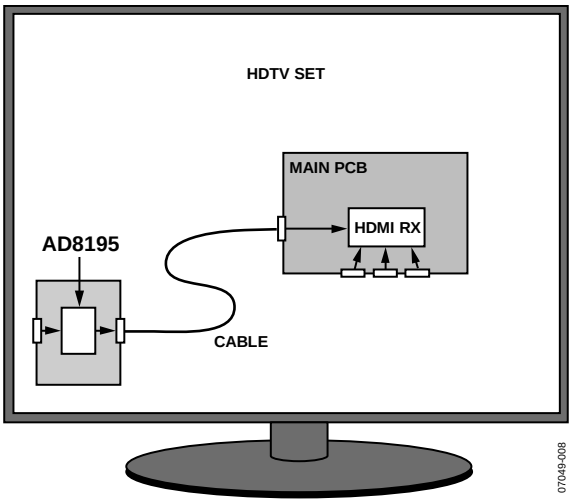


Figure 33. AD8195 as a Front Panel Buffer for an HDTV

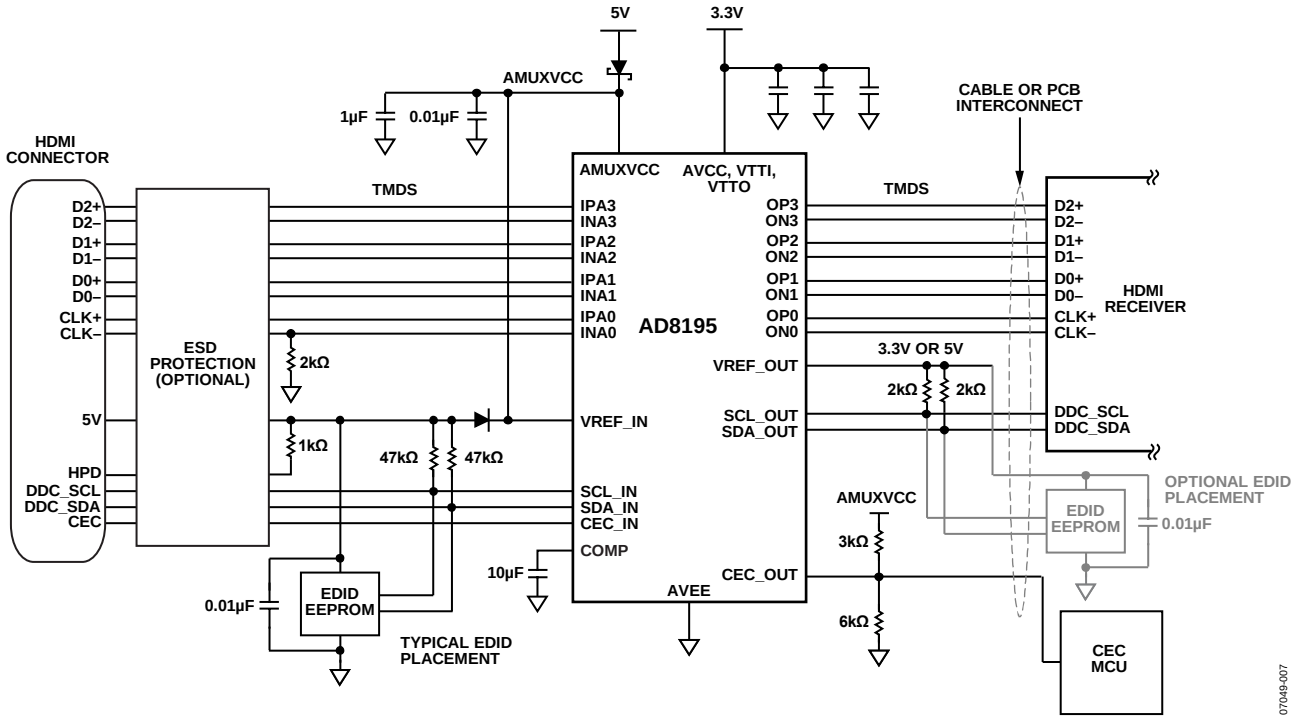


Figure 34. AD8195 Typical Application Simplified Schematic

CABLE LENGTHS AND EQUALIZATION

The AD8195 offers 12 dB of equalization for the high speed inputs. The equalizer of the AD8195 is optimized for video data rates of 2.25 Gbps and can equalize more than 20 meters of 24 AWG HDMI cable at the input for 1080p video with deep color.

The length of cable that can be used in a typical HDMI/DVI application depends on a large number of factors, including the following:

- Cable quality: the quality of the cable in terms of conductor wire gauge and shielding. Thicker conductors have lower signal degradation per unit length.
- Data rate: the data rate being sent over the cable. The signal degradation of HDMI cables increases with data rate.
- Edge rates: the edge rates of the source input. Slower input edges result in more significant data eye closure at the end of a cable.
- Receiver sensitivity: the sensitivity of the terminating receiver.

TMDS OUTPUT RISE/FALL TIMES

The TMDS outputs of the AD8195 are designed for optimal performance even when external components are connected, such as external ESD protection, common-mode filters, and the HDMI connector. In applications where the output of the AD8195 is connected to an HDMI output connector, additional ESD protection is recommended. The capacitance of the additional ESD protection circuits for the TMDS outputs should be as low as possible. In a typical application, the output rise/fall times are compliant with the HDMI specification at the output of the HDMI connector.

PCB LAYOUT GUIDELINES

The AD8195 is used to buffer two distinctly different types of signals, both of which are required for HDMI and DVI video. These signal groups require different treatment when laying out a PCB.

The first group of signals carries the audiovisual (AV) data encoded by a technique called transition minimized differential signaling (TMDS) and, in the case of HDMI, is also encrypted according to the high bandwidth digital copy protection (HDCP) standard.

HDMI/DVI video signals are differential, unidirectional, and high speed (up to 2.25 Gbps). The channels that carry the video data must have controlled impedance, be terminated at the receiver, and be capable of operating up to at least 2.25 Gbps. It is especially important to note that the differential traces that carry the TMDS signals should be designed with a controlled differential impedance of 100 Ω. The AD8195 provides single-ended 50 Ω terminations on chip for both its inputs and outputs. Transmitter termination is not fully specified by the HDMI standard, but its inclusion improves the overall system signal integrity.

The second group of signals consists of low speed auxiliary control signals used for communication between a source and a sink. These signals include the DDC bus (this is an I^2C bus used to send EDID information and HDCP encryption keys between the source and the sink) and the CEC line. These auxiliary signals are bidirectional, low speed, and transferred over a single-ended transmission line that does not need to have controlled impedance. The primary concern with laying out the auxiliary lines is ensuring that they conform to the I^2C bus standard and do not have excessive capacitive loading.

TMDS Signals

In the HDMI/DVI standard, four differential pairs carry the TMDS signals. In DVI, three of these pairs are dedicated to carrying RGB video and sync data. For HDMI, audio data is also interleaved with the video data; the DVI standard does not incorporate audio information. The fourth high speed differential pair is used for the AV data-word clock and runs at one-tenth the speed of the TMDS data channels.

The four high speed channels of the AD8195 are identical. No concession was made to lower the bandwidth of the fourth channel for the pixel clock, so any channel can be used for any TMDS signal. The user chooses which signal is routed over which channel. Additionally, the TMDS channels are symmetric; therefore, the p and n of a given differential pair are interchangeable, provided the inversion is consistent across all inputs and outputs of the AD8195. However, the routing between inputs and outputs through the AD8195 is fixed. For example, Input Channel 0 is always buffered to Output Channel 0, and so forth.

The AD8195 buffers the TMDS signals, and the input traces can be considered electrically independent of the output traces. In most applications, the quality of the signal on the input TMDS traces is more sensitive to the PCB layout. Regardless of the data being carried on a specific TMDS channel, or whether the TMDS line is at the input or the output of the AD8195, all four high speed signals should be routed on a PCB in accordance with the same RF layout guidelines.

Layout for the TMDS Signals

The TMDS differential pairs can be either microstrip traces, routed on the outer layer of a board, or stripline traces, routed on an internal layer of the board. If microstrip traces are used, there should be a continuous reference plane on the PCB layer directly below the traces. If stripline traces are used, they must be sandwiched between two continuous reference planes in the PCB stack-up. Additionally, the p and n of each differential pair must have a controlled differential impedance of 100 Ω. The characteristic impedance of a differential pair is a function of several variables, including the trace width, the distance separating the two traces, the spacing between the traces and the reference plane, and the dielectric constant of the PCB binder material. Interlayer vias introduce impedance discontinuities that can cause reflections and jitter on the signal path; therefore, it is preferable to route the TMDS lines exclusively on one layer of the board, particularly for the input traces. In addition, to prevent unwanted signal coupling and interference, route the TMDS signals away from other signals and noise sources on the PCB.

Both traces of a given differential pair must be equal in length to minimize intrapair skew. Maintaining the physical symmetry of a differential pair is integral to ensuring its signal integrity; excessive intrapair skew can introduce jitter through duty cycle distortion (DCD). The p and n of a given differential pair should always be routed together in order to establish the required 100 Ω differential impedance. Enough space should be left between the differential pairs of a given group so that the n of one pair does not couple to the p of another pair. For example, one technique is to make the interpair distance 4 to 10 times wider than the intrapair spacing.

Any group of four TMDS channels (input or output) should have closely matched trace lengths to minimize interpair skew. Severe interpair skew can cause the data on the four different channels of a group to arrive out of alignment with one another. A good practice is to match the trace lengths for a given group of four channels to within 0.05 inches on FR4 material.

The length of the TMDS traces should be minimized to reduce overall signal degradation. Commonly used PCB material, such as FR4, is lossy at high frequencies, so long traces on the circuit board increase signal attenuation, resulting in decreased signal swing and increased jitter through intersymbol interference (ISI).

Controlling the Characteristic Impedance of a TMDS Differential Pair

The characteristic impedance of a differential pair depends on a number of variables, including the trace width, the distance between the two traces, the height of the dielectric material between the trace and the reference plane below it, and the dielectric constant of the PCB binder material. To a lesser extent, the characteristic impedance also depends upon the trace thickness and the presence of solder mask.

There are many combinations that can produce the correct characteristic impedance. It is generally required to work with the PCB fabricator to obtain a set of parameters to produce the desired results.

One consideration is how to guarantee a differential pair with a differential impedance of 100 Ω over the entire length of the trace. One technique is to change the width of the traces in a differential pair based on how closely one trace is coupled to the other. When the two traces of a differential pair are close and strongly coupled, they should have a width that produces a 100 Ω differential impedance. When the traces split apart to go into a connector, for example, and are no longer so strongly coupled, the width of the traces should be increased to yield a differential impedance of 100 Ω in the new configuration.

TMDS Terminations

The AD8195 provides internal 50 Ω single-ended terminations for all of its high speed inputs and outputs. It is not necessary to include external termination resistors for the TMDS differential pairs on the PCB.

The output termination resistors of the AD8195 back terminate the output TMDS transmission lines. These back terminations act to absorb reflections from impedance discontinuities on the output traces, improving the signal integrity of the output traces and adding flexibility to how the output traces can be routed. For example, interlayer vias can be used to route the AD8195 TMDS outputs on multiple layers of the PCB without severely degrading the quality of the output signal.

Auxiliary Control Signals

There are three single-ended control signals associated with each source or sink in an HDMI/DVI application. These are CEC and two DDC lines. The two signals on the DDC bus are SDA and SCL (serial data and serial clock, respectively). These three signals can be buffered through the AD8195 and do not need to be routed with the same strict considerations as the high speed TMDS signals.

In general, it is sufficient to route each auxiliary signal as a single-ended trace. These signals are not sensitive to impedance discontinuities, do not require a reference plane, and can be routed on multiple layers of the PCB. However, it is best to follow strict layout practices whenever possible to prevent the PCB design from affecting the overall application. The specific routing of the CEC and DDC lines depends on the application in which the AD8195 is being used.

For example, the maximum speed of signals present on the auxiliary lines is 100 kHz I^2C data on the DDC lines; therefore, any layout that enables 100 kHz I^2C to be passed over the DDC bus should suffice. The HDMI specification, however, places a strict 50 pF limit on the amount of capacitance that can be measured on either SDA or SCL at the HDMI input connector. This 50 pF limit includes the HDMI connector, the PCB, and whatever capacitance is seen at the input of the AD8195. There is a similar limit of 150 pF of input capacitance for the CEC line.

The parasitic capacitance of traces on a PCB increases with trace length. To help ensure that a design satisfies the HDMI specification, the length of the CEC and DDC lines on the PCB should be made as short as possible. Additionally, if there is a reference plane in the layer adjacent to the auxiliary traces in the PCB stack-up, relieving or clearing out this reference plane immediately under the auxiliary traces significantly decreases the amount of parasitic trace capacitance. An example of the board stack-up is shown in Figure 35.

The AD8195 buffers the auxiliary signals; therefore, only the input traces, connector, and AD8195 input capacitance must be considered when designing a PCB to meet HDMI specifications.

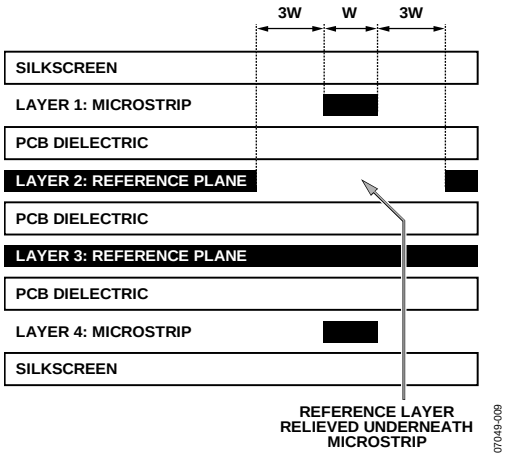


Figure 35. Example Board Stack-Up

Power Supplies

The AD8195 has four separate power supplies referenced to a single ground, AVEE. The supply/ground pairs are

- AVCC/AVEE
- VTTI/AVEE
- VTTO/AVEE
- AMUXVCC/AVEE.

The AVCC/AVEE (3.3 V) supply powers the core of the AD8195. The VTTI/AVEE supply (3.3 V) powers the input termination (see Figure 30). Similarly, the VTTO/AVEE supply (3.3 V) powers the output termination (see Figure 31). The AMUXVCC/AVEE supply (5 V) powers the auxiliary buffer core.

In a typical application, all pins labeled AVEE should be connected directly to ground. All pins labeled AVCC, VTTI, or VTTO should be connected to 3.3 V, and Pin AMUXVCC should be tied to 5 V. The AVCC supply powers the TMDS buffers while AMUXVCC powers the DDC/CEC buffers. The AMUXVCC pin can be connected to the 5 V supply provided from the input HDMI connector to ensure that the DDC and CEC buffers remain functional when the system is powered off. The supplies can also be powered individually, but care must be taken to ensure that each stage of the AD8195 is powered correctly.

DDC Reference Inputs

The VREF_IN and VREF_OUT voltages (3.3 V to 5 V) provide reference levels for the DDC buffers. Both voltages are referenced to AVEE. The voltage applied at these reference inputs should be the same as the pull-up voltage for corresponding DDC bus.

Unused DDC/CEC Buffers

If the DDC and the CEC buffers are not used, the AD8195 does not require a 5 V supply for AMUXVCC. For operation without the buffers, tie AMUXVCC to AVCC (nominally 3.3 V) and tie VREF_IN and VREF_OUT to AVEE (nominally ground). Other buffer pins can be left floating.

OUTLINE DIMENSIONS

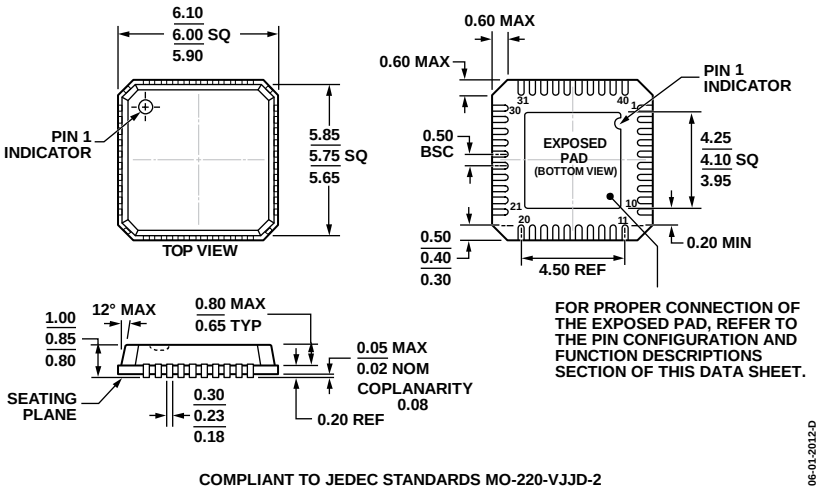


Figure 36. 40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
6 mm × 6 mm Body, Very Thin Quad
(CP-40-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
AD8195ACPZ	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-40-1	
AD8195ACPZ-R7	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_VQ], 7″Tape and Reel	CP-40-1	750
AD8195-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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