Xstream™ 3.2 Gbps Quad Buffer Mux/Demux

Data Sheet

AD8159

FEATURES

- Port level 2:1 mux/1:2 demux
- Each port consists of 4 lanes
- Each lane runs from dc to 3.2 Gbps, independent of the other lanes
- Compensates over 40 inches of FR4 at 3.2 Gbps through 2 levels of input equalization or 4 levels of output pre-emphasis
- Accepts ac- or dc-coupled differential CML inputs
- Low deterministic jitter, typically 20 ps p-p
- Low random jitter, typically 1 ps rms
- BER < 10^{-16}
- On-chip termination
- Reversible inputs and outputs on one port
- Unicast or bicast on 1:2 demux function
- Port level loopback capability
- Single lane switching capability
- 3.3 V core supply
- Flexible I/O supply down to 2.5 V
- Low power, typically 1 W in basic configuration
- 100-lead TQFP_EP
- –40°C to +85°C operating temperature range

APPLICATIONS

- Low cost redundancy switch
- SONET OC-48/SDH-16 and lower data rates
- XAUI (10 gigabit Ethernet) over backplane
- Gigabit Ethernet over backplane
- Fibre Channel 1.06 Gbps and 2.125 Gbps over backplane
- InfiniBand® over backplane
- PCI Express (PCIe) over backplane

FUNCTIONAL BLOCK DIAGRAM

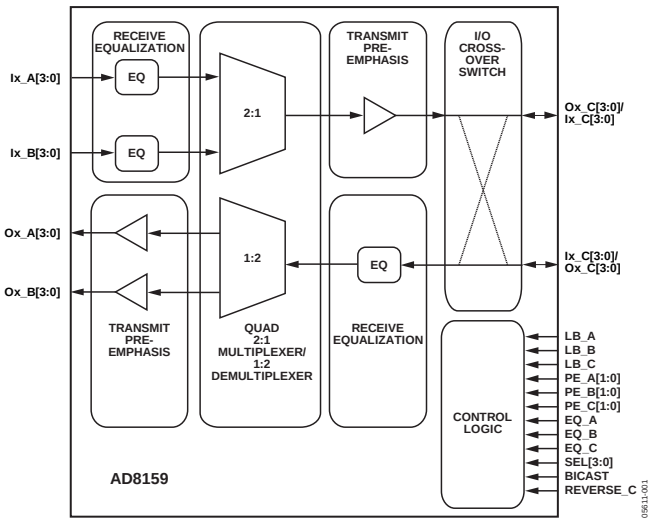


Figure 1.

GENERAL DESCRIPTION

The AD8159[1] is an asynchronous, protocol agnostic, quad-lane 2:1 switch with 12 differential PECL-/CML-compatible inputs and 12 differential CML outputs. The operation of this product is optimized for NRZ signaling with data rates of up to 3.2 Gbps per lane. Each lane offers two levels of input equalization and four levels of output pre-emphasis.

The AD8159 consists of four multiplexers and four demultiplexers, one per lane. Each port is a four-lane link, and each lane runs up to a 3.2 Gbps data rate, independent of the other lanes. The lanes are switched independently using the four select pins, SEL[3:0]; each select pin controls one lane of the port. The AD8159 has low latency and very low lane-to-lane skew.

The main application of the AD8159 is to support redundancy on both the backplane side and the line interface side of a serial link. The device has unicast and bicast capability; therefore, it can be configured to support either 1 + 1 or 1:1 redundancy.

The AD8159 supports reversing of the output and input pins on one of its ports, which helps to connect two ASICs with opposite pinouts.

The AD8159 is also used for testing high speed serial links by duplicating incoming data and sending it to the destination port and to the test equipment simultaneously.

[1] Product covered by one or more patents: U.S. Patent No. 7,813,706.

Rev. C

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REVISION HISTORY

10/2018—Rev. B to Rev. C

Added Patent Information ... 1

5/2009—Rev. A to Rev. B

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4/2006—Rev. 0 to Rev. A

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9/2005—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 3.3 V, V_{EE} = 0 V, R_L = 50 Ω, basic configuration,[1] data rate = 3.2 Gbps, input common-mode voltage = 2.7 V, differential input swing = 800 mV p-p, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Data Rate/Channel (NRZ)		DC		3.2	Gbps
Deterministic Jitter	Data rate = 3.2 Gbps; see Figure 21		20		ps p-p
Random Jitter	RMS; see Figure 24		1		ps
Propagation Delay	Input to output		600		ps
Lane-to-Lane Skew			100		ps
Switching Time			5		ns
Output Rise/Fall Time	20% to 80%		100		ps
INPUT CHARACTERISTICS					
Input Voltage Swing	Port C, differential, V_{ICM}[2] = V_{CC} − 0.6 V; see Figure 22	200		2000	mV p-p
	Port A/Port B, differential, V_{ICM}[2] = V_{CC} − 0.6 V; see Figure 22	100		2000	mV p-p
Input Voltage Range	Common mode, V_{ID}[3] = 800 mV p-p; see Figure 25	V_{EE} + 1.8		V_{CC} + 0.3	V
Input Bias Current			4		µA
Input Capacitance			2		pF
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Differential, PE = 0		800		mV p-p
Output Voltage Range	Single-ended absolute voltage level; see Figure 26	V_{CC} − 1.6		V_{CC} + 0.6	V
Output Current	Port A/Port B, PE_A/PE_B = 0		16		mA
	Port C, PE_C = 0		20		mA
	Port A/Port B, PE_A/PE_B = 3		28		mA
	Port C, PE_C = 3		32		mA
Output Capacitance			2		pF
TERMINATION CHARACTERISTICS					
Resistance	Differential	90	100	110	Ω
Temperature Coefficient			0.15		Ω/°C
POWER SUPPLY					
Operating Range					
V_{CC}	V_{EE} = 0 V	3.0	3.3	3.6	V
V_{TTI}, V_{TTO}, V_{TTIO}, V_{TTOI}		2.4	3.3	3.6	V
Supply Current	Basic configuration,[1] dc-coupled inputs/outputs, 400 mV I/O swings (800 mV p-p differential), 50 Ω far-end terminations				
I_{CC}			175		mA
$I_{I/O}$ = I_{TTO} + I_{TTOI} + I_{TTI} + I_{TTIO}			144		mA
Supply Current	BICAST = 1, PE = 3 on all ports, dc-coupled inputs/outputs, 400 mV I/O swings (800 mV p-p differential), 50 Ω far-end terminations				
I_{CC}			255		mA
$I_{I/O}$ = I_{TTO} + I_{TTOI} + I_{TTI} + I_{TTIO}			352		mA
THERMAL CHARACTERISTICS					
Operating Temperature Range		−40		+85	°C
θ_{JA}	Still air		29		°C/W
θ_{JB}	Still air		16		°C/W
θ_{JC}	Still air		13		°C/W
LOGIC INPUT CHARACTERISTICS					
Input Voltage High, V_{IH}		2.4		V_{CC}	V
Input Voltage Low, V_{IL}		V_{EE}		0.8	V

[1] BICAST off, loopback off on all ports, pre-emphasis off on all ports, equalization set to minimum on all ports.
[2] V_{ICM} is the input common-mode voltage.
[3] V_{ID} is the input differential peak-to-peak voltage swing.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{CC} to V_{EE}	3.7 V
V_{TTI}	V_{CC} + 0.6 V
V_{TTIO}	V_{CC} + 0.6 V
V_{TTO}	V_{CC} + 0.6 V
V_{TTOI}	V_{CC} + 0.6 V
Internal Power Dissipation	4.26 W
Differential Input Voltage	2.0 V
Logic Input Voltage	V_{EE} − 0.3 V < V_{IN} < V_{CC} + 0.6 V
Storage Temperature Range	−65°C to +125°C
Lead Temperature	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

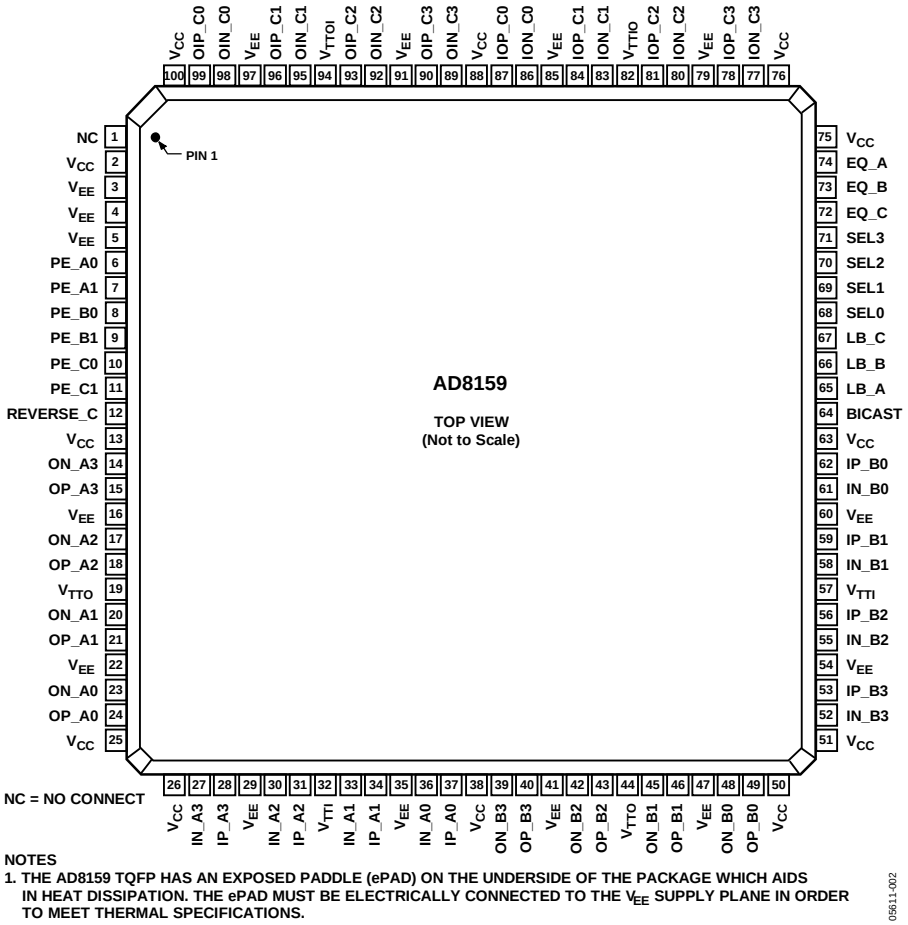


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	NC	N/A	No Connect
2, 13, 25, 26, 38, 50, 51, 63, 75, 76, 88, 100	V_{CC}	Power	Positive Supply
3 to 5, 16, 22, 29, 35, 41, 47, 54, 60, 79, 85, 91, 97, EPAD	V_{EE}	Power	Negative Supply
6	PE_A0	Control	Pre-Emphasis Control for Port A (LSB)
7	PE_A1	Control	Pre-Emphasis Control for Port A (MSB)
8	PE_B0	Control	Pre-Emphasis Control for Port B (LSB)
9	PE_B1	Control	Pre-Emphasis Control for Port B (MSB)
10	PE_C0	Control	Pre-Emphasis Control for Port C (LSB)
11	PE_C1	Control	Pre-Emphasis Control for Port C (MSB)
12	REVERSE_C	Control	Reverse Inputs and Outputs on Port C
14	ON_A3	Output	High Speed Output Complement
15	OP_A3	Output	High Speed Output
17	ON_A2	Output	High Speed Output Complement
18	OP_A2	Output	High Speed Output
19, 44	V_{TTO}	Power	Port A and Port B Output Termination Supply

Pin No.	Mnemonic	Type	Description
20	ON_A1	Output	High Speed Output Complement
21	OP_A1	Output	High Speed Output
23	ON_A0	Output	High Speed Output Complement
24	OP_A0	Output	High Speed Output
27	IN_A3	Input	High Speed Input Complement
28	IP_A3	Input	High Speed Input
30	IN_A2	Input	High Speed Input Complement
31	IP_A2	Input	High Speed Input
32, 57	V_{TTI}	Power	Port A and Port B Input Termination Supply
33	IN_A1	Input	High Speed Input Complement
34	IP_A1	Input	High Speed Input
36	IN_A0	Input	High Speed Input Complement
37	IP_A0	Input	High Speed Input
39	ON_B3	Output	High Speed Output Complement
40	OP_B3	Output	High Speed Output
42	ON_B2	Output	High Speed Output Complement
43	OP_B2	Output	High Speed Output
45	ON_B1	Output	High Speed Output Complement
46	OP_B1	Output	High Speed Output
48	ON_B0	Output	High Speed Output Complement
49	OP_B0	Output	High Speed Output
52	IN_B3	Input	High Speed Input Complement
53	IP_B3	Input	High Speed Input
55	IN_B2	Input	High Speed Input Complement
56	IP_B2	Input	High Speed Input
58	IN_B1	Input	High Speed Input Complement
59	IP_B1	Input	High Speed Input
61	IN_B0	Input	High Speed Input Complement
62	IP_B0	Input	High Speed Input
64	BICAST	Control	Bicast Enable
65	LB_A	Control	Loopback Enable for Port A
66	LB_B	Control	Loopback Enable for Port B
67	LB_C	Control	Loopback Enable for Port C
68	SEL0	Control	$\overline{A}$/B Select for Lane 0
69	SEL1	Control	$\overline{A}$/B Select for Lane 1
70	SEL2	Control	$\overline{A}$/B Select for Lane 2
71	SEL3	Control	$\overline{A}$/B Select for Lane 3
72	EQ_C	Control	Equalization Control for Port C
73	EQ_B	Control	Equalization Control for Port B
74	EQ_A	Control	Equalization Control for Port A
77	ION_C3	Input/Output	High Speed Input/Output Complement
78	IOP_C3	Input/Output	High Speed Input/Output
80	ION_C2	Input/Output	High Speed Input/Output Complement
81	IOP_C2	Input/Output	High Speed Input/Output
82	V_{TTIO}	Power	Port C Input/Output Termination Supply
83	ION_C1	Input/Output	High Speed Input/Output Complement
84	IOP_C1	Input/Output	High Speed Input/Output
86	ION_C0	Input/Output	High Speed Input/Output Complement
87	IOP_C0	Input/Output	High Speed Input/Output

Pin No.	Mnemonic	Type	Description
89	OIN_C3	Output/Input	High Speed Output/Input Complement
90	OIP_C3	Output/Input	High Speed Output/Input
92	OIN_C2	Output/Input	High Speed Output/Input Complement
93	OIP_C2	Output/Input	High Speed Output/Input
94	V_{TTOI}	Power	Port C Output/Input Termination Supply
95	OIN_C1	Output/Input	High Speed Output/Input Complement
96	OIP_C1	Output/Input	High Speed Output/Input
98	OIN_C0	Output/Input	High Speed Output/Input Complement
99	OIP_C0	Output/Input	High Speed Output/Input

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3 V, V_{EE} = 0 V, R_L = 50 Ω, basic configuration, data rate = 3.2 Gbps, input common-mode voltage = 2.7 V, differential input swing = 800 mV p-p, T_A = 25°C, unless otherwise noted. All graphs were generated using the setup shown in Figure 31, unless otherwise specified.

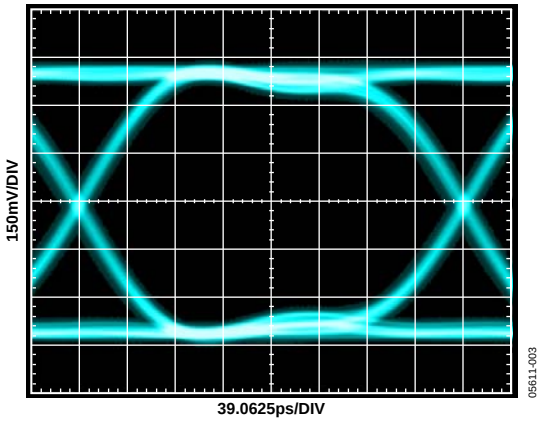


Figure 3. Output Port A Eye Diagram, 3.2 Gbps, Input Port A or Input Port C

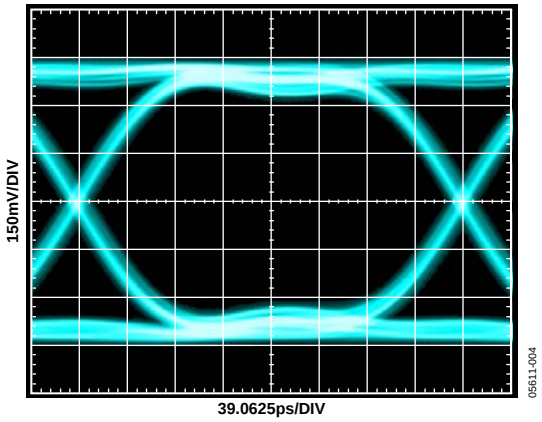


Figure 4. Output Port B Eye Diagram, Input Port B or Input Port C

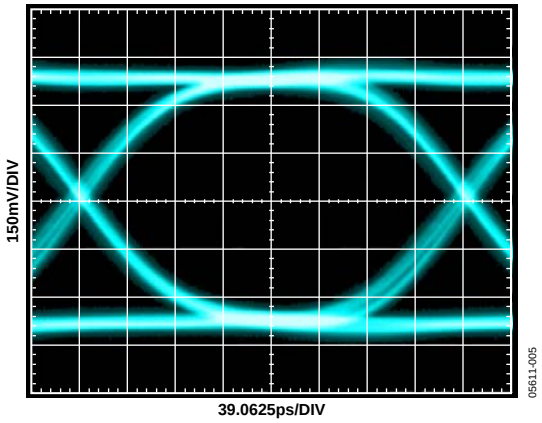


Figure 5. Output Port C Eye Diagram, 3.2 Gbps, Input Port A or Input Port B

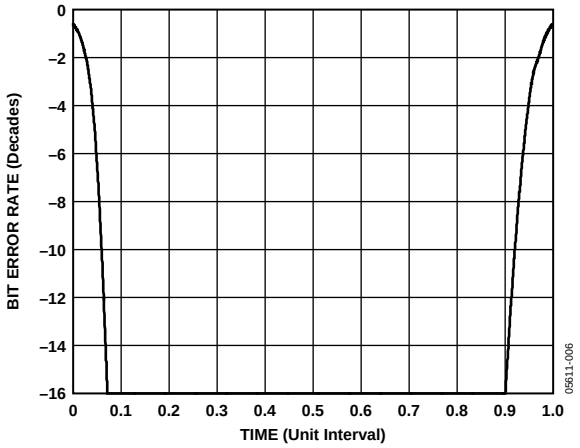


Figure 6. Output Port A Bathtub Curve, 3.2 Gbps

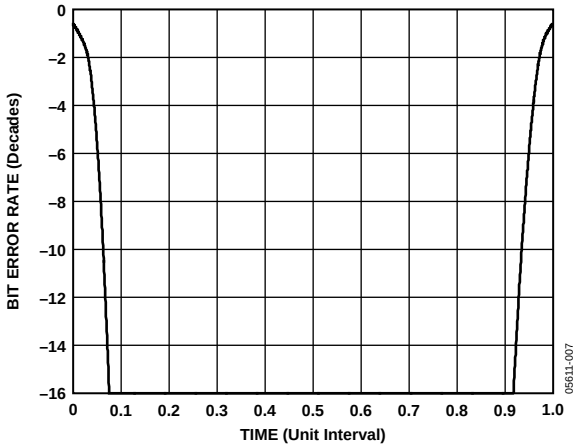


Figure 7. Output Port B Bathtub Curve, 3.2 Gbps

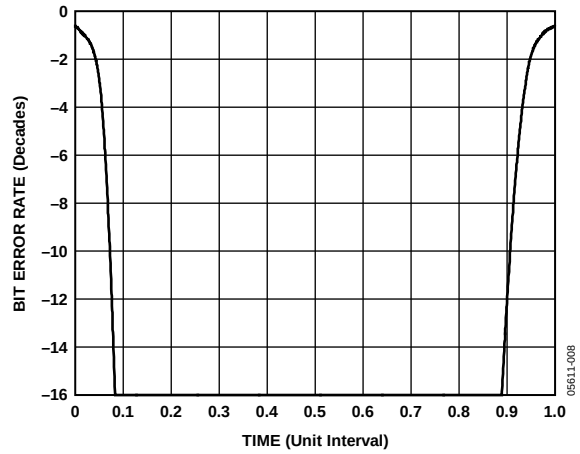


Figure 8. Output Port C Bathtub Curve, 3.2 Gbps

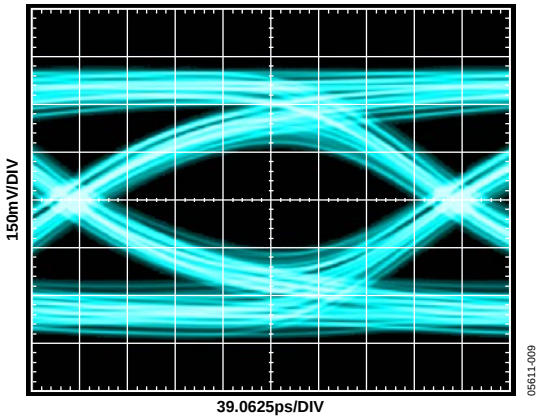


Figure 9. Eye Diagram over Backplane
(18″ FR4 + 2 GbX Connectors), PE = 0

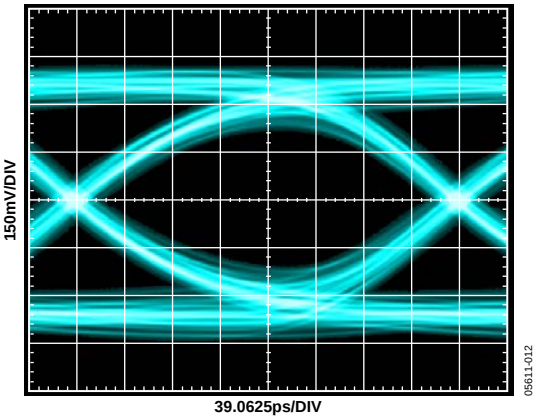


Figure 12. Eye Diagram over Backplane
(18″ FR4 + 2 GbX Connectors), PE = 1

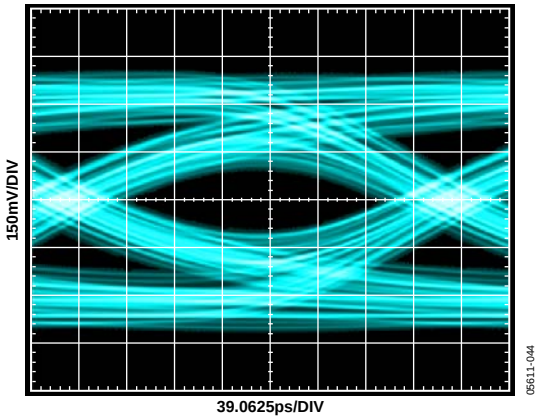


Figure 10. Eye Diagram over Backplane
(30″ FR4 + 2 GbX Connectors), PE = 0

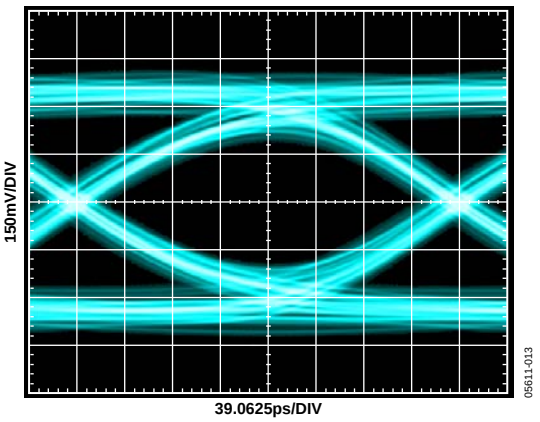


Figure 13. Eye Diagram over Backplane
(30″ FR4 + 2 GbX Connectors), PE = 2

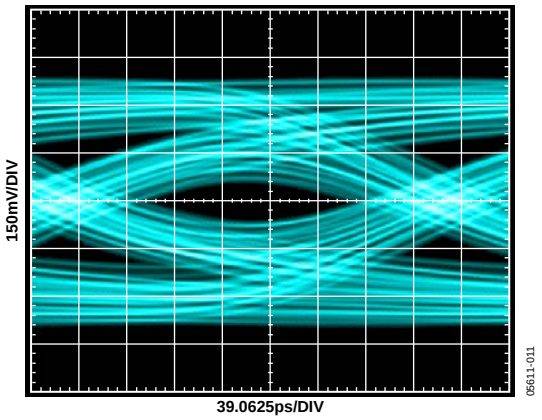


Figure 11. Eye Diagram over Backplane
(36″ FR4 + 2 GbX Connectors), PE = 0

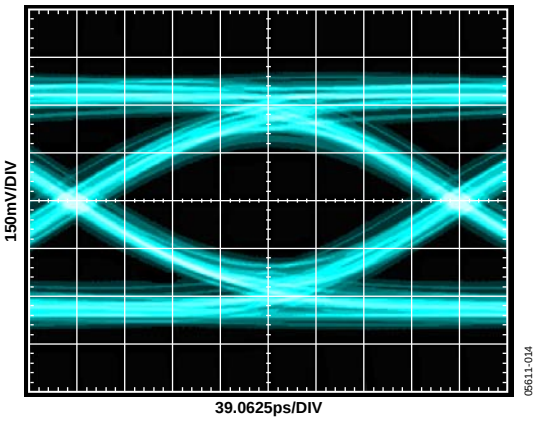


Figure 14. Eye Diagram over Backplane
(36″ FR4 + 2 GbX Connectors), PE = 3

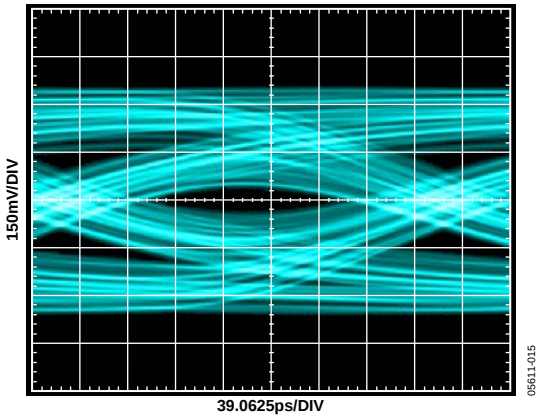


Figure 15. Eye Diagram over Backplane (42" FR4 + 2 GbX Connectors), PE = 0

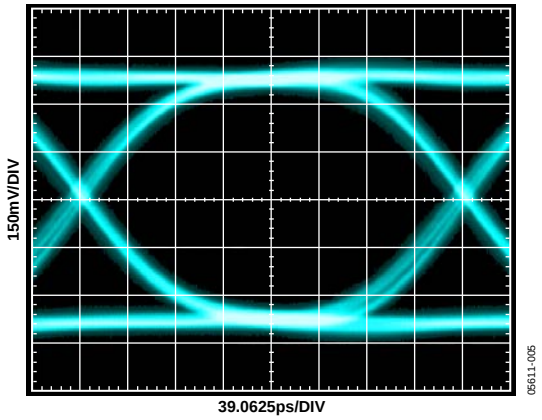


Figure 16. Reference Eye Diagram for Figure 19

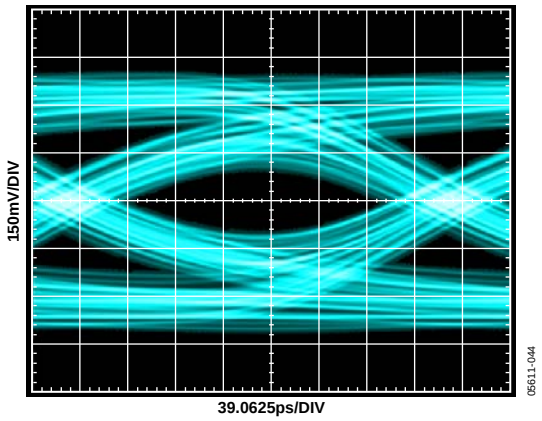


Figure 17. Reference Eye Diagram for Figure 20

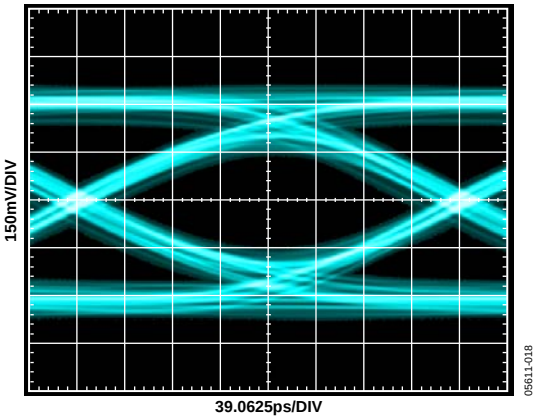


Figure 18. Eye Diagram over Backplane (42" FR4 + 2 GbX Connectors), PE = 3

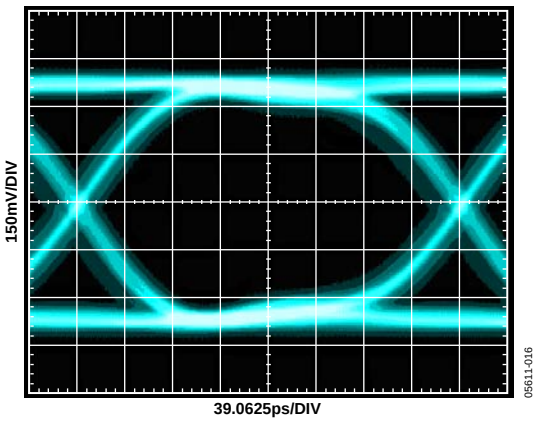


Figure 19. Eye Diagram with Equalization (10" FR4), EQ = 0, See Figure 32 for Test Circuit Used

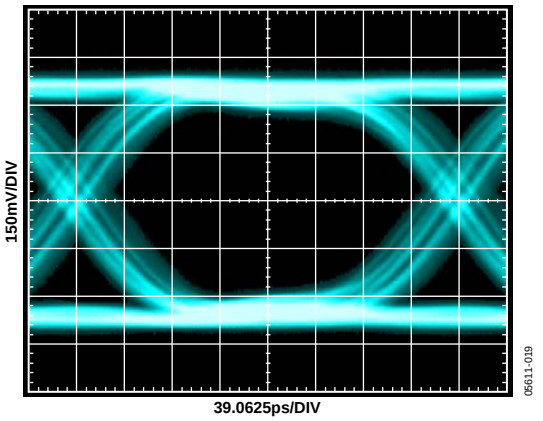


Figure 20. Eye Diagram with Equalization (34" FR4 + 2 GbX Connectors), EQ = 1, See Figure 32 for Test Circuit Used

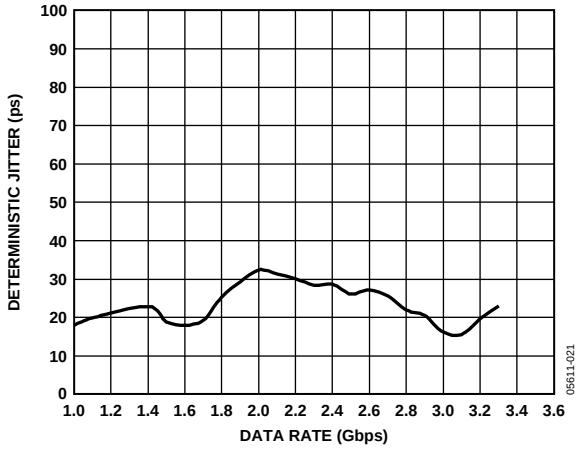


Figure 21. Deterministic Jitter vs. Data Rate

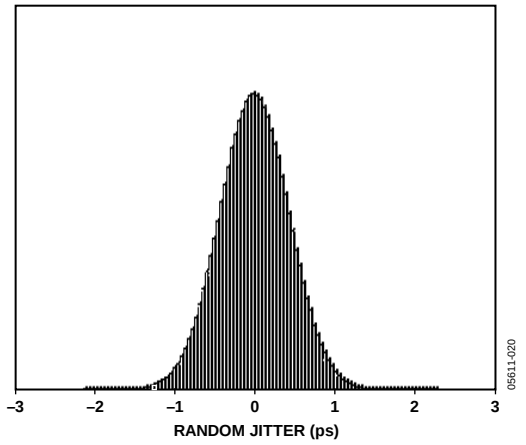


Figure 24. Random Jitter Histogram, See Figure 33 for Test Circuit Used

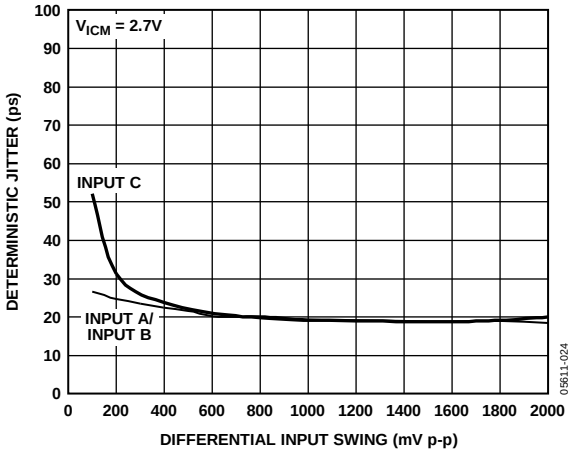


Figure 22. Deterministic Jitter vs. Differential Input Swing

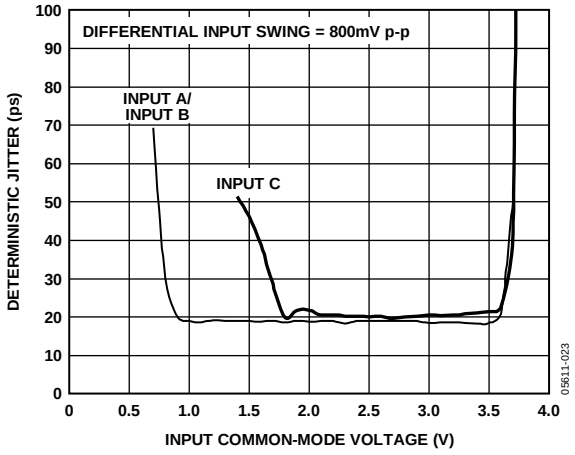


Figure 25. Deterministic Jitter vs. Input Common-Mode Voltage

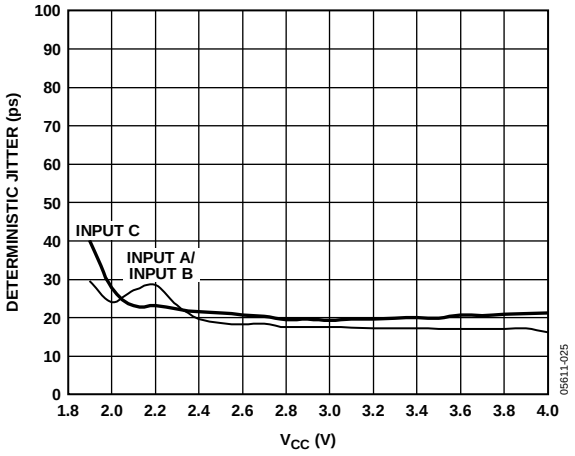


Figure 23. Deterministic Jitter vs. Core Supply Voltage

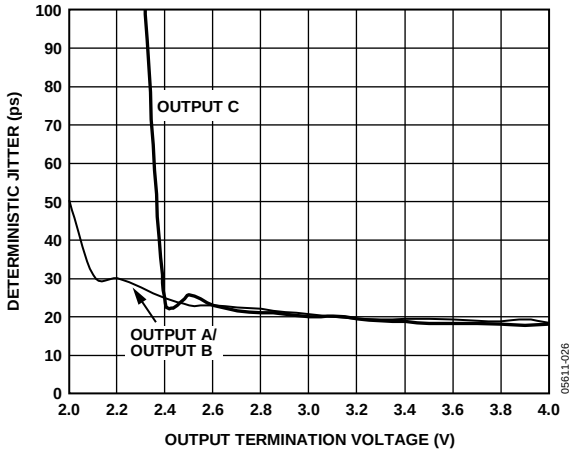


Figure 26. Deterministic Jitter vs. Output Termination Voltage

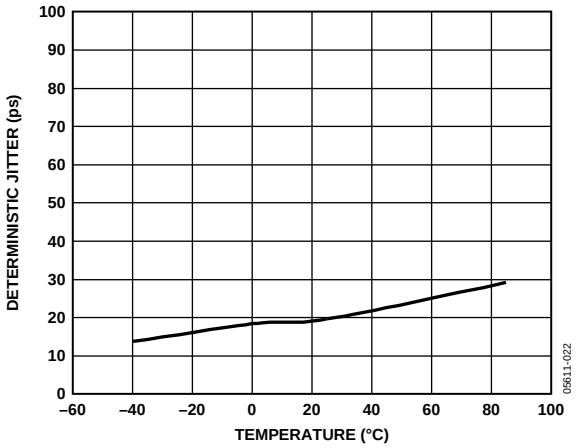


Figure 27. Deterministic Jitter vs. Temperature

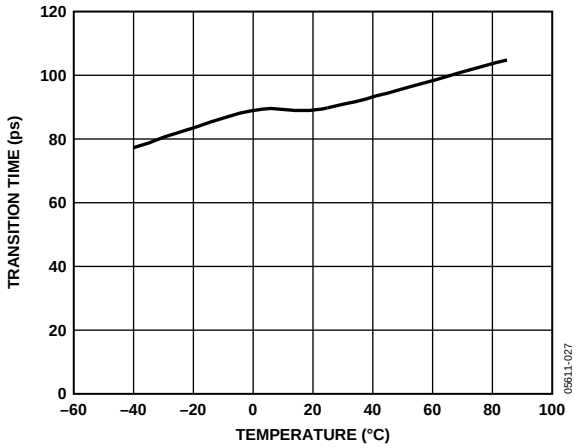


Figure 28. Transition Time vs. Temperature,

EVALUATION BOARD SIMPLIFIED BLOCK DIAGRAM

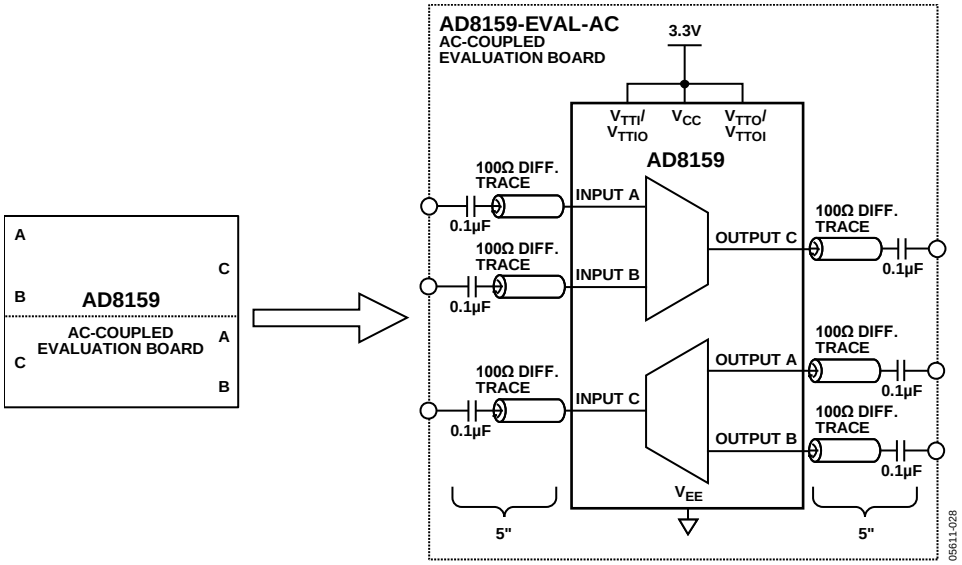


Figure 29. AC-Coupled Evaluation Board Simplified Block Diagram

TEST CIRCUITS

All graphs were generated using the setup shown in Figure 31, unless otherwise specified.

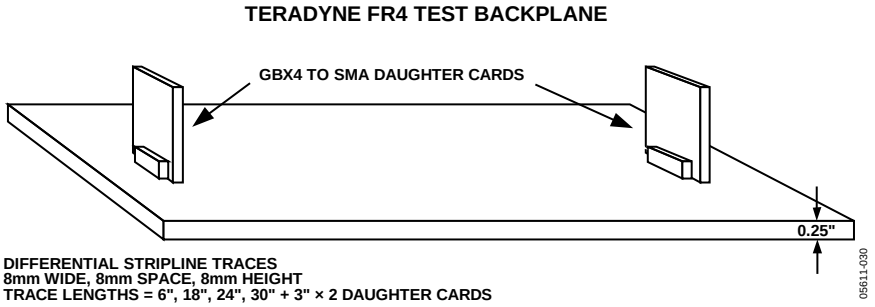


Figure 30. Test Backplane

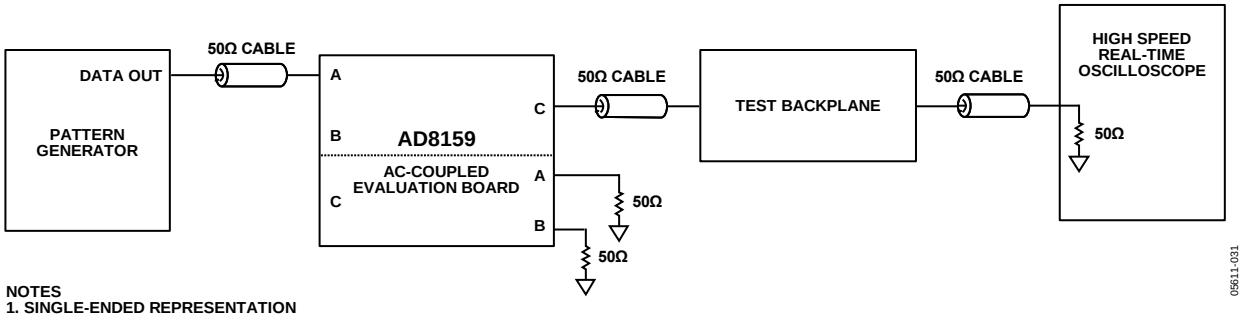


Figure 31. AC-Coupled Test Circuit

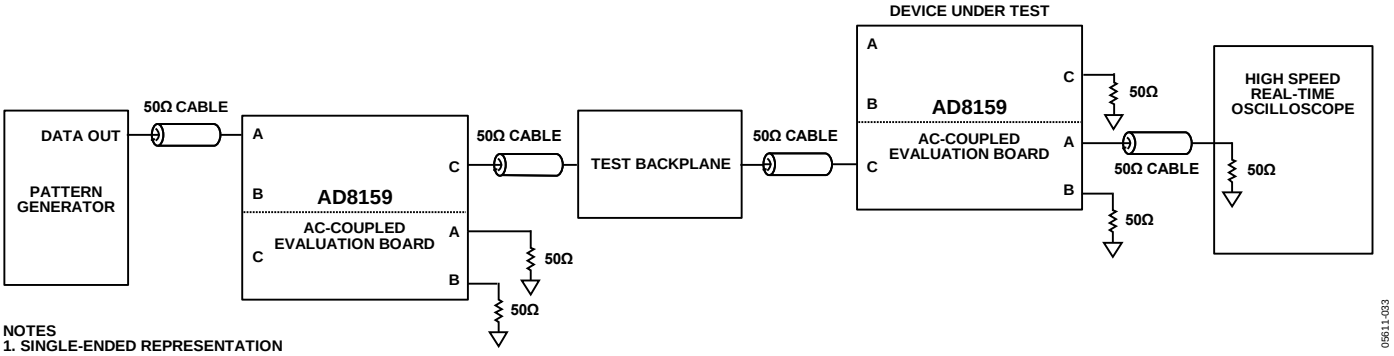


Figure 32. Equalization Test Circuit, Test Circuit Used for Figure 19 and Figure 20

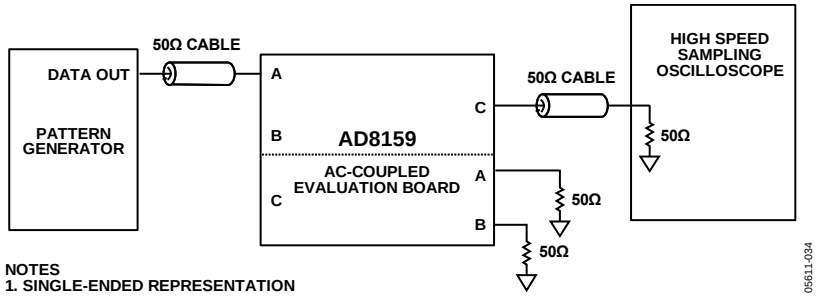


Figure 33. Random Jitter Test Circuit, Test Circuit Used for Figure 24

THEORY OF OPERATION

The AD8159 relays received data on the demultiplexer Input Port C to Output Port A and/or Output Port B, depending on the mode selected by the BICAST control pin. On the multiplexer side, the AD8159 relays received data on either Input Port A or Input Port B to the Output Port C, based on the SEL[3:0] pin states.

The AD8159 is configured by toggling control pins. On the demultiplexer side, when the device is configured in unicast mode, it sends the received data on Input Port C to Output Port A or Output Port B. When the device is configured in bicast mode, received data on Input Port C is sent to both Output Port A and Output Port B.

On the multiplexer side, only received data on Input Port A or Input Port B is sent to Output Port C, depending on the state of the SEL[3:0] pins. Table 4 summarizes port selection and configuration when loopback is disabled (LB_A = LB_B = LB_C = 0).

When the device is in unicast mode, the output lanes on either Port A or Port B are in an idle state. In the idle state, the output tail current is set to 0 mA, and the P and N sides of the lane are pulled up to the output termination voltage through the on-chip termination resistors.

Table 4. Port Selection and Configuration Table

SELx	BICAST	OUT_A	OUT_B	OUT_C
0	0	IN_C	Idle	IN_A
0	1	IN_C	IN_C	IN_A
1	0	Idle	IN_C	IN_B
1	1	IN_C	IN_C	IN_B

INPUT EQUALIZATION (EQ) AND OUTPUT PRE-EMPHASIS (PE)

In backplane applications, the AD8159 needs to compensate for signal degradation over potentially long traces. The device supports two levels of input equalization, configured on a per-port basis. Table 5 summarizes the high frequency gain (EQ) for each control setting, as well as the typical length of backplane trace that can be compensated for each setting.

Table 5. Input Equalization Settings

EQ_x	EQ (dB)	Typical Backplane Length (Inches)
0	6	0 to 20
1	12	20 to 40+

The AD8159 also has four levels of output pre-emphasis, configured for each port. The pre-emphasis circuitry adds a controlled amount of overshoot to the output waveform to compensate for the loss in a backplane trace.

Table 6 summarizes the high frequency gain, amount of overshoot, and the typical backplane channel length (including two connectors) that can be compensated for using each setting. A typical backplane is made of FR4 material with 8 mil wide traces and 8 mil spacing, loosely coupled differential traces. Each backplane channel consists of two connectors. The total length of the channel includes 3 inches of traces on each card.

Table 6. Output Pre-Emphasis Settings

PE_x[1]	PE_x[0]	PE (dB)	Overshoot	Typical Backplane Length (Inches)
0	0	0	0%	0 to 10
0	1	1.9	15%	10 to 20
1	0	3.5	35%	20 to 30
1	1	4.9	60%	30 to 40+

LOOPBACK

The AD8159 also supports port level loopback, as is shown in Figure 34. The loopback control pins override the lane select (SEL[3:0]) and bicast control (BICAST) pins. Table 7 summarizes the different loopback configurations.

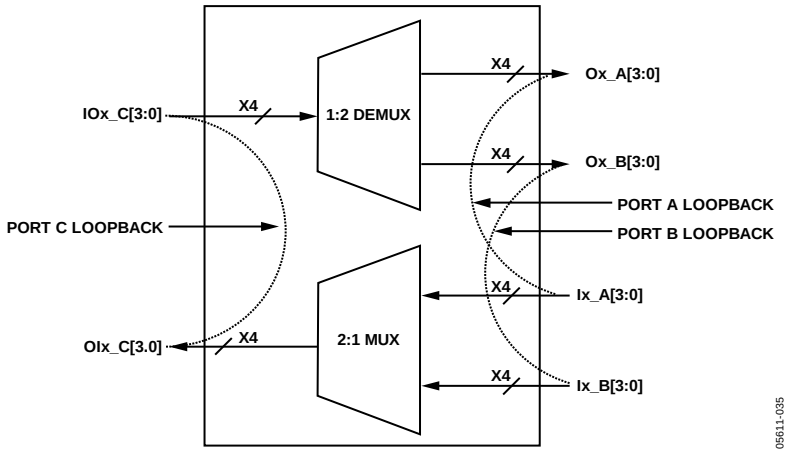


Figure 34. Port-Based Loopback Capability

Table 7. Loopback, Bicast, and Port Select Settings[1]

LB_A	LB_B	LB_C	SELx	BICAST	OUT_A	OUT_B	OUT_C
0	0	0	0	0	IN_C	Idle	IN_A
0	0	0	0	1	IN_C	IN_C	IN_A
0	0	0	1	0	Idle	IN_C	IN_B
0	0	0	1	1	IN_C	IN_C	IN_B
0	0	1	0	0	IN_C	Idle	IN_C
0	0	1	X[2]	1	IN_C	IN_C	IN_C
0	0	1	1	0	Idle	IN_C	IN_C
0	1	0	0	X[2]	IN_C	IN_B	IN_A
0	1	0	1	0	Idle	IN_B	IN_B
0	1	0	1	1	IN_C	IN_B	IN_B
0	1	1	0	X[2]	IN_C	IN_B	IN_C
0	1	1	1	0	Idle	IN_B	IN_C
0	1	1	X[2]	1	IN_C	IN_B	IN_C
1	0	0	0	0	IN_A	Idle	IN_A
1	0	0	0	1	IN_A	IN_C	IN_A
1	0	0	1	X[2]	IN_A	IN_C	IN_B
1	0	1	0	0	IN_A	Idle	IN_C
1	0	1	X[2]	1	IN_A	IN_C	IN_C
1	0	1	1	X[2]	IN_A	IN_C	IN_C
1	1	0	0	X[2]	IN_A	IN_B	IN_A
1	1	0	1	X[2]	IN_A	IN_B	IN_B
1	1	1	X[2]	X[2]	IN_A	IN_B	IN_C

[1] Switching is done on a lane-by-lane basis, but input equalization, output pre-emphasis, and loopback are set for each port.
[2] Don't care.

PORT C REVERSE (CROSSOVER) CAPABILITY

Port C has a reversible I/O capability. The sense (input vs. output) of the Port C pins can be swapped by toggling the REVERSE_C control pin. This feature was added to facilitate the connection to different ASICs that may have the opposite pinouts.

Figure 35 illustrates the reversible I/O function of Port C, and Table 8 describes this function in a selection table that corresponds to a TQFP-100 package. Note that the reverse capability is supported only on Port C.

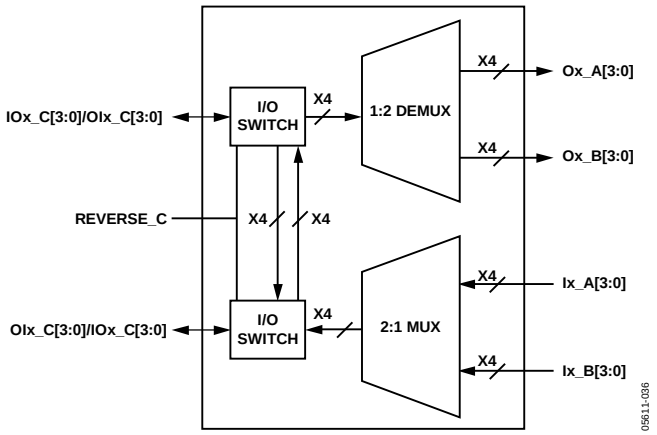


Figure 35. Port C Reverse I/O Capability

Table 8. Port C I/O Selection

	Port C When REVERSE_C = 0		Port C When REVERSE_C = 1	
Port C Pin List on 100-Lead TQFP	**Pin Name**	**Input/Output Pin**	**Pin Name**	**Input/Output Pin**
77	ION_C3 = INN_C3	Input	ION_C3 = OUTN_C3	Output
78	IOP_C3 = INP_C3	Input	IOP_C3 = OUTP_C3	Output
80	ION_C2 = INN_C2	Input	ION_C2 = OUTN_C2	Output
81	IOP_C2 = INP_C2	Input	IOP_C2 = OUTP_C2	Output
83	ION_C1 = INN_C1	Input	ION_C1 = OUTN_C1	Output
84	IOP_C1 = INP_C1	Input	IOP_C1 = OUTP_C1	Output
86	ION_C0 = INN_C0	Input	ION_C0 = OUTN_C0	Output
87	IOP_C0 = INP_C0	Input	IOP_C0 = OUTP_C0	Output
89	OIN_C3 = OUTN_C3	Output	OIN_C3 = INN_C3	Input
90	OIP_C3 = OUTP_C3	Output	OIP_C3 = INP_C3	Input
92	OIN_C2 = OUTN_C2	Output	OIN_C2 = INN_C2	Input
93	OIP_C2 = OUTP_C2	Output	OIP_C2 = INP_C2	Input
95	OIN_C1 = OUTN_C1	Output	OIN_C1 = INN_C1	Input
96	OIP_C1 = OUTP_C1	Output	OIP_C1 = INP_C1	Input
98	OIN_C0 = OUTN_C0	Output	OIN_C0 = INN_C0	Input
99	OIP_C0 = OUTP_C0	Output	OIP_C0 = INP_C0	Input

APPLICATIONS INFORMATION

The main application of the AD8159 is to support redundancy on both the backplane side and the line interface side of a serial link. Each port consists of four lanes to support standards such as XAUI. Figure 36 illustrates redundancy in an XAUI backplane system. Each line card is connected to two switch fabrics (primary and redundant). The device can be configured to support either 1 + 1 or 1:1 redundancy.

Another application for the AD8159 is test equipment for evaluating high speed serial I/Os running at data rates at or lower than 3.2 Gbps. Figure 37 illustrates the module redundancy of a line card application. Figure 38 illustrates a possible application of the AD8159 in a simple XAUI link tester.

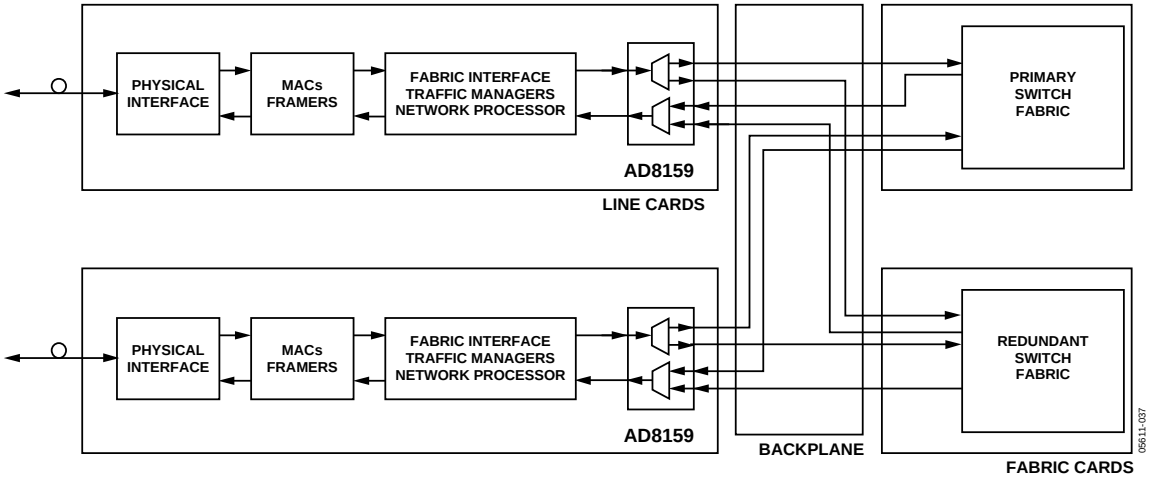


Figure 36. Using the AD8159 for Switch Redundancy

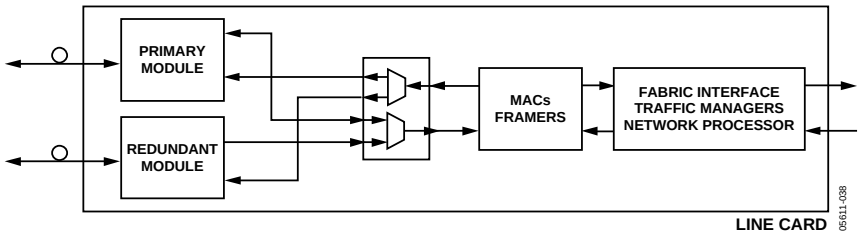


Figure 37. Using the AD8159 for Line Interface Redundancy

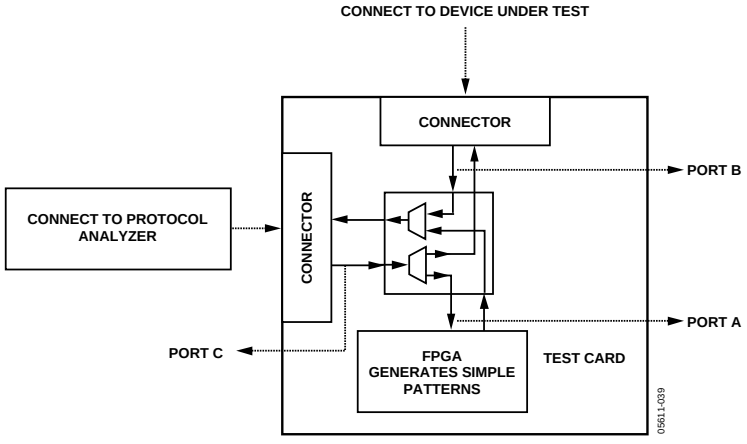


Figure 38. Using the AD8159 in Test Equipment

INTERFACING TO THE AD8159

TERMINATION STRUCTURES

To determine the best strategy for connecting to the high speed pins of the AD8159, the user must first be familiar with the on-chip termination structures. The AD8159 contains multiple types of these structures (see Figure 39, Figure 40, and Figure 41). Note that Port C has a slightly modified termination structure to support the bidirectional feature.

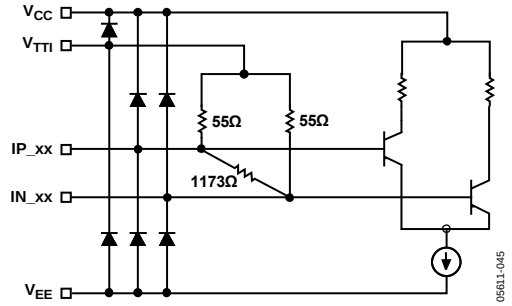


Figure 39. Simplified Input Circuit

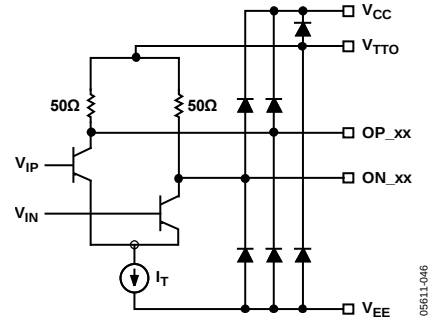


Figure 40. Simplified Output Circuit (Port A or Port B)

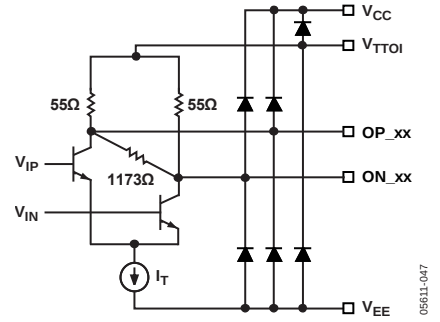


Figure 41. Simplified Output Circuit (Port C)

For input and bidirectional ports, the termination structure consists of two 55 Ω resistors connected to a termination supply and an 1173 Ω resistor connected across the differential inputs, the latter being a result of the finite differential input impedance of the equalizer.

For output ports, there are two 50 Ω resistors connected to the termination supply. Note that the differential input resistance for both structures is the same, 100 Ω.

INPUT COMPLIANCE

The range of allowable input voltages is determined by the fundamental limitations of the active input circuitry. This range of signals is normally a function of the common-mode level of the input signal, the signal swing, and the supply voltage. For a given input signal swing, there is a range of common-mode voltages that keeps the high and low voltage excursions within acceptable limits. Similarly, for a given common-mode input voltage, there is a maximum acceptable input signal swing. There is also a minimum signal swing that the active input circuitry can resolve reliably.

Figure 22 and Figure 25 summarize the input voltage ranges for all ports. Note that the input range is different when comparing bidirectional ports to strictly input ports. This is a consequence of the additional circuitry required to support the bidirectional feature on Port C.

AC Coupling

One way to simplify the input circuit and make it compatible with a wide variety of driving devices is to use ac coupling. This has the effect of isolating the dc common-mode levels of the driver and the AD8159 input circuitry. AC coupling requires a capacitor in series with each single-ended input signal, as shown in Figure 42. This should be done in a manner that does not interfere with the high speed signal integrity of the PCB.

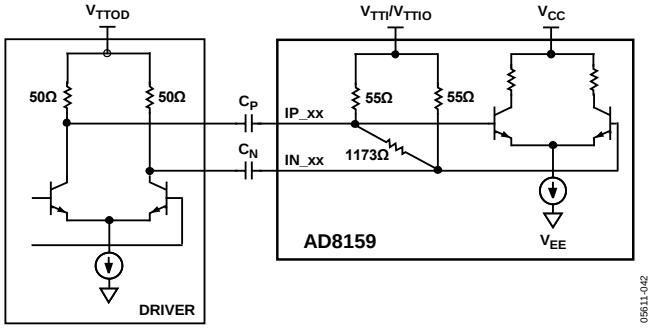


Figure 42. AC Coupling Input Signal of the AD8159

When ac coupling is used, the common-mode level at the input of the device is equal to V_{TTI}. The single-ended input signal swings above and below V_{TTI} equally. The user can then use Figure 22 and Figure 25 to determine the acceptable range of common-mode levels and signal swing levels that satisfy the input range of the AD8159.

If dc coupling is required, determining the input common-mode level is less straightforward because the configuration of the driver must also be considered. In most cases, the user sets V_{TTI} on the AD8159 to the same level as the driver output termination voltage, V_{TTOD}. This prevents a continuous dc current from flowing between the two supplies. As a practical matter, both devices can be terminated to the same physical supply.

Consider the following example: a driver dc-coupled to the input of the AD8159. The AD8159 input termination voltage (V_{TTI}) and the driver output termination voltage (V_{TTOD}) are both set to the same level; that is, $V_{TTI} = V_{TTOD} = 3.3$ V. If an 800 mV p-p differential swing is desired, the total output current of the driver is 16 mA. At balance, the output current is divided evenly between the two sides of the differential signal path, 8 mA to each side. This 8 mA of current flows through the parallel combination of the 55 Ω input termination resistor on the AD8159 and the 50 Ω output termination resistor on the driver, resulting in a common-mode level of

$$V_{TTI} - 8\text{ mA} \times (50\ \Omega \parallel 55\ \Omega) = V_{TTI} - 210\text{ mV}$$

The user can then use Figure 25 to determine the allowable range of values for V_{TTI} that meets the input compliance range based on an 800 mV p-p differential swing.

OUTPUT COMPLIANCE

Figure 43 is depicts the single-ended waveform at the output of the AD8159. The common-mode level (V_{OCM}) and the amplitude ($V_{OSE-BOOST}$) of this waveform are a function of the output tail current (I_T), the output termination supply voltage (V_{TTO}), the topology of the far-end receiver, and whether ac coupling or dc coupling is used. Keep in mind that the output tail current varies with the pre-emphasis level. The user must ensure that the high (V_H) and low (V_L) voltage excursions at the output are within the single-ended absolute voltage range limits as specified in Table 1. Failure to understand the implications of output signal levels and the choice of ac coupling or dc coupling may lead to transistor saturation and poor transmitter performance.

Table 9 and Table 10 show the typical output levels for Port A/ Port B and Port C, respectively, where $V_{CC} = V_{TTO} = 3.3$ V, with 50 Ω far-end terminations to a 3.3 V supply.

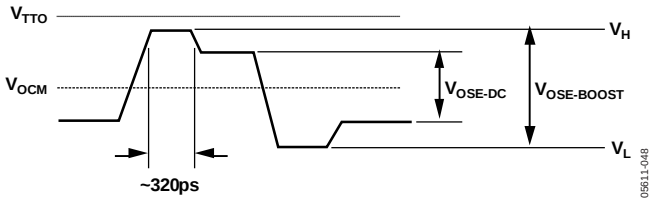


Figure 43. Single-Ended Output Waveform

Table 9. Output Voltage Levels for Port A and Port B

				DC-Coupled			AC-Coupled		
PE Setting	**I_T (mA)**	**V_{OSE-DC} (mV p-p)**	**$V_{OSE-BOOST}$ (mV p-p)**	**V_{OCM} (V)**	**V_H (V)**	**V_L (V)**	**V_{OCM} (V)**	**V_H (V)**	**V_L (V)**
0	16	400	400	3.1	3.3	2.9	2.9	3.1	2.7
1	20	400	500	3.05	3.3	2.8	2.8	3.05	2.55
2	24	400	600	3	3.3	2.7	2.7	3	2.4
3	28	400	700	2.95	3.3	2.6	2.6	2.95	2.25

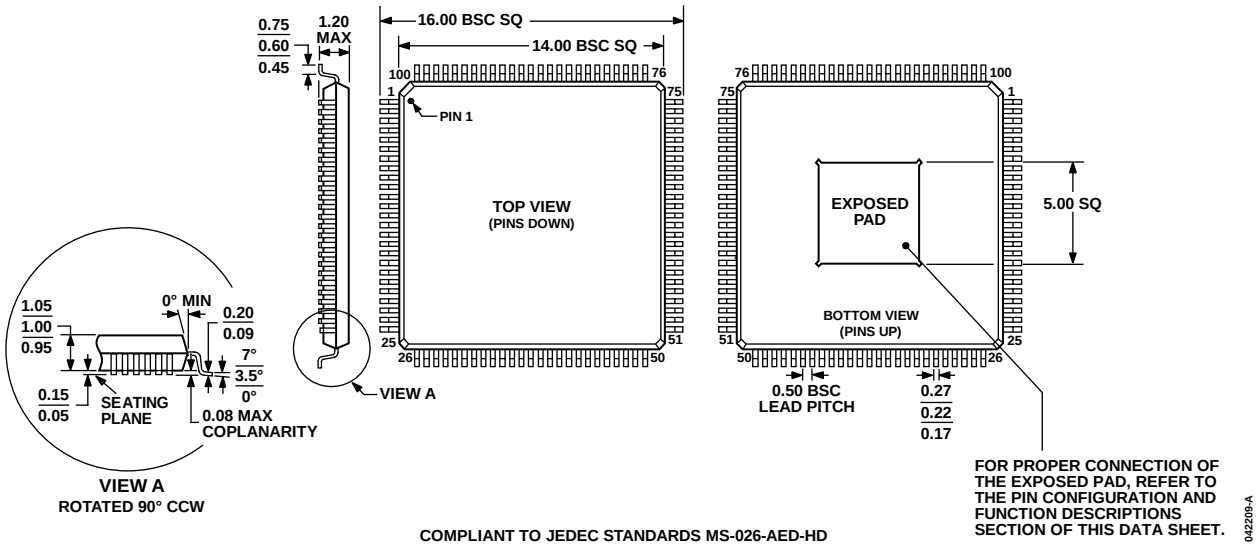
Table 10. Output Voltage Levels for Port C

				DC-Coupled			AC-Coupled		
PE Setting	**I_T (mA)**	**V_{OSE-DC} (mV p-p)**	**$V_{OSE-BOOST}$ (mV p-p)**	**V_{OCM} (V)**	**V_H (V)**	**V_L (V)**	**V_{OCM} (V)**	**V_H (V)**	**V_L (V)**
0	20	400	400	3.05	3.25	2.85	2.8	3	2.6
1	24	400	500	3	3.25	2.75	2.7	2.95	2.45
2	28	400	600	2.95	3.25	2.65	2.6	2.9	2.3
3	32	400	700	2.9	3.25	2.55	2.5	2.85	2.15

Table 11. Symbol Definitions

Symbol	Formula	Definition
V_{OSE-DC}	$I_T\big\|_{PE=0} \times 25\ \Omega$	Single-ended output voltage swing after settling
$V_{OSE-BOOST}$	$I_T \times 25\ \Omega$	Boosted single-ended output voltage swing
V_{OCM} (dc-coupled)	$V_{TTO} - I_T/2 \times 25\ \Omega$	Common-mode voltage when the output is dc-coupled
V_{OCM} (ac-coupled)	$V_{TTO} - I_T/2 \times 50\ \Omega$	Common-mode voltage when the output is ac-coupled
V_H	$V_{OCM} + V_{OSE-BOOST}/2$	High single-ended output voltage excursion
V_L	$V_{OCM} - V_{OSE-BOOST}/2$	Low single-ended output voltage excursion

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-AED-HD

Figure 44. 100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-100-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8159ASVZ[1]	−40°C to +85°C	100-Lead TQFP_EP	SV-100-4
AD8159-EVAL-AC		AC-Coupled Evaluation Board	

[1] Z = RoHS Compliant Part.

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