Quad 350 MHz 24 V Amplifier

AD8024

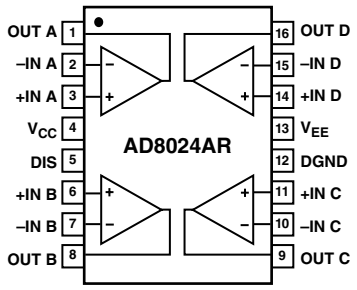
FEATURES

Quad High-Speed Current Feedback Amplifier with Disable
–3 dB Bandwidth 350 MHz @ G = +1
Slew Rate 2400 V/μs, V_S = ±12 V
Drives High Capacitive Loads
Settling Time to 0.1% in 35 ns; 300 pF Load, 6 V Step
Settling Time to 0.1% in 18 ns; 5 pF Load, 2 V Step
Low Power
Operates on +5 V to ±12 V (24 V)
4 mA/Amplifier Supply Current
Excellent Video Specs (R_L = 150 Ω, G = +2)
Gain Flatness 0.1 dB to 70 MHz
0.04% Differential Gain
0.09° Differential Phase
Crosstalk –58 dB @ 5 MHz
THD –72 dBc @ 5 MHz
Outstanding DC Accuracy
V_{OFFSET} is 2 mV (Typ)
I_{BIAS} is 3 μA (Max)
16-Lead SOIC Package

APPLICATIONS

LCD Column Drivers
High-Performance Test Equipment
Video Line Driver
ATE

FUNCTIONAL BLOCK DIAGRAM



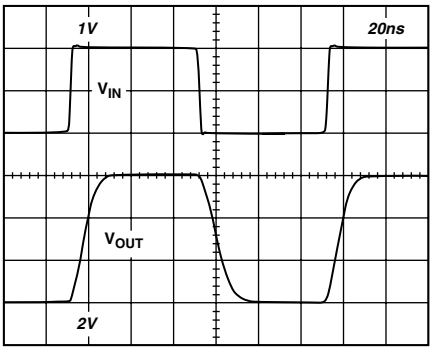


Figure 1. Pulse Response Driving a Large Load Capacitance, C_L = 300 pF, G = +3, R_{FB} = 2.32 kΩ, R_S = 10.5 Ω, R_L = 1 kΩ, V_S = ±7.5 V

PRODUCT DESCRIPTION

The AD8024 is a low settling time, high-speed, high output voltage quad current feedback operational amplifier. Manufactured on ADI's proprietary XFHV high-speed bipolar process, the AD8024 is capable of driving to within 1.3 V of its 24 V supply rail. Each amplifier has high-output current capability and can drive high capacitive loads.

The AD8024 outputs settle to 0.1% within 35 ns into a 300 pF load (6 V swing). The AD8024 can run on both 5 V as well as ±12 V rails. Slew rate on ±12 V supplies is 2400 V/μs. DC Characteristics are outstanding with typical 2 mV offset, and 3 μA maximum input bias current. High-speed disable pin allows the AD8024 to be shut down when not in use. Low-power operation is assured with the 4 mA/Amplifier supply current draw.

The high voltage drive capability, low settling time, high slew rate, low offset, and high bandwidth make the AD8024 ideally suited as an LCD column driver, a video line driver, and for use in high-performance test equipment.

The AD8024 is available in a 16-lead SOIC package.

REV. C

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AD8024–SPECIFICATIONS (@ T_A = 25°C, V_S = ±7.5 V, C_{LOAD} = 10 pF, R_L = 150 Ω, unless otherwise noted.)

Model	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Bandwidth (3 dB)	R_{FB} = 800 Ω, No Peaking, G = +3	160	200		MHz
Bandwidth (0.1 dB)	No Peaking, G = +3		25		MHz
Slew Rate	6 V Step, G = +3, C_{LOAD} = 300 pF	370	390		V/µs
Settling Time to 0.1%	T_A = 25°C to 85°C, ±3 V (6 V Step)		30		ns
	C_{LOAD} = 300 pF, R_S = 10.5 Ω, R_{LOAD} > 1 kΩ, R_{FB} = 2.32 kΩ				
	±1 V (2 V Step), C_{LOAD} = 5 pF, R_S = 0 Ω, R_{LOAD} > 1 kΩ, R_{FB} = 750 kΩ		18		ns
NOISE/HARMONIC PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, R_L = 1 kΩ		–72		dBc
	f_C = 5 MHz, R_L = 150 Ω		–67		dBc
Input Voltage Noise	f = 10 kHz		3		nV/√Hz
Input Current Noise	f = 10 kHz ($-I_{IN}$)		8		pA/√Hz
Differential Gain (R_L = 150 Ω)	f = 3.58 MHz, G = +2		0.04		%
Differential Phase (R_L = 150 Ω)	f = 3.58 MHz, G = +2		0.09		Degrees
DC PERFORMANCE					
Input Offset Voltage	T_{MIN} to T_{MAX}		2	5	mV
Offset Drift			1.5		µV/°C
+Input Bias Current			1	7.5	µA
–Input Bias Current			1	3	µA
Open-Loop Transresistance		0.850	1.2		MΩ
	T_{MIN} to T_{MAX}		0.840		MΩ
INPUT CHARACTERISTICS					
Input Resistance					
+Input	T_{MIN} to T_{MAX}		1		MΩ
–Input	T_{MIN} to T_{MAX}		135		Ω
Input Capacitance			2		pF
Input Common-Mode Voltage		$-V_S$ + 1.2		$+V_S$ – 2	V
Common-Mode Rejection Ratio					
Input Offset Voltage		62	66		dB
–Input Current			0.2		µA/V
+Input Current			1		µA/V
OUTPUT CHARACTERISTICS					
Output Voltage Swing					
R_L = 1 kΩ	$V_{OL} - V_{EE}$		0.8	1.0	V
	$V_{CC} - V_{OH}$		1.1	1.3	V
R_L = 150 Ω	$V_{OL} - V_{EE}$		1.0	1.35	V
	$V_{CC} - V_{OH}$		1.3	1.55	V
Linear Output Current	Error <3%, R1 = 50 Ω	35	50		mA
Max Dynamic Output Current			300		mA
Capacitive Load Drive			1000		pF
MATCHING CHARACTERISTICS					
Dynamic					
Crosstalk (Worst Between Any 2)	G = +2, f = 5 MHz		–58		dB
DC					
Input Offset Voltage Match			0.4	1.5	mV
Input Current Match			0.1	2.0	µA
POWER SUPPLY					
Operating Range	Single Supply	5		24	V
	Dual Supply	±2.5		±12	V
Total Quiescent Current			16	17	mA
	T_{MIN} to T_{MAX}		19.5		mA
	Disable = HIGH		0.5	1	mA
Power Supply Rejection Ratio					
Input Offset Voltage	V_S = ±6.5 V to ±8.5 V	64	70		dB
–Input Current			0.03		µA/V
+Input Current			0.07		µA/V

Model	Conditions	Min	Typ	Max	Unit
DISABLE CHARACTERISTICS					
Off Isolation	f = 6 MHz		49		dB
Off Output Impedance			20		pF
Turn-On Time			25		ns
Turn-Off Time			20		ns
Switching Threshold	V_{TH} – DGND	1.3	1.6	1.9	V
OPERATING TEMPERATURE RANGE		–40		+85	°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage $V_{CC} – V_{EE}$ . . . . . 26 V Total
Internal Power Dissipation
Small Outline (R) . . . . . 1.0 Watts (Observe Derating Curve)
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±3 V (Clamped)
Output Voltage Limit
Maximum . . . . . $+V_S$
Minimum . . . . . $–V_S$
Output Short Circuit Duration
. . . . . Observe Power Derating Curve
Storage Temperature Range
R Package . . . . . –65°C to +125°C
Operating Temperature Range
AD8024A . . . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Maximum Power Dissipation

The maximum power that can be safely dissipated by the AD8024 is limited by the associated rise in junction temperature. The maximum safe junction temperature for the plastic encapsulated parts is determined by the glass transition temperature of the plastic, about 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

Output Short Circuit Limit

The AD8024's internal short circuit limitation is not sufficient to protect the device in the event of a direct short circuit between a video output and a power supply voltage rail (V_{CC} or V_{EE}). Temporary short circuits can reduce an output's ability to source or sink current and therefore impact the device's ability to drive a load. Short circuits of extended duration can cause metal lines to fuse open, rendering the device nonfunctional.

To prevent these problems, it is recommended that a series resistor be placed as close as possible to the outputs. This will serve to substantially reduce the magnitude of the fault currents and protect the outputs from damage caused by intermittent short circuits. This may not be enough to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curve in Figure 2.

It must also be noted that in (noninverting) gain configurations (with low values of gain resistor), a high level of input overdrive can result in a large input error current, which may then result in a significant power dissipation in the input stage. This power must be included when computing the junction temperature rise due to total internal power.

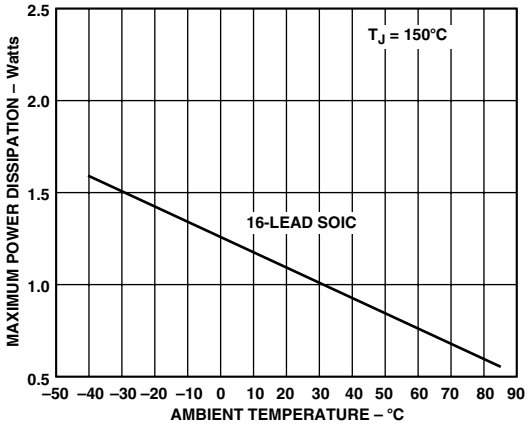


Figure 2. Maximum Power Dissipation vs. Ambient Temperature

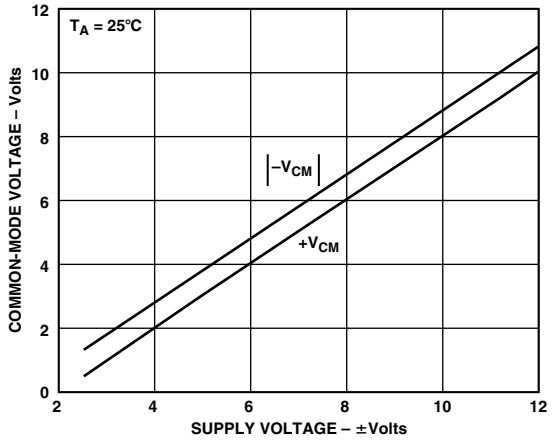
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8024AR	–40°C to +85°C	16-Lead Narrow-Body SOIC	R-16A
AD8024AR-REEL	–40°C to +85°C	16-Lead Narrow-Body SOIC	13" Tape and Reel
AD8024AR-REEL7	–40°C to +85°C	16-Lead Narrow-Body SOIC	7" Tape and Reel

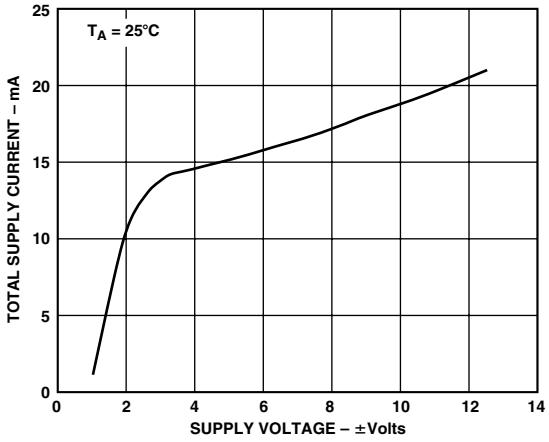
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8024 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

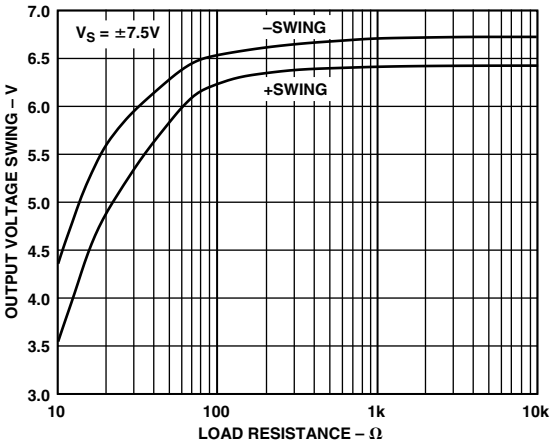
AD8024–Typical Performance Characteristics



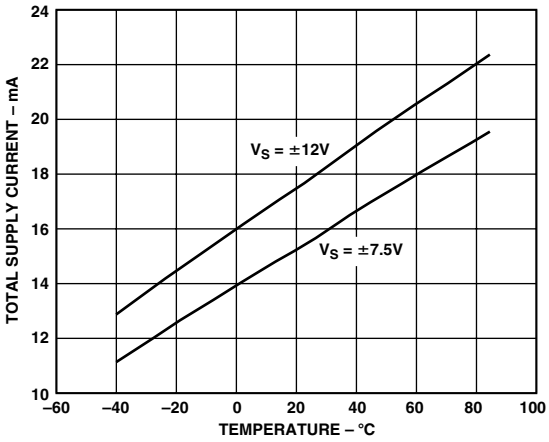
TPC 1. Input Common-Mode Voltage Range vs. Supply Voltage



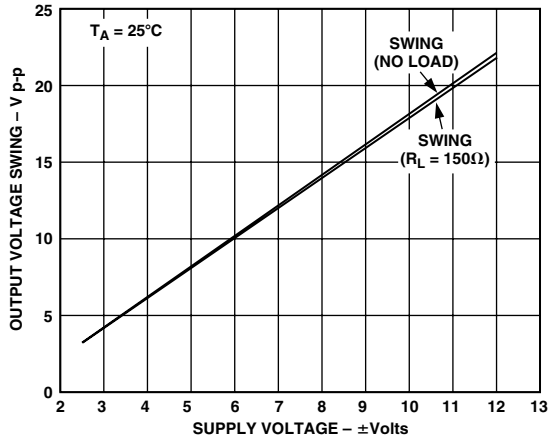
TPC 4. Total Supply Current vs. Supply Voltage



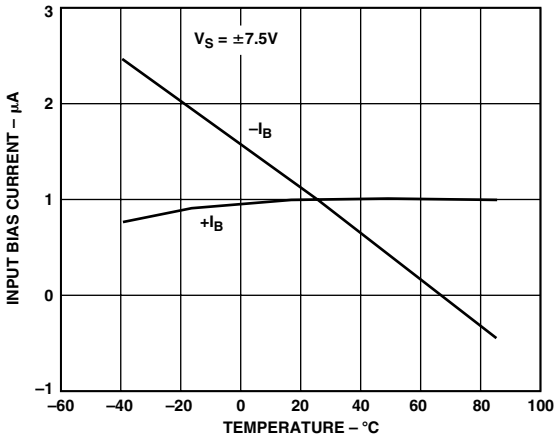
TPC 2. Output Voltage Swing vs. Load Resistance



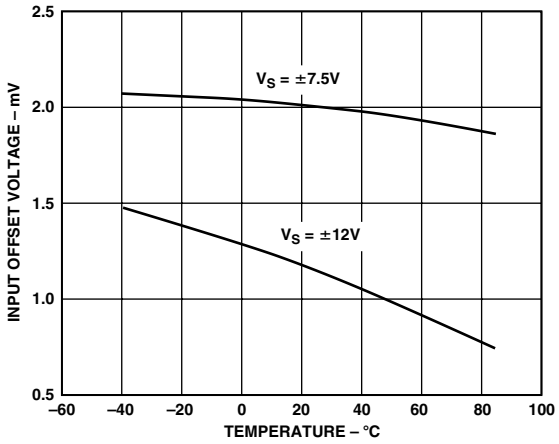
TPC 5. Total Supply Current vs. Temperature



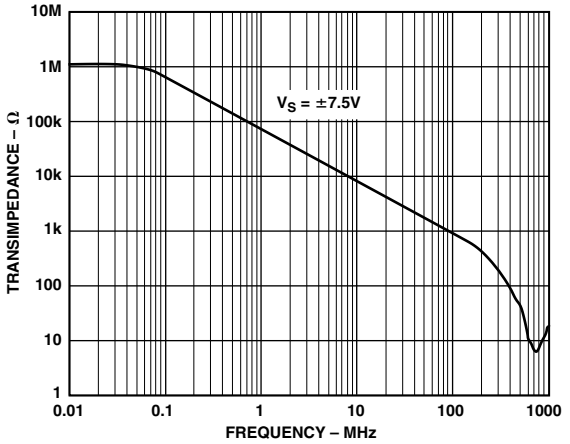
TPC 3. Output Voltage Swing vs. Supply Voltage



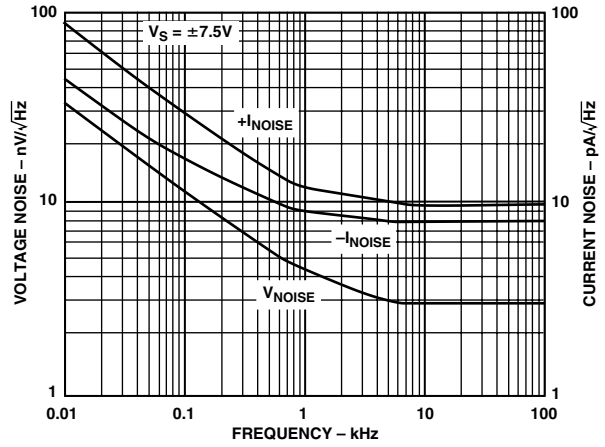
TPC 6. Input Bias Current vs. Temperature



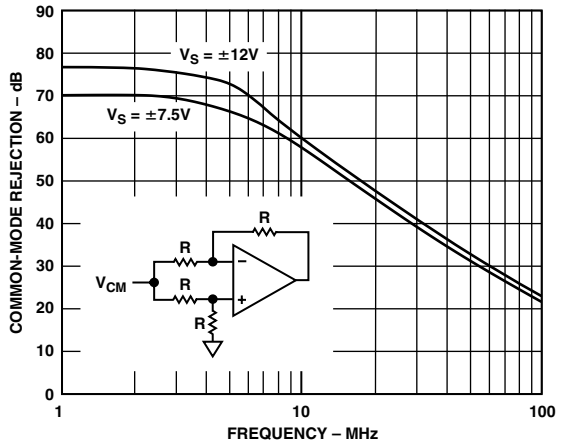
TPC 7. Input Offset Voltage vs. Temperature



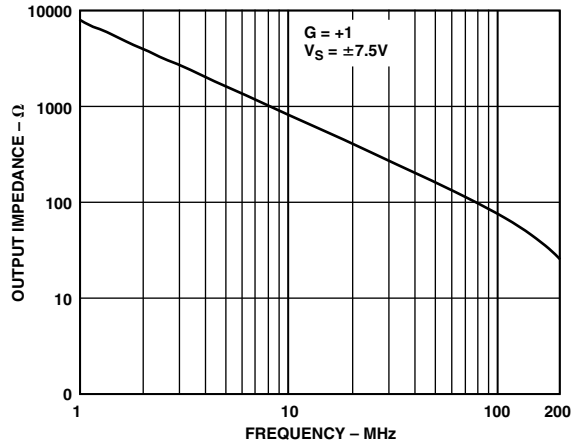
TPC 10. Open-Loop Transimpedance vs. Frequency, R_L = 150 Ω



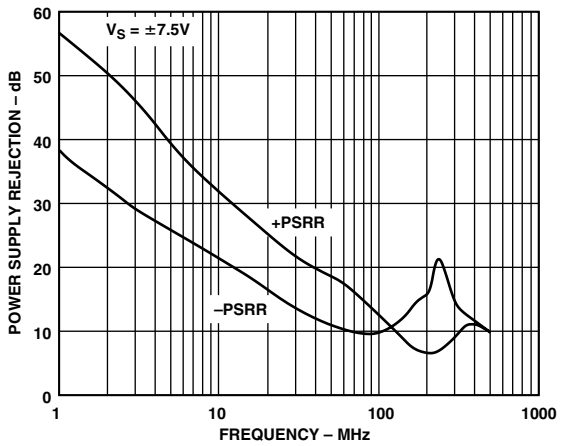
TPC 8. Input Current and Voltage Noise vs. Frequency



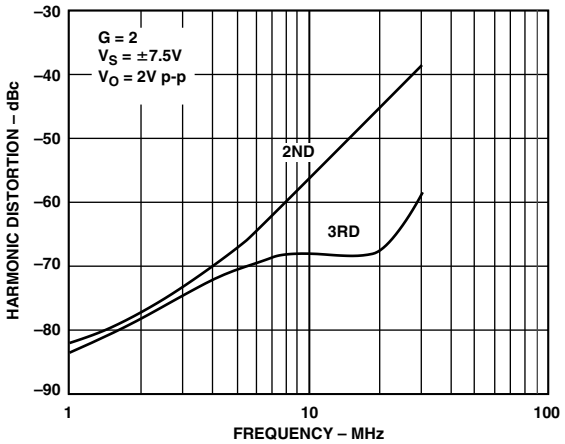
TPC 11. Common-Mode Rejection vs. Frequency



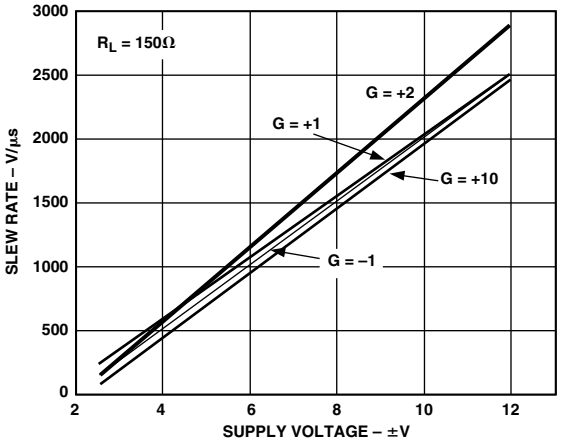
TPC 9. Output Impedance vs. Frequency, Disabled State



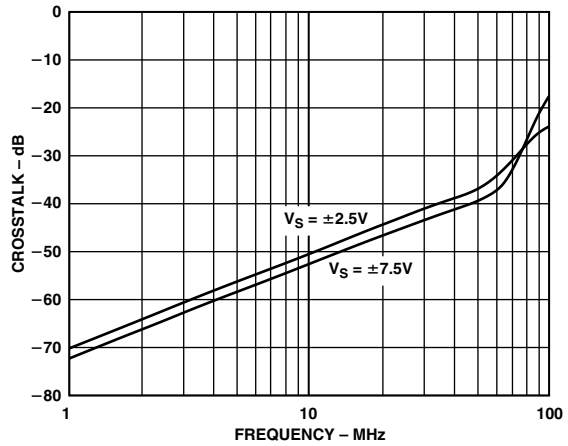
TPC 12. Power Supply Rejection vs. Frequency



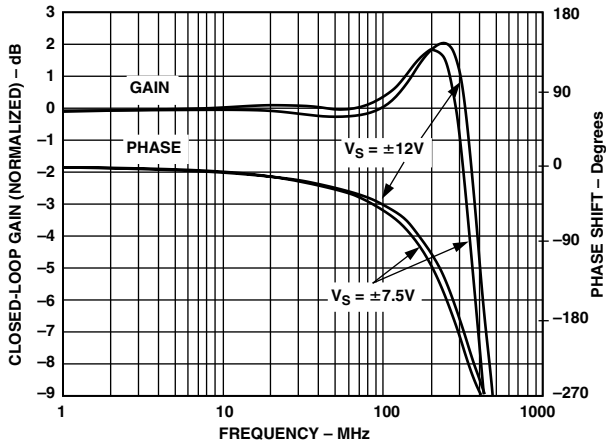
TPC 13. Harmonic Distortion vs. Frequency, R_L = 150 Ω



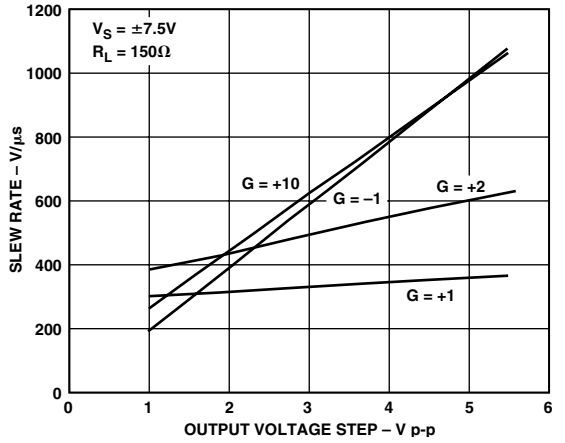
TPC 16. Maximum Slew Rate vs. Supply Voltage



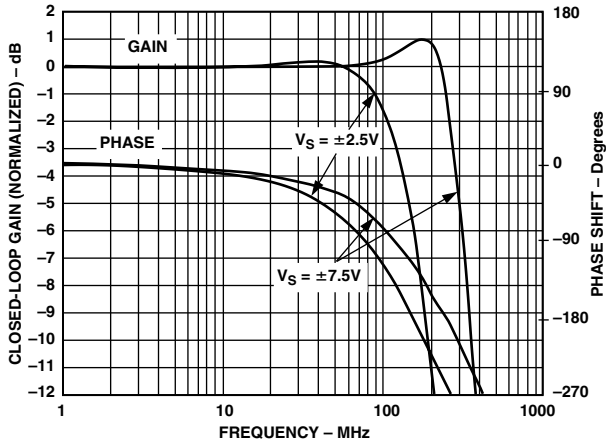
TPC 14. Crosstalk vs. Frequency, G = +2, R_L = 150 Ω



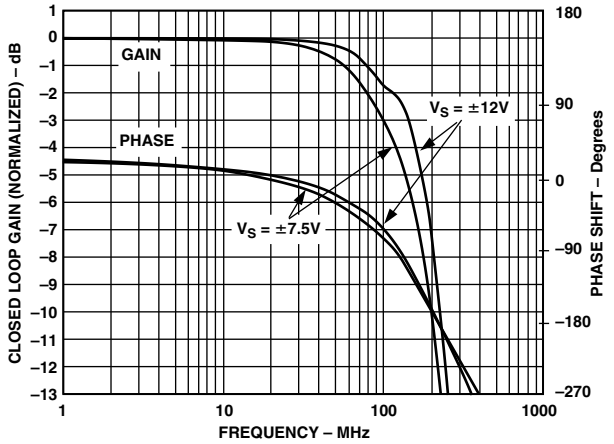
TPC 17. Closed-Loop Gain and Phase vs. Frequency, G = +1, R_L = 150 Ω



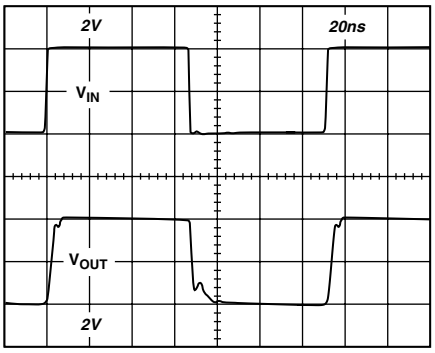
TPC 15. Slew Rate vs. Output Step Size



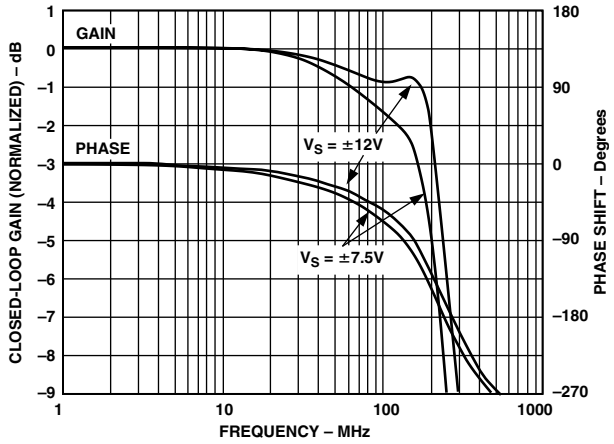
TPC 18. Closed-Loop Gain and Phase vs. Frequency, G = +2, R_L = 150 Ω



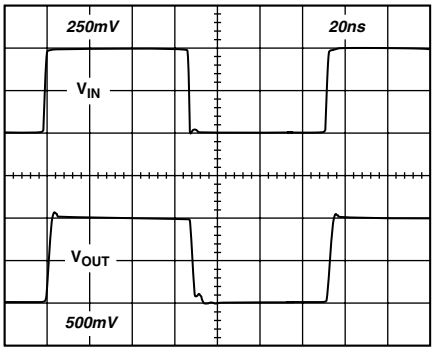
TPC 19. Closed-Loop Gain and Phase vs. Frequency, G = +10, R_L = 150 Ω



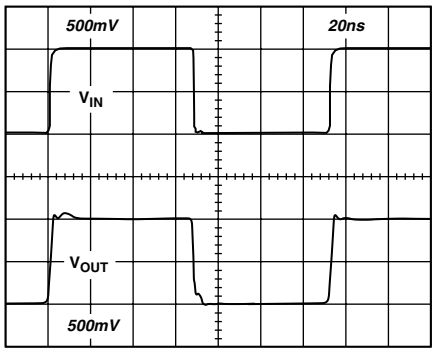
TPC 22. Large Signal Pulse Response, Gain = +1 (R_{FB} = 5 kΩ, R_L = 150 Ω, V_S = ±7.5 V)



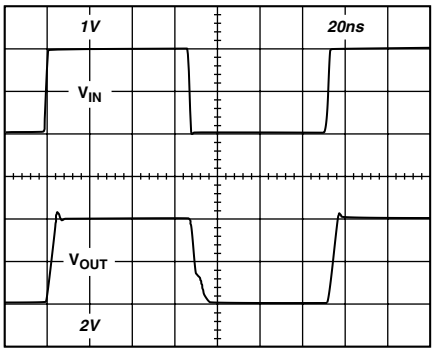
TPC 20. Closed-Loop Gain and Phase vs. Frequency, G = –1, R_L = 150 Ω



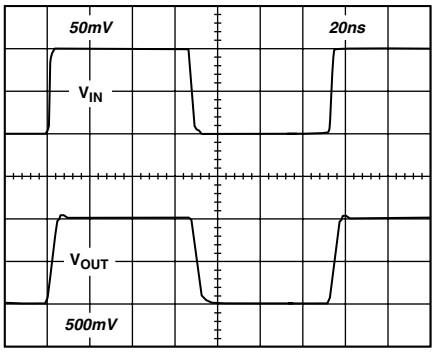
TPC 23. Small Signal Pulse Response, Gain = +2 (R_{FB} = 750 Ω, R_L = 150 Ω, V_S = ±7.5 V)



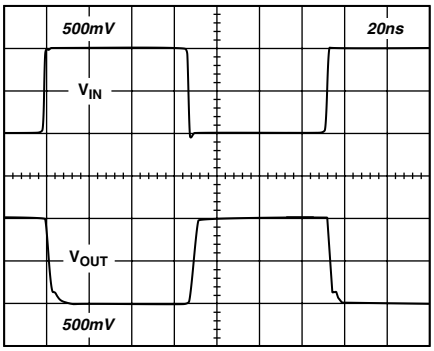
TPC 21. Small Signal Pulse Response, Gain = +1 (R_{FB} = 5 kΩ, R_L = 150 Ω, V_S = ±7.5 V)



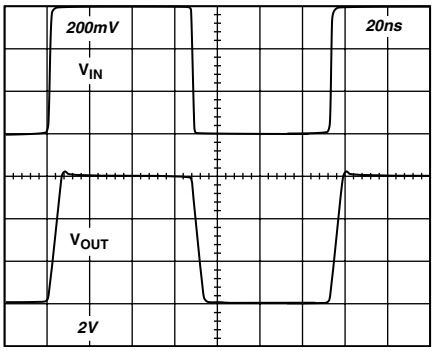
TPC 24. Large Signal Pulse Response, Gain = +2 (R_{FB} = 750 Ω, R_L = 150 Ω, V_S = ±7.5 V)



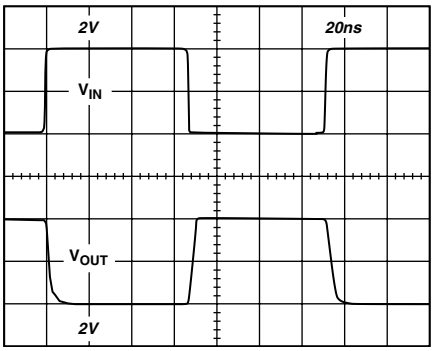
TPC 25. Small Signal Pulse Response, Gain = +10 (R_{FB} = 400 Ω, R_L = 150 Ω, V_S = ±7.5 V)



TPC 27. Small Signal Pulse Response, Gain = –1 (R_{FB} = 909 Ω, R_L = 150 Ω, V_S = ±7.5 V)



TPC 26. Large Signal Pulse Response, Gain = +10 (R_{FB} = 400 Ω, R_L = 150 Ω, V_S = ±7.5 V)



TPC 28. Large Signal Pulse Response, Gain = –1 (R_{FB} = 909 Ω, R_L = 150 Ω, V_S = ±7.5 V)

General

The AD8024 is a wide bandwidth, quad video amplifier. It offers a high level of performance on 16 mA total quiescent supply current for closed-loop gains of ±1 or greater.

Bandwidth up to 380 MHz, low differential gain and phase errors, and high output current make the AD8024 an efficient video amplifier.

The AD8024's wide phase margin and high output current make it an excellent choice when driving any capacitive load.

Choice of Feedback Resistor

Because it is a current feedback amplifier, the closed-loop bandwidth of the AD8024 may be customized with the feedback resistor.

A larger feedback resistor reduces peaking and increases the phase margin at the expense of reduced bandwidth. A smaller feedback resistor increases bandwidth at the expense of increased peaking and reduced phase margin.

The closed-loop bandwidth is affected by attenuation due to the finite output resistance. The open-loop output resistance of ≈6 Ω reduces the bandwidth somewhat when driving load resistors less than ≈150 Ω. The bandwidth will be ≈10% greater for load resistance above a few hundred ohms.

The value of the feedback resistor is not critical unless maintaining the widest or flattest frequency response is desired. Table I shows the bandwidth at different supply voltages for some useful closed-loop gains when driving a 150 Ω load. The recommended resistors are for the widest bandwidth with less than 2 dB peaking.

Table I. –3 dB Bandwidth vs. Closed-Loop Gain Resistor, R_L = 150 Ω

V_S – Volts	Gain	R_F – Ω	BW – MHz
±7.5	+1	5000	350
	+2	750	275
	+10	400	105
	–1	750	165
±12	+1	8000	380
	+10	215	150
	–1	750	95
±2.5	+2	1125	125

Driving Capacitive Loads

When used in combination with the appropriate feedback resistor, the AD8024 will drive any load capacitance without oscillation. In accordance with the general rule for current feedback amplifiers, increased load capacitance requires the use of a higher feedback resistor for stable operation.

Due to the high open-loop transresistance and low inverting input current of the AD8024, large feedback resistors do not create large closed-loop gain errors. In addition, the high output current allows rapid voltage slewing on large load capacitors.

For wide bandwidth and clean pulse response, an additional small series output resistor of about 10 Ω is recommended.

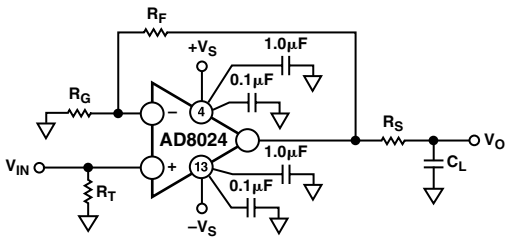


Figure 3. Circuit for Driving a Capacitive Load

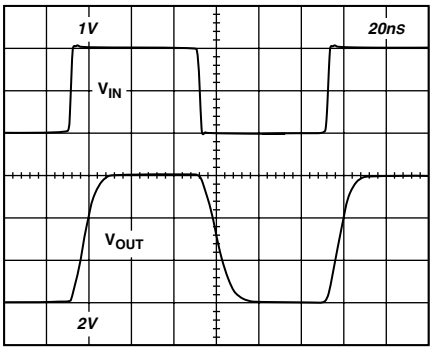


Figure 4. Pulse Response Driving a Large Load Capacitance, C_L = 300 pF, G = +3, R_{FB} = 2.32 kΩ, R_S = 10.5 Ω, R_L = 1 kΩ, V_S = ±7.5 V

Overload Recovery

The most important overload conditions are:

Input Common-Mode Voltage Overdrive
Output Voltage Overdrive
Input Current Overdrive.

When configured for a low closed-loop gain, the AD8024 recovers quickly from an input common-mode voltage overdrive; typically in <25 ns.

When configured for a higher gain and overloaded at the output, recovery from an output voltage overdrive is also short; approximately 55 ns (see Figure 5). For higher overdrive, the response is somewhat slower. For 100% overdrive, the recovery time is substantially longer.

When configured for a high noninverting gain, a high input overdrive can result in a large current into the input stage. Although this current is internally limited to approximately 30 mA, its effect on the total power dissipation may be significant. See also the warning under Maximum Power Dissipation.

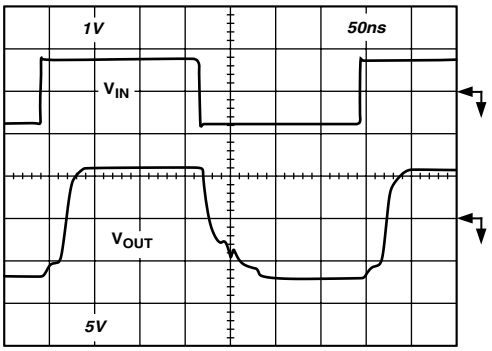


Figure 5. 15% Overload Recovery, Gain = +10 (R_{FB} = 400 Ω, R_L = 1 kΩ, V_S = ±7.5 V)

Disable Mode Operation

When the Disable pin is tied to DGND, all amplifiers are operational, in the enabled state.

When the voltage on the Disable pin is raised to 1.6 V or more above DGND, all amplifiers are in the disabled, powered-down state. In this condition, the DISABLE pin sources approximately 0.1 μA, the total quiescent current is reduced to approximately 500 μA, all outputs are in a high impedance state, and there is a high level of isolation from inputs to outputs.

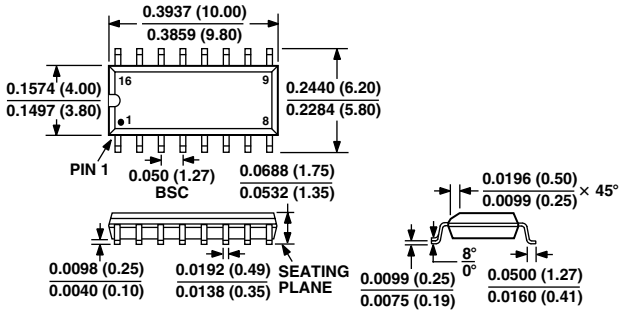
The output impedance in the disabled mode is the equivalent of all external resistors, seen from the output pin, in parallel with the total disabled output impedance of the amplifier, typically 20 pF.

The input stages of the AD8024 include protection from large differential input voltages that may be present in the disabled mode. Internal clamps limit this voltage to 1.5 V. The high input-to-output isolation is maintained for voltages below this limit.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead Plastic SOIC
(R-16A)



AD8024–Revision History

Location	Page
Data Sheet changed from REV. B to REV. C.	
Addition of callouts to Functional Block Diagram	1
Addition of Tape and Reel Packages to Ordering Guide	3

C01054–0–3/01 (rev. C)

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