16-Bit, 5 MSPS PulSAR Differential ADC

Data Sheet

AD7961

FEATURES

- Throughput: 5 MSPS
- 16-bit resolution with no missing codes
- Excellent ac and dc performance
  - Dynamic range: 96 dB
  - SNR: 95.5 dB
  - THD: −116 dB
  - INL: ±0.2 LSB (typical), ±0.55 LSB (maximum)
  - DNL: ±0.14 LSB (typical), ±0.25 LSB (maximum)
- True differential analog input voltage range: ±4.096 V or ±5 V
- Low power dissipation
  - 46.5 mW at 5 MSPS with external reference buffer (echoed clock mode)
  - 64.5 mW at 5 MSPS with internal reference buffer (echoed clock mode)
  - 39 mW at 5 MSPS with external reference buffer (self clocked mode, CNV± in CMOS mode)
- SAR architecture
  - No latency/pipeline delay
- External reference options: 2.048 V buffered to 4.096 V (internal reference buffer), 4.096 V, and 5 V
- Serial LVDS interface
  - Self clocked mode
  - Echoed clock mode
  - LVDS or CMOS option for conversion control (CNV± signal)
- Operating temperature range of −40°C to +85°C
- 32-lead, 5 mm × 5 mm LFCSP (QFN)

APPLICATIONS

- Digital imaging systems
  - Digital X-rays
  - Computed tomography
  - IR cameras
  - MRI gradient control
- High speed data acquisition
- Spectroscopy
- Test equipment

FUNCTIONAL BLOCK DIAGRAM

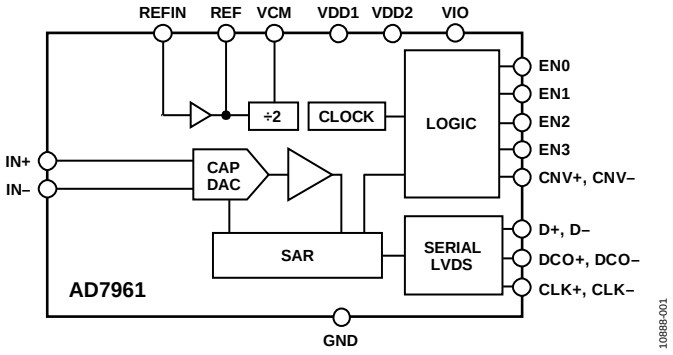


Figure 1.

GENERAL DESCRIPTION

The AD7961 is a 16-bit, 5 MSPS, charge redistribution successive approximation (SAR), analog-to-digital converter (ADC). The SAR architecture allows unmatched performance both in noise and in linearity. The AD7961 contains a low power, high speed, 16-bit sampling ADC, an internal conversion clock, and an internal reference buffer. On the CNV± edge, the AD7961 samples the voltage difference between the IN+ and IN− pins. The voltages on these pins swing in opposite phase between 0 V and 4.096 V and between 0 V and 5 V. The reference voltage is applied to the part externally. All conversion results are available on a single LVDS self clocked or echoed clock serial interface.

The AD7961 is available in a 32-lead LFCSP (QFN) with operation specified from −40°C to +85°C.

Table 1. Fast PulSAR® ADC Selection

Input Type	1 MSPS to <2 MSPS	2 MSPS to 3 MSPS	5 MSPS to 6 MSPS	10 MSPS
Pseudo-Differential, 16-Bit	AD7653 AD7667 AD7980 AD7983	AD7985		
True Bipolar, 16-Bit	AD7671			
Differential,[1] 16-Bit	AD7677 AD7623	AD7621 AD7622	AD7625 AD7961	AD7626
Differential,[1] 18-Bit	AD7643 AD7982 AD7984	AD7641 AD7986	AD7960	

[1] Antiphase.

Rev. B
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REVISION HISTORY

3/14—Rev. A to Rev. B

Changes to Table 4 ... 7
Deleted Table 6; Renumbered Sequentially ... 7
Changes to Figure 19 ... 11

11/13—Rev. 0 to Rev. A

Change to Table 1 ... 1
Changes to Table 2 ... 3
Change to Table 3 ... 5
Changes to Table 4 ... 7
Added Table 6; Renumbered Sequentially ... 7
Change to Figure 4 ... 8
Changes to Figure 32 ... 16
Change to Voltage Reference Options Section ... 17

8/13—Revision 0: Initial Version

SPECIFICATIONS

VDD1 = 5 V; VDD2 = 1.8 V; VIO = 1.8 V; REF = 5 V or 4.096 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	$V_{IN+} - V_{IN-}$	$-V_{REF}$		$+V_{REF}$	V
Operating Input Voltage	V_{IN+}, V_{IN-} to GND	−0.1		V_{REF} + 0.1	V
Common-Mode Input Range[1]		$V_{REF}/2 - 0.05$	$V_{REF}/2$	$V_{REF}/2 + 0.05$	V
CMRR	f_{IN} = 500 kHz		70		dB
Input Leakage Current	Acquisition phase		60		nA
THROUGHPUT					
Complete Cycle		200			ns
Throughput Rate		0		5	MSPS
DC ACCURACY					
No Missing Codes		16			Bits
Integral Linearity Error		−0.55	±0.2	+0.55	LSB
Differential Linearity Error		−0.25	±0.14	+0.25	LSB
Transition Noise			0.5		LSB
Zero Error		−2.5		+2.5	LSB
Zero Error Drift[1]		−0.25	±0.01	+0.25	ppm/°C
Gain Error		−8.5	±1	+8.5	LSB
Gain Error Drift[1]		−0.5	±0.05	+0.5	ppm/°C
Power Supply Sensitivity[2]	VDD1 = 5 V ± 5%		±0.25		LSB
	VDD2 = 1.8 V ± 5%		±0.5		LSB
AC ACCURACY					
f_{IN} = 1 kHz, −0.5 dBFS, V_{REF} = 5 V					
Dynamic Range		95	96		dB
Signal-to-Noise Ratio		94.5	95.5		dB
Spurious-Free Dynamic Range			118		dB
Total Harmonic Distortion			−116		dB
Signal-to-Noise-and-Distortion Ratio		94	95		dB
f_{IN} = 1 kHz, −0.5 dBFS, V_{REF} = 4.096 V					
Dynamic Range		94	95		dB
Signal-to-Noise Ratio		93.5	94.5		dB
Spurious-Free Dynamic Range			114		dB
Total Harmonic Distortion			−112		dB
Signal-to-Noise-and-Distortion Ratio		93	94		dB
−3 dB Input Bandwidth[3]	EN2 = 0		28		MHz
Oversampled Dynamic Range[4]	OSR = 256, REF = 5 V		115		dB
Aperture Delay[5]			1.6		ns
Aperture Jitter[5]			1		ps
REFERENCE BUFFER					
REFIN Input Voltage Range[1]		2.042	2.048	2.054	V
REF Output Voltage Range	REF at 25°C, EN3 to EN0 = XX01 or XX10	4.086	4.096	4.106	V
Line Regulation	VDD1 = 5 V ± 5%, VDD2 = 1.8 V ± 5%		±20		µV
Gain Drift[1]		−25	±4	+25	ppm/°C

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
EXTERNAL REFERENCE					
Voltage Range	REFIN pin, EN1 to EN0 = 01		2.048		V
	REF pin, EN1 to EN0 = 10[6]		4.096		V
	REF pin, EN1 to EN0 = 01[6]		5		V
Current Drain	5 MSPS, REF = 4.096 V		1.05	1.11	mA
	5 MSPS, REF = 5 V		1.36	1.43	mA
VCM PIN					
VCM Output			REF/2		
VCM Error		−0.01		+0.01	V
Output Impedance			5.1		kΩ
LVDS I/O (ANSI-644)					
Data Format			Serial LVDS twos complement		
Differential Output Voltage, V_{OD}	R_L = 100 Ω	245	290	454	mV
Common-Mode Output Voltage, V_{OCM}	R_L = 100 Ω	980[7]	1130	1375	mV
Differential Input Voltage, V_{ID}		100		650	mV
Common-Mode Input Voltage, V_{ICM}		800		1575	mV
POWER SUPPLIES					
Specified Performance					
VDD1		4.75	5	5.25	V
VDD2		1.71	1.8	1.89	V
VIO		1.71	1.8	1.89	V
Operating Currents[8]					
Static—Not Converting, Internal Reference Buffer Disabled	Self clocked mode, CNV± in CMOS mode[9]				
VDD1			8	40	µA
VDD2			8	70	µA
VIO			5	5.3	mA
Static—Not Converting, Internal Reference Buffer Enabled	Self clocked mode, CNV± in CMOS mode[9]				
VDD1			2.6	2.9	mA
VDD2			9	72	µA
VIO			4.4	5.3	mA
Converting: Internal Reference Buffer Disabled	Echoed clock mode, CNV± in LVDS mode				
VDD1			2	2.2	mA
VDD2			11.4	13.5	mA
VIO			9	10.3	mA
Converting: Internal Reference Buffer Enabled	Echoed clock mode, CNV± in LVDS mode				
VDD1			5.6	6	mA
VDD2			11.4	13.5	mA
VIO			9	10.3	mA
Converting: Internal Reference Buffer Disabled	Self clocked mode, CNV± in CMOS mode[9]				
VDD1			2	2.2	mA
VDD2			11.4	13.5	mA
VIO			4.9	5.6	mA
Snooze Mode					
VDD1			2	4.1	µA
VDD2			1	40.3	µA
VIO			0.1	4.8	µA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Power-Down	EN3 to EN0 = X000				
VDD1			1	2.8	µA
VDD2			1	37.8	µA
VIO			0.2	4.6	µA
Power Dissipation					
Static—Not Converting, Internal Reference Buffer Disabled	Self clocked mode, CNV± in CMOS mode[9]		9	10.3	mW
Static—Not Converting, Internal Reference Buffer Enabled	Self clocked mode, CNV± in CMOS mode[9]		21	25	mW
Converting: Internal Reference Buffer Disabled	Echoed clock mode, CNV± in LVDS mode		46.5	56.2	mW
Converting: Internal Reference Buffer Enabled	Echoed clock mode, CNV± in LVDS mode		64.5	76.4	mW
Converting: Internal Reference Buffer Disabled	Self clocked mode, CNV± in CMOS mode[9]		39	47.4	mW
Power-Down	EN3 to EN0 = X000		7.2	94.5	µW
Energy per Conversion	Self clocked, CNV± in CMOS mode[9]		7.8	9.5	nJ/sample
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] The minimum and maximum values are guaranteed by characterization.
[2] Using an external reference.
[3] See Table 9 for logic levels of enable pins. When EN2 = 1, the −3 dB input bandwidth is 9 MHz. Use this lower bandwidth only when the throughput rate is 2 MSPS or lower.
[4] The oversampled dynamic range is the ratio of the peak signal power to the noise power (for a small input) measured in the ADC output FFT from dc up to $f_S/(2 \times OSR)$, where f_S is the ADC sample rate and OSR is the oversampling ratio.
[5] Guaranteed by design.
[6] The REFIN pin is tied to 0 V in this mode.
[7] The ANSI-644 LVDS specification has a minimum common-mode output (V_{OCM}) of 1125 mV.
[8] The current dissipated in the V_{CM} circuitry when enabled is REF/20 kΩ and is not included in the operating currents listed.
[9] CNV+ works as a CMOS input when CNV− is grounded. See Table 7 for additional information.

TIMING SPECIFICATIONS

VDD1 = 5 V; VDD2 = 1.8 V; VIO = 1.71 V to 1.89 V; REF = 5 V or 4.096 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
Time Between Conversions	t_{CYC}	200			ns
Acquisition Time	t_{ACQ}		t_{CYC} − 115		ns
CNV± High Time	t_{CNVH}	10		$0.6 \times t_{CYC}$	ns
CNV± to D± (MSB) Ready	t_{MSB}			200	ns
CNV± to Last CLK± (LSB) Delay	t_{CLKL}			160	ns
CLK± Period[1]	t_{CLK}	3.33	4	$(t_{CYC} - t_{MSB} + t_{CLKL})/n$	ns
CLK± Frequency	f_{CLK}		250	300	MHz
CLK± to DCO± Delay (Echoed Clock Mode)	t_{DCO}	0	3	5	ns
DCO± to D± Delay (Echoed Clock Mode)	t_D		0	1	ns
CLK± to D± Delay	t_{CLKD}	0	3	5	ns

[1] For the maximum CLK± period, the window available to read data is $t_{CYC} - t_{MSB} + t_{CLKL}$. Divide this time by the number of bits (n) to be read giving the maximum CLK± frequency that can be used for a given conversion CNV± frequency. In echoed clock interface mode, n = 16; in self clocked interface mode, n = 18.

Timing Diagrams

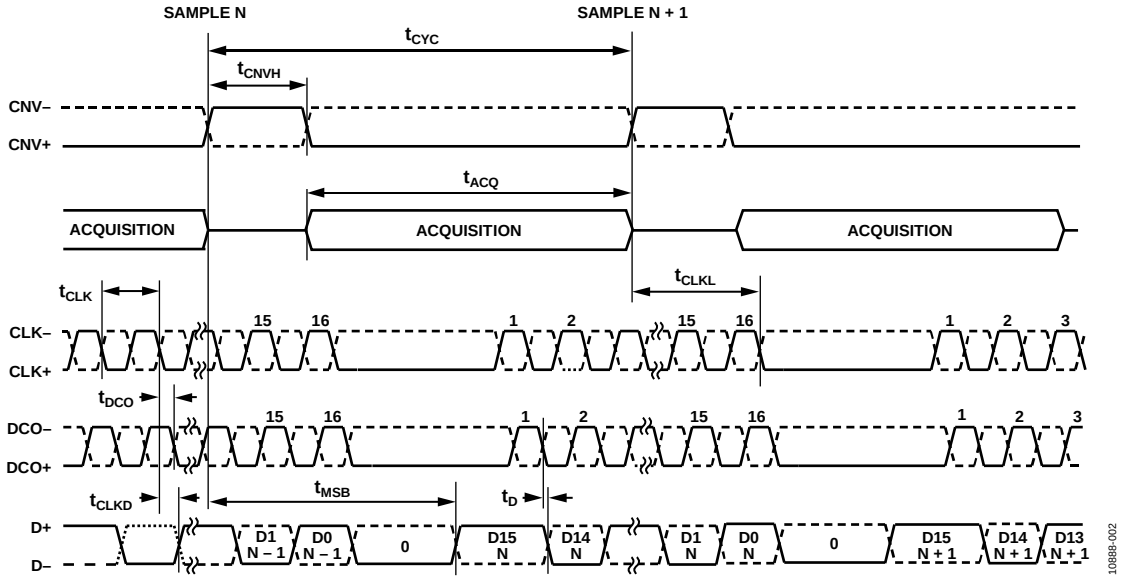


Figure 2. Echoed Clock Interface Mode Timing Diagram

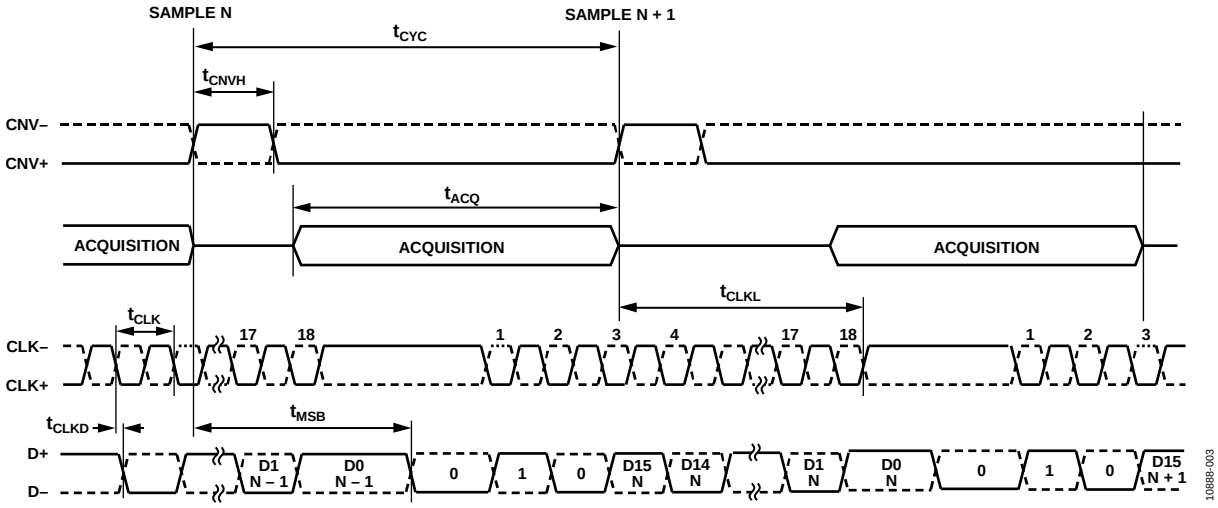


Figure 3. Self-Clocked Interface Mode Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Analog Inputs/Outputs	
IN+, IN− to GND	−0.3 V to VDD1
REF[1] to GND	−0.3 V to +6 V
VCM to GND	−0.3 V to +6 V
REFIN to GND	−0.3 V to +6 V
Supply Voltages	
VDD1	−0.3 V to +6 V
VDD2, VIO	−0.3 V to +2.1 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
Digital Outputs to GND	−0.3 V to VIO + 0.3 V
Input Current to Any Pin Except Supplies	±10 mA
Operating Temperature Range (Commercial)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
ESD Ratings	
Human Body Model	4 kV
Machine Model	200 V
Field-Induced Charged-Device Model	1.25 kV

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
32-Lead LFCSP_VQ	40	4	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

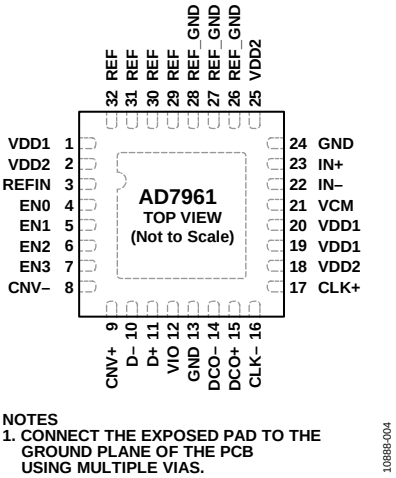


Figure 4. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 19, 20	VDD1	P	Analog 5 V Supply. Decouple the 5 V supply with a 100 nF capacitor.
2, 18, 25	VDD2	P	Analog 1.8 V Supply. Decouple this pin with a 100 nF capacitor.
12	VIO	P	Input/Output Interface Supply. Use a 1.8 V supply and decouple this pin with a 100 nF capacitor.
13, 24	GND	P	Ground.
26, 27, 28	REF_GND	P	Reference Ground. Connect the capacitors on the REF pin between REF and REF_GND. Tie REF_GND to GND.
3	REFIN	AI	Prebuffer Reference Voltage. It is driven with an external reference voltage of 2.048 V. When driving an external 2.048 V reference, a 100 nF capacitor is required. If using an external 5 V or 4.096 V reference (connected to REF), connect this pin to ground.
4, 5, 6, 7	EN0, EN1, EN2,[2] EN3	DI	Enable.[2] The logic levels of these pins set the operation of the device as described in Table 9.
8, 9	CNV–, CNV+	DI	Convert Input. These pins act as the conversion control pin. On the rising edge of these pins, the analog inputs are sampled and a conversion cycle is initiated. CNV+ works as a CMOS input when CNV– is grounded; otherwise, CNV+ and CNV– are differential LVDS inputs.
10, 11	D–, D+	DO	LVDS Data Outputs. The conversion data is output serially on these pins.
14, 15	DCO–, DCO+	DO	LVDS Buffered Clock Outputs. When DCO+ is grounded, the self-clocked interface mode is selected. In this mode, the 16-bit results on D± are preceded by an initial 0 (which is output at the end of the previous conversion), followed by a 2-bit header (10) to allow synchronization of the data by the digital host with extra logic. The 1 in this header provides the reference to acquire the subsequent conversion result correctly. When DCO+ is not grounded, the echoed clock interface mode is selected. In this mode, DCO± is a copy of CLK±. The data bits are output on the falling edge of DCO+ and can be captured in the digital host on the next rising edge of DCO+.
16, 17	CLK–, CLK+	DI	LVDS Clock Inputs. This clock shifts out the conversion results on the falling edge of CLK+.
21	VCM	AO	Common-Mode Output. When using any reference scheme, this pin produces one-half the voltage present on the REF pin, which can be useful for driving the common mode of the input amplifiers.
22	IN–	AI	Differential Negative Analog Input. Referenced to and must be driven 180° out of phase with IN+.
23	IN+	AI	Differential Positive Analog Input. Referenced to and must be driven 180° out of phase with IN–.
29, 30, 31, 32	REF	AI/O	Buffered Reference Voltage. When using the 2.048 V external reference (REFIN input), the 4.096 V system reference is produced at this pin. When using an external reference of 4.096 V or 5 V on this pin, the internal reference buffer must be disabled. Connect the REF pins with the shortest trace possible to a single 10 µF, low ESR, low ESL capacitor. The other side of the capacitor must be placed close to GND.
33	EP		Exposed Pad. The exposed pad is located on the underside of the package. Connect the exposed pad to the ground plane of the PCB using multiple vias.

[1] AI = analog input; AI/O = bidirectional analog; AO = analog output; DI = digital input; DO = digital output; P = power.
[2] EN2 = 0 sets the 28 MHz of input bandwidth and EN2 = 1 sets the 9 MHz of input bandwidth. EN3 = 1 enables the V_{CM} reference output.

TYPICAL PERFORMANCE CHARACTERISTICS

VDD1 = 5 V; VDD2 = 1.8 V; VIO = 1.8 V; all specifications T = 25°C, unless otherwise noted.

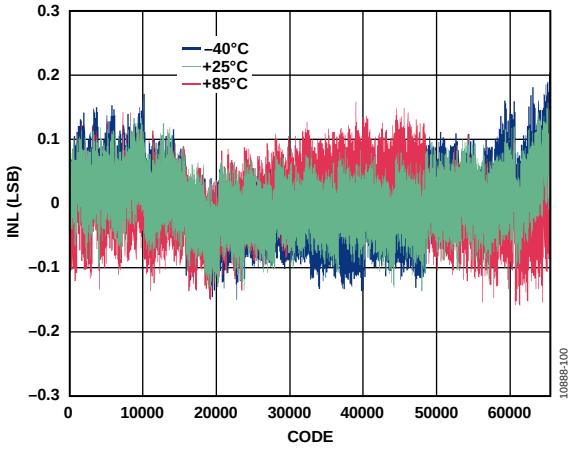


Figure 5. Integral Nonlinearity vs. Code and Temperature, REF = 5 V

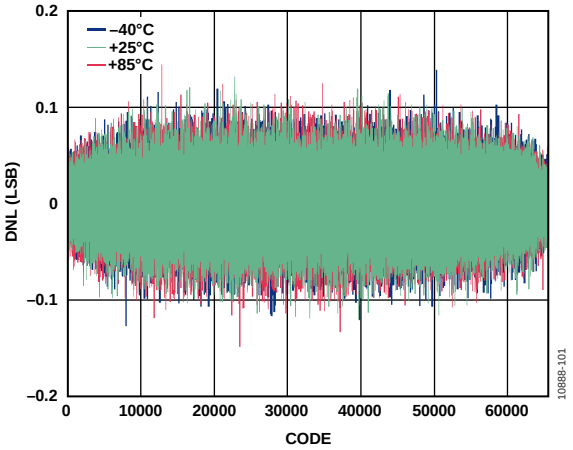


Figure 8. Differential Nonlinearity vs. Code and Temperature, REF = 5 V

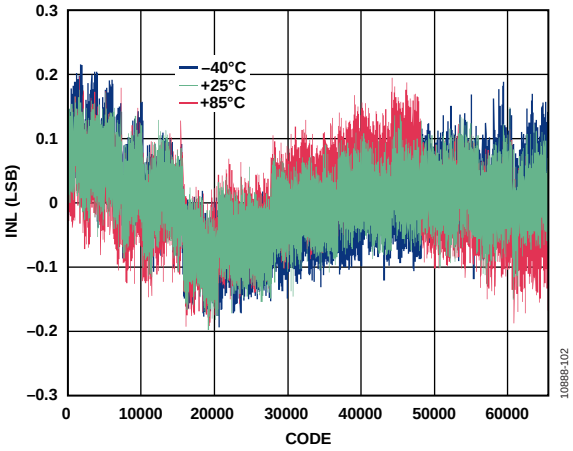


Figure 6. Integral Nonlinearity vs. Code and Temperature, REF = 4.096 V

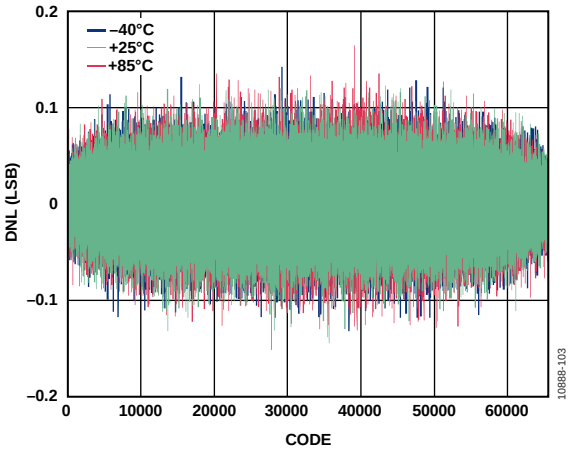


Figure 9. Differential Nonlinearity vs. Code and Temperature, REF = 4.096 V

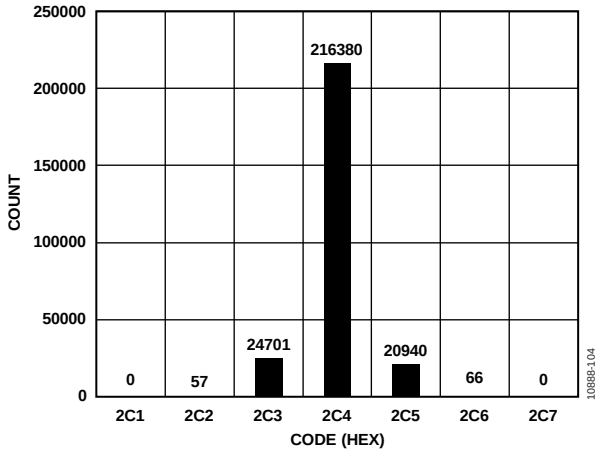


Figure 7. Histogram of DC Input at Code Center, REF = 5 V

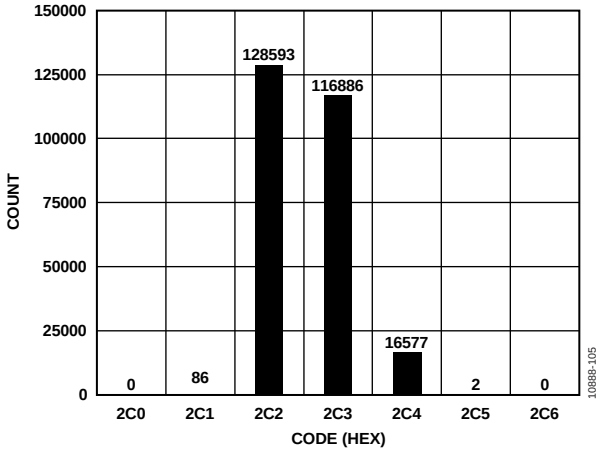


Figure 10. Histogram of DC Input at Code Transition, REF = 5 V

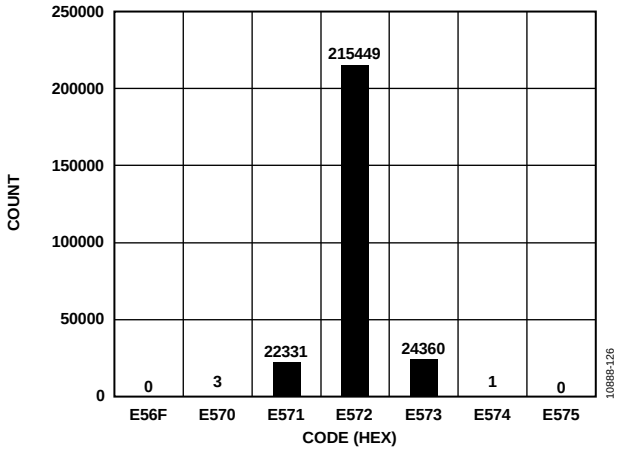


Figure 11. Histogram of DC Input at Code Center, REF = 4.096 V

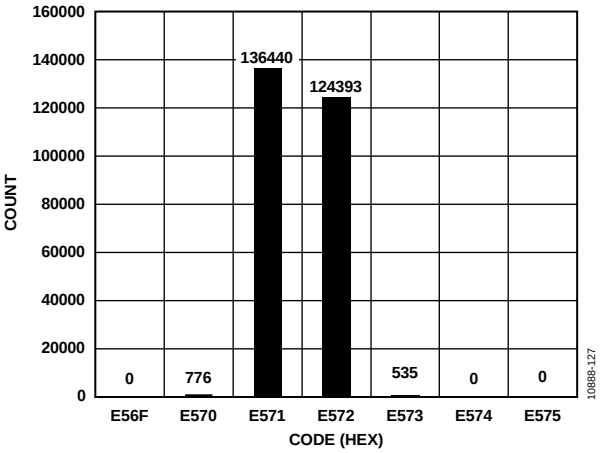


Figure 14. Histogram of DC Input at Code Transition, REF = 4.096 V

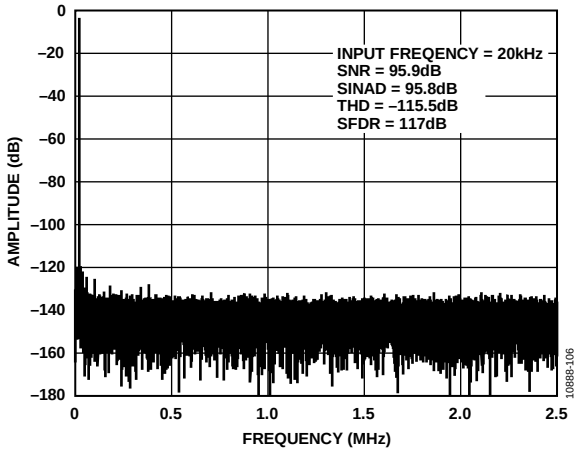


Figure 12. 20 kHz, −0.5 dBFS Input Tone FFT, Wide View, REF = 5 V

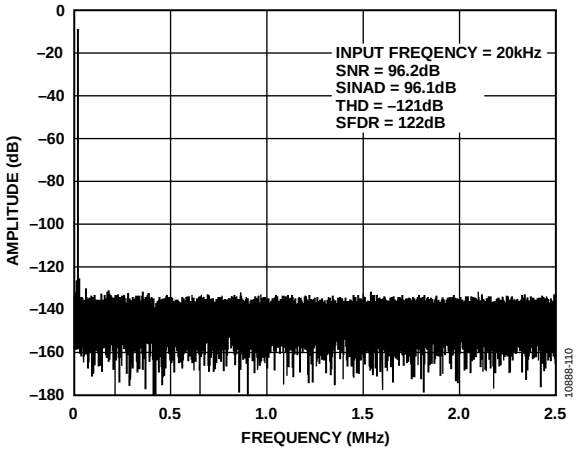


Figure 15. 20 kHz, −6 dBFS Input Tone FFT, Wide View, REF = 5 V

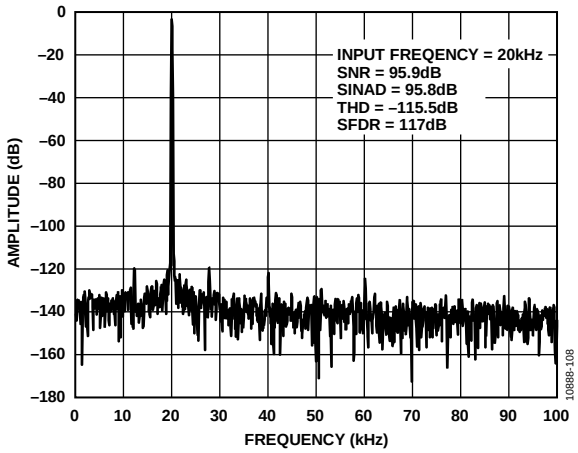


Figure 13. 20 kHz, −0.5 dBFS Input Tone FFT, Zoomed View, REF = 5 V

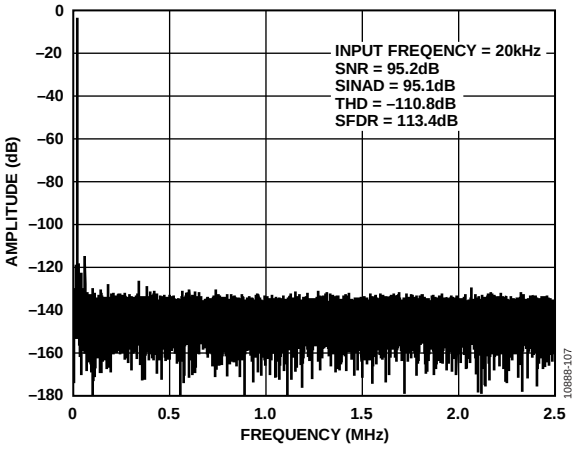


Figure 16. 20 kHz, −0.5 dBFS Input Tone FFT, Wide View, REF = 4.096 V

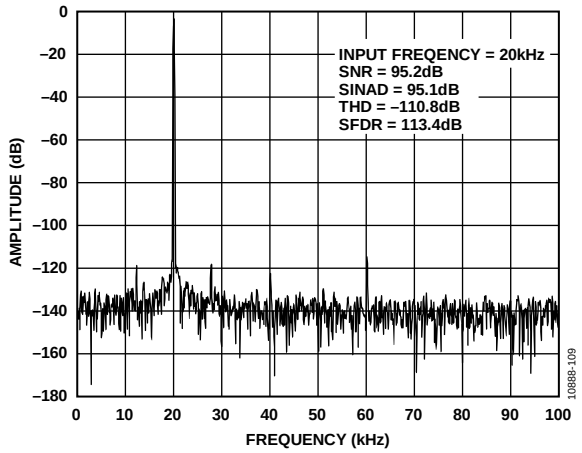


Figure 17. 20 kHz, −0.5 dBFS Input Tone FFT, Zoomed View, REF = 4.096 V

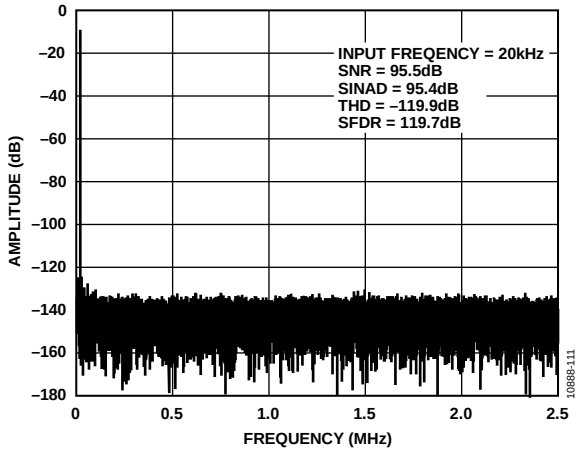


Figure 18. 20 kHz, −6 dBFS Input Tone FFT, Wide View, REF = 4.096 V

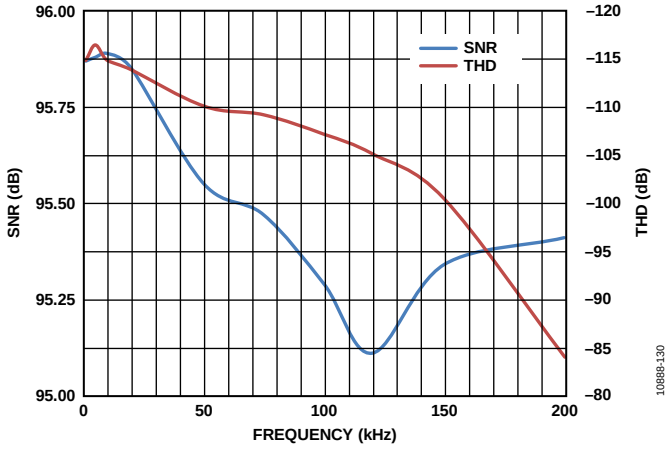


Figure 19. SNR and THD vs. Frequency, −0.5 dBFS, REF = 5 V

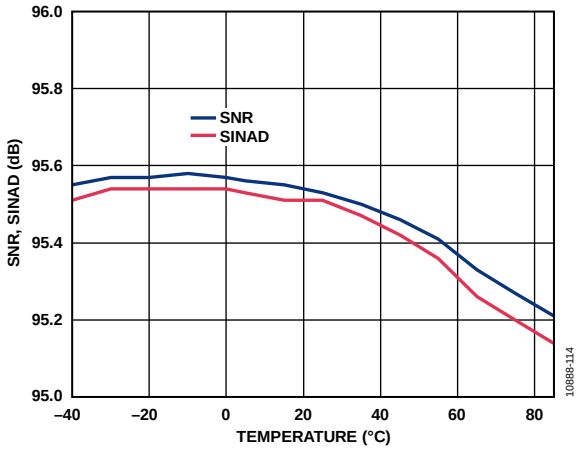


Figure 20. SNR and SINAD vs. Temperature, REF = 5 V

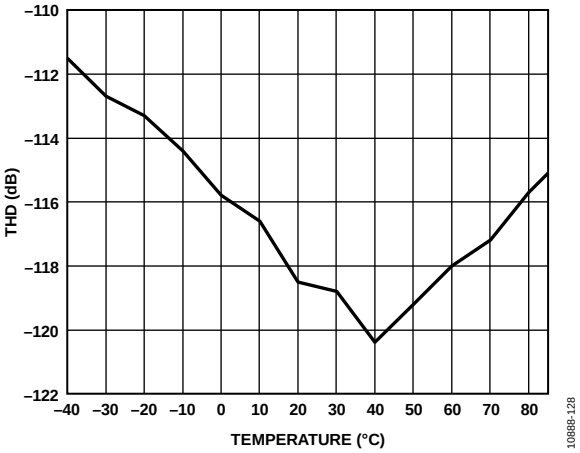


Figure 21. THD vs. Temperature, REF = 5 V

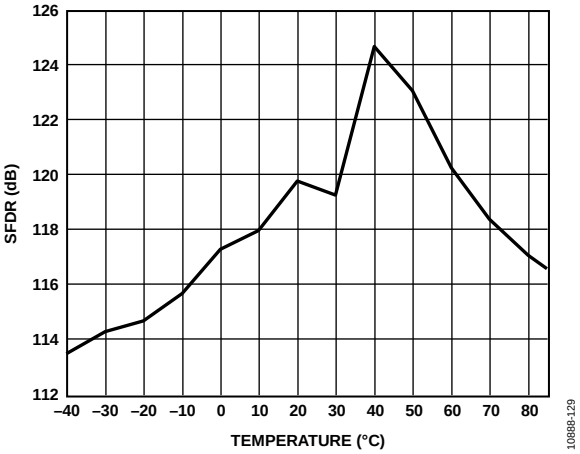


Figure 22. SFDR vs. Temperature, REF = 5 V

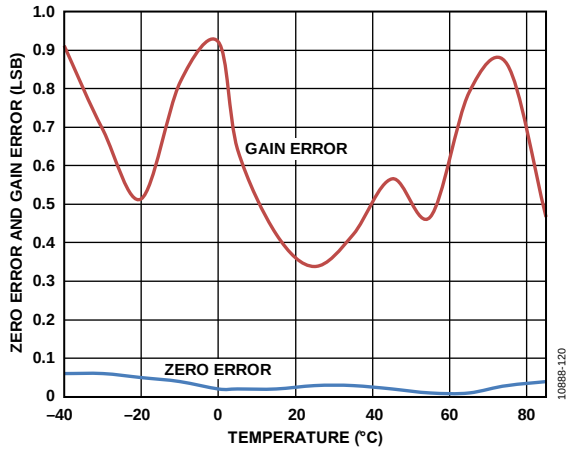


Figure 23. Zero Error and Gain Error vs. Temperature, REF = 5 V

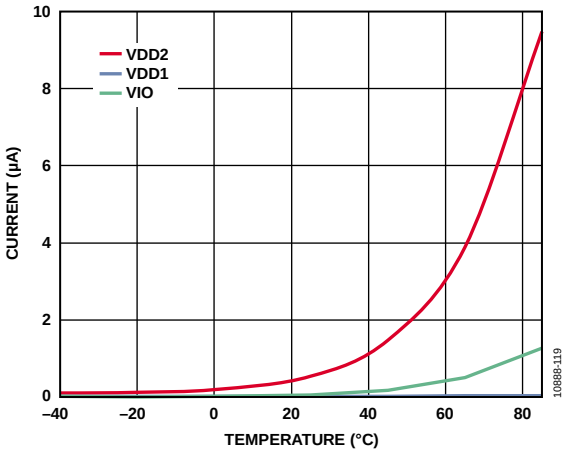


Figure 26. Power-Down Current vs. Temperature, REF = 5 V

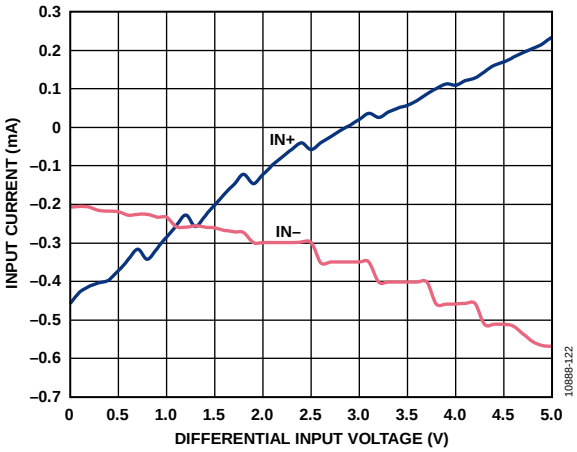


Figure 24. Input Current (IN+, IN–) vs. Differential Input Voltage, REF = 5 V

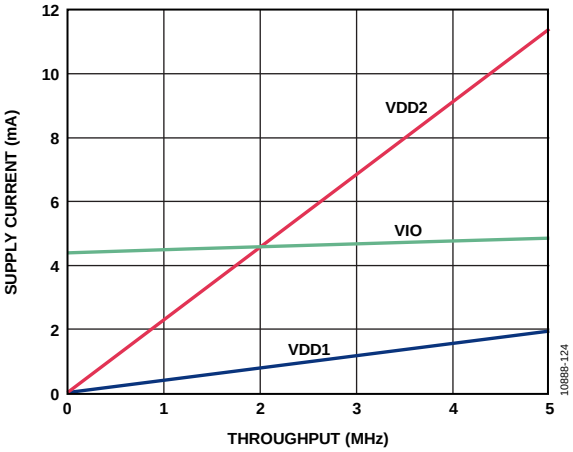


Figure 27. Supply Current vs. Throughput, Self Clocked Mode, CNV± in CMOS Mode, Internal Reference Buffer Disabled

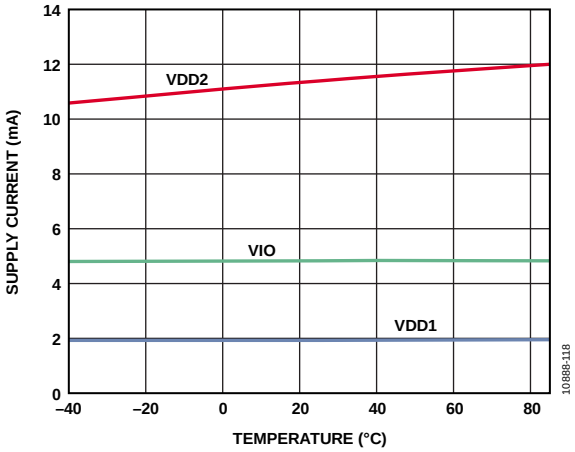


Figure 25. Supply Current vs. Temperature, REF = 5 V, Self Clocked Mode, CNV± in CMOS Mode, Internal Reference Buffer Disabled

TERMINOLOGY

Differential Nonlinearity (DNL) Error
In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Integral Nonlinearity (INL) Error
Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the rms noise measured for an input typically at −60 dB. The value for dynamic range is expressed in decibels.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD and is expressed in bits by

$$ENOB = [(SINAD_{dB} - 1.76)/6.02]$$

Gain Error
The first transition (from 100 … 000 to 100 …001) should occur at a level ½ LSB above nominal negative full scale (−4.0959844 V for the ±4.096 V range). The last transition (from 011 … 110 to 011 … 111) occurs for an analog voltage 1½ LSB below the nominal full scale (+4.095953 V for the ±4.096 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Gain Error Drift
The ratio of the gain error change due to a temperature change of 1°C and the full-scale range (2^N). It is expressed in parts per million.

Least Significant Bit (LSB)
The least significant bit, or LSB, is the smallest increment that can be represented by a converter. For a fully differential input ADC with N bits of resolution, the LSB expressed in volts is

$$LSB\ (\mathrm{V}) = \frac{V_{INp\text{-}p}}{2^N}$$

Power Supply Rejection Ratio (PSRR)

Variations in power supply affect the full-scale transition but not the linearity of the converter. PSRR is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion (SINAD) Ratio
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal (including harmonics).

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Zero Error
Zero error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

Zero Error Drift
The ratio of the zero error change due to a temperature change of 1°C and the full scale code range (2^N). It is expressed in parts per million.

THEORY OF OPERATION

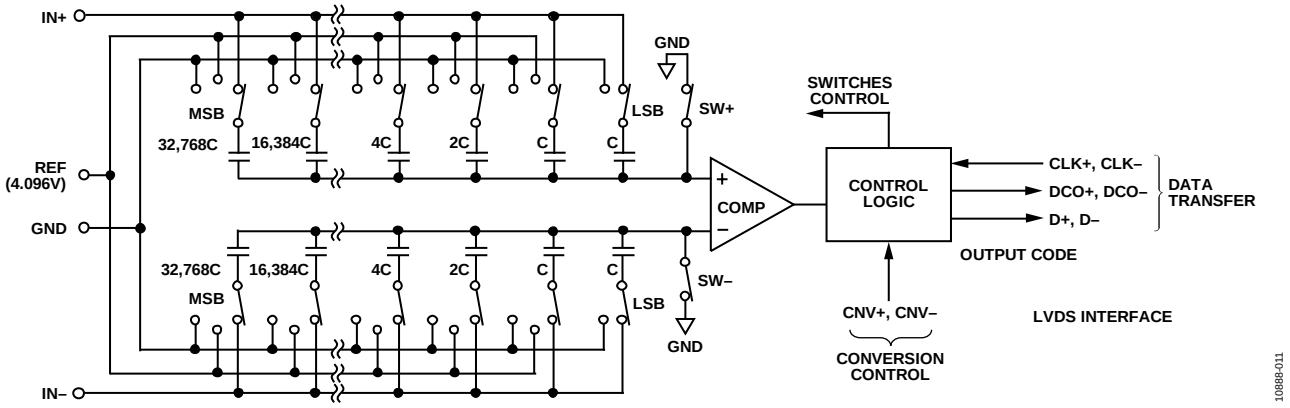


Figure 28. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7961 is a 5 MSPS, high precision, power efficient, 16-bit ADC that uses SAR-based architecture to provide performance of 95.5 dB SNR, ±0.2 LSB INL, and ±0.14 LSB DNL. The AD7961 does not exhibit any pipeline delay or latency, making it ideal for multiplexed channel applications.

The AD7961 is capable of converting 5,000,000 samples per second (5 MSPS). The device typically consumes 46.5 mW of power. The AD7961 offers the added functionality of an on-chip reference buffer. If the internal reference buffer is enabled, the AD7961 consumes approximately an additional 18 mW of power.

The AD7961 is specified for use with 5 V and 1.8 V supplies (VDD1, VDD2). The interface from the digital host to the AD7961 uses 1.8 V logic only. The AD7961 uses an LVDS interface to transfer data conversions. The CNV+ and CNV− inputs to the part activate the conversion of the analog input. The CNV+ and CNV− pins can be applied using a CMOS or LVDS source.

The AD7961 is housed in a space-saving, 32-lead, 5 mm × 5 mm LFCSP package.

CONVERTER INFORMATION

The AD7961 is a 5 MSPS ADC that uses SAR-based architecture based on a charge redistribution DAC. Figure 28 shows a simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors that are connected to the two comparator inputs.

During the acquisition phase, the terminals of the array tied to the input of the comparator are connected to GND via SW+ and SW−. All independent switches are connected to the analog inputs. In this way, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN− inputs. A conversion phase is initiated when the acquisition phase is complete and the CNV± input goes high. Note that the AD7961 can receive a CMOS or LVDS format CNV± signal.

When the conversion phase begins, SW+ and SW− are opened first. The two-capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the inputs (IN+ and IN−) captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REF (the reference voltage), the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ … $V_{REF}/262,144$). The control logic toggles these switches, MSB first, to bring the comparator back into a balanced condition. At the completion of this process, the control logic generates the ADC output code.

The AD7961 digital interface uses low voltage differential signaling (LVDS) to enable high data transfer rates.

The AD7961 conversion result is available for reading after t_{MSB} (time from the conversion start until MSB is available) elapses. The user must apply a burst LVDS CLK± signal to the AD7961 to transfer data to the digital host.

The CLK± signal outputs the ADC conversion result onto the data output D±. The bursting of the CLK± signal, illustrated in Figure 35 and Figure 36, is characterized as follows:

- Hold the differential voltage on CLK± in a steady state in the window of time between t_{CLKL} and t_{MSB}.
- The AD7961 has two data read modes. For more information about the echoed clock and self clocked interface modes, see the Digital Interface section.

TRANSFER FUNCTION

The AD7961 uses a 5 V or a 4.096 V reference. The AD7961 converts the differential voltage of the antiphase analog inputs (IN+ and IN−) into a digital output. IN+ and IN− require a REF/2 V common-mode voltage.

The 16-bit conversion result is in MSB first, twos complement format. The ideal transfer functions for the AD7961 are shown in Figure 29 and Table 8.

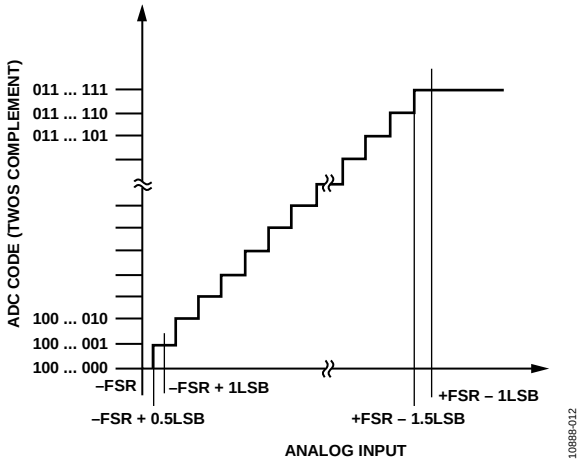


Figure 29. ADC Ideal Transfer Functions (FSR = Full-Scale Range)

ANALOG INPUTS

The analog inputs applied to the AD7961, IN+ and IN−, must be 180° out of phase with each other. Figure 30 shows an equivalent circuit of the input structure of the AD7961.

The two diodes provide ESD protection for IN+ and IN−. Care must be taken to ensure that the analog input signals do not exceed the supply rails of the AD7961 by more than 0.3 V (VDD1 and GND). If the analog input signals exceed this level, the diodes become forward-biased and start conducting current. These diodes can handle a forward-biased current of 130 mA maximum. However, if the supplies of the input buffer amplifier are different from the VDD1/GND supply, the analog input signal may eventually exceed the supply rails by more than 0.3 V. In such a case (for example, an input buffer with a short circuit), the current limitation can be used to protect the part.

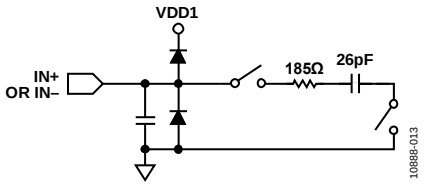


Figure 30. Equivalent Analog Input Circuit

The analog input structure allows the sampling of the true differential signal between IN+ and IN−. By using these differential inputs, signals common to both inputs are rejected. The AD7961 shows some degradation in THD with higher analog input frequencies.

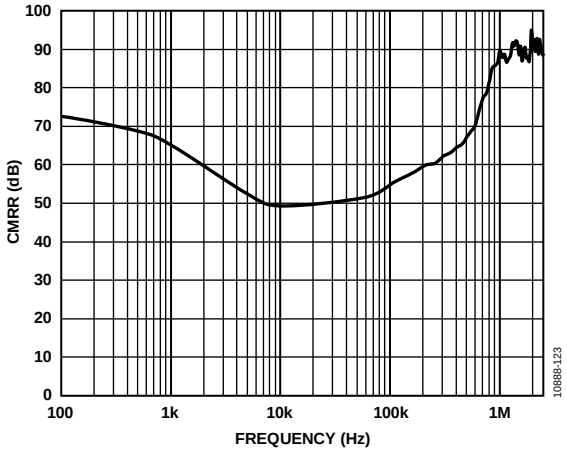


Figure 31. Analog Input CMRR vs. Frequency

Table 8. Output Codes and Ideal Input Voltages

Description	Analog Input (IN+ – IN–), REF = 5 V	Analog Input (IN+ – IN–), REF = 4.096 V	Digital Output Code, Twos Complement (Hex)
FSR – 1 LSB	+4.999847 V	+4.095875 V	0x7FFF
Midscale + 1 LSB	+152.6 µV	+125 µV	0x0001
Midscale	0 V	0 V	0x0000
Midscale – 1 LSB	−152.6 µV	−125 µV	0xFFFF
−FSR + 1 LSB	−4.999847 V	−4.095875 V	0x8001
−FSR	−5 V	−4.096 V	0x8000

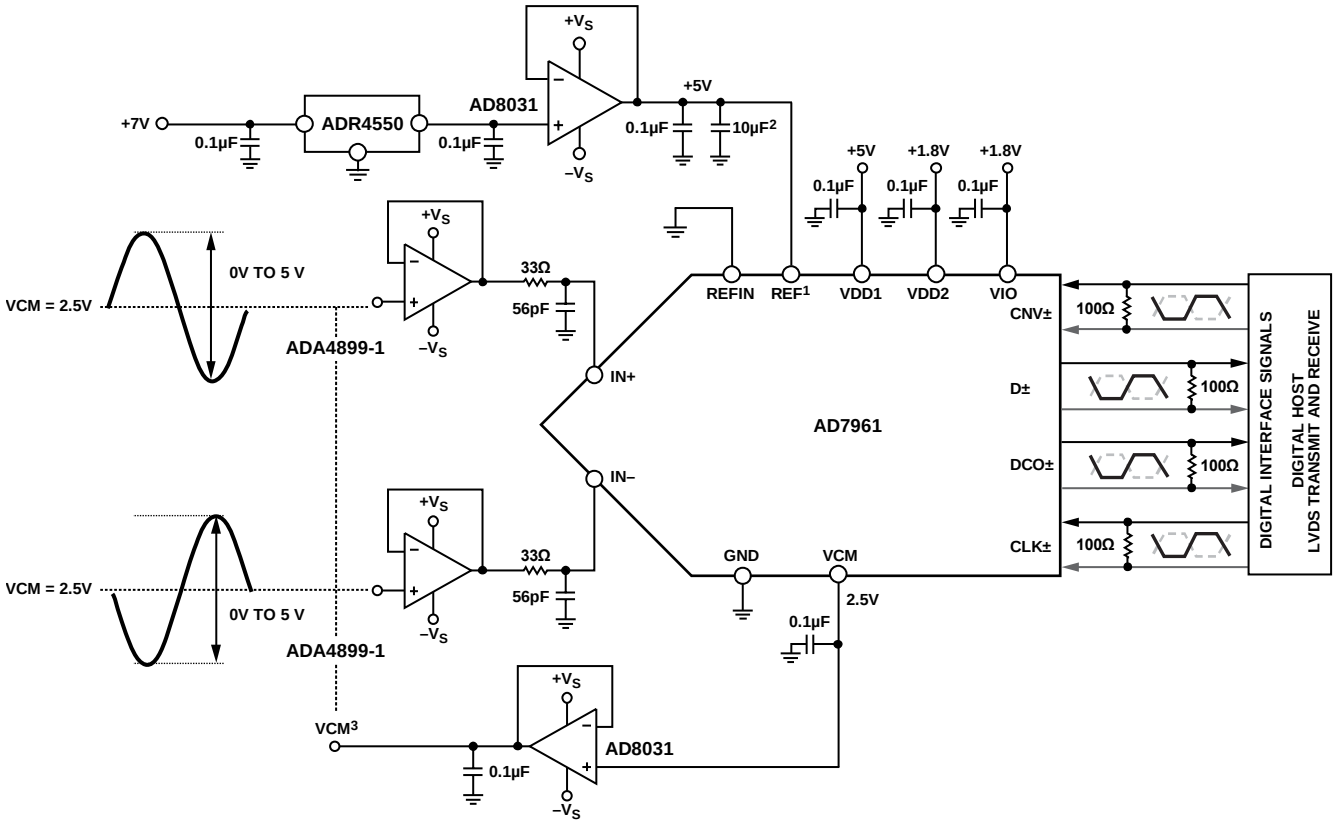
TYPICAL APPLICATIONS

Figure 32 shows an example of a typical connection diagram for driving the AD7961 using the two single-ended ADA4899-1 devices. The alternative ADC drivers are two single-ended ADA4897-1 op amps or a differential amplifier ADA4932-1 that can drive the inputs of the AD7961.

The AD7961 is an ideal fit for high speed multiplexed applications such as digital X-ray, computed tomography, and infrared cameras that require superior performance in terms of noise, power, and throughput, which significantly reduces cost in these types of applications. The AD7961 has a quiet time requirement of 90 ns to 110 ns during the conversion, where the switching of multiplexer inputs (channels) must not occur to avoid the corruption of conversion. In other words, a delay of less than 90 ns and greater than 110 ns from the CNV± rising edge to the multiplexer inputs switching event results in no corruption. If the analog inputs are multiplexed during this quiet conversion time, the current conversion may be corrupted by up to 4 LSBs.

If the analog inputs are multiplexed early enough, the inputs can slew fast enough to a full-scale signal and settle the input within the allowed time.

The AD7961 offers extremely low noise floor relative to its full-scale input. The combination of high throughput rate, low noise floor, and linearity also makes this part suitable for oversampling applications such as spectroscopy, MRI gradient control, and gas chromatography. The wide dynamic range of the AD7961 allows accurate measurements of both small and large signals from multiple channels.



1SEE THE VOLTAGE REFERENCE OPTIONS SECTION. CONNECTION TO EXTERNAL REFERENCE SIGNALS IS DEPENDENT ON THE EN1 AND EN0 SETTINGS.
2A 10µF CAPACITOR WITH LOW ESL AND ESR IS USUALLY CONNECTED BETWEEN THE REF PIN AND REF_GND. CONNECT REF_GND TO THE COMMON GROUND OF THE BOARD. THE REF AND REFIN PINS ARE DECOUPLED REGARDLESS OF EN1 AND EN0 SETTINGS.
3BUFFERED VCM PIN OUTPUT GIVES THE REQUIRED 2.5V COMMON-MODE SUPPLY FOR ANALOG INPUTS.

10888-015

Figure 32. Typical Application Diagram

Table 8. Voltage Reference Options

EN3	EN2	EN1	EN0	REFIN	Reference Mode Description
X[1]	0	0	0	X[1]	Power-down mode. Everything is powered down, including the LVDS interface.
X[1]	0	0	1	0 V	Interface powered up. Reference buffer disabled. An external 5 V reference is applied to the REF pin. Connect REFIN to 0 V in this mode. The bandwidth of the input sampling network is set to 28 MHz.
X[1]	0	0	1	2.048 V	Internal reference buffer enabled. An external 2.048 V reference applied to REFIN pin is required. A buffered 4.096 V reference is available on the REF pin. The bandwidth of the input sampling network is set to 28 MHz.
X[1]	0	1	0	0 V	Internal reference buffer disabled. Drive the REF pins with a 4.096 V external reference. Connect REFIN to 0 V in this mode. The bandwidth of the input sampling network is set to 28 MHz.
X[1]	0	1	1	0 V	Snooze mode.[2] LVDS powers down. The chip is unresponsive to CNV± start pulses. The wake-up time is fast (5 µs) when EN3 to EN0 are set to XX01 or XX10. Ensure that the CNV± start pulse is low when transitioning in and out of this mode.
0	1	0	0	X[1]	Test patterns output on LVDS. The ADC output is not available on the interface.
1	1	0	0	X[1]	Invalid mode.
X[1]	1	0	1	0 V	Reference buffer disabled. Drive the REF pins with a 5 V external reference. The bandwidth of the input sampling network is set to narrow (9 MHz).
X[1]	1	0	1	2.048 V	Internal reference buffer enabled and driving REF pin to 4.096 V. The bandwidth of the input sampling network is set to narrow (9 MHz).
X[1]	1	1	0	0 V	Reference buffer disabled. Drive the REF pins with a 4.096 V external reference. The bandwidth of the input sampling network is set to narrow (9 MHz).
X[1]	1	1	1	0 V	Snooze mode.[2] LVDS powers down. The chip is unresponsive to CNV± start pulses. The wake-up time is fast (5 µs) when EN3 to EN0 are set to XX01 or XX10.

[1] X = don't care.
[2] The snooze mode is not useful when the internal reference buffer is used because the fast wake-up is not possible due to the settling of the internal reference buffer.

VOLTAGE REFERENCE OPTIONS

The AD7961 allows buffering of the reference voltage. The AD7961 conversions are referred to a 5 V or 4.096 V reference voltage. There are three options for using an external reference:

- Externally buffered reference source of 5 V applied to the REF pin.
- Externally buffered reference source of 4.096 V applied to the REF pin.
- External reference of 2.048 V applied to the REFIN pin (high impedance input). The on-chip buffer gains this by 2 and drives the REF pin with 4.096 V.

The recommended external references for the AD7961 are the ADR4520/ADR4540/ADR4550 and ADR440/ADR444/ADR445. The various options for creating this reference are controlled by the EN1 and EN0 pins (see Table 8). The −3 dB input bandwidth is controlled by EN2. EN2 = 0 sets a −3 dB input bandwidth of 28 MHz, and EN2 = 1 sets a −3 dB input bandwidth of 9 MHz. Use this lower bandwidth (9 MHz) only when the sample rate is 2 MSPS or lower. EN3 = 1 enables the VCM reference output, and EN3 = 0 disables the VCM reference output voltage. The best SNR and dynamic range performance is achieved by using the larger 5 V external voltage reference option. The improvement achieved is approximately 1.7 dB and is calculated using the following equation:

$$\Delta SNR = 20 \log\left(\frac{5.0}{4.096}\right)$$

Wake-Up Time from Power-Down and Snooze Modes

The AD7961 powers down when EN3 to EN0 = X000 and operates in snooze mode when EN3 to EN0 = XX11 using the correct reference choice as shown in Table 8. Typical wake-up times for the selected reference settings from power-down and snooze mode are shown in Table 9 and Table 10. Each wake-up time represents the duration from the EN3 to EN0 logic transition to when the ADC is ready for a CNV± rising edge. For example, the user must wait 1.4 ms from power-down before applying CNV± pulses to receive data conversion results when using REFIN = 0 V.

Table 9. Wake-Up Time from Power-Down Mode, EN3 to EN0 = X000

To Active Mode	Wake-Up Time
EN3 to EN0 = XX01, REFIN = 0 V	1.4 ms
EN3 to EN0 = XX01, REFIN = 2.048 V	8 ms
EN3 to EN0 = XX10, REFIN = 0 V	1.4 ms

Table 10. Wake-Up Time from Snooze Mode, EN3 to EN0 = XX11

To Active Mode	Wake-Up Time
EN3 to EN0 = XX01, REFIN = 0 V	5 µs
EN3 to EN0 = XX01, REFIN = 2.048 V	8 ms
EN3 to EN0 = XX10, REFIN = 0 V	5 µs

POWER SUPPLY

The AD7961 uses both 5 V (VDD1) and 1.8 V (VDD2) power supplies, as well as a digital input/output interface supply (VIO). Drive the EN0 to EN3 pins with a 1.8 V logic level. VIO and VDD2 can be taken from the same 1.8 V source; however, it is best practice to isolate the VIO and VDD2 pins using separate traces as well as to decouple each pin separately.

The 5 V and 1.8 V supplies required for the AD7961 can be generated using Analog Devices, Inc., LDOs such as the ADP7104-5 and the ADP124-1.8. Figure 33 shows the PSRR vs. supply frequency of the AD7961. The AD7961 core power scales with throughput as shown in Figure 34, offering significant power budget savings at lower speed operation.

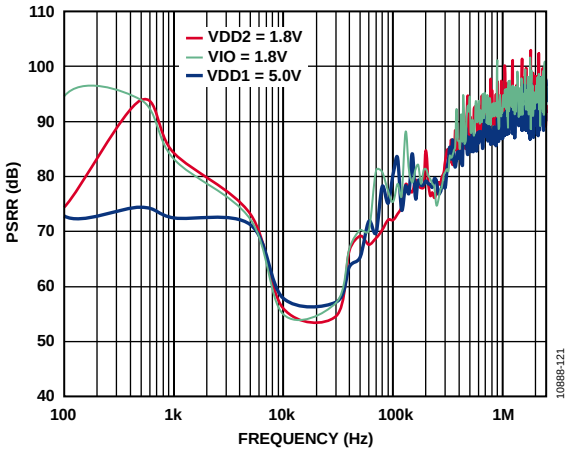


Figure 33. PSRR vs. Supply Frequency

Power-Up

As is best practice for all ADCs, power on the core supplies prior to applying an external reference (where applicable). Apply the analog inputs last.

When powering up the AD7961 device, first apply 1.8 V (VDD2, VIO) to the device, then ramp 5 V (VDD1). Set the reference configuration pins, EN0, EN1, and EN2, to the correct values. When an internal reference buffer is used (governed by the EN1 and EN0 values), apply the external reference of 2.048 V to the REFIN pin or 5 V/4.096 V to the REF pin.

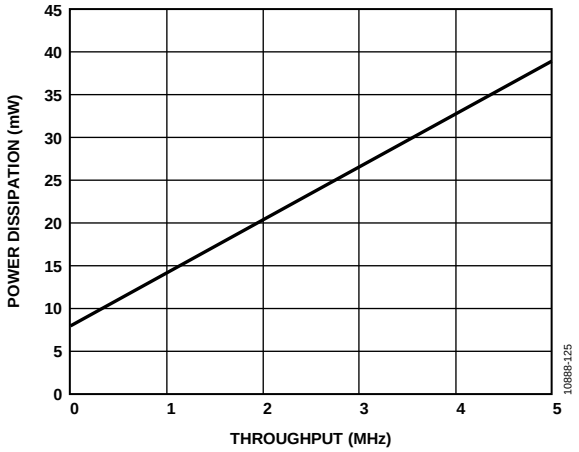


Figure 34. ADC Core Power Dissipation vs. Throughput, Self Clocked Mode, CNV± in CMOS Mode, Internal Reference Buffer Disabled

DIGITAL INTERFACE

CONVERSION CONTROL

All analog-to-digital conversions are controlled by the CNV± signal. This signal can be applied in the form of a CNV+/CNV− LVDS signal, or it can be applied in the form of a 1.8 V CMOS logic signal to the CNV+ pin when CNV− is grounded. The conversion is initiated by the rising edge of the CNV± signal.

After the AD7961 is powered up, the first conversion result generated is valid. The key beneficial feature of the AD7961 is that the user can return to the acquisition phase before the end of the conversion.

The two methods for acquiring the digital data output of the AD7961 via the LVDS interface are described in the Echoed Clock Interface Mode and Self Clocked Mode sections.

Echoed Clock Interface Mode

The digital operation of the AD7961 in echoed clock interface mode is shown in Figure 35. This interface mode, requiring only a shift register on the digital host, can be used with many digital hosts (such as FPGA, shift register, and microprocessor). It requires three LVDS pairs (D±, CLK±, and DCO±) between each AD7961 and the digital host.

The clock DCO± is a buffered copy of CLK± and is synchronous to the data, D±, which is updated on the falling edge of DCO± (t_D). By maintaining good propagation delay matching between D± and DCO± through the board and the digital host, DCO± can be used to latch D± with good timing margin for the shift register.

Conversions are initiated by a rising edge of the CNV± pulse. The CNV± pulse must be returned low (≤t_{CNVH} maximum) for valid operation. After a conversion begins, it continues until completion. Additional CNV± pulses are ignored during the conversion phase. After t_{MSB} elapses, the host begins to burst the CLK±. Note that t_{MSB} is the maximum time for the MSB of the new conversion result. Use t_{MSB} as the gating device for CLK±. The echoed clock, DCO±, and the data, D±, are driven in phase with D± being updated on the falling edge of DCO±; the host uses the rising edge of DCO± to capture D±. The only requirement is that the 16 CLK± pulses finish before t_{CLKL} of the next conversion phase elapses, or the data is lost. After all 16 bits are read, up to t_{MSB}, D± and DCO± are driven to 0. Set CLK± to idle low between CLK± bursts.

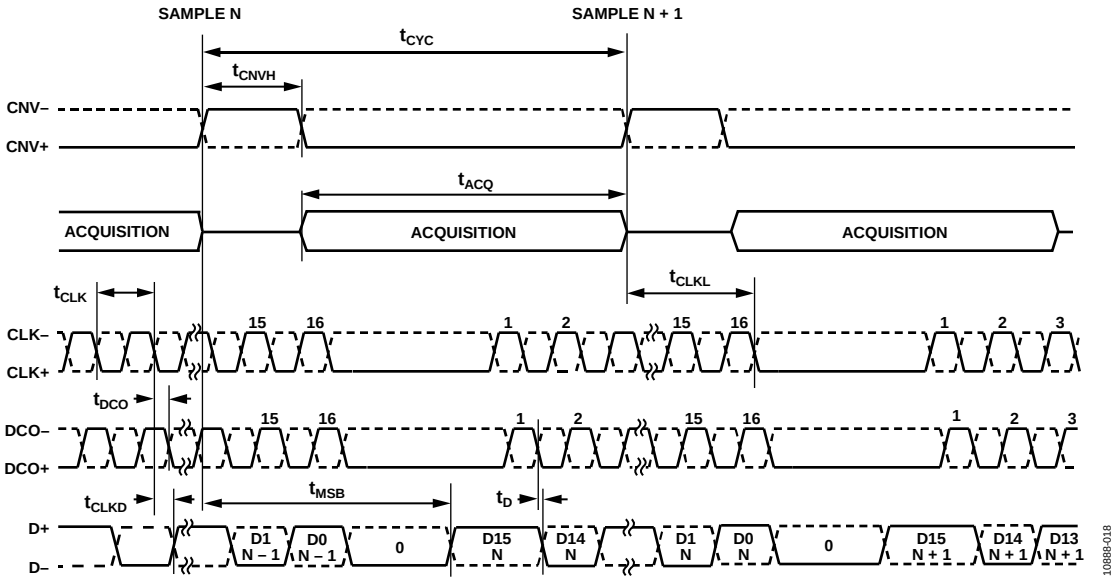


Figure 35. Echoed Clock Interface Mode Timing Diagram

Self Clocked Mode

The digital operation of the AD7961 in self-clocked interface mode is shown in Figure 36. This interface mode reduces the number of traces between the ADC and the digital host to two LVDS pairs (CLK± and D±) or to a single pair if sharing a common CLK±. Multiple AD7961 devices can share a common CLK± signal. This can be useful in reducing the number of LVDS connections to the digital host.

When the self-clocked interface mode is used, each ADC data-word is preceded by a 010 header sequence. After t_{MSB} has elapsed, the first bit of the header, 0, automatically appears on D±, and the remaining two bits of the header, 10, are then clocked out by the first two CLK± falling edges at the beginning of the next sample. This header (010) is used to synchronize D± of each conversion in the digital host because, in this mode, there is no clock output synchronous to the data (D±) to allow the digital host to acquire the data output.

Synchronization of the D± data to the acquisition clock of the digital host is accomplished by using one state machine per AD7961 device. For example, using a state machine that runs at the same speed as CLK± incorporates three phases of this clock frequency (120° apart). Each phase acquires the D± data as output by the ADC.

The AD7961 data captured on each phase of the state machine clock is then compared. The location of the 1 in the header in each set of acquired data allows the user to choose the state machine clock phase that occurs during the data valid window of D±.

The self-clocked mode data capture method allows the digital host to adapt its result capture timing to accommodate variations in propagation delay through any AD7961, for example, where data is captured from multiple AD7961 devices sharing a common input clock.

Conversions are initiated by a CNV± pulse. The CNV± pulse must be returned low (t_{CNVH} maximum) for valid operation. After a conversion begins, it continues until completion. Additional CNV± pulses are ignored during the conversion phase. After the time, t_{MSB}, elapses, the host begins to burst the CLK± signal to the AD7961. All 18 CLK± pulses must be applied in the window of time framed by t_{MSB} and the subsequent t_{CLKL}. The required 18 CLK± pulses must finish before tCLKL (referenced to the next conversion phase) elapses. Otherwise, the data is lost because it is overwritten by the next conversion result.

Set CLK± to idle high between bursts of 18 CLK± pulses. The header bit and conversion data of the next ADC result are output on subsequent falling edges of CLK± during the next burst of the CLK± signal.

When the self-clocked interface mode is used, the AD7961 also allows the user to provide an extra (19th) clock pulse to see a guaranteed 0 state at the end of the frame, as shown in Figure 37. After t_{MSB} has elapsed, the first bit of the header sequence, 0, automatically appears on D± and the remaining two bits of the header, 10, are then clocked out by the first two CLK± falling edges at the beginning of the next sample. This header (010) is used to synchronize D± of each conversion in the digital host because, in this mode, there is no clock output synchronous to the data (D±) to allow the digital host to acquire the data output.

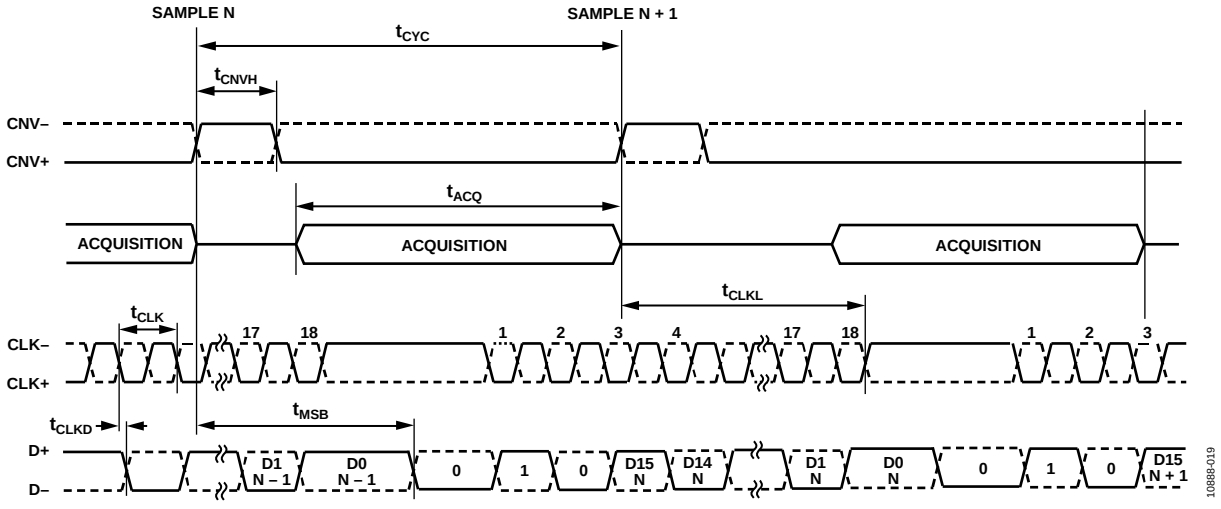


Figure 36. Self Clocked Interface Mode Timing Diagram

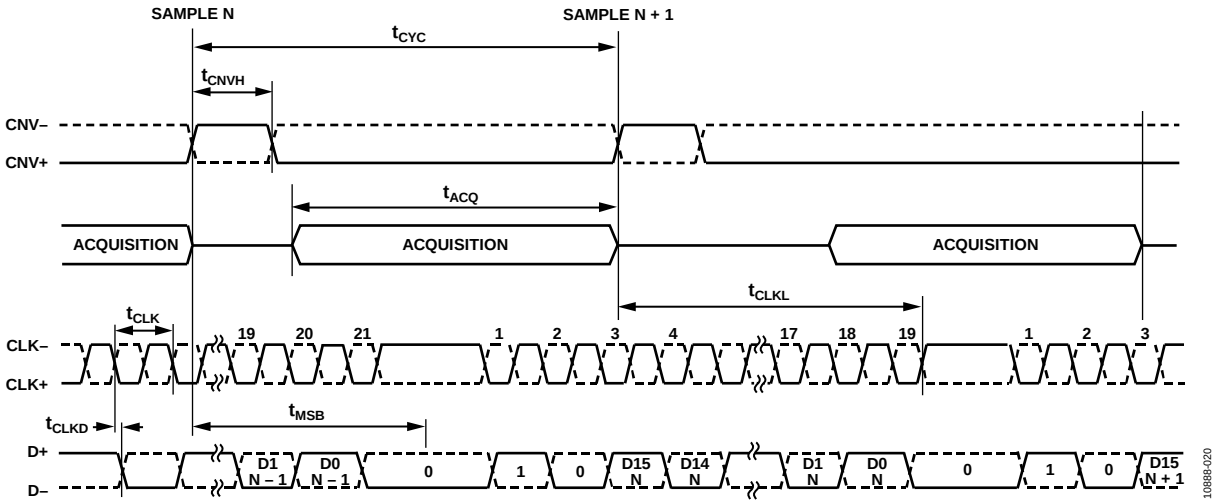


Figure 37. Self Clocked Interface Mode with Extra Clock Pulse Timing Diagram

APPLICATIONS INFORMATION

LAYOUT

Design the printed circuit board that houses the AD7961 so that the analog and digital sections are separated and confined to certain areas of the board. Avoid running digital lines under the device because these couple noise onto the device, unless a ground plane under the AD7961 is used as a shield. Do not run fast switching signals, such as CNV± or CLK±, near analog signal paths. Avoid crossover of digital and analog signals. Use at least one ground plane. It can be common or split between the digital and analog sections. In the latter case, join the planes underneath the AD7961 devices.

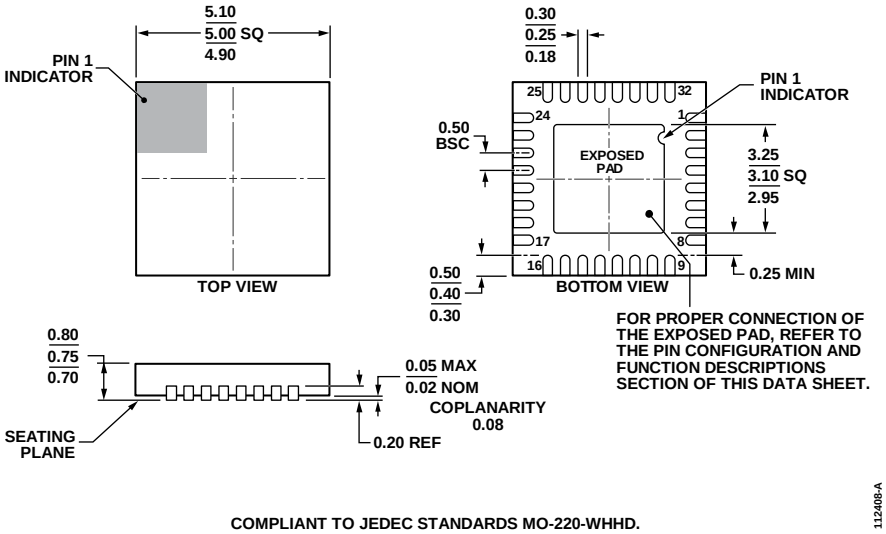
The AD7961 voltage reference input pin, REF, has dynamic input impedance. Decouple REF with minimal parasitic inductances by placing the reference decoupling ceramic capacitor close to and, ideally, right up against the REF and REF_GND pins and connecting them with wide, low impedance traces.

Finally, decouple the VDD1, VDD2, and VIO power supplies of the AD7961 with ceramic capacitors, typically 100 nF, placed close to the AD7961 and connected using short, wide traces to provide low impedance paths and to reduce the effect of glitches on the power supply lines.

EVALUATING AD7961 PERFORMANCE

Other recommended guidelines for the AD7961 schematic and layout are outlined in the user guide of the EVAL-AD7961FMCZ board (UG-581). The fully assembled and tested evaluation board, user guide, and software for controlling the EVAL-AD7961FMCZ board from a PC via the EVAL-SDP-CH1Z are available from the Analog Devices website at www.analog.com.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD.

Figure 38. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7961BCPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-7
AD7961BCPZ-RL7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-7
EVAL-AD7961FMCZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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