Dual Pseudo Differential 16-Bit, 1 MSPS PulSAR ADC 12.0 mW in QSOP

Data Sheet **AD7902**

FEATURES

- 16-bit resolution with no missing codes
- Throughput: 1 MSPS
- Low power dissipation
  - 7.0 mW at 1 MSPS (V_{DD1} and V_{DD2} only)
  - 12.0 mW at 1 MSPS (total)
  - 140 µW at 10 kSPS
- INL: ±1.0 LSB typical, ±2.5 LSB maximum
- SINAD: 91 dB at 1 kHz
- THD: −105 dB at 1 kHz
- Pseudo differential analog input range
  - 0 V to V_{REF} with V_{REF} between 2.4 V to 5.1 V
  - Allows use of any input range
  - Easy to drive with the ADA4841-1/ADA4841-2
- No pipeline delay
- Single-supply 2.5 V operation with 1.8 V/2.5 V/3 V/5 V logic interface
- Serial port interface (SPI) QSPI/MICROWIRE/DSP compatible
- 20-lead QSOP package
- Wide operating temperature range: −40°C to +125°C

APPLICATIONS

- Battery-powered equipment
- Communications
- Automated test equipment (ATE)
- Data acquisition
- Medical instrumentation
- Redundant measurement
- Simultaneous sampling

GENERAL DESCRIPTION

The AD7902 is a dual 16-bit, successive approximation, analog-to-digital converter (ADC) that operates from a single power supply, VDDx, per ADC. It contains two low power, high speed, 16-bit sampling ADCs and a versatile serial port interface (SPI). On the CNVx rising edge, the AD7902 samples an analog input, IN+, in the range of 0 V to V_{REF} with respect to a ground sense, IN−. The externally applied reference voltage of the REFx pins (V_{REF}) can be set independently from the supply voltage pins, VDDx. The power of the device scales linearly with throughput.

Using the SDIx inputs, the SPI-compatible serial interface can also daisy-chain multiple ADCs on a single 3-wire bus and provide an optional busy indicator. It is compatible with 1.8 V, 2.5 V, 3 V, or 5 V logic, using the separate VIOx supplies.

The AD7902 is available in a 20-lead QSOP package with operation specified from −40°C to +125°C.

Table 1. MSOP 14-/16-/18-Bit PulSAR® ADCs

Bits	100 kSPS	250 kSPS	400 kSPS to 500 kSPS	1000 kSPS	ADC Driver
18		AD7691[1]	AD7690[1]	AD7982[1]	ADA4941-1
					ADA4841-1
					ADA4841-2
16	AD7680	AD7685[1]	AD7686[1]	AD7980[1]	ADA4941-1
	AD7683	AD7687[1]	AD7688[1]	AD7903	ADA4841-1
	AD7684	AD7694	AD7693[1]	AD7902	ADA4841-2
14	AD7940	AD7942[1]	AD7946[1]		

[1] Pin-for-pin compatible.

FUNCTIONAL BLOCK DIAGRAM

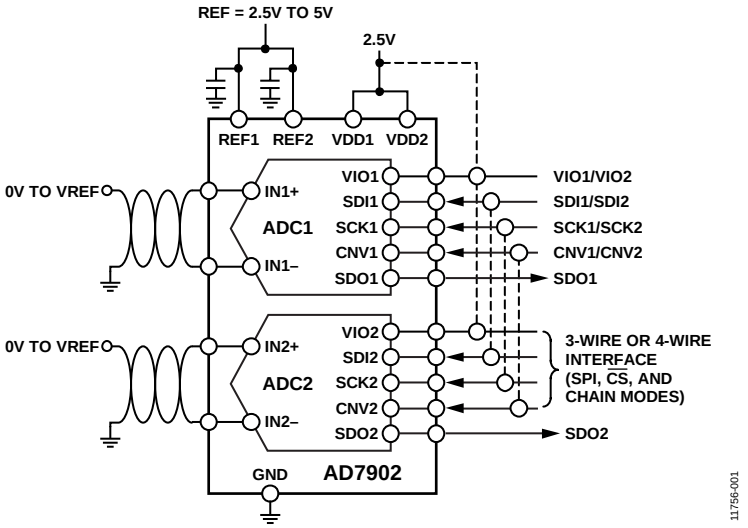


Figure 1.

Rev. B

Document Feedback

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REVISION HISTORY

8/15—Rev. A to Rev. B

Changed ADA4841-x to ADA4841-1/ADA4841-2 .. Throughout
Change to Absolute Input Voltage Parameter, Table 2 ... 3
Changes to Voltage Reference Input Section ... 16
Updated Outline Dimensions ... 27

7/14—Rev. 0 to Rev. A

Changed Standby Current Unit from nA to μA ... 4
Changes to Power Supply Section ... 17

2/14—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.5 V, V_{IO} = 2.3 V to 5.5 V, V_{REF} = 5 V, T_A = −40°C to +125°C, unless otherwise noted.[1]

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT[2]					
Voltage Range	INx+ − INx−	0		V_{REF}	V
Absolute Input Voltage	INx+	−0.1		V_{REF} + 0.1	V
	INx−	−0.1	0	+0.1	V
Analog Input CMRR	f_{IN} = 450 kHz		67		dB
Leakage Current at 25°C	Acquisition phase		200		nA
ACCURACY					
No Missing Codes		16			Bits
Differential Nonlinearity Error[3]	V_{REF} = 5 V	−1.0	±0.5	+1.0	LSB
	V_{REF} = 2.5 V		±0.8		LSB
Integral Nonlinearity Error[3]	V_{REF} = 5 V	−2.5	±1.0	+2.5	LSB
	V_{REF} = 2.5 V		±0.9		LSB
Transition Noise[3]	V_{REF} = 5 V		0.75		LSB
	V_{REF} = 2.5 V		1.2		LSB
Gain Error[4]	T_{MIN} to T_{MAX}	−0.08	±0.012	+0.08	% FS
Gain Error Temperature Drift			0.3		ppm/°C
Gain Error Match[4]	T_{MIN} to T_{MAX}		0.016	0.08	% FS
Zero Error[4]	T_{MIN} to T_{MAX}	−1.25	±0.25	+1.25	mV
Zero Temperature Drift			0.19		ppm/°C
Zero Error Match[4]	T_{MIN} to T_{MAX}		0.2	1.0	mV
Power Supply Sensitivity[3]	V_{DD} = 2.5 V ± 5%		±0.1		LSB
THROUGHPUT					
Conversion Rate	V_{IO} ≥ 2.3 V up to 85°C, V_{IO} ≥ 3.3 V above 85°C, up to 125°C	0		1	MSPS
Transient Response	Full-scale step			290	ns
AC ACCURACY[5]					
Dynamic Range	V_{REF} = 5 V		92		dB
	V_{REF} = 2.5 V		87		dB
Oversampled Dynamic Range	f_{OUT} = 10 kSPS		111		dB
Signal-to-Noise Ratio (SNR)	f_{IN} = 1 kHz, V_{REF} = 5 V	89.5	91.5		dB
	f_{IN} = 1 kHz, V_{REF} = 2.5 V	84.5	86.5		dB
Spurious-Free Dynamic Range (SFDR)	f_{IN} = 1 kHz		−105		dB
Total Harmonic Distortion (THD)	f_{IN} = 1 kHz		−105		dB
Signal-to-Noise-and-Distortion Ratio (SINAD)	f_{IN} = 1 kHz, V_{REF} = 5 V	89	91		dB
	f_{IN} = 1 kHz, V_{REF} = 2.5 V	84	86		dB
Channel-to-Channel Isolation	f_{IN} = 10 kHz		−112		dB

[1] The voltages for the VDDx, VIOx, and REFx pins are indicated by V_{DD}, V_{IO}, and V_{REF}, respectively.
[2] For information regarding input impedance, see the Analog Inputs section.
[3] For the 5 V input range, 1 LSB = 76.3 µV. For the 2.5 V input range, 1 LSB = 38.2 µV.
[4] See the Terminology section. These specifications include full temperature range variation, but they do not include the error contribution from the external reference.
[5] All specifications in decibels (dB) are referred to a full-scale input FSR. Although these parameters are referred to full scale, they are tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

V_{DD} = 2.5 V, V_{IO} = 2.3 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise noted.[1]

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
REFERENCE					
Voltage Range		2.4		5.1	V
Load Current	1 MSPS, V_{REF} = 5 V, each ADC		330		µA
SAMPLING DYNAMICS					
−3 dB Input Bandwidth			10		MHz
Aperture Delay	V_{DD} = 2.5 V		2.0		ns
Aperture Delay Match	V_{DD} = 2.5 V		2.0		ns
DIGITAL INPUTS					
Logic Levels					
V_{IL}	V_{IO} > 3 V	−0.3		$+0.3 \times V_{IO}$	V
	V_{IO} ≤ 3 V	−0.3		$+0.1 \times V_{VIO}$	V
V_{IH}	V_{IO} > 3 V	$0.7 \times V_{IO}$		V_{IO} + 0.3	V
	V_{IO} ≤ 3 V	$0.9 \times V_{IO}$		V_{IO} + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format			Straight binary		Bits
Pipeline Delay	No delay, conversion results available immediately after conversion is complete			0	Samples
V_{OL}	I_{SINK} = 500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	V_{IO} − 0.3			V
POWER SUPPLIES					
VDDx		2.375	2.5	2.625	V
VIOx	Specified performance	2.3		5.5	V
VIOx Range	Full range	1.8		5.5	V
I_{VDDx}	Each ADC		1.4	1.6	mA
I_{VIOx}	Each ADC		0.2	0.45	mA
Standby Current[2, 3]	V_{DD} and V_{IO} = 2.5 V, 25°C		0.35		µA
Power Dissipation	10 kSPS throughput		140		µW
	1 MSPS throughput		12.0	16	mW
VDDx Only	1 MSPS throughput		7.0		mW
REF Only			3.3		mW
VIO Only			1.7		mW
Energy per Conversion			7.0		nJ/sample
TEMPERATURE RANGE[4]					
Specified Performance	T_{MIN} to T_{MAX}	−40		+125	°C

[1] In this data sheet, the voltages for the VDDx, VIOx, and REFx pins are indicated by V_{DD}, V_{IO}, and V_{REF}, respectively.
[2] With all digital inputs forced to VIOx or to ground, as required.
[3] During the acquisition phase.
[4] Contact Analog Devices, Inc., for the extended temperature range.

TIMING SPECIFICATIONS

−40°C to +125°C, V_{DD} = 2.37 V to 2.63 V, V_{IO} = 2.3 V to 5.5 V, unless otherwise stated. See Figure 2 and Figure 3 for load conditions. See Figure 39, Figure 41, Figure 43, Figure 45, Figure 47, Figure 49, and Figure 51 for timing diagrams.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
Conversion Time (CNVx Rising Edge to Data Available)	t_{CONV}	500		710	ns
Acquisition Time	t_{ACQ}	290			ns
Time Between Conversions	t_{CYC}				
VIOx Above 2.3 V		1000			ns
CNVx Pulse Width ($\overline{CS}$ Mode)	t_{CNVH}	10			ns
SCKx Period ($\overline{CS}$ Mode)	t_{SCK}				
VIOx Above 4.5 V		10.5			ns
VIOx Above 3 V		12			ns
VIOx Above 2.7 V		13			ns
VIOx Above 2.3 V		15			ns
SCKx Period (Chain mode)	t_{SCK}				
VIOx Above 4.5 V		11.5			ns
VIOx Above 3 V		13			ns
VIOx Above 2.7 V		14			ns
VIOx Above 2.3 V		16			ns
SCKx Low Time	t_{SCKL}	4.5			ns
SCKx High Time	t_{SCKH}	4.5			ns
SCKx Falling Edge to Data Remains Valid	t_{HSDO}	3			ns
SCKx Falling Edge to Data Valid Delay	t_{DSDO}				
VIOx Above 4.5 V				9.5	ns
VIOx Above 3 V				11	ns
VIOx Above 2.7 V				12	ns
VIOx Above 2.3 V				14	ns
CNVx or SDIx Low to SDOx, D15 (MSB) Valid ($\overline{CS}$ Mode)	t_{EN}				
VIOx Above 3 V				10	ns
VIOx Above 2.3 V				15	ns
CNVx or SDIx High or Last SCKx Falling Edge to SDOx High Impedance ($\overline{CS}$ Mode)	t_{DIS}			20	ns
SDIx Valid Setup Time from CNVx Rising Edge($\overline{CS}$ Mode)	$t_{SSDICNV}$	5			ns
SDIx Valid Hold Time from CNVx Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$	2			ns
SCKx Valid Setup Time from CNVx Rising Edge (Chain Mode)	$t_{SSCKCNV}$	5			ns
SCKx Valid Hold Time from CNVx Rising Edge (Chain Mode)	$t_{HSCKCNV}$	5			ns
SDIx Valid Setup Time from SCKx Falling Edge (Chain Mode)	$t_{SSDISCK}$	2			ns
SDIx Valid Hold Time from SCKx Falling Edge (Chain Mode)	$t_{HSDISCK}$	3			ns
SDIx High to SDOx High (Chain Mode with Busy Indicator)	$t_{DSDOSDI}$			15	ns

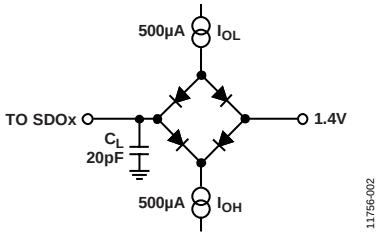


Figure 2. Load Circuit for Digital Interface Timing

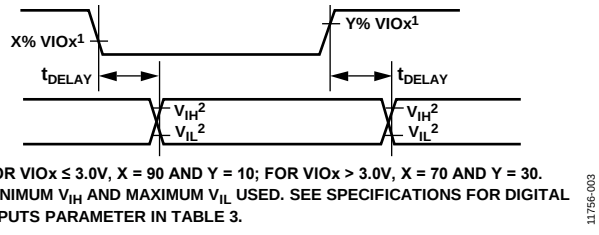


Figure 3. Voltage Levels for Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Analog Inputs	
INx+, INx− to GND[1]	−0.3 V to V_{REF} + 0.3 V or ±10 mA
Supply Voltage	
REFx, VIOx to GND	−0.3 V to +6.0 V
VDDx to GND	−0.3 V to +3.0 V
VDDx to VIOx	+3 V to −6 V
Digital Inputs to GND	−0.3 V to V_{IO} + 0.3 V
Digital Outputs to GND	−0.3 V to V_{IO} + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temperatures	
Vapor Phase (60 sec)	255°C
Infrared (15 sec)	260°C

[1] See the Analog Inputs section for an explanation of INx+ and INx−.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

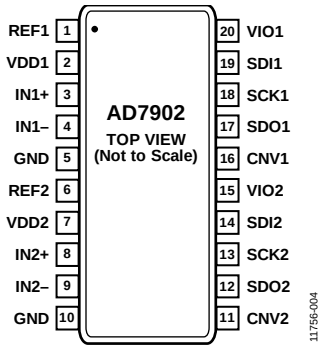


Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 6	REF1, REF2	AI	Reference Input Voltage. The REFx range is 2.4 V to 5.1 V. These pins are referred to the GND pin, and decouple each pin closely to the GND pin with a 10 µF capacitor.
2, 7	VDD1, VDD2	P	Power Supplies.
3, 8	IN1+, IN2+	AI	Pseudo Differential Positive Analog Inputs.
4, 9	IN1−, IN2−	AI	Pseudo Differential Negative Analog Inputs.
5, 10	GND	P	Power Supply Ground.
11, 16	CNV2, CNV1	DI	Conversion Inputs. These inputs have multiple functions. On the leading edge, they initiate conversions and select the interface mode of the device: chain mode or active low chip select mode ($\overline{CS}$ mode). In $\overline{CS}$ mode, the SDOx pins are enabled when the CNVx pins are low. In chain mode, the data must be read when the CNVx pins are high.
12, 17	SDO2, SDO1	DO	Serial Data Outputs. The conversion result is output on these pins. The conversion result is synchronized to SCKx.
13, 18	SCK2, SCK1	DI	Serial Data Clock Inputs. When the device is selected, the conversion results are shifted out by these clocks.
14, 19	SDI2, SDI1	DI	Serial Data Inputs. These inputs provide multiple functions. They select the interface mode of the ADC, as follows: $\overline{CS}$ mode is selected if the SDIx pins are high during the CNVx rising edge. In this mode, either SDIx or CNVx can enable the serial output signals when low. If SDIx or CNVx is low when the conversion is complete, the busy indicator feature is enabled.
15, 20	VIO2, VIO1	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (2.5 V or 3 .3 V).

[1] AI is analog input, DI is digital input, DO is digital output, and P is power.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 2.5 V, V_{REF} = 5.0 V, V_{IO} = 3.3 V, T_A = 25°C, f_{SAMPLE} = 1 MSPS, f_{IN} = 10 kHz, unless otherwise noted.

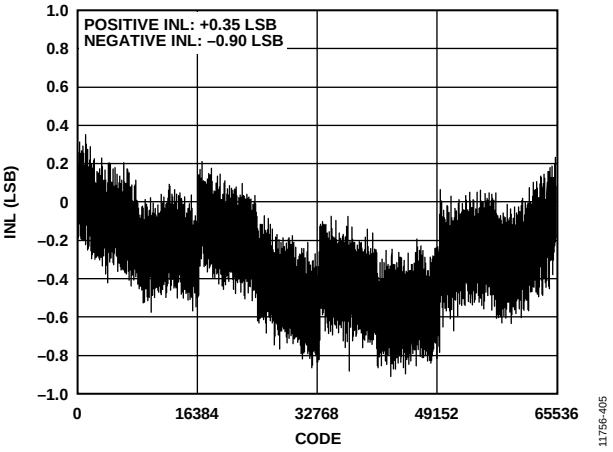


Figure 5. Integral Nonlinearity vs. Code, V_{REF} = 5 V

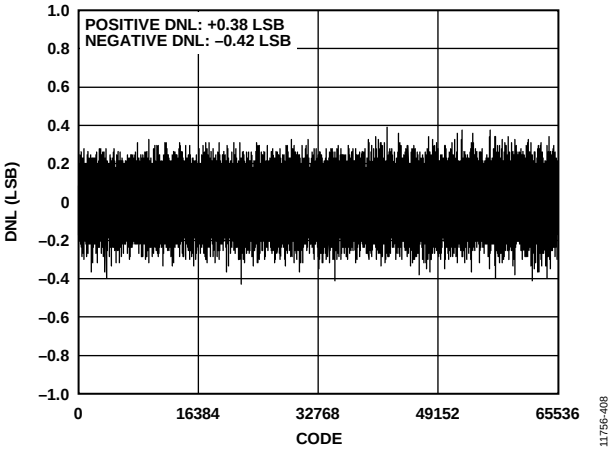


Figure 8. Differential Nonlinearity vs. Code, V_{REF} = 5 V

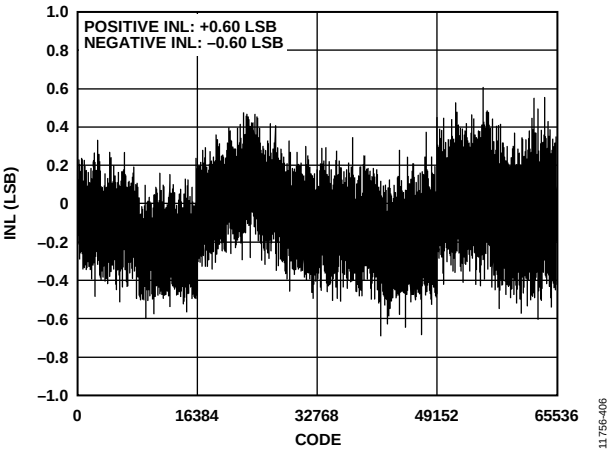


Figure 6. Integral Nonlinearity vs. Code, V_{REF} = 2.5 V

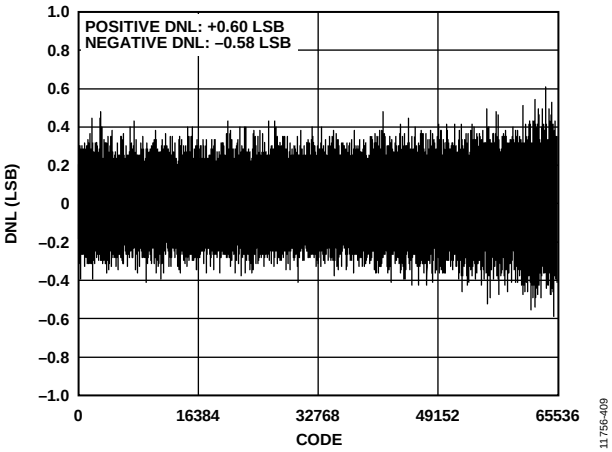


Figure 9. Differential Nonlinearity vs. Code, V_{REF} = 2.5 V

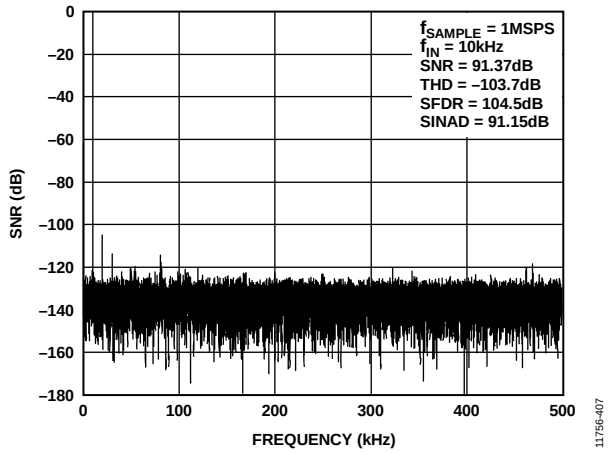


Figure 7. FFT Plot, V_{REF} = 5 V

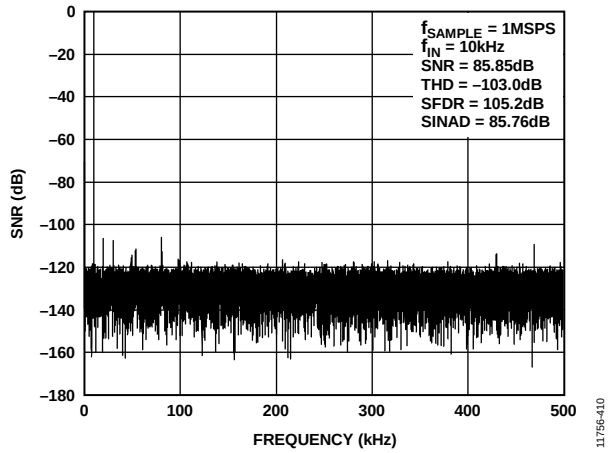


Figure 10. FFT Plot, V_{REF} = 2.5 V

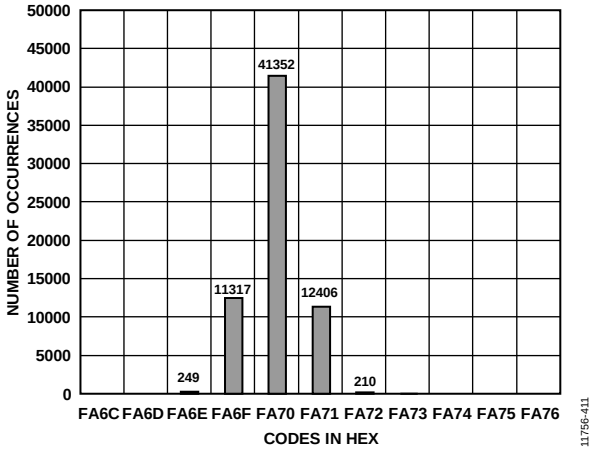


Figure 11. Histogram of a DC Input at the Code Center, V_{REF} = 5 V

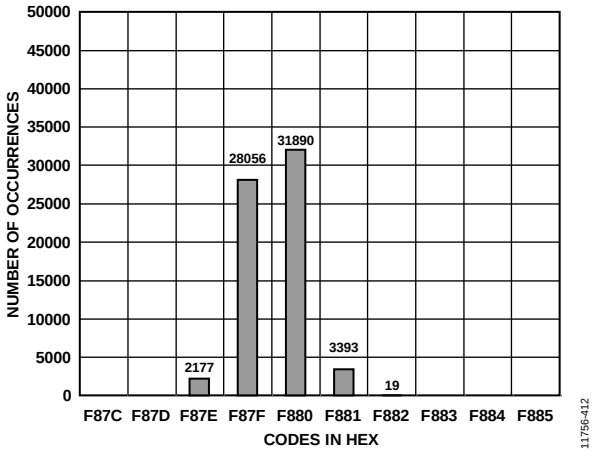


Figure 12. Histogram of a DC Input at the Code Transition, V_{REF} = 5 V

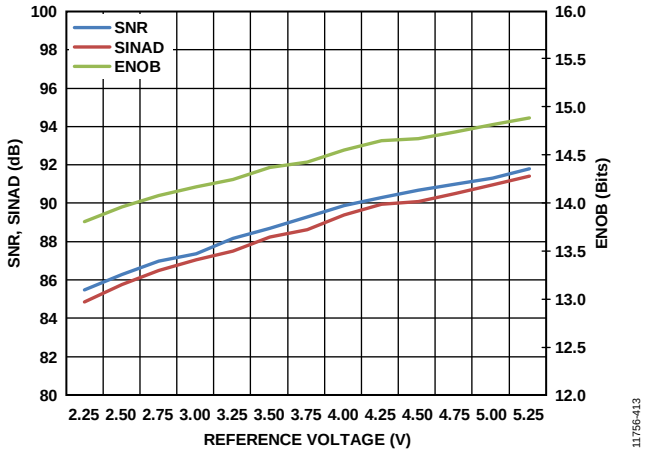


Figure 13. SNR, SINAD, and ENOB vs. Reference Voltage

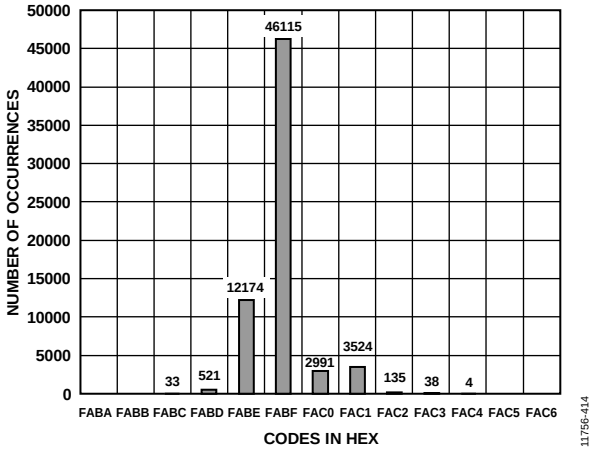


Figure 14. Histogram of a DC Input at the Code Center, V_{REF} = 2.5 V

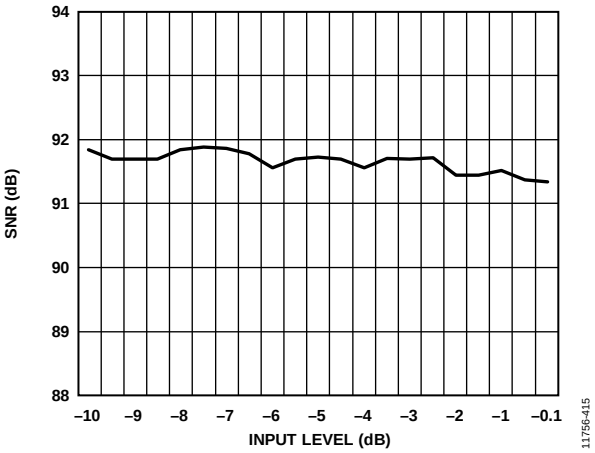


Figure 15. SNR vs. Input Level

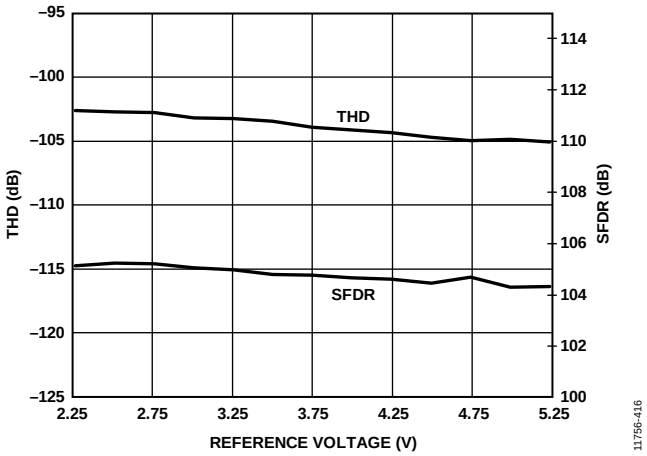


Figure 16. THD and SFDR vs. Reference Voltage

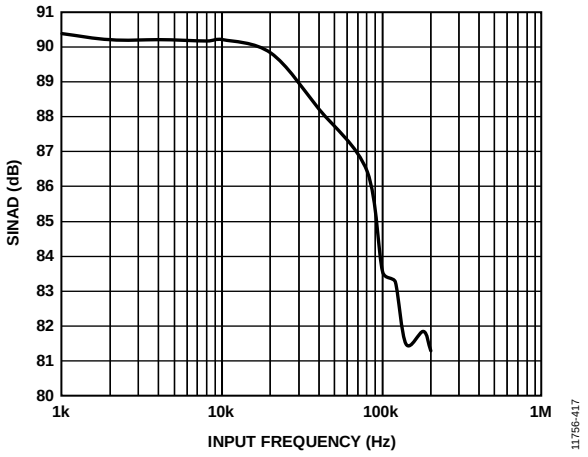


Figure 17. SINAD vs. Input Frequency

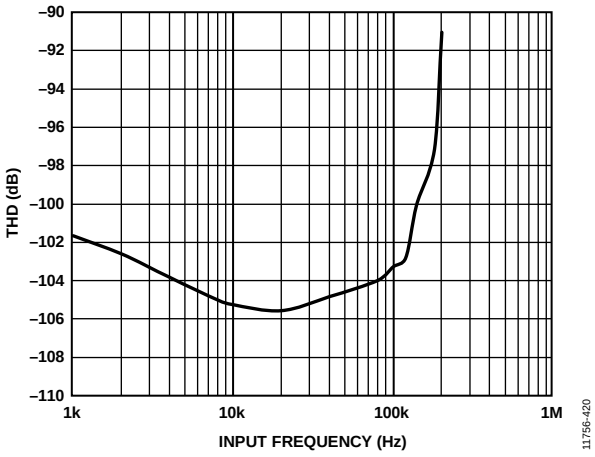


Figure 20. THD vs. Input Frequency

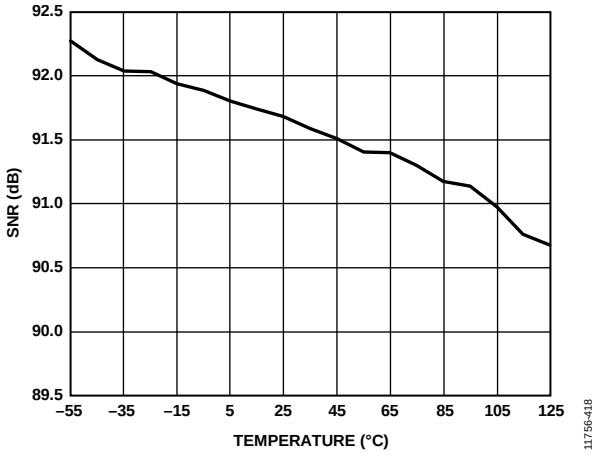


Figure 18. SNR vs. Temperature

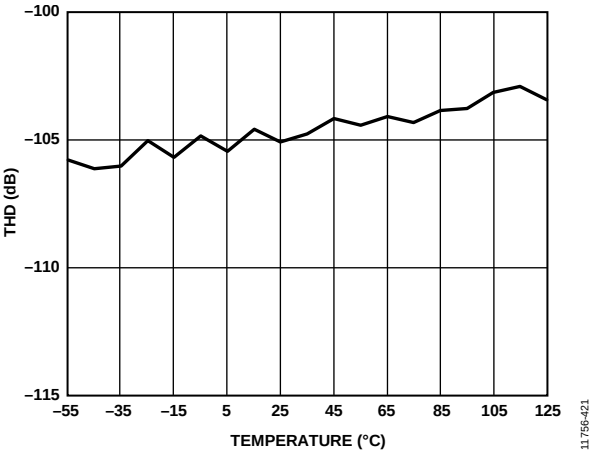


Figure 21. THD vs. Temperature

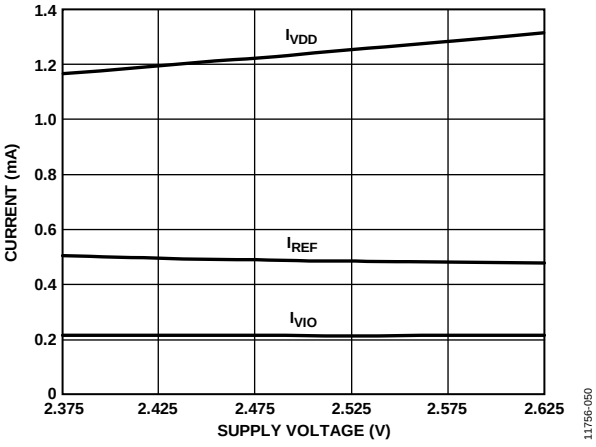


Figure 19. Operating Currents for Each ADC vs. Supply Voltage

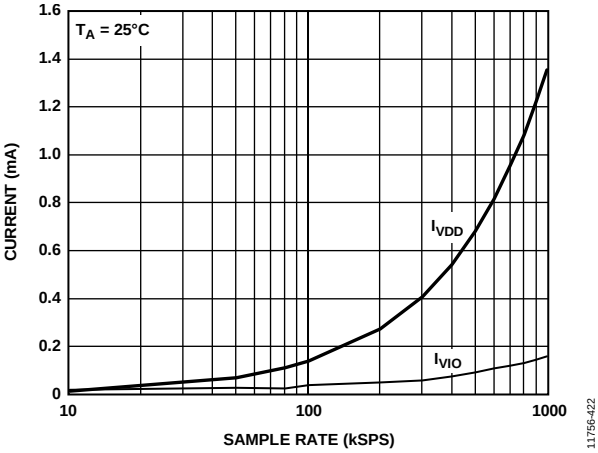


Figure 22. Operating Currents for Each ADC vs. Throughput

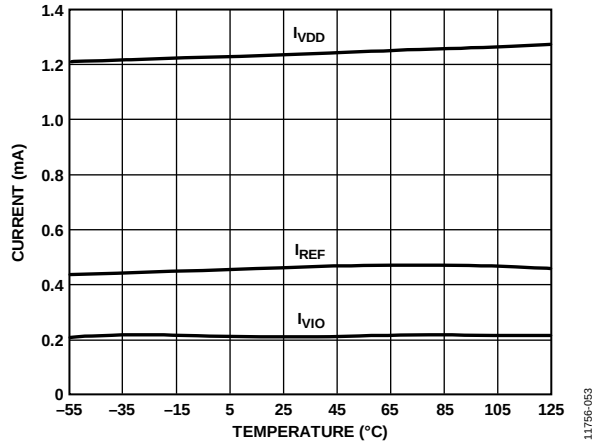


Figure 23. Operating Currents for Each ADC vs. Temperature

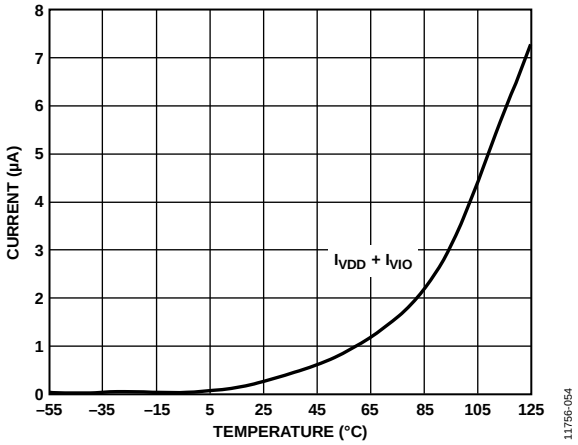


Figure 26. Power-Down Current for Each ADC vs. Temperature

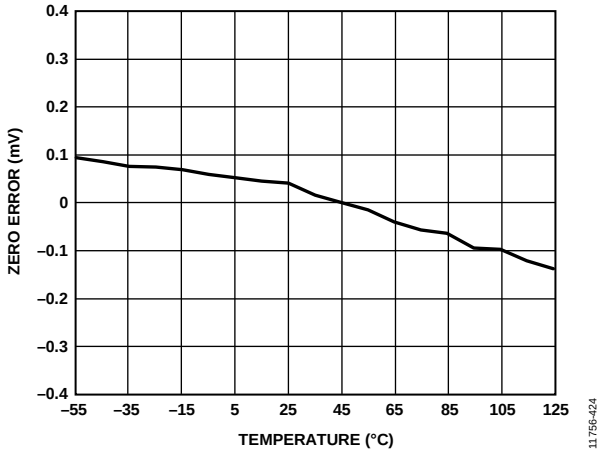


Figure 24. Zero Error vs. Temperature

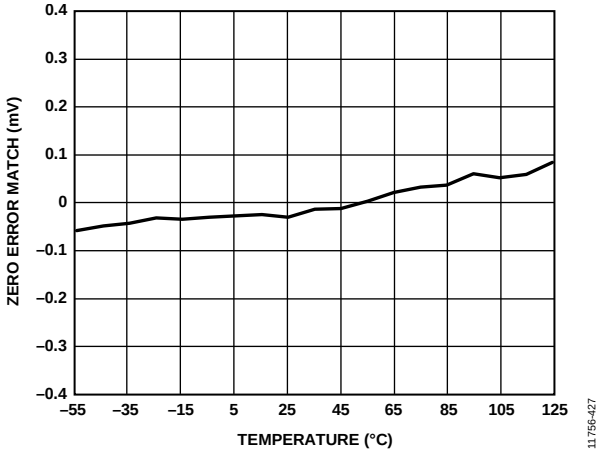


Figure 27. Zero Error Match vs. Temperature

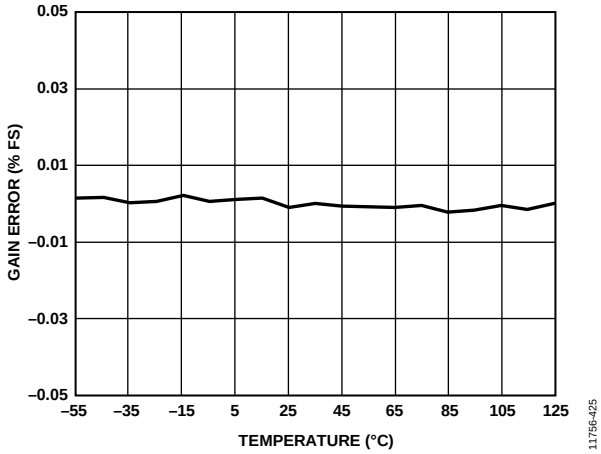


Figure 25. Gain Error vs. Temperature

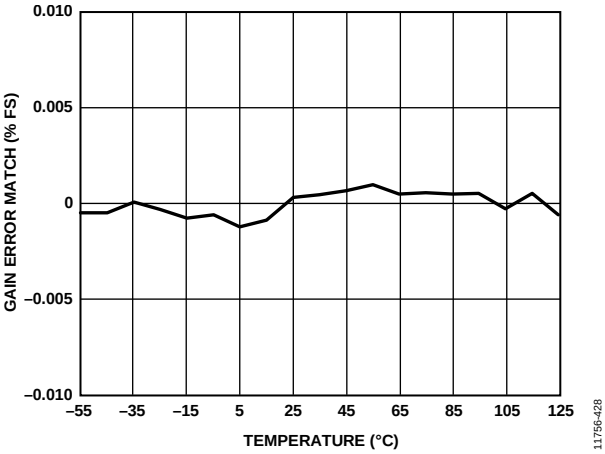


Figure 28. Gain Error Match vs. Temperature

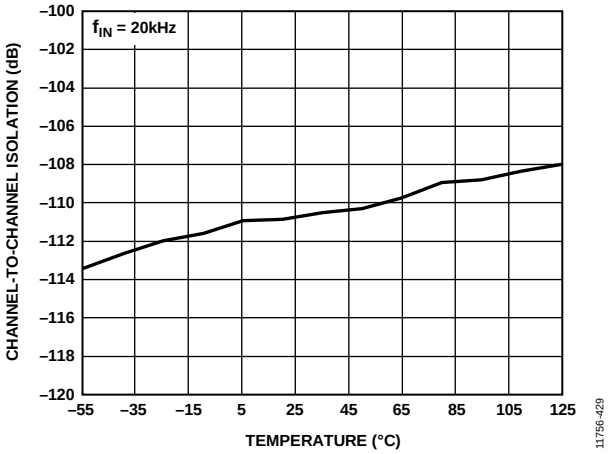


Figure 29. Channel-to-Channel Isolation vs. Temperature

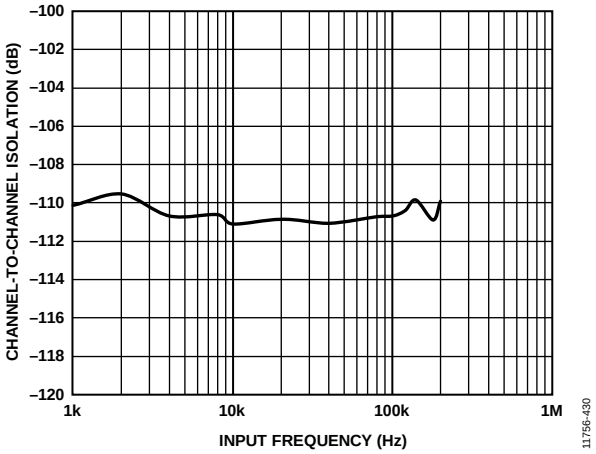


Figure 30. Channel-to-Channel Isolation vs. Input Frequency

TERMINOLOGY

Integral Nonlinearity Error (INL)

INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 32).

Differential Nonlinearity Error (DNL)

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Zero Error
The first transition should occur at a level ½ LSB above analog ground (38.1 µV for the 0 V to 5 V range). The zero error is the deviation of the actual transition from that point.

Zero Error Match
It is the difference in offsets, expressed in millivolts between the channels of a multichannel converter. It is computed with the following equation:

$$Zero\ Matching = V_{ZEROMAX} - V_{ZEROMIN}$$

where:
$V_{ZEROMAX}$ is the most positive zero error.
$V_{ZEROMIN}$ is the most negative zero error.

Zero error matching is usually expressed in millivolts with the full-scale input range stated in the product data sheet.

Gain Error
The last transition (from 111 … 10 to 111 … 11) should occur for an analog voltage 1½ LSB below the nominal full scale (4.999886 V for the 0 V to 5 V range). The gain error is the deviation of the actual level of the last transition from the ideal level after the offset is adjusted out.

Gain Error Match

It is the ratio of the maximum full scale to the minimum full scale of a multichannel ADC. It is expressed as a percentage of full scale using the following equation:

$$Gain\ Matching = \left(\frac{FSR_{MAX} - FSR_{MIN}}{2^N}\right) \times 100\%$$

where:
FSR_{MAX} is the most positive gain error of the ADC.
FSR_{MIN} is the most negative gain error.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD by the following formula:

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

ENOB is expressed in bits.

Noise Free Code Resolution
Noise free code resolution is the number of bits beyond which it is impossible to distinctly resolve individual codes. It is calculated as follows:

$$Noise\ Free\ Code\ Resolution = \log_2(2^N/Peak\text{-}to\text{-}Peak\ Noise)$$

Noise free code resolution is expressed in bits.

Effective Resolution
Effective resolution is calculated as follows:

$$Effective\ Resolution = \log_2(2^N/RMS\ Input\ Noise)$$

Effective resolution is expressed in bits.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels (dB).

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels (dB). It is measured with a signal at −60 dBFS to include all noise sources and DNL artifacts.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels (dB).

Signal-to-Noise-and-Distortion Ratio (SINAD)

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels (dB).

Aperture Delay
Aperture delay is the measure of the acquisition performance. It is the time between the rising edge of the CNVx input and when the input signal is held for a conversion.

Transient Response
Transient response is the time required for the ADC to accurately acquire its input after a full-scale step function is applied.

THEORY OF OPERATION

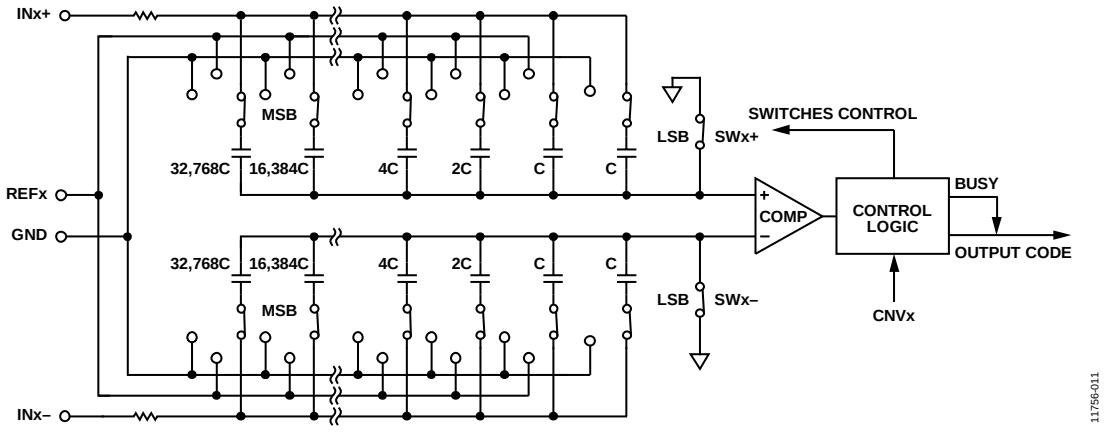


Figure 31. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7902 is a fast, low power, precise, dual 16-bit ADC using a successive approximation architecture.

The AD7902 is capable of simultaneously converting 1,000,000 samples per second (1 MSPS) and powers down between conversions. When operating at 10 kSPS, for example, it typically consumes 70 µW per ADC, making it ideal for battery-powered applications.

The AD7902 provides the user with an on-chip track-and-hold and does not exhibit any pipeline delay or latency, making it ideal for multichannel multiplexed applications.

The AD7902 can be interfaced to any 1.8 V to 5 V digital logic family. It is available in a 20-lead QSOP that allows for flexible configurations. The device is pin-for-pin compatible with the differential, 16-bit AD7903.

CONVERTER OPERATION

The AD7902 is a dual successive approximation ADC based on a charge redistribution DAC. Figure 31 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary-weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase of each ADC, terminals of the array tied to the input of the comparator are connected to GND via the switches, SWx+ and SWx–. All independent switches are connected to the analog inputs. Therefore, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the INx+ and INx– inputs. When the acquisition phase is complete and the CNVx input goes high, a conversion phase is initiated. When the conversion phase begins, SWx+ and SWx– are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the INx+ and INx– inputs, captured at the end of the acquisition phase, is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REFx, the comparator input varies by binary-weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ ... $V_{REF}/65,536$). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition. After the completion of this process, the device returns to the acquisition phase, and the control logic generates the ADC output code and a busy signal indicator.

Because the AD7902 has an on-board conversion clock, the serial clock, SCKx, is not required for the conversion process.

Transfer Functions

The ideal transfer characteristic for the AD7902 is shown in Figure 32 and Table 7.

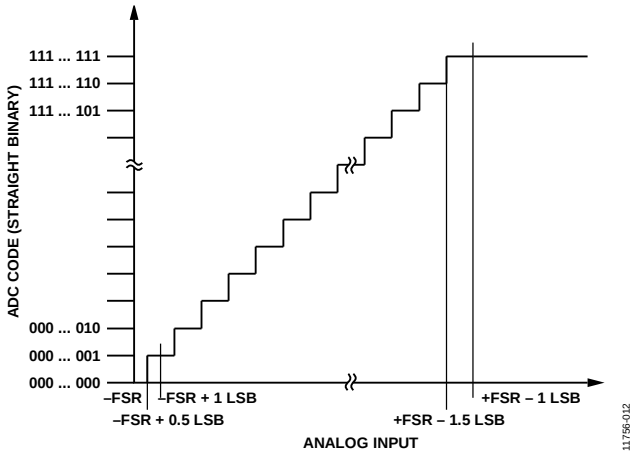


Figure 32. ADC Ideal Transfer Function

Table 7. Output Codes and Ideal Input Voltages

Description	Analog Input, V_{REF} = 5 V	Digital Output Code (Hex)
FSR – 1 LSB	4.999924 V	FFFF[1]
Midscale + 1 LSB	2.500076 V	8001
Midscale	2.5 V	8000
Midscale – 1 LSB	2.499924 V	7FFF
–FSR + 1 LSB	76.3 µV	0001
–FSR	0 V	0000[2]

[1] This is also the code for an overranged analog input ($V_{IN+} – V_{IN–}$ above $V_{REF} – V_{GND}$).
[2] This is also the code for an underranged analog input ($V_{IN+} – V_{IN–}$ below V_{GND}).

TYPICAL CONNECTION DIAGRAM

Figure 35 shows an example of the recommended connection diagram for the AD7902 when multiple supplies are available.

ANALOG INPUTS

Figure 33 shows an equivalent circuit of the input structure of the AD7902.

The two diodes, D1 and D2, provide ESD protection for the analog inputs, INx+ and INx−. The analog input signal must not exceed the reference input voltage (V_{REF}) by more than 0.3 V. If the analog input signal exceeds this level, the diodes become forward-biased and start conducting current. These diodes can handle a forward-biased current of 130 mA maximum. However, if the supplies of the input buffer (for example, the supplies of the ADA4841-1 in Figure 35) are different from those of the V_{REF}, the analog input signal may eventually exceed the supply rails by more than 0.3 V. In such a case (for example, an input buffer with a short circuit), the current limitation can be used to protect the device.

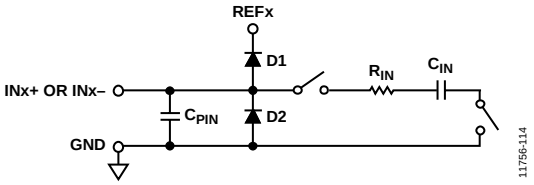


Figure 33. Equivalent Analog Input Circuit

The analog input structure allows for the sampling of the differential signal between INx+ and INx−. By using these differential inputs, signals common to both inputs, and within the allowable common-mode input range, are rejected.

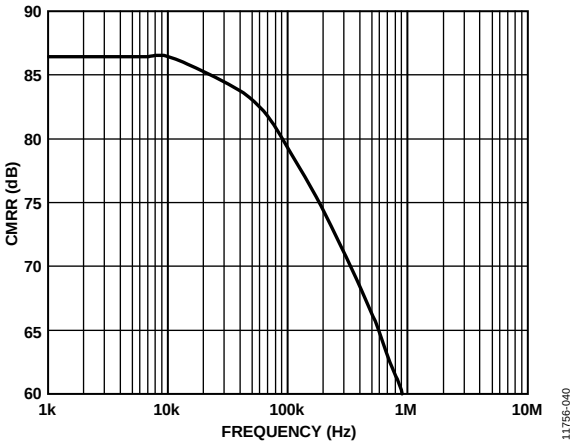
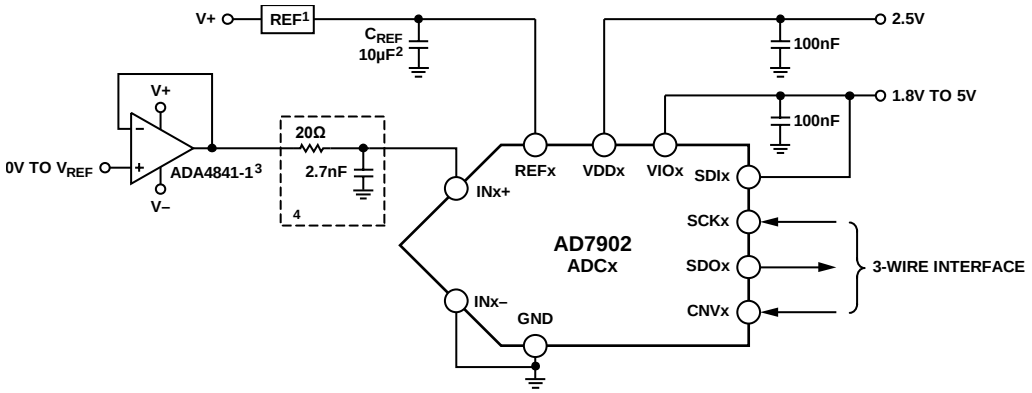


Figure 34. Analog Input CMRR vs. Frequency

During the acquisition phase, the impedance of the analog inputs (INx+ or INx−) can be modeled as a parallel combination of the C_{PIN} capacitor and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 400 Ω and is a lumped component composed of serial resistors and the on resistance of the switches. C_{IN} is typically 30 pF and is mainly the ADC sampling capacitor.

During the sampling phase, where the switches are closed, the input impedance is limited to C_{PIN}. R_{IN} and C_{IN} make a one-pole, low-pass filter that reduces undesirable aliasing effects and limits noise.

When the source impedance of the driving circuit is low, the AD7902 can be driven directly. Large source impedances significantly affect the ac performance, especially THD. The dc performances are less sensitive to the input impedance. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency.



1SEE THE VOLTAGE REFERENCE INPUT SECTION FOR REFERENCE SELECTION.
2C_{REF} IS USUALLY A 10µF CERAMIC CAPACITOR (X5R).
SEE RECOMMENDED LAYOUT IN FIGURE 53.
3SEE THE DRIVER AMPLIFIER CHOICE SECTION.
4OPTIONAL FILTER. SEE THE ANALOG INPUTS SECTION.

Figure 35. Typical Application Diagram with Multiple Supplies

DRIVER AMPLIFIER CHOICE

Although the AD7902 is easy to drive, the driver amplifier must meet the following requirements:

- The noise generated by the driver amplifier must be kept as low as possible to preserve the SNR and transition noise performance of the AD7902. The noise from the driver is filtered by the one-pole, low-pass filter of the AD7902 analog input circuit, made by R_{IN} and C_{IN} or by the external filter, if one is used. Because the typical noise of the AD7902 is 56 μV rms, the SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20 \log \left(\frac{47.3}{\sqrt{47.3^2 + \frac{\pi}{2} f_{-3dB} (Ne_N)^2}} \right)$$

  where:
  f_{-3dB} is the input bandwidth, in megahertz, of the AD7902 (10 MHz) or the cutoff frequency of the input filter, if one is used.
  N is the noise gain of the amplifier (for example, gain = 1 in buffer configuration; see Figure 35).
  e_N is the equivalent input noise voltage of the op amp, in nV/√Hz.
- For ac applications, the driver must have a THD performance that is commensurate with the AD7902.
- For multichannel, multiplexed applications, the driver amplifier and the AD7902 analog input circuit must settle for a full-scale step onto the capacitor array at a 16-bit level (0.0015%, 15 ppm). In the amplifier data sheet, settling at 0.1% to 0.01% is more commonly specified. This may differ significantly from the settling time at a 16-bit level. Be sure to verify the settling time prior to driver selection.

Table 8. Recommended Driver Amplifiers

Amplifier	Typical Application
ADA4841-1/ ADA4841-2	Very low noise, small, and low power
AD8021	Very low noise and high frequency
AD8022	Low noise and high frequency
OP184	Low power, low noise, and low frequency
AD8655	5 V single supply, low noise
AD8605, AD8615	5 V single supply, low power

VOLTAGE REFERENCE INPUT

The AD7902 voltage reference input, REF, has a dynamic input impedance and must therefore be driven by a low impedance source with efficient decoupling between the REFx and GND pins, as explained in the Layout section.

When REF is driven by a very low impedance source (for example, a reference buffer using the AD8031 or the AD8605), a 10 μF (X5R, 0805 size) ceramic chip capacitor is appropriate for optimum performance.

If an unbuffered reference voltage is used, the decoupling value depends on the reference used. For instance, a 22 μF (X5R, 1206 size) ceramic chip capacitor is appropriate for optimum performance using a low temperature drift ADR430, ADR431, ADR433, ADR434, or ADR435 reference.

If desired, a reference decoupling capacitor with values as small as 2.2 μF can be used with a minimal impact on performance, especially DNL.

Regardless, there is no need for an additional lower value ceramic decoupling capacitor (for example, 100 nF) between the REFx and GND pins.

POWER SUPPLY

The AD7902 uses two power supply pins per ADC: a core supply (VDDx) and a digital input/output interface supply (VIOx). VIOx allows direct interface with any logic between 1.8 V and 5.5 V. To reduce the number of supplies needed, VIOx and VDDx can be tied together. The AD7902 is independent of power supply sequencing between VIOx and VDDx. Additionally, it is very insensitive to power supply variations over a wide frequency range, as shown in Figure 36.

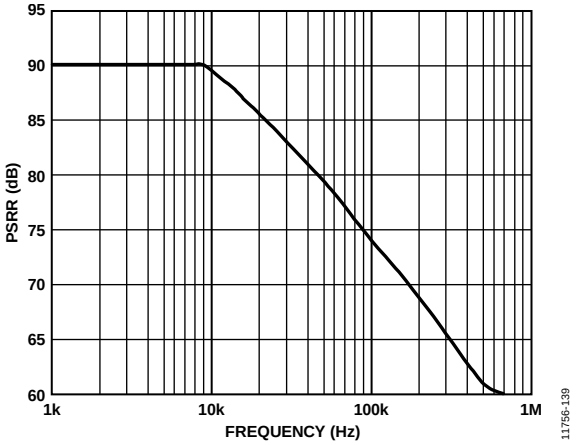


Figure 36. PSRR vs. Frequency

The AD7902 powers down automatically at the end of each conversion phase; therefore, the power scales linearly with the sampling rate. This makes the device ideal for low sampling rates (of even a few hertz) and low battery-powered applications.

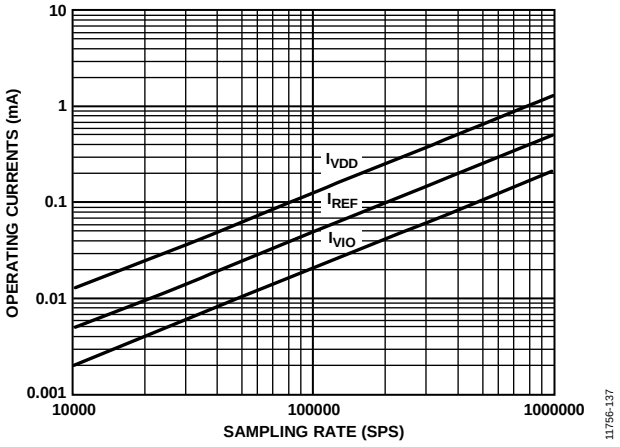


Figure 37. Operating Currents per ADC vs. Sampling Rate

DIGITAL INTERFACE

Although the AD7902 has a reduced number of pins, it offers flexibility in its serial interface modes.

When in $\overline{CS}$ mode, the AD7902 is compatible with SPI, QSPI, digital hosts, and DSPs. In this mode, the AD7902 can use either a 3-wire or 4-wire interface. A 3-wire interface using the CNVx, SCKx, and SDOx signals minimizes wiring connections useful, for instance, in isolated applications. A 4-wire interface using the SDIx, CNVx, SCKx, and SDOx signals allows CNVx, which initiates the conversions, to be independent of the readback timing (SDIx). This is useful in low jitter sampling or simultaneous sampling applications.

When in chain mode, the AD7902 provides a daisy-chain feature using the SDIx input for cascading multiple ADCs on a single data line similar to a shift register. With the AD7902 housing two ADCs in one package, chain mode can be utilized to acquire data from both ADCs while using only one set of 4-wire user interface signals.

The mode in which the device operates depends on the SDIx level when the CNVx rising edge occurs. $\overline{CS}$ mode is selected if SDIx is high, and chain mode is selected if SDIx is low. The SDIx hold time is such that when SDIx and CNVx are connected together, chain mode is always selected.

In either mode, the AD7902 offers the option of forcing a start bit in front of the data bits. This start bit can be used as a busy signal indicator to interrupt the digital host and trigger the data reading. Otherwise, without a busy indicator, the user must time out the maximum conversion time prior to readback.

The busy indicator feature is enabled as follows:

- In $\overline{CS}$ mode when CNVx or SDIx is low when the ADC conversion ends (see Figure 41 and Figure 45).
- In chain mode when SCKx is high during the CNVx rising edge (see Figure 49).

$\overline{CS}$ MODE

$\overline{CS}$ Mode, 3-Wire Interface Without Busy Indicator

$\overline{CS}$ mode, using a 3-wire interface without a busy indicator, is usually used when a single AD7902 is connected to a SPI-compatible digital host.

The connection diagram is shown in Figure 38, and the corresponding timing diagram is shown in Figure 39.

With SDIx tied to VIOx, a rising edge on CNVx initiates a conversion, selects $\overline{CS}$ mode, and forces SDOx to high impedance. When a conversion is initiated, it continues until completion, regardless of the state of CNVx. This can be useful, for instance, to bring CNVx low to select other SPI devices, such as analog multiplexers.

However, to avoid generation of the busy signal indicator, CNVx must be returned high before the minimum conversion time elapses and then held high for the maximum possible conversion time. When the conversion is complete, the AD7902 enters the acquisition phase and powers down. When CNVx goes low, the MSB is automatically output onto SDOx. The remaining data bits are clocked by subsequent SCKx falling edges. The data is valid on both SCKx edges. Although the rising edge can be used to capture the data, a digital host using the falling edge of SCKx allows a faster reading rate, provided that it has an acceptable hold time. After the 16th SCKx falling edge or when CNVx goes high (whichever occurs first), SDOx returns to high impedance.

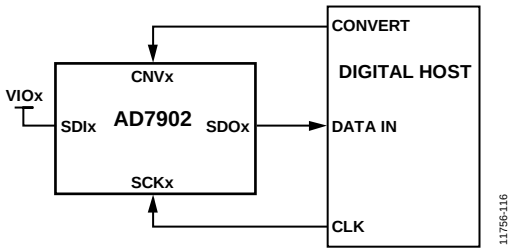


Figure 38. $\overline{CS}$ Mode, 3-Wire Interface Without a Busy Indicator Connection Diagram (SDIx High)

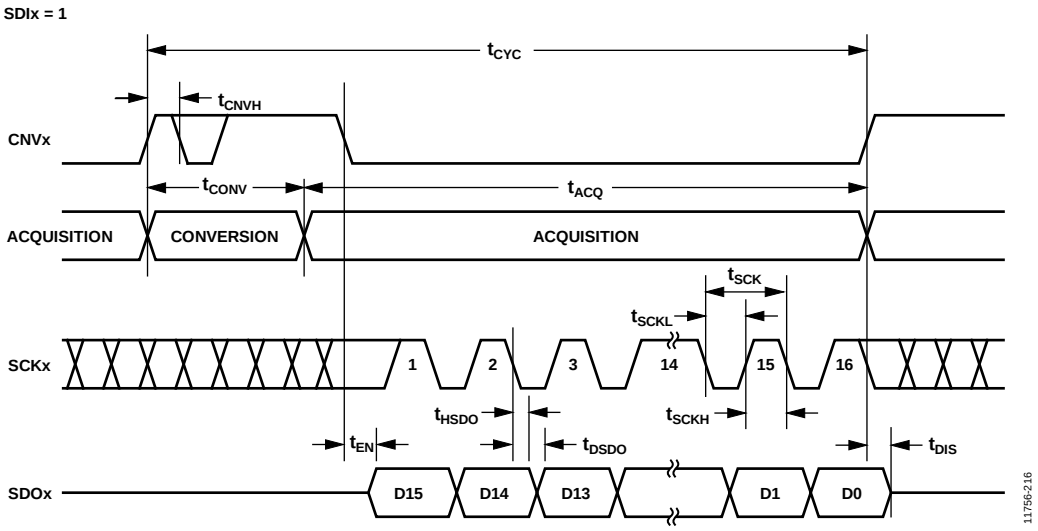


Figure 39. $\overline{CS}$ Mode, 3-Wire Interface Without a Busy Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ Mode, 3-Wire Interface with Busy Indicator

$\overline{CS}$ mode, using a 3-wire interface with a busy indicator, is usually used when a single AD7902 is connected to an SPI-compatible digital host having an interrupt input.

The connection diagram is shown in Figure 40, and the corresponding timing is shown in Figure 41.

With SDIx tied to VIOx, a rising edge on CNVx initiates a conversion, selects $\overline{CS}$ mode, and forces SDOx to high impedance. SDOx is maintained in high impedance until the completion of the conversion, regardless of the state of CNVx. Prior to the minimum conversion time, CNVx can be used to select other SPI devices, such as analog multiplexers, but CNVx must be returned low before the minimum conversion time elapses and then held low for the maximum possible conversion time to guarantee the generation of the busy signal indicator.

When the conversion is complete, SDOx goes from high impedance to low impedance. With a pull-up on the SDOx line, this transition can be used as an interrupt signal to initiate the data reading controlled by the digital host. The AD7902 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCKx falling edges. The data is valid on both SCKx edges. Although the rising edge can be used to capture the data, a digital host using the SCKx falling edge allows a faster reading rate, provided that it has an acceptable hold time. After the optional 17th SCKx falling edge or when CNVx goes high (whichever occurs first), SDOx returns to high impedance.

If multiple ADCs are selected at the same time, the SDOx output pin handles this contention without damage or induced latch-up. Meanwhile, it is recommended that this contention be kept as short as possible to limit extra power dissipation.

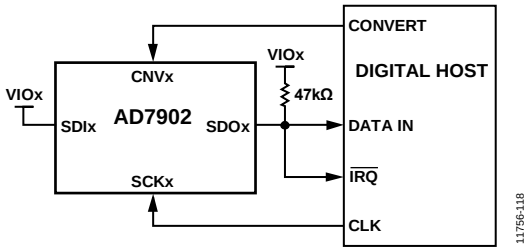


Figure 40. $\overline{CS}$ Mode, 3-Wire Interface with a Busy Indicator Connection Diagram (SDIx High)

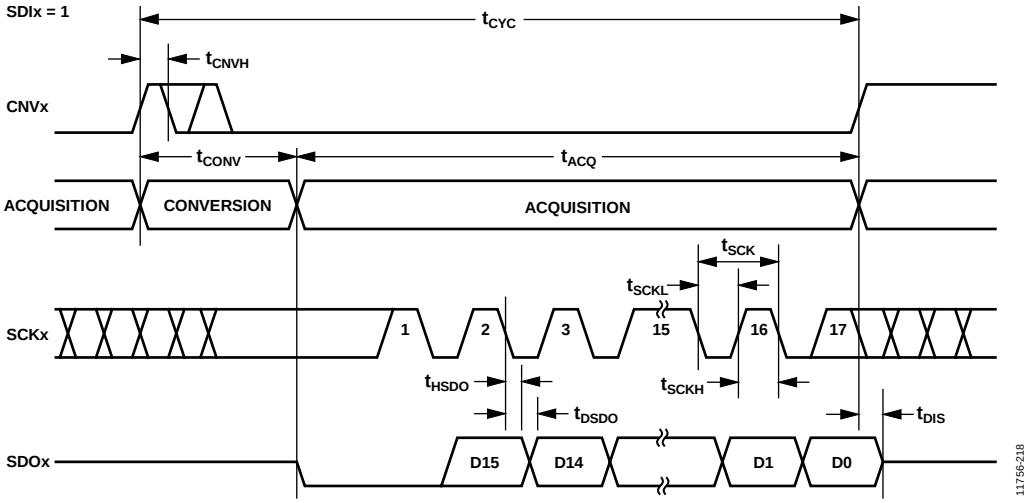


Figure 41. $\overline{CS}$ Mode, 3-Wire Interface with a Busy Indicator Serial Interface Timing (SDIx High)

$\overline{CS}$ Mode, 4-Wire Interface Without Busy Indicator

$\overline{CS}$ mode, using a 4-wire interface without a busy indicator, is usually used when both ADCs within the AD7902 are connected to a SPI-compatible digital host.

See Figure 42 for an AD7902 connection diagram example. The corresponding timing diagram is shown in Figure 43.

With SDIx high, a rising edge on CNVx initiates a conversion, selects $\overline{CS}$ mode, and forces SDOx to high impedance. In this mode, CNVx must be held high during the conversion phase and the subsequent data readback. (If SDIx and CNVx are low, SDOx is driven low.) Prior to the minimum conversion time, SDIx can be used to select other SPI devices, such as analog multiplexers, but SDIx must be returned high before the minimum conversion time elapses and then held high for the maximum possible conversion time to avoid the generation of the busy signal indicator. When the conversion is complete, the AD7902 enters the acquisition phase and powers down. Each ADC result can be read by bringing its respective SDIx input low, which consequently outputs the MSB onto SDOx. The remaining data bits are then clocked by subsequent SCKx falling edges. The data is valid on both SCKx edges. Although the rising edge can be used to capture the data, a digital host using the SCKx falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 16th SCKx falling edge or when SDIx goes high (whichever occurs first), SDOx returns to high impedance, and another ADC result can be read.

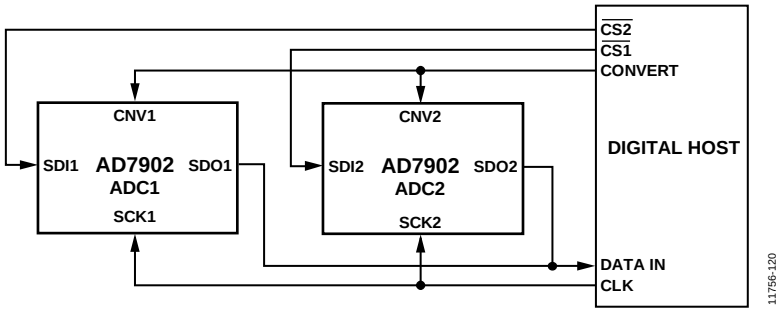


Figure 42. $\overline{CS}$ Mode, 4-Wire Interface Without a Busy Indicator Connection Diagram

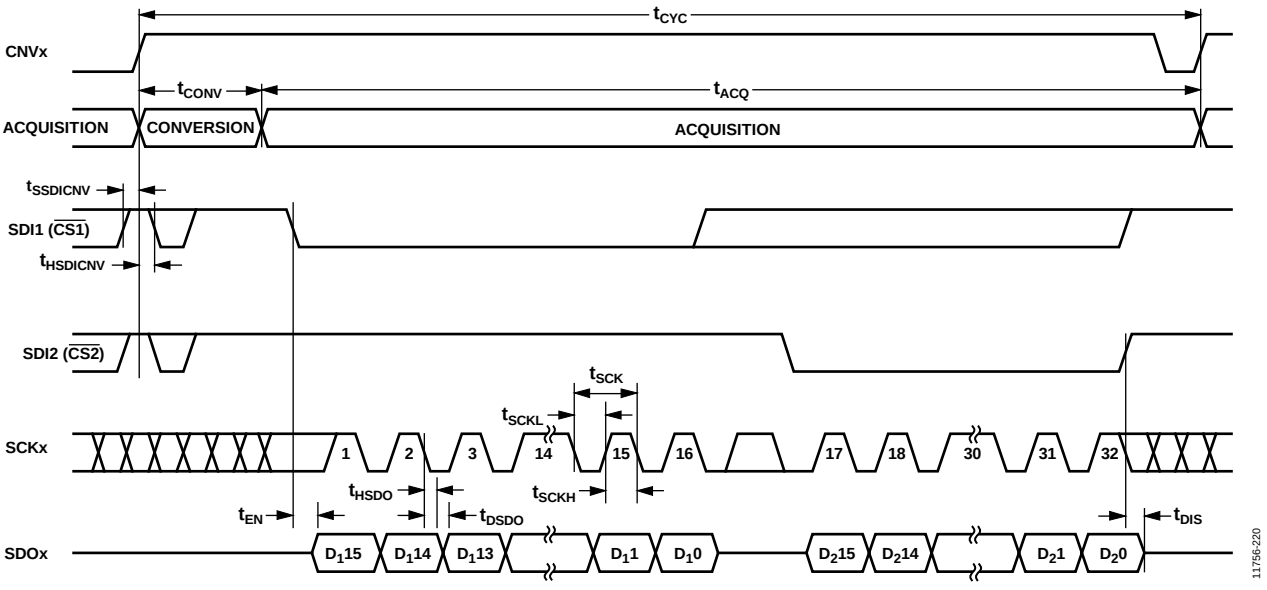


Figure 43. $\overline{CS}$ Mode, 4-Wire Interface Without a Busy Indicator Serial Interface Timing

$\overline{CS}$ Mode, 4-Wire Interface with Busy Indicator

$\overline{CS}$ mode, 4-wire with busy indicator, is usually used when an AD7902 is connected to a SPI-compatible digital host with an interrupt input. This $\overline{CS}$ mode is also used when it is desirable to keep CNVx, which is used to sample the analog input, independent of the signal that is used to select the data reading. This independence is particularly important in applications where low jitter on CNVx is desired.

The connection diagram is shown in Figure 44, and the corresponding timing is given in Figure 45.

With SDIx high, a rising edge on CNVx initiates a conversion, selects $\overline{CS}$ mode, and forces SDOx to high impedance. In this mode, CNVx must be held high during the conversion phase and the subsequent data readback. (If SDIx and CNVx are low, SDOx is driven low.) Prior to the minimum conversion time, SDIx can be used to select other SPI devices, such as analog multiplexers, but SDIx must be returned low before the minimum conversion time elapses and then held low for the maximum possible conversion time to guarantee the generation of the busy signal indicator. When the conversion is complete, SDOx goes from high impedance to low impedance. With a pull-up on the SDOx line, this transition can be used as an interrupt signal to initiate the data readback controlled by the digital host. The AD7902 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCKx falling edges. The data is valid on both SCKx edges. Although the rising edge can be used to capture the data, a digital host using the SCKx falling edge allows a faster reading rate, provided that it has an acceptable hold time. After the optional 17th SCKx falling edge or SDIx going high (whichever occurs first), SDOx returns to high impedance.

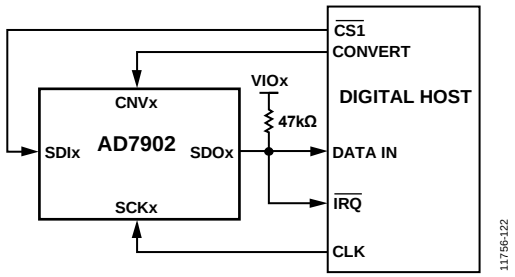


Figure 44. $\overline{CS}$ Mode, 4-Wire Interface with a Busy Indicator Connection Diagram

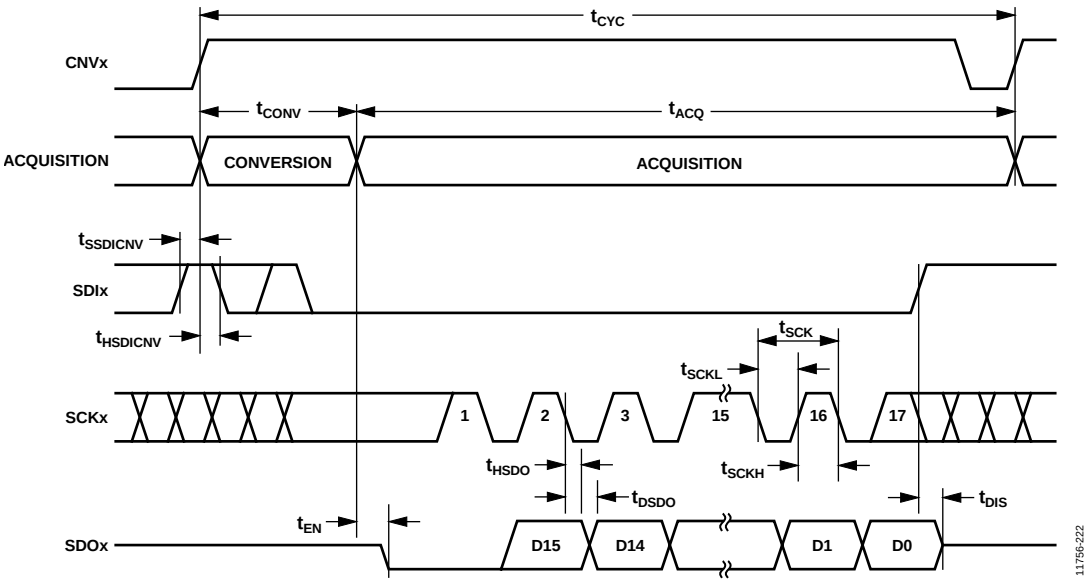


Figure 45. $\overline{CS}$ Mode, 4-Wire Interface with a Busy Indicator Serial Interface Timing

CHAIN MODE

Chain Mode Without Busy Indicator

Chain mode without a busy indicator can be used to daisy-chain both ADCs within an AD7902 on a 3-wire serial interface. This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

See Figure 46 for a connection diagram example using both ADCs in an AD7902. The corresponding timing is shown in Figure 47.

When SDIx and CNVx are low, SDOx is driven low. With SCKx low, a rising edge on CNVx initiates a conversion, selects chain mode, and disables the busy indicator. In this mode, CNVx is held high during the conversion phase and the subsequent data readback. When the conversion is complete, the MSB is output onto SDOx and the AD7902 enters the acquisition phase and powers down. The remaining data bits stored in the internal shift register are clocked by subsequent SCKx falling edges. For each ADC, SDIx feeds the input of the internal shift register and is clocked by the SCKx falling edge. Each ADC in the chain outputs its data MSB first, and 16 × N clocks are required to read back the N ADCs. The data is valid on both SCKx edges. Although the rising edge can be used to capture the data, a digital host using the SCKx falling edge allows a faster reading rate and, consequently, more AD7902 devices in the chain, provided that the digital host has an acceptable hold time. The maximum conversion rate may be reduced due to the total readback time.

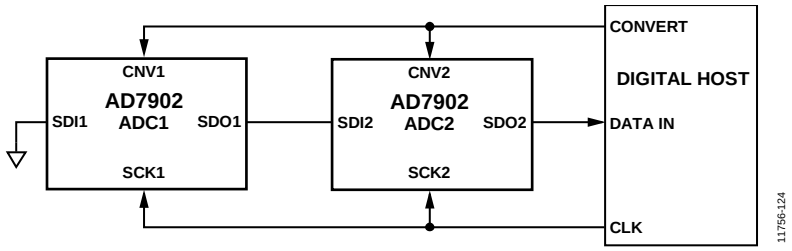


Figure 46. Chain Mode Without a Busy Indicator Connection Diagram

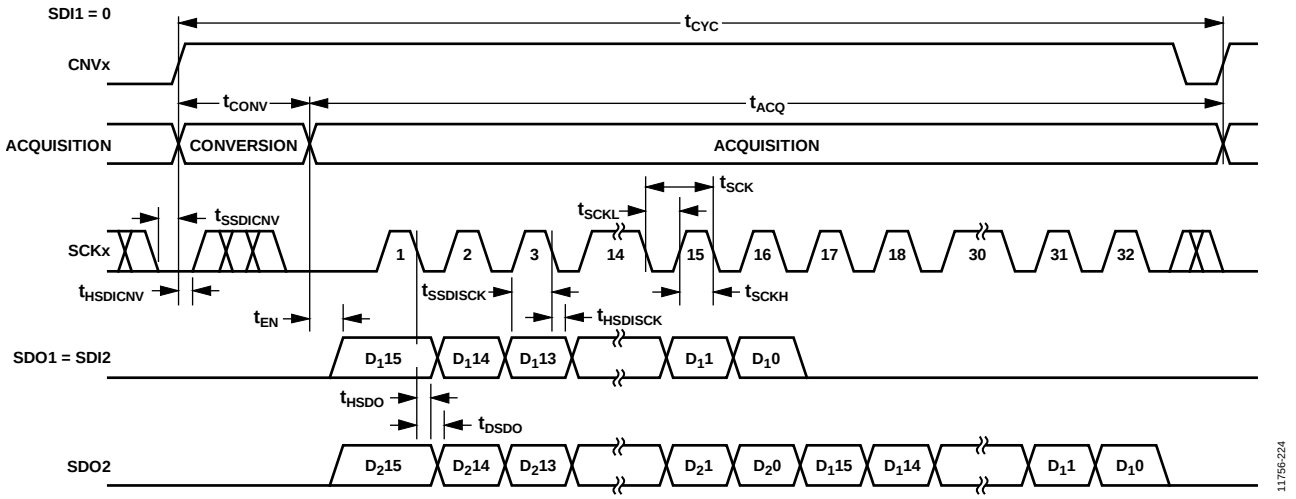


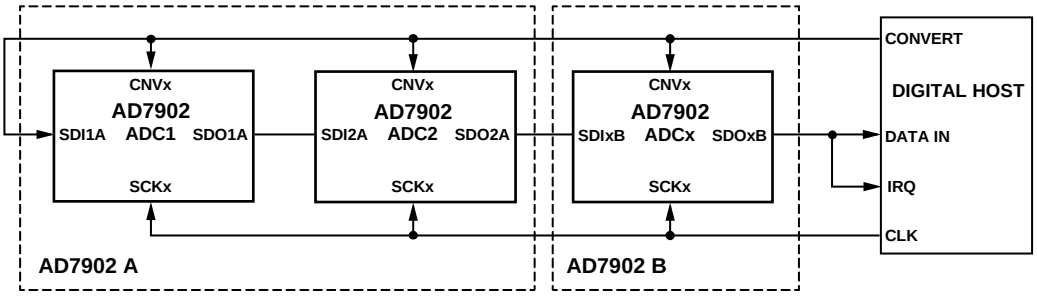
Figure 47. Chain Mode Without a Busy Indicator Serial Interface Timing

Chain Mode with Busy Indicator

Chain mode with a busy indicator can also be used to daisy-chain both ADCs within an AD7902 on a 3-wire serial interface while providing a busy indicator. This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with limited interfacing capacity. Data readback is analogous to clocking a shift register.

See Figure 48 for a connection diagram example using three AD7902 ADCs. The corresponding timing is shown in Figure 49.

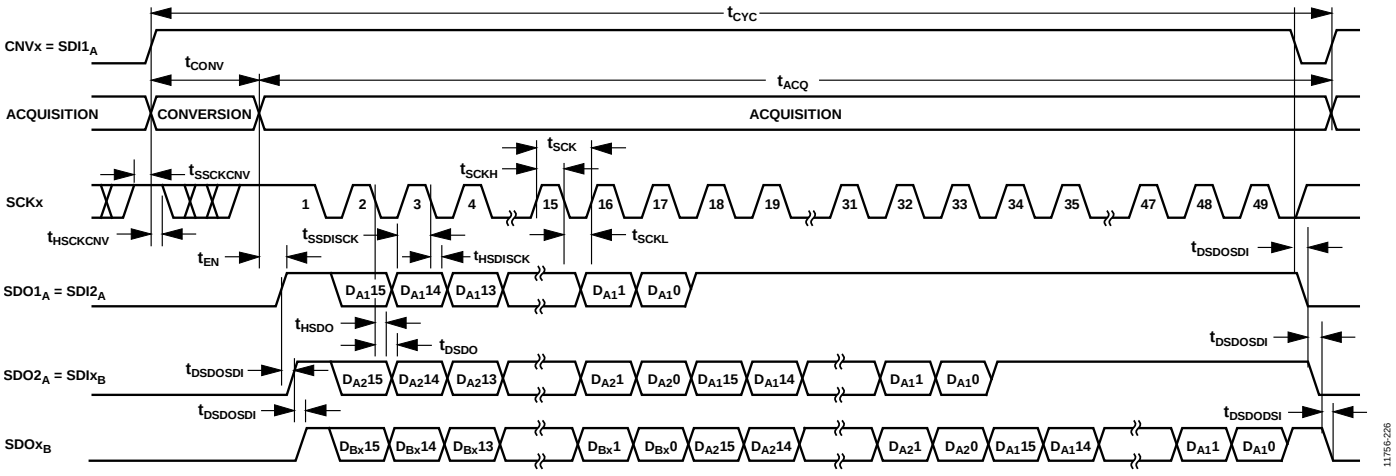
When SDIx and CNVx are low, SDOx is driven low. With SCKx high, a rising edge on CNVx initiates a conversion, selects chain mode, and enables the busy indicator feature. In this mode, CNVx is held high during the conversion phase and the subsequent data readback. When all ADCs in the chain have completed their conversions, the SDOx pin of the ADC closest to the digital host (see the ADC labeled ADCx in the AD7902 B box in Figure 48) is driven high. This transition on SDOx can be used as a busy indicator to trigger the data readback controlled by the digital host. The AD7902 then enters the acquisition phase and powers down. The data bits stored in the internal shift register are clocked out, MSB first, by subsequent SCKx falling edges. For each ADC, SDIx feeds the input of the internal shift register and is clocked by the SCKx falling edge. Each ADC in the chain outputs its data MSB first, and 16 × N + 1 clocks are required to read back the N ADCs. Although the rising edge can be used to capture the data, a digital host using the SCKx falling edge allows a faster reading rate and, consequently, more ADCs in the chain, provided that the digital host has an acceptable hold time.



NOTES
1. DASHED LINE DENOTED ADCs ARE WITHIN A GIVEN PACKAGE.
2. SDI1A AND SDO1A REFER TO THE SDI1 AND SDO1 PINS IN ADC1 IN THE FIRST AD7902 OF THE CHAIN (AD7902 A). SDI2A AND SDO2A REFER TO THE SDI2 AND SDO2 PINS IN ADC2 OF AD7902 A. LIKEWISE, SDIxB AND SDOxB REFER TO THE SDIx AND SDOx PINS IN BOTH ADC1 AND ADC2 OF THE SECOND AD7902 IN THE CHAIN (AD7902 B).

11756-126

Figure 48. Chain Mode with a Busy Indicator Connection Diagram



11756-226

Figure 49. Chain Mode with a Busy Indicator Serial Interface Timing

APPLICATIONS INFORMATION

SIMULTANEOUS SAMPLING

By having two unique user interfaces, the AD7902 provides maximum flexibility with respect to how conversion results are accessed from the device. The AD7902 provides an option for the two user interfaces to share the convert start (CNVx) signal from the digital host, creating a 2-channel, simultaneous sampling device. In applications such as control applications, where latency between the sampling instant and the availability of results in the digital host is critical, it is recommended that the AD7902 be configured as shown in Figure 50. This configuration allows simultaneous data read, in addition to simultaneous sampling. However, this configuration also requires an additional data input pin on the digital host. This scenario allows for the fastest throughput because it requires only 15 or 16 SCKx falling edges (depending on the status of the busy indicator) to acquire data from the ADC.

Alternatively, for applications where simultaneous sampling is required but pins on the digital host are limited, the two user interfaces on the AD7902 can be connected in one of the daisy-chain configurations shown in Figure 46 and Figure 48. This daisy chaining allows the user to implement simultaneous sampling functionality while requiring only one digital host input pin. This scenario requires 31 or 32 SCKx falling edges (depending on the status of the busy indicator) to acquire data from the ADC.

Figure 50 shows an example of a simultaneous sampling system using two data inputs for the digital host. The corresponding timing diagram in Figure 51 shows a $\overline{CS}$ mode, 3-wire simultaneous sampling serial interface without busy indicator. However, any of the 3-wire or 4-wire serial interface timing options can be used.

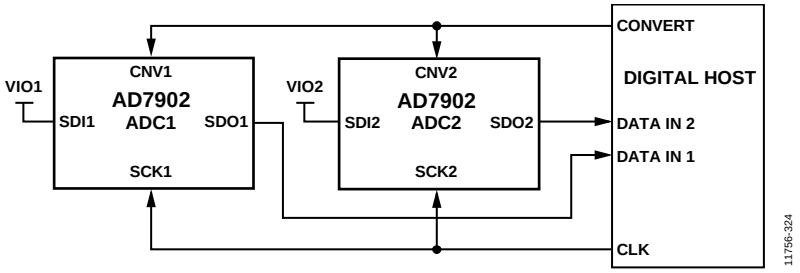


Figure 50. Potential Simultaneous Sampling Connection Diagram

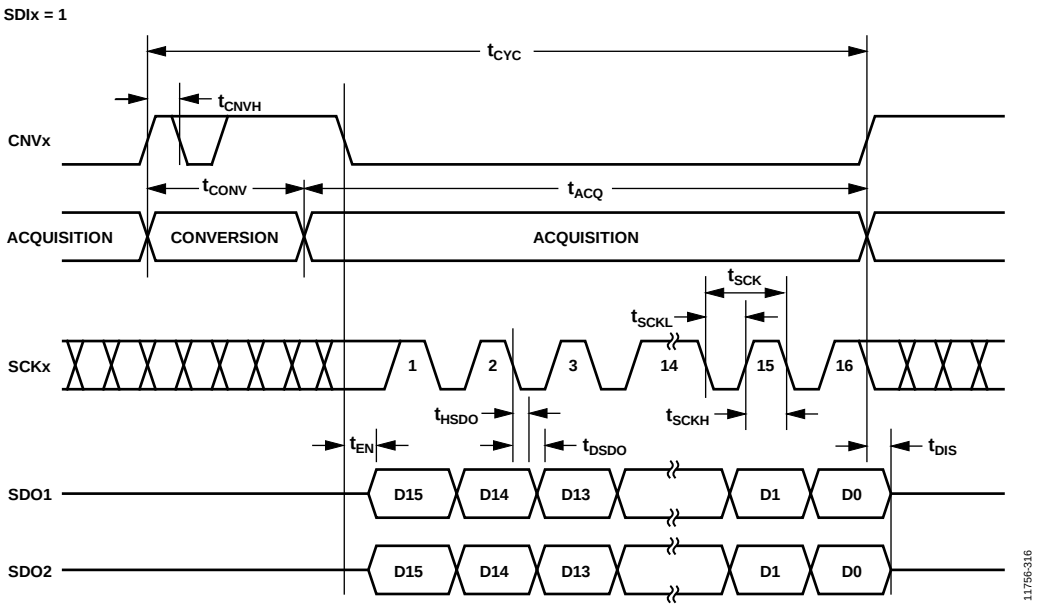


Figure 51. Potential Simultaneous Sampling Serial Interface Timing

FUNCTIONAL SAFTEY CONSIDERATIONS

The AD7902 contains two physically isolated ADCs, making it ideally suited for functional safety applications. Because of this isolation, each ADC features an independent user interface, an independent reference input, an independent analog input, and independent supplies. Physical isolation renders the device suitable for taking verification/backup measurements while separating the verification ADC from the system under control.

Although the Simultaneous Sampling section describes how to operate the device in a simultaneous nature, the circuit is actually composed of two individual signal chains. This separation makes the AD7902 ideal for handling redundant measurement applications. Implementing a signal chain with redundant ADC measurement can contribute to a no single error system. Figure 52 shows a typical functional safety application circuit consisting of a redundant measurement with the employment of monitoring the inverted signal. The inversion is applied to detect common cause failures where it is expected that the circuit output moves in the same direction during a fault condition, instead of moving in the opposite direction as expected.

In addition, the QSOP package that houses the device provides access to the leads for inspection.

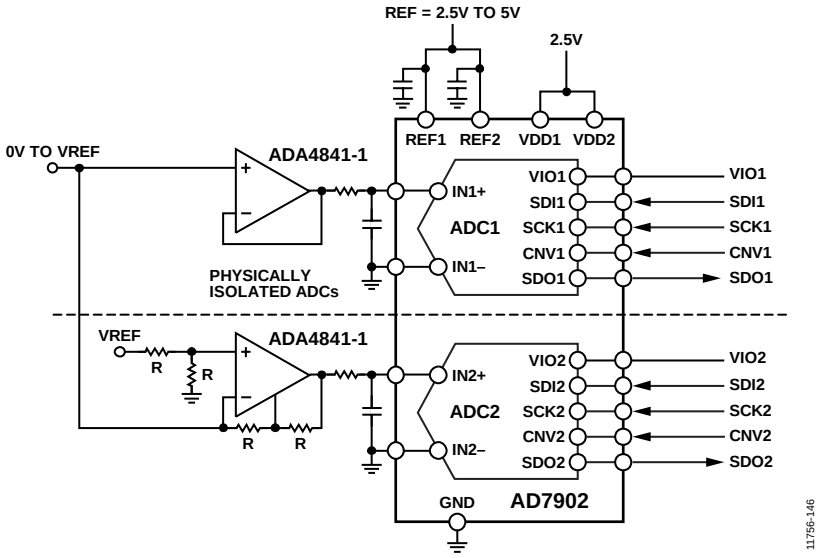


Figure 52. Typical Functional Safety Block Diagram

LAYOUT

Design the printed circuit board (PCB) of the AD7902 such that the analog and digital sections are separated and confined to certain areas of the board. The pinout of the AD7902, with its analog signals on the left side and its digital signals on the right side, eases this task.

Avoid running digital lines under the device because these couple noise onto the die unless a ground plane under the AD7902 is used as a shield. Do not run fast switching signals, such as CNVx or clocks, near analog signal paths. Avoid crossover of digital and analog signals. To avoid signal fidelity issues, take care to ensure monotonicity of digital edges in the PCB layout.

Use at least one ground plane. It can be shared between or split between the digital and analog sections. In the latter case, join the planes underneath the AD7902.

The AD7902 voltage reference inputs, REF1 and REF2, have a dynamic input impedance. Decouple these reference inputs with minimal parasitic inductances by placing the reference decoupling ceramic capacitor in close proximity to (ideally, right up against) the REFx and GND pins and then connecting them with wide, low impedance traces.

Finally, decouple the power supplies, VDDx and VIOx, with ceramic capacitors, typically 100 nF. Place them in close proximity to the AD7902 and connect them using short, wide traces to provide low impedance paths and to reduce the effect of glitches on the power supply lines.

See Figure 53 for an example of layout following these rules.

EVALUATING PERFORMANCE OF THE AD7902

Other recommended layouts for the AD7902 are outlined in the EVAL-AD7902SDZ User Guide. The package for the evaluation board (EVAL-AD7902SDZ) includes a fully assembled and tested evaluation board, user guide, and software for controlling the board from a PC via the EVAL-SDP-CB1Z.

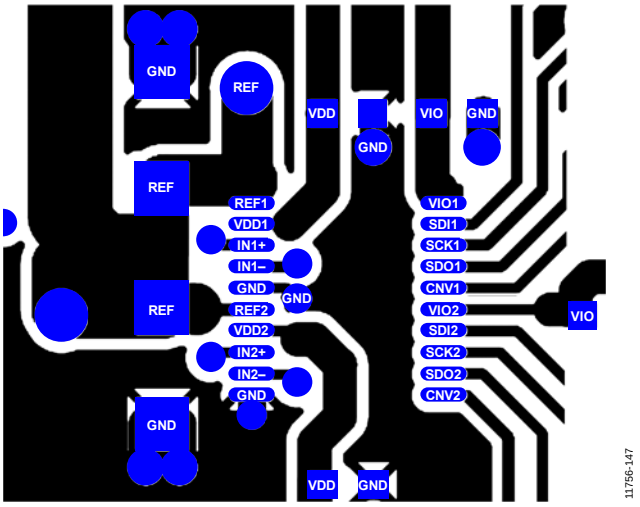
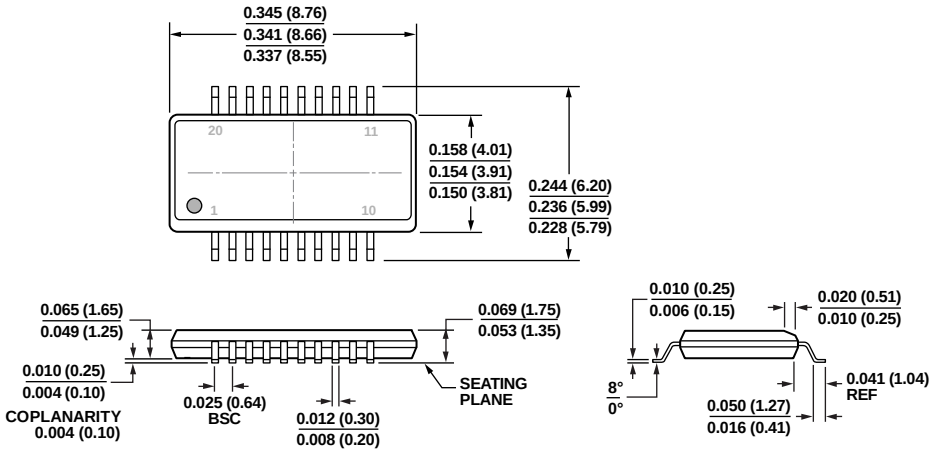


Figure 53. Example Layout of the AD7902 (Top Layer)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-137-AD
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

09-12-2014-A

Figure 54. 20-Lead Shrink Small Outline Package [QSOP]
(RQ-20)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
AD7902BRQZ	−40°C to +125°C	20-Lead Shrink Small Outline Package [QSOP], Tube	RQ-20	56
AD7902BRQZ-RL7	−40°C to +125°C	20-Lead Shrink Small Outline Package [QSOP], Reel	RQ-20	1,000
EVAL-AD7902SDZ		Evaluation Board		
EVAL-SDP-CB1Z		Controller Board		

[1] Z = RoHS Compliant Part.

NOTES

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