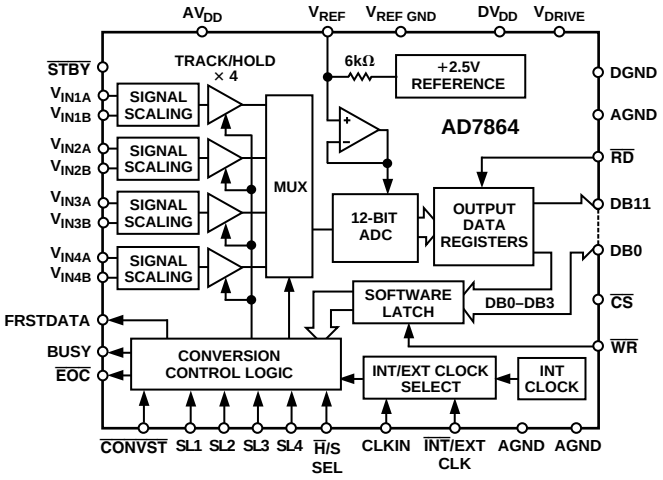
4-Channel, Simultaneous Sampling, High Speed, 12-Bit ADC

AD7864

FEATURES
High Speed (1.65 μs) 12-Bit ADC
Four Simultaneously Sampled Inputs
Four Track/Hold Amplifiers
0.35 μs Track/Hold Acquisition Time
1.65 μs Conversion Time per Channel
HW/SW Select of Channel Sequence for Conversion
Single Supply Operation
Selection of Input Ranges:
±10 V, ±5 V for AD7864-1
±2.5 V for AD7864-3
0 V to 2.5 V, 0 V to 5 V for AD7864-2
High Speed Parallel Interface Which Also Allows Interfacing to 3 V Processors
Low Power, 90 mW Typ
Power Saving Mode, 20 μW Typ
Overvoltage Protection on Analog Inputs

APPLICATIONS
AC Motor Control
Uninterrupted Power Supplies
Data Acquisition Systems
Communications

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7864 is a high speed, low power, 4-channel simultaneous sampling 12-bit A/D converter that operates from a single +5 V supply. The part contains a 1.65 μs successive approximation ADC, four track/hold amplifiers, 2.5 V reference, on-chip clock oscillator, signal conditioning circuitry and a high speed parallel interface. The input signals on four channels are sampled simultaneously, thus preserving the relative phase information of the signals on the four analog inputs. The part accepts analog input ranges of ±10 V, ±5 V (AD7864-1), 0 V to 2.5 V, 0 V to 5 V for AD7864-2 and ±2.5 V (AD7864-3).

The part allows any subset of the four channels to be converted in order to maximize the throughput rate on the selected sequence. The channels to be converted can be selected via either hardware (channel select input pins) or software (programming the channel select register).

A single conversion start signal ($\overline{\text{CONVST}}$) simultaneously places all the track/holds into hold and initiates conversion sequence for the selected channels. The $\overline{\text{EOC}}$ signal indicates the end of each individual conversion in the selected conversion sequence. The BUSY signal indicates the end of the conversion sequence.

Data is read from the part by means of a 12-bit parallel data bus using the standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals. Maximum throughput for a single channel is 500 kSPS. For all four channels the maximum throughput is 130 kSPS for the read during conversion sequence operation. The throughput rate for the read after conversion sequence operation will depend on the read cycle time of the processor. See Timing and Control section.

The AD7864 is available in a small (0.3 sq. inch area) 44-lead MQFP.

PRODUCT HIGHLIGHTS

1. The AD7864 features four Track/Hold amplifiers and a fast (1.65 μs) ADC allowing simultaneous sampling and then conversion of any subset of the four channels.
2. The AD7864 operates from a single +5 V supply and consumes only 90 mW typ making it ideal for low power and portable applications. Also see Standby Mode Operation.
3. The part offers a high speed parallel interface for easy connection to microprocessors, microcontrollers and digital signal processors.
4. The part is offered in three versions with different analog input ranges. The AD7864-1 offers the standard industrial input ranges of ±10 V and ±5 V; the AD7864-3 offers the common signal processing input range of ±2.5 V; the AD7864-2 can be used in unipolar 0 V to 2.5 V, 0 V to 5 V applications.
5. The part features very tight aperture delay matching between the four input sample-and-hold amplifiers.

REV. A

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AD7864–SPECIFICATIONS

(V_{DD} = +5 V ± 5%, AGND = DGND = 0 V, V_{REF} = Internal. Clock = Internal; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Version[1]	B Version	Units	Test Conditions/Comments
SAMPLE AND HOLD				
–3 dB Full Power Bandwidth	3	3	MHz typ	
Aperture Delay	20	20	ns max	
Aperture Jitter	50	50	ps typ	
Aperture Delay Matching	4	4	ns max	
DYNAMIC PERFORMANCE[2]				f_{IN} = 100.0 kHz, f_S = 500 kSPS
Signal to (Noise + Distortion) Ratio[3]				
@ +25°C	70	72	dB min	
T_{MIN} to T_{MAX}	70	70	dB min	
Total Harmonic Distortion[3]	–80	–80	dB max	
Peak Harmonic or Spurious Noise[3]	–80	–80	dB max	
Intermodulation Distortion[3]				fa = 49 kHz, fb = 50 kHz
2nd Order Terms	–80	–80	dB typ	
3rd Order Terms	–80	–80	dB typ	
Channel-to-Channel Isolation[3]	–80	–80	dB max	f_{IN} = 50 kHz Sine Wave
DC ACCURACY				Any Channel
Resolution	12	12	Bits	
Relative Accuracy[3]	±1	±1/2	LSB max	
Differential Nonlinearity[3]	±0.9	±0.9	LSB max	No Missing Codes
AD7864-1				
Positive Gain Error[3]	±3	±3	LSB max	
Positive Gain Error Match[3]	3	±3	LSB max	
Negative Gain Error[3]	±3	±3	LSB max	
Negative Gain Error Match[3]	3	±3	LSB max	
Bipolar Zero Error	±4	±3	LSB max	
Bipolar Zero Error Match	2	±2	LSB max	
AD7864-3				
Positive Gain Error[3]	±3		LSB max	
Positive Gain Error Match[3]	2		LSB max	
Negative Gain Error[3]	±3		LSB max	
Negative Gain Error Match[3]	2		LSB max	
Bipolar Zero Error	±3		LSB max	
Bipolar Zero Error Match	2		LSB max	
AD7864-2				
Positive Gain Error[3]	±3		LSB max	
Positive Gain Error Match[3]	3		LSB max	
Unipolar Offset Error	±3		LSB max	
Unipolar Offset Error Match	2		LSB max	
ANALOG INPUTS				
AD7864-1				
Input Voltage Range	±5, ±10	±5, ±10	Volts	
Input Resistance	9, 18	9, 18	kΩ min	
AD7864-3				
Input Voltage Range	±2.5	±2.5	Volts	
Input Resistance	4.5	4.5	kΩ min	
AD7864-2				
Input Voltage Range	+2.5, +5	+2.5, +5	Volts	
Input Current (0 V–2.5 V Option)	±100	±100	nA max	
Input Resistance (0 V–5 V Option)	9	9	kΩ min	
REFERENCE INPUT/OUTPUT				
V_{REF} IN Input Voltage Range	2.375/2.625	2.375/2.625	V_{MIN}/V_{MAX}	2.5 V ± 5%
V_{REF} IN Input Capacitance[4]	10	10	pF max	
V_{REF} OUT Output Voltage	2.5	2.5	V nom	
V_{REF} OUT Error @ +25°C	±10	±10	mV max	
V_{REF} OUT Error T_{MIN} to T_{MAX}	±20	±20	mV max	
V_{REF} OUT Temperature Coefficient	25	25	ppm/°C typ	
V_{REF} OUT Output Impedance	6	6	kΩ typ	See Reference Section

Parameter	A Version[1]	B Version	Units	Test Conditions/Comments
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	μA max	
Input Capacitance, C_{IN}[4]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	4.0	4.0	V min	I_{SOURCE} = 400 μA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0				
High Impedance				
Leakage Current	±10	±10	μA max	
Capacitance[4]	10	10	pF max	
Output Coding				
AD7864-1, AD7864-3	Twos Complement			
AD7864-2	Straight (Natural) Binary			
CONVERSION RATE				
Conversion Time	1.65	1.65	μs max	For One Channel
Track/Hold Acquisition Time[2, 3]	0.35	0.35	μs max	
Throughput Time	130	130	kSPS max	For All Four Channels
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
I_{DD}				(5 μA typ) Logic Inputs = 0 V or V_{DD}
Normal Mode	24	24	mA max	
Standby Mode	20	20	μA max	Typically 4 μA
Power Dissipation				
Normal Mode	120	120	mW max	Typically 90 mW
Standby Mode	100	100	μW max	Typically 20 μW

NOTES

[1]Temperature ranges are as follows: A, B Versions: –40°C to +85°C. Note: The A Version is fully specified up to +105°C with degraded INL and DNL specifications of ±2 LSBs max.

[2]Performance measured through full channel (SHA and ADC).

[3]See Terminology.

[4]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_D = +5 V ± 5%, AGND = DGND = 0 V, V_{REF} = Internal, Clock = Internal; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A, B Versions	Units	Test Conditions/Comments
t_{CONV}	1.65	µs max	Conversion Time, Internal Clock
	13	Clock Cycles	Conversion Time, External Clock
	2.6	µs max	CLKIN = 5 MHz
t_{ACQ}	0.34	µs max	Acquisition Time
t_{BUSY}	No. of Channels		Selected Number of Channels Multiplied by
	x (t_{CONV} + t_9) – t_9	µs max	(t_{CONV} + $\overline{EOC}$ Pulsewidth)—$\overline{EOC}$ Pulsewidth
$t_{WAKE-UP}$—External V_{REF}	2	µs max	$\overline{STBY}$ Rising Edge to $\overline{CONVST}$ Rising Edge
$t_{WAKE-UP}$—Internal V_{REF}[3]	6	ms max	$\overline{STBY}$ Rising Edge to $\overline{CONVST}$ Rising Edge
t_1	35	ns min	$\overline{CONVST}$ Pulsewidth
t_2	70	ns min	$\overline{CONVST}$ Rising Edge to BUSY Rising Edge
Read Operation			
t_3	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_4	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_5	35	ns min	Read Pulsewidth
t_6[4]	35	ns max	Data Access Time After Falling Edge of $\overline{RD}$, V_{DRIVE} = 5 V
	40	ns max	Data Access Time After Falling Edge of $\overline{RD}$, V_{DRIVE} = 3 V
t_7[5]	5	ns min	Bus Relinquish Time After Rising Edge of $\overline{RD}$
	30	ns max	
t_8	10	ns min	Time Between Consecutive Reads
t_9	75	ns min	$\overline{EOC}$ Pulsewidth
	180	ns max	
t_{10}	70	ns max	$\overline{RD}$ Rising Edge to FRSTDATA Edge (Rising or Falling)
t_{11}	15	ns max	$\overline{EOC}$ Falling Edge to FRSTDATA Falling Delay
t_{12}	0	ns min	$\overline{EOC}$ to $\overline{RD}$ Delay
Write Operation			
t_{13}	20	ns min	$\overline{WR}$ Pulsewidth
t_{14}	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_{15}	0	ns min	$\overline{WR}$ to $\overline{CS}$ Hold Time
t_{16}	5	ns min	Input Data Setup Time of Rising Edge of $\overline{WR}$
t_{17}	5	ns min	Input Data Hold Time

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are measured with tr = tf = 1 ns (10% to 90% of +5 V) and timed from a voltage level of +1.6 V.

[2]See Figures 7, 8 and 9.

[3]Refer to the Standby Mode Operation section. The MAX specification of 6 ms is valid when using a 0.1 µF decoupling capacitor on the V_{REF} pin.

[4]Measured with the load circuit of Figure 2 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[5]These times are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

Specifications subject to change without notice.

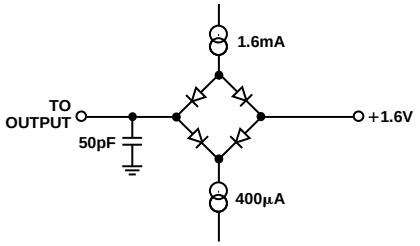


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND . . . . . –0.3 V to +7 V
V_{DD} to DGND . . . . . –0.3 V to +7 V
Analog Input Voltage to AGND
  AD7864-1 (±10 V Input Range) . . . . . ±20 V
  AD7864-1 (±5 V Input Range) . . . . . –7 V to +20 V
  AD7864-3 . . . . . –7 V to +20 V
  AD7864-2 . . . . . –1 V to +20 V
Reference Input Voltage to AGND . . . –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
  Commercial (A, B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . +150°C
MQFP Package, Power Dissipation . . . . . 450 mW
  θ_{JA} Thermal Impedance . . . . . 95°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . . +215°C
    Infrared (15 sec) . . . . . +220°C

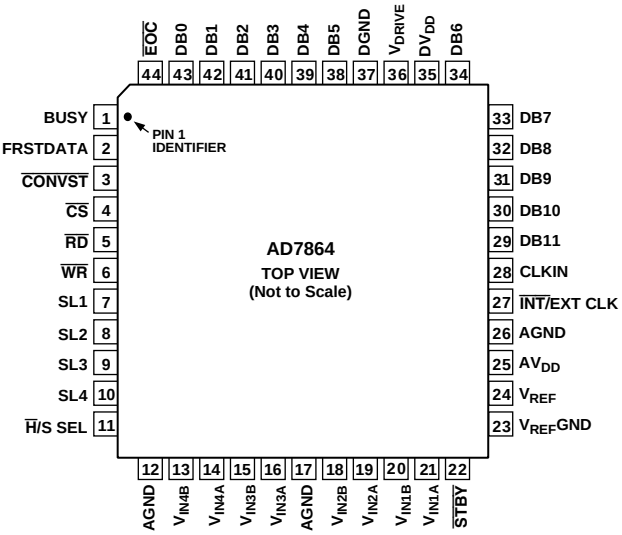
*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Input Ranges	Relative Accuracy	Temperature Range*	Package Description	Package Option
AD7864AS-1	±5 V, ±10 V	±1 LSB	–40°C to +85°C	Plastic Lead Quad Flatpack	S-44
AD7864BS-1	±5 V, ±10 V	±0.5 LSB	–40°C to +85°C	Plastic Lead Quad Flatpack	S-44
AD7864AS-3	±2.5 V	±1 LSB	–40°C to +85°C	Plastic Lead Quad Flatpack	S-44
AD7864AS-2	0 V to 2.5 V, 0 V to 5 V	±1 LSB	–40°C to +85°C	Plastic Lead Quad Flatpack	S-44

*The A Version is fully specified up to +105°C with degraded INL and DNL specifications of ±2 LSBs max.

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7864 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	BUSY	Busy Output. The busy output is triggered high by the rising edge of $\overline{\text{CONVST}}$ and remains high until conversion is completed on all selected channels.
2	FRSTDATA	First Data Output. FRSTDATA is a logic output which, when high, indicates that the Output Data Register Pointer is addressing Register 1—See Accessing the Output Data Registers.
3	$\overline{\text{CONVST}}$	Convert Start Input. Logic Input. A low-to-high transition on this input puts all track/holds into their hold mode and starts conversion on the selected channels. In addition, the state of the Channel Sequence Selection is also latched on the rising edge of $\overline{\text{CONVST}}$.
4	$\overline{\text{CS}}$	Chip Select Input. Active Low Logic Input. The device is selected when this input is active.
5	$\overline{\text{RD}}$	Read Input. Active Low Logic Input that is used in conjunction with $\overline{\text{CS}}$ low to enable the data outputs. Ensure the $\overline{\text{WR}}$ pin is at logic high while performing a read operation.
6	$\overline{\text{WR}}$	Write Input. A rising edge on the $\overline{\text{WR}}$ input, with $\overline{\text{CS}}$ low and $\overline{\text{RD}}$ high, latches the logic state on DB0 to DB3 into the channel select register.
7–10	SL1–SL4	Hardware Channel Select. Conversion sequence selection can also be made via the SL1–SL4 pins if $\overline{\text{H}}$/S SEL is logic zero. The selection is latched on the rising edge of $\overline{\text{CONVST}}$. See Selecting a Conversion Sequence.
11	$\overline{\text{H}}$/S SEL	Hardware/Software Select Input. When this pin is at a Logic 0, the AD7864 conversion sequence selection is controlled via the SL1–SL4 input pins. When this pin is at Logic 1, the sequence is controlled via the channel select register. See Selecting a Conversion Sequence.
12	AGND	Analog Ground. General Analog Ground. This AGND pin should be connected to the system's AGND plane.
13–16	V_{IN4X}, V_{IN3X}	Analog Inputs. See Analog Input section.
17	AGND	Analog Ground. Analog Ground reference for the attenuator circuitry. This AGND pin should be connected to the system's AGND plane.
18–21	V_{IN2X}, V_{IN1X}	Analog Inputs. See Analog Input section.
22	$\overline{\text{STBY}}$	Standby Mode Input. TTL-compatible input that is used to put the device into the power save or standby mode. The $\overline{\text{STBY}}$ input is high for normal operation and low for standby operation.
23	V_{REF} GND	Reference Ground. Ground reference for the part's on-chip reference buffer. The V_{REF} GND pin should be connected to the system's AGND plane.
24	V_{REF}	Reference Input/Output. This pin provides access to the internal reference (2.5 V ± 5%) and also allows the internal reference to be overdriven by an external reference source (2.5 V). A 0.1 μF decoupling capacitor should be connected between this pin and AGND.
25	AV_{DD}	Analog Positive Supply Voltage, +5.0 V ± 5%.
26	AGND	Analog Ground. Analog Ground reference for the DAC circuitry.
27	$\overline{\text{INT}}$/EXT CLK	Internal/External Clock Select Input. When this pin is at a Logic 0, the AD7864 uses its internally generated master clock. When this pin is at Logic 1, the master clock is generated externally to the device.
28	CLKIN	Conversion Clock Input. This is an externally applied clock that allows the user to control the conversion rate of the AD7864. Each conversion needs fourteen clock cycles in order for the conversion to be completed and an $\overline{\text{EOC}}$ pulse to be generated. The clock should have a duty cycle that is no worse than 60/40. See Using an External Clock.
29–34	DB11–DB6	Data Bit 11 is the MSB, followed by Data Bit 10 to Data Bit 6. Three-state TTL outputs. Output coding is 2s complement for the AD7864-1 and AD7864-3. Output coding is straight (natural) binary for the AD7864-2.
35	DV_{DD}	Positive supply voltage for digital section, +5.0 V ± 5%. A 0.1 μF decoupling capacitor should be connected between this pin and AGND. Both DV_{DD} and AV_{DD} should be externally tied together.
36	V_{DRIVE}	This pin provides the positive supply voltage for the output drivers (DB0 to DB11), BUSY, $\overline{\text{EOC}}$ and FRSTDATA. It is normally tied to DV_{DD}. V_{DRIVE} should be decoupled with a 0.1 μF capacitor. It allows improved performance when reading during the conversion sequence. To facilitate interfacing to 3 V processors and DSPs the output data drivers may also be powered by a 3 V ± 10% supply .
37	DGND	Digital Ground. Ground reference for digital circuitry. This DGND pin should be connected to the system's AGND plane at the AGND pin.
38, 39	DB5, DB4	Data Bit 5 to Data Bit 4. Three-state TTL Outputs.
40–43	DB3–DB0	Data Bit 3 to Data Bit 0. Bidirectional Data Pins. When a read operation takes place, these pins are three-state TTL outputs. The channel select register is programmed with the data on the DB0–DB3 pins with standard $\overline{\text{CS}}$ and $\overline{\text{WR}}$ signals. DB0 represents Channel 1 and DB3 which represents Channel 4.
44	$\overline{\text{EOC}}$	End-of-Conversion. Active low logic output indicating conversion status. The end of each conversion in a conversion sequence is indicated by a low-going pulse on this line.

TERMINOLOGY

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\textit{Signal to (Noise + Distortion)} = (6.02\ N + 1.76)\ dB$$

Thus for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7864 it is defined as:

$$THD\ (dB) = 20\ log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4 and V_5 are the rms amplitudes of the second through the fifth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2 fa + fb), (2 fa – fb), (fa + 2 fb) and (fa – 2 fb).

The AD7864 is tested using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used. In this case, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

Channel-to-Channel Isolation
Channel-to-Channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale 50 kHz sine wave signal to all nonselected input channels and determining how much that signal is attenuated in the selected channel. The figure given is the worst case across all four channels.

Relative Accuracy
Relative accuracy or endpoint nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Positive Full-Scale Error
This is the deviation of the last code transition (01 . . . 110 to 01 . . . 111) from the ideal 4 × VREF – 3/2 LSB (AD7864-1 ±10 V), 2 × VREF – 3/2 LSB (AD7864-1 ±5 V range) or VREF – 3/2 LSB (AD7864-3, ±2.5 V range), after the Bipolar Offset Error has been adjusted out.

Positive Full-Scale Error (AD7864-2, 0 V to 2.5 V and 0 V to 5 V)
This is the deviation of the last code transition (11 . . . 110 to 11 . . . 111) from the ideal 2 × VREF – 3/2 LSB (AD7864-2 0 V to 5 V range), or VREF – 3/2 LSB (AD7864-2 0 V to 2.5 V range), after the Unipolar Offset Error has been adjusted out.

Bipolar Zero Error (AD7864-1, ±10/±5 V, AD7864-3 , ±2.5 V)
This is the deviation of the midscale transition (all 0s to all 1s) from the ideal AGND – 1/2 LSB.

Unipolar Offset Error (AD7864-2, 0 V to 2.5 V and 0 V to 5 V)
This is the deviation of the first code transition (00 . . . 000 to 00 . . . 001) from the ideal AGND + 1/2 LSB.

Negative Full-Scale Error (AD7864-1, ±10/±5 V, AD7864-3, ±2.5 V)
This is the deviation of the first code transition (10 . . . 000 to 10 . . . 001) from the ideal –4 × VREF + 1/2 LSB (AD7864-1 ±10 V), –2 × VREF + 1/2 LSB (AD7864-1 ±5 V range) or –VREF + 1/2 LSB (AD7864-3, ±2.5 V range), after Bipolar Zero Error has been adjusted out.

Track/Hold Acquisition Time
Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion (the point at which the track/hold returns to track mode). It also applies to situations where there is a step input change on the input voltage applied to the selected V_{INXA}/V_{INXB} input of the AD7864. It means that the user must wait for the duration of the track/hold acquisition time after the end of conversion or after a step input change to V_{INXA}/V_{INXB} before starting another conversion, to ensure that the part operates to specification.

CONVERTER DETAILS

The AD7864 is a high speed, low power, 4-channel simultaneous sampling 12-bit A/D converter that operates from a single +5 V supply. The part contains a 1.65 μs successive approximation ADC, four track/hold amplifiers, an internal +2.5 V reference and a high speed parallel interface. There are four analog inputs that can be simultaneously sampled thus preserving the relative phase information of the signals on all four analog inputs. Thereafter, conversions will be completed on the selected subset of the four channels. The part accepts an analog input range of ±10 V or ±5 V (AD7864-1), ±2.5 V (AD7864-3) and 0 V–2.5 V or 0 V–5 V (AD7864-2). Overvoltage protection on the analog inputs of the part allows the input voltage to go to ±20 V, (AD7864-1 ±10 V range), –7 V or +20 V (AD7864-1 ±5 V range) –1 V to +20 V (AD7864-2) and –7 V to +20 V (AD7864-3) without causing damage or effecting a conversion in progress. The AD7864 has two operating modes Reading Between Conversions and Reading after the Conversion Sequence. These modes are discussed in more detail in the Timing and Control section.

A conversion is initiated on the AD7864 by pulsing the $\overline{\text{CONVST}}$ input. On the rising edge of $\overline{\text{CONVST}}$, all four on-chip track/holds are placed into hold simultaneously and the conversion sequence is started on all the selected channels. Channel selection is made via the SL1–SL4 pins if $\overline{\text{H}}$/S SEL is logic zero or via the channel select register if $\overline{\text{H}}$/S SEL is logic one—see Selecting a Conversion Sequence. The channel select register is programmed via the bidirectional data lines DB0–DB3 and a standard write operation. The selected conversion sequence is latched on the rising edge of $\overline{\text{CONVST}}$ so changing a selection will only take effect once a new conversion sequence is initiated. The BUSY output signal is triggered high on the rising edge of $\overline{\text{CONVST}}$ and will remain high for the duration of the conversion sequence. The conversion clock for the part is generated internally using a laser-trimmed clock oscillator circuit. There is also the option of using an external clock, by tying the $\overline{\text{INT}}$/EXT CLK pin logic high, and applying an external clock to the CLKIN pin. However, the optimum throughput is obtained by using the internally generated clock—see Using an External Clock. The $\overline{\text{EOC}}$ signal indicates the end of each conversion in the conversion sequence. The BUSY signal indicates the end of the full conversion sequence and at this time all four Track and Holds return to tracking mode. The conversion results can either be read at the end of the full conversion sequence (indicated by BUSY going low) or as each result becomes available (indicated by $\overline{\text{EOC}}$ going low). Data is read from the part via a 12-bit parallel data bus with standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals—see Timing and Control.

Conversion time for each channel of the AD7864 is 1.65 μs and the track/hold acquisition time is 0.35 μs. To obtain optimum performance from the part, the read operation should not occur during a channel conversion or during the 100 ns prior to the next $\overline{\text{CONVST}}$ rising edge. This allows the part to operate at throughput rates up to 130 kHz for all four channels and achieve data sheet specifications.

Track/Hold Section

The track/hold amplifiers on the AD7864 allows the ADCs to accurately convert an input sine wave of full-scale amplitude to 12-bit accuracy. The input bandwidth of the track/hold is greater than the Nyquist rate of the ADC even when the ADC is operated at its maximum throughput rate of 500 kSPS (i.e., the track/hold can handle input frequencies in excess of 250 kHz).

The track/hold amplifiers acquire input signals to 12-bit accuracy in less than 350 ns. The operation of the track/holds are essentially transparent to the user. The four track/hold amplifiers sample their respective input channels simultaneously, on the rising edge of $\overline{\text{CONVST}}$. The aperture time for the track/holds (i.e., the delay time between the external $\overline{\text{CONVST}}$ signal and the track/hold actually going into hold) is typically 15 ns and, more importantly, is well matched across the four track/holds on one device and also well matched from device to device. This allows the relative phase information between different input channels to be accurately preserved. It also allows multiple AD7864s to sample more than four channels simultaneously. At the end of a conversion sequence, the part returns to its tracking mode. The acquisition time of the track/hold amplifiers begin at this point.

Reference Section

The AD7864 contains a single reference pin, labelled V_{REF}, which either provides access to the part's own +2.5 V reference or to which an external +2.5 V reference can be connected to provide the reference source for the part. The part is specified with a +2.5 V reference voltage. Errors in the reference source will result in gain errors in the AD7864's transfer function and will add to the specified full-scale errors on the part. On the AD7864-1 and AD7864-3, it will also result in an offset error injected in the attenuator stage, see Figures 2 and 4.

The AD7864 contains an on-chip +2.5 V reference. To use this reference as the reference source for the AD7864, simply connect a 0.1 μF disc ceramic capacitor from the V_{REF} pin to AGND. The voltage that appears at this pin is internally buffered before being applied to the ADC. If this reference is used externally to the AD7864, it should be buffered, as the part has a FET switch in series with the reference output resulting in a source impedance for this output of 6 kΩ nominal. The tolerance on the internal reference is ±10 mV at 25°C with a typical temperature coefficient of 25 ppm/°C and a maximum error over temperature of ±20 mV.

If the application requires a reference with a tighter tolerance or the AD7864 needs to be used with a system reference, the user has the option of connecting an external reference to this V_{REF} pin. The external reference will effectively overdrive the internal reference and thus provide the reference source for the ADC. The reference input is buffered before being applied to the ADC with the maximum input current of ±100 μA. Suitable reference sources for the AD7864 include the AD680, AD780, REF192 and REF43 precision +2.5 V references.

CIRCUIT DESCRIPTION

Analog Input Section

The AD7864 is offered as three part types: the AD7864-1, where each input can be configured for ±10 V or a ±5 V input voltage range; the AD7864-3 which handles input voltage range ±2.5 V; the AD7864-2, where each input can be configured to have a 0 V to +2.5 V or 0 V to +5 V input voltage range.

AD7864-1

Figure 2 shows the analog input section of the AD7864-1. Each input can be configured for ±5 V or ±10 V operation on the AD7864-1. For ±5 V (AD7864-1) operation, the V_{INXA} and V_{INXB} inputs are tied together and the input voltage is applied to both. For ±10 V (AD7864-1) operation, the V_{INXB} input is tied to AGND and the input voltage is applied to the V_{INXA} input. The V_{INXA} and V_{INXB} inputs are symmetrical and fully interchangeable. Thus for ease of PCB layout on the ±10 V range, the input voltage may be applied to the V_{INXB} input while the V_{INXA} input is tied to AGND.

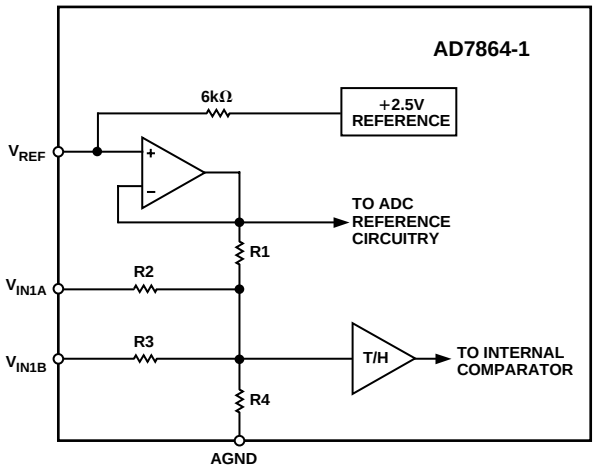


Figure 2. AD7864-1 Analog Input Structure

For the AD7864-1, R1 = 6 kΩ, R2 = 24 kΩ, R3 = 24 kΩ and R4 = 12 kΩ. The resistor input stage is followed by the high input impedance stage of the track/hold amplifier.

The designed code transitions take place midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs etc.) LSB size is given by the formula, 1 LSB = FSR/4096. For the ±5 V range, 1 LSB = 10 V/4096 = 2.44 mV. For the ±10 V range, 1 LSB = 20 V/4096 = 4.88 mV. Output coding is twos complement binary with 1 LSB = FSR/4096. The ideal input/output transfer function for the AD7864-1 is shown in Table I.

Table I. Ideal Input/Output Code Table for the AD7864-1

Analog Input[1]	Digital Output Code Transition
+FSR/2 – 3/2 LSB[2]	011 . . . 110 to 011 . . . 111
+FSR/2 – 5/2 LSB	011 . . . 101 to 011 . . . 110
+FSR/2 – 7/2 LSB	011 . . . 100 to 011 . . . 101
AGND + 3/2 LSB	000 . . . 001 to 000 . . . 010
AGND + 1/2 LSB	000 . . . 000 to 000 . . . 001
AGND – 1/2 LSB	111 . . . 111 to 000 . . . 000
AGND – 3/2 LSB	111 . . . 110 to 111 . . . 111
–FSR/2 + 5/2 LSB	100 . . . 010 to 100 . . . 011
–FSR/2 + 3/2 LSB	100 . . . 001 to 100 . . . 010
–FSR/2 + 1/2 LSB	100 . . . 000 to 100 . . . 001

NOTES
[1]FSR is full-scale range and is 20 V for the ±10 V range and 10 V for the ±5 V range, with V_{REF} = +2.5 V.
[2]1 LSB = FSR/4096 = 4.883 mV (±10 V—AD7864-1) and 2.441 mV (±5 V—AD7864-1) with V_{REF} = +2.5 V.

AD7864-2

Figure 3 shows the analog input section of the AD7864-2. Each input can be configured for 0 V to +5 V operation or 0 V to +2.5 V operation. For 0 V to +5 V operation, the V_{INXB} input is tied to AGND and the input voltage is applied to the V_{INXA} input. For 0 V to 2.5 V operation, the V_{INXA} and V_{INXB} inputs are tied together and the input voltage is applied to both. The V_{INXA} and V_{INXB} inputs are symmetrical and fully interchangeable. Thus for ease of PCB layout on the 0 V to +5 V range, the input voltage may be applied to the V_{INXB} input while the V_{INXA} input is tied to AGND.

For the AD7864-2, R1 = 6 kΩ and R2 = 6 kΩ. Once again, the designed code transitions occur on successive integer LSB values. Output coding is straight (natural) binary with 1 LSB = FSR/4096 = 2.5 V/4096 = 0.61 mV, and 5 V/4096 = 1.22 mV, for the 0 V to 2.5 V and the 0 V to 5 V options respectively. Table II shows the ideal input and output transfer function for the AD7864-2.

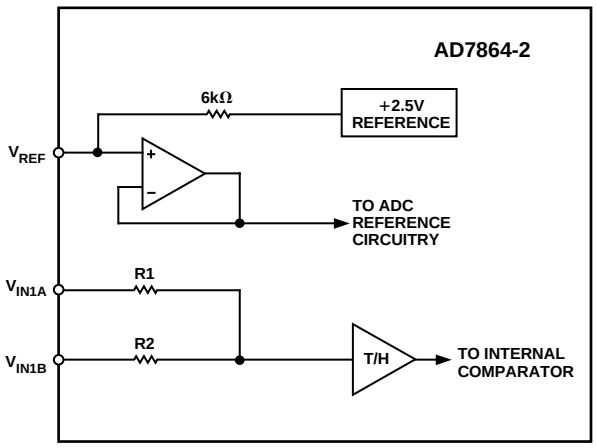


Figure 3. AD7864-2 Analog Input Structure

Table II. Ideal Input/Output Code Table for the AD7864-2

Analog Input[1]	Digital Output Code Transition
+FSR – 3/2 LSB[2]	111 . . . 110 to 111 . . . 111
+FSR – 5/2 LSB	111 . . . 101 to 111 . . . 110
+FSR – 7/2 LSB	111 . . . 100 to 111 . . . 101
AGND + 5/2 LSB	000 . . . 010 to 000 . . . 011
AGND + 3/2 LSB	000 . . . 001 to 000 . . . 010
AGND + 1/2 LSB	000 . . . 000 to 000 . . . 001

NOTES
[1]FSR is full-scale range and is 0 V to 2.5 V and 0 V to 5 V for AD7864-2 with V_{REF} = +2.5 V.
[2]1 LSB = FSR/4096 and is 0.61 mV (0 V to 2.5 V) and 1.22 mV (0 V to 5 V) for AD7864-2 with V_{REF} = +2.5 V.

AD7864-3

Figure 4 shows the analog input section of the AD7864-3. The analog input range is ±2.5 V on the V_{IN1A} input. The V_{IN1B} input can be left unconnected but if it is connected to a potential then that potential must be AGND.

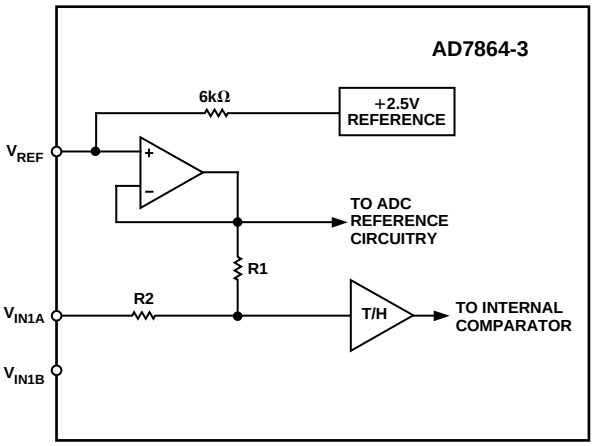


Figure 4. AD7864-3 Analog Input Structure

For the AD7864-3, R1 = 6 kΩ and R2 = 6 kΩ. As a result, the V_{IN1A} input should be driven from a low impedance source. The resistor input stage is followed by the high input impedance stage of the track/hold amplifier.

The designed code transitions take place midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs, etc.) LSB size is given by the formula, 1 LSB = FSR/4096. Output coding is 2s complement binary with 1 LSB = FSR/4096 = 5 V/4096 = 1.22 mV. The ideal input/output transfer function for the AD7864-3 is shown in Table III.

Table III. Ideal Input/Output Code Table for the AD7864-3

Analog Input[1]	Digital Output Code Transition
+FSR/2 – 3/2 LSB[2]	011 . . . 110 to 011 . . . 111
+FSR/2 – 5/2 LSB	011 . . . 101 to 011 . . . 110
+FSR/2 – 7/2 LSB	011 . . . 100 to 011 . . . 101
AGND + 3/2 LSB	000 . . . 001 to 000 . . . 010
AGND + 1/2 LSB	000 . . . 000 to 000 . . . 001
AGND – 1/2 LSB	111 . . . 111 to 000 . . . 000
AGND – 3/2 LSB	111 . . . 110 to 111 . . . 111
–FSR/2 + 5/2 LSB	100 . . . 010 to 100 . . . 011
–FSR/2 + 3/2 LSB	100 . . . 001 to 100 . . . 010
–FSR/2 + 1/2 LSB	100 . . . 000 to 100 . . . 001

NOTES
[1]FSR is full-scale range is 5 V, with V_{REF} = +2.5 V.
[2]1 LSB = FSR/4096 = 1.22 mV (±2.5 V - AD7864-3) with V_{REF} = +2.5 V.

SELECTING A CONVERSION SEQUENCE

Any subset of the four channels VIN1 to VIN4 can be selected for conversion. The selected channels are converted in an ascending order. For example if the channel selection includes VIN4, VIN1 and VIN3 then the conversion sequence will be VIN1, VIN3 and then VIN4. The conversion sequence selection my be made by using either the hardware channel select input pins (SL1 through SL4) or programming the channel select register. A logic high on a hardware channel select pin (or logic one in the channel select register) when $\overline{\text{CONVST}}$ goes logic high, marks the associated analog input channel for inclusion in the conversion sequence.

Figure 5 shows the arrangement used. The $\overline{\text{H}}$/S SEL controls a multiplexer which selects the source of the conversion sequence information, i.e., from the Hardware channel select pins (SL1 to SL4) or from the channel selection register. When a conversion is started the output from the multiplexer is latched until the end of the conversion sequence. The data bus Bits DB0 to DB3 (DB0 representing Channel 1 through DB3 representing Channel 4) are bidirectional and become inputs to the channel select register when $\overline{\text{RD}}$ is logic high and $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are logic low. The logic state on DB0 to DB3 is latched into the channel select register when $\overline{\text{WR}}$ goes logic high.

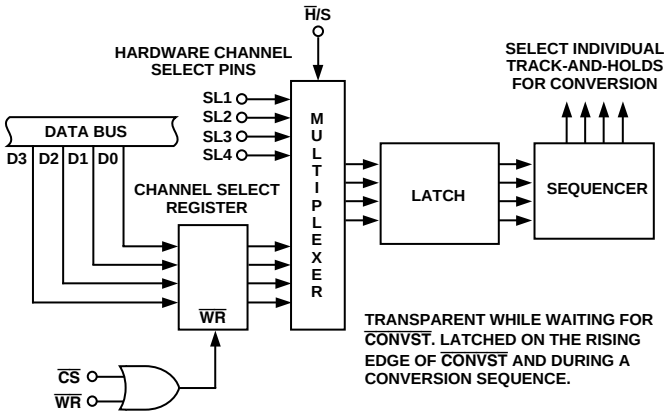


Figure 5. Channel Select Inputs and Registers

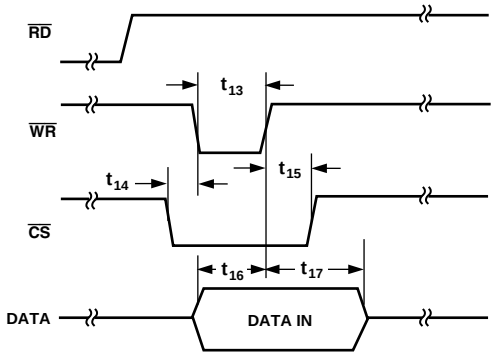


Figure 6. Channel Selection via Software Control

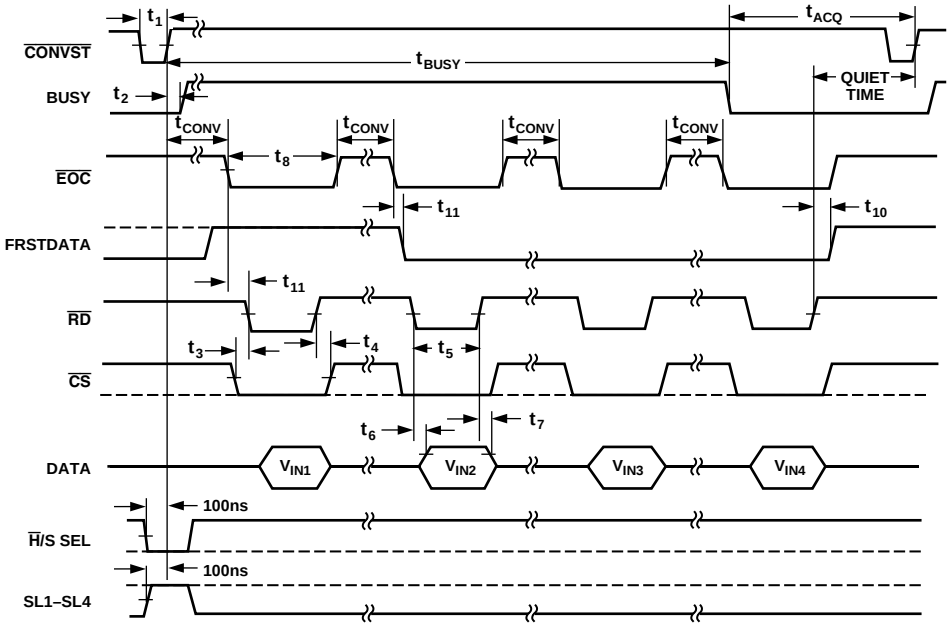


Figure 7. Timing Diagram for Reading During Conversion

TIMING AND CONTROL

Reading Between Each Conversion in the Conversion Sequence

Figure 7 shows the timing and control sequence required to obtain the optimum throughput rate from the AD7864. To obtain the optimum throughput from the AD7864 the user must read the result of each conversion as it becomes available. The timing diagram in Figure 7 shows a read operation each time the $\overline{EOC}$ signal goes logic low. The timing in Figure 7 shows a conversion on all four analog channels (SL1 to SL4 = 1, see Channel Selection), hence there are four $\overline{EOC}$ pulses and four read operations to access the result of each of the four conversions.

A conversion is initiated on the rising edge of $\overline{CONVST}$. This places all four track/holds into hold simultaneously. New data from this conversion sequence is available for the first channel selected (V_{IN1}) 1.65 μs later. The conversion on each subsequent channel is completed at 1.65 μs intervals. The end of each conversion is indicated by the falling edge of the $\overline{EOC}$ signal. The BUSY output signal indicates the end of conversion for all selected channels (four in this case).

Data is read from the part via a 12-bit parallel data bus with standard $\overline{CS}$ and $\overline{RD}$ signals. The $\overline{CS}$ and $\overline{RD}$ inputs are internally gated to enable the conversion result onto the data bus. The data lines DB0 to DB11 leave their high impedance state when both $\overline{CS}$ and $\overline{RD}$ are logic low. Therefore, $\overline{CS}$ may be permanently tied logic low and the $\overline{RD}$ signal used to access the conversion result. Since each conversion result is latched into its output data register prior to $\overline{EOC}$ going logic low a further option would be to tie the $\overline{EOC}$ and $\overline{RD}$ pins together and use the rising edge of $\overline{EOC}$ to latch the conversion result. Although the AD7864 has some special features that permit reading during a conversion (e.g., a separate supply for the output data drivers, V_{DRIVE}), for optimum performance it is recommended that the read operation be completed when $\overline{EOC}$ is logic low, i.e., before the start of the next conversion. Although Figure 8 shows the read operation taking place during the $\overline{EOC}$ pulse, a read operation can take place at any time. Figure 8 shows a timing specification called "Quiet Time." This is the amount of time that should be left after a read operation and before the next conversion is initiated. The quiet time depends heavily on data bus capacitance but a figure of 50 ns to 100 ns is typical.

The signal labeled FRSTDATA (First Data Word) indicates to the user that the pointer associated with the output data registers is pointing to the first conversion result by going logic high. The pointer is reset to point to the first data location (i.e., first conversion result,) at the end of the first conversion (FRSTDATA logic high). The pointer is incremented to point to the next register (next conversion result) when that conversion result is available. Hence, FRSTDATA in Figure 7 is seen to go low just prior to the second $\overline{EOC}$ pulse. Repeated read operations during a conversion will continue to access the data at the current pointer location until the pointer is incremented at the end of that conversion. Note FRSTDATA has an indeterminate logic state after initial power up. This means that for the first conversion sequence after power up, the FRSTDATA logic output may already be logic high before the end of the first conversion. This condition is indicated by the dashed line in Figure 7. Also the FRSTDATA logic output may already be high as a result of the previous read sequence as is the case after the fourth read in Figure 7. The fourth read (rising edge of $\overline{RD}$) resets the pointer to the first data location. Therefore, FRSTDATA is already high when the next conversion sequence is initiated. See Accessing the Output Data Registers.

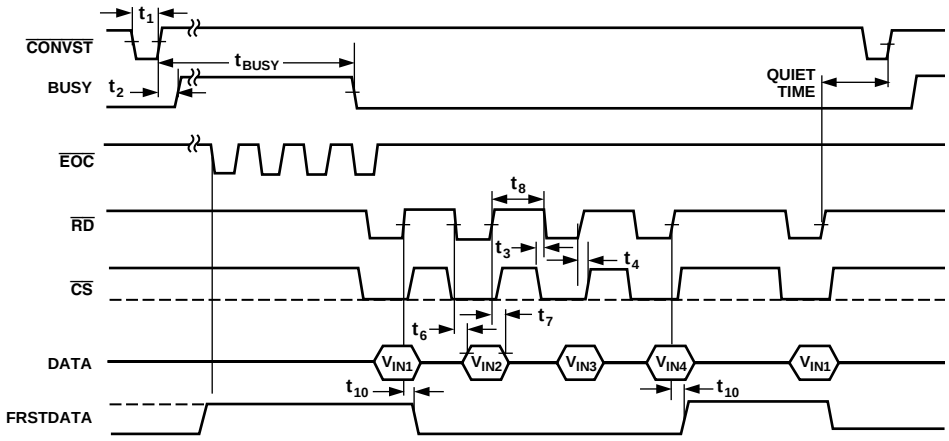


Figure 8. Timing Diagram, Reading After the Conversion Sequence

Reading After the Conversion Sequence

Figure 8 shows the same conversion sequence as Figure 7. In this case, however, the results of the four conversions (on VIN1 to VIN4) are read after all conversions have finished, i.e., when BUSY goes logic low. The FRSTDATA signal goes logic high at the end of the first conversion just prior to $\overline{EOC}$ going logic low. As mentioned previously FRSTDATA has an indeterminate state after initial power up, therefore FRSTDATA may already be logic high. Unlike the case when reading between each conversion the output data register pointer is incremented on the rising edge of $\overline{RD}$ because the next conversion result is available. This means FRSTDATA will go logic low after the first rising edge on $\overline{RD}$.

Successive read operations will access the remaining conversion results in an ascending channel order. Each read operation increments the output data register pointer. The read operation that accesses the last conversion result causes the output data register pointer to be reset so that the next read operation will access the first conversion result again. This is shown in Figure 8 with the fifth read after BUSY goes low accessing the result of the conversion on VIN1. Thus the output data registers act as a circular buffer in which the conversion results may be continually accessed. The FRSTDATA signal will go high when the first conversion result is available.

Data is enabled onto the data bus DB0 to DB11 using $\overline{CS}$ and $\overline{RD}$. Both $\overline{CS}$ and $\overline{RD}$ have the same functionality as described in the previous section. There are no restrictions or performance implications associated to the position of the read operations after BUSY goes low. The only restriction is that there is minimum time between read operations. Notice also that a "Quiet Time" is needed before the start of the next conversion.

Using an External Clock

The logic input $\overline{INT}$/EXT CLK allows the user to operate the AD7864 using the internal clock oscillator or an external clock. The optimum performance is achieved by using the internal clock on the AD7864. The highest external clock frequency allowed is 5 MHz. This means a conversion time of 2.6 µs compared to 1.65 µs using the internal clock. In some instances, however, it may be useful to use an external clock when high throughput rates are not required. For example, two or more AD7864s may be synchronized by using the same external clock for all devices. In this way there is no latency between output logic signals like $\overline{EOC}$ due to differences in the frequency of the internal clock oscillators. Figure 9 shows how the various logic outputs are synchronized to the CLK signal. Each conversion requires 14 clocks. The output data register pointer is reset to point to the first register location on the falling edge of the 12 clock cycle of the first conversion in the conversion sequence—See Accessing the Output Data Registers. At this point the logic output FRSTDATA goes logic high. The result of the first conversion is transferred to the output data registers on the falling edge of the 13 clock cycle. The FRSTDATA signal is reset on the falling edge of the 13 clock cycle of the next conversion, i.e., when the result of the second conversion is transferred to its output data register. As mentioned previously, the pointer is incremented by the rising edge of the $\overline{RD}$ signal if the result of the next conversion is available. The $\overline{EOC}$ signal goes logic low on the falling edge of the 13 clock cycle and is reset high again on the falling edge of the 14 clock cycle.

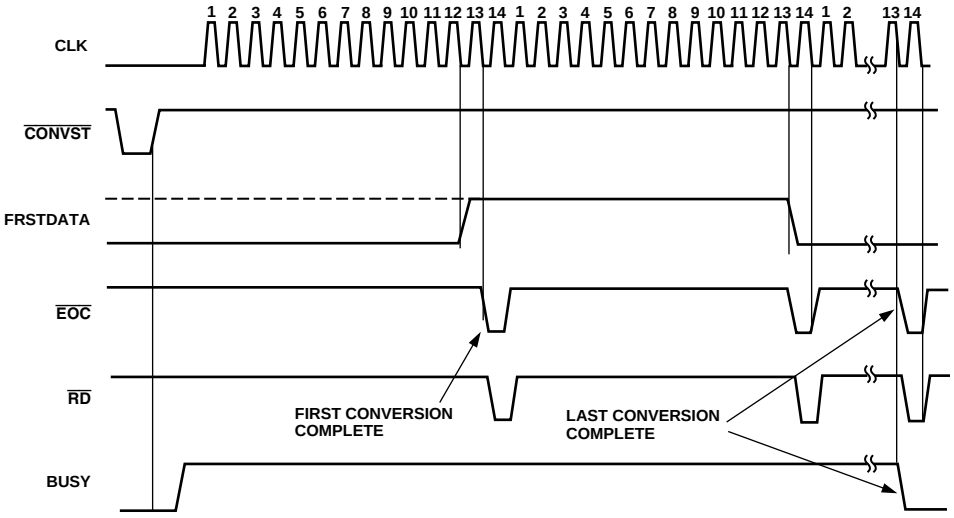


Figure 9. Using an External Clock

Standby Mode Operation

The AD7864 has a Standby Mode whereby the device can be placed in a low current consumption mode (5 μA typ). The AD7864 is placed in standby by bringing the logic input $\overline{\text{STBY}}$ low. The AD7864 can be powered up again for normal operation by bringing $\overline{\text{STBY}}$ logic high. The output data buffers are still operational while the AD7864 is in standby. This means the user can still continue to access the conversion results while the AD7864 is in standby. This feature can be used to reduce the average power consumption in a system using low throughput rates. To reduce the average power consumption the AD7864 can be placed in standby at the end of each conversion sequence, i.e., when BUSY goes low and taken out of standby again prior the start of the next conversion sequence. The time it takes the AD7864 to come out of standby is called the "wake up" time. This wake-up time will limit the maximum throughput rate at which the AD7864 can be operated when powering down between conversion sequences. The AD7864 will wake-up in approximately 2 μs when using an external reference. The "wake up" time is also 2 μs when the standby time is less than 1 millisecond while using the internal reference. Figure 11 shows the wake-up time of the AD7864 for standby times greater than 1 millisecond. Note when the AD7864 is left in standby for periods of time greater than 1 millisecond the part will require more than 2 μs to wake up. For example after initial power up, using the internal reference the AD7864 takes 6 ms to power up. The maximum throughput rate that can be achieved when powering down between conversions is $1/(t_{BUSY} + 2\ \mu s) = 100$ kSPS, approximately. When operating the AD7864 in a standby mode between conversions the power savings can be significant. For example with a throughput rate of 10 kSPS the AD7864 will be powered down (I_{DD} = 5 μA) for 90 μs out of every 100 μs. See Figure 10. Therefore the average power consumption drops to (125/10) mW or 12.5 mW approximately.

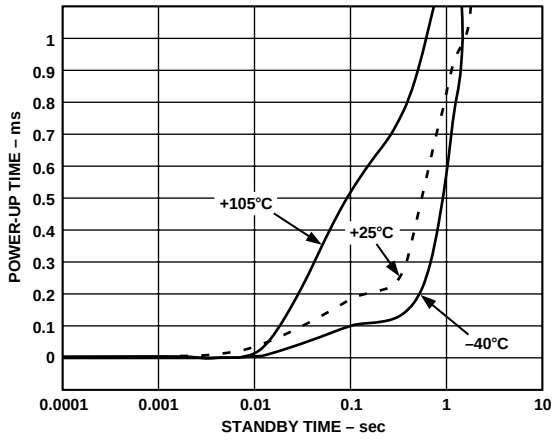


Figure 11. Power-Up Time vs. Standby Time Using the On-Chip Reference (Decoupled with 0.1 μF Capacitor)

Accessing the Output Data Registers

There are four Output Data Registers, one for each of the four possible conversion results from a conversion sequence. The result of the first conversion in a conversion sequence is placed in Register 1 and the second result is placed in Register Number 2 and so on. For example if the conversion sequence VIN1, VIN3 and VIN4 is selected (see Conversion Sequence Selection) then the results of the conversion on VIN1, VIN3 and VIN4 are placed in Registers 1 to 3 respectively. The Output Data register pointer is reset to point to Register 1 at the end of the first conversion in the sequence, just prior to $\overline{\text{EOC}}$ going

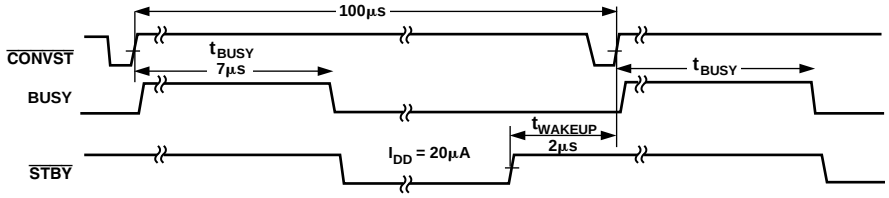


Figure 10. Power-Down Between Conversion Sequences

low. At this point the logic output FRSTDATA will go logic high to indicate that the output data register pointer is addressing Register Number 1. When $\overline{CS}$ and $\overline{RD}$ are both logic low the contents of the addressed register are enabled onto the data bus (DB0–DB11).

When reading the output data registers after a conversion sequence, i.e., when BUSY goes low, the register pointer is incremented on the rising edge of the $\overline{RD}$ signal as shown in Figure 12. However, when reading the conversion results during the conversion sequence the pointer will not be incremented until a valid conversion result is in the register to be addressed. In this case the pointer is incremented when the conversion has ended and the result has been transferred to the output data register. This happens just prior to $\overline{EOC}$ going low, therefore $\overline{EOC}$ may be used to enable the register contents onto the data bus as described in Reading During the Conversion Sequence. The pointer is reset to point to Register 1 on the rising edge of the $\overline{RD}$ signal when the last conversion result in the sequence is being read. In the example shown this means the pointer is set to Register 1 when the contents of Register 3 are read.

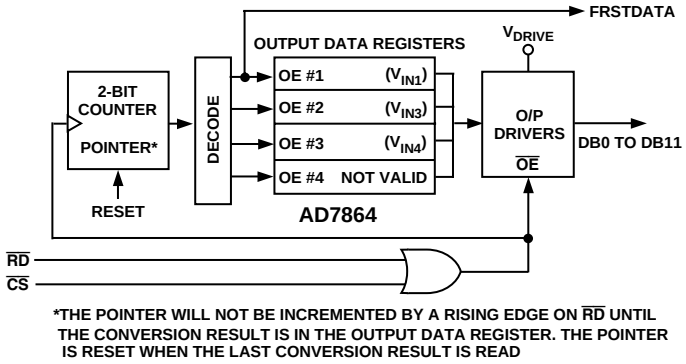


Figure 12. Output Data Registers

OFFSET AND FULL-SCALE ADJUSTMENT

In most Digital Signal Processing (DSP) applications, offset and full-scale errors have little or no effect on system performance. Offset error can always be eliminated in the analog domain by ac coupling. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. Invariably, some applications will require that the input signal span the full analog input dynamic range. In such applications, offset and full-scale error will have to be adjusted to zero.

Figure 13 shows a circuit which can be used to adjust the offset and full-scale errors on the AD7864 (V_{A1} on the AD7864-1 version is shown for example purposes only). Where adjustment is required, offset error must be adjusted before full-scale error. This is achieved by trimming the offset of the op amp driving the analog input of the AD7864 while the input voltage is a 1/2 LSB below analog ground. The trim procedure is as follows: apply a voltage of –2.44 mV (–1/2 LSB) at V_1 in Figure 13 and adjust the op amp offset voltage until the ADC output code flickers between 1111 1111 1111 and 0000 0000 0000.

Gain error can be adjusted at either the first code transition (ADC negative full scale) or the last code transition (ADC positive full scale). The trim procedures for both cases are as follows.

Positive Full-Scale Adjust

Apply a voltage of +9.9927 V (FS – 3/2 LSBs) at V_1. Adjust R2 until the ADC output code flickers between 0111 1111 1110 and 0111 1111 1111.

Negative Full-Scale Adjust

Apply a voltage of –9.9976 V (–FS + 1/2 LSB) at V_1 and adjust R2 until the ADC output code flickers between 1000 0000 0000 and 1000 0000 0001.

An alternative scheme for adjusting full-scale error in systems which use an external reference is to adjust the voltage at the VREF pin until the full-scale error for any of the channels is adjusted out. The good full-scale matching of the channels will ensure small full-scale errors on the other channels.

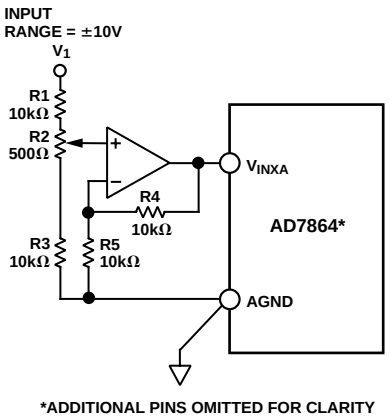


Figure 13. Full-Scale Adjust Circuit

DYNAMIC SPECIFICATIONS

The AD7864 is specified and 100% tested for dynamic performance specifications as well as traditional dc specifications such as integral and differential nonlinearity. These ac specifications are required for the signal processing applications such as phased array sonar, adaptive filters and spectrum analysis. These applications require information on the ADC's effect on the spectral content of the input signal. Hence, the parameters for which the AD7864 is specified include SNR, harmonic distortion, intermodulation distortion and peak harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal to noise ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency ($f_S/2$) excluding dc. SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to noise ratio for a sine wave input is given by

$$SNR = (6.02N + 1.76)\ dB \quad (1)$$

where N is the number of bits.

Thus for an ideal 12-bit converter, SNR = 74 dB.

Figure 14 shows a histogram plot for 8192 conversions of a dc input using the AD7864 with 5 V supply. The analog input was set at the center of a code. It can be seen that all the codes appear in the one output bin indicating very good noise performance from the ADC.

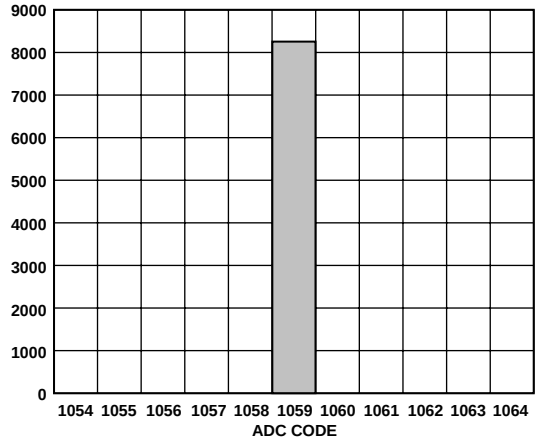


Figure 14. Histogram of 8192 Conversions of a DC Input

The output spectrum from the ADC is evaluated by applying a sine wave signal of very low distortion to the analog input. A Fast Fourier Transform (FFT) plot is generated from which the SNR data can be obtained. Figure 15 shows a typical 4096 point FFT plot of the AD7864 with an input signal of 99.9 kHz and a sampling frequency of 500 kHz. The SNR obtained from this graph is 72.6 dB. It should be noted that the harmonics are taken into account when calculating the SNR.

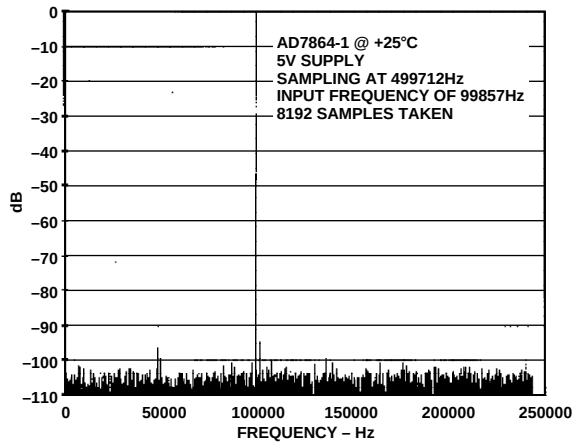


Figure 15. FFT Plot

Effective Number of Bits

The formula given in Equation 1 relates the SNR to the number of bits. Rewriting the formula, as in Equation 2, it is possible to get a measure of performance expressed in effective number of bits (N).

$$N = \frac{SNR - 1.76}{6.02} \quad (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR. Figure 16 shows a typical plot of effective number of bits versus frequency for an AD7864-2.

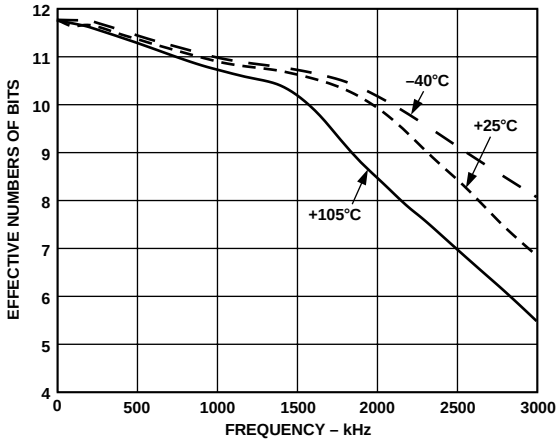


Figure 16. Effective Numbers of Bits vs. Frequency

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3 . . ., etc. Intermodulation terms are those for which neither m or n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb) while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

Using the CCIF standard where two input frequencies near the top end of the input bandwidth are used, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs. In this case, the input consists of two, equal amplitude, low distortion sine waves. Figure 17 shows a typical IMD plot for the AD7864.

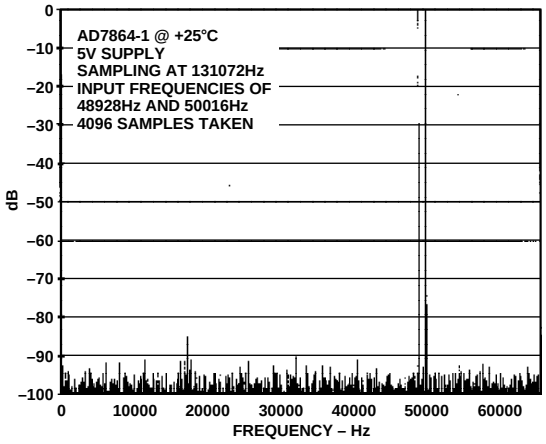


Figure 17. IMD Plot

AC Linearity Plots

The plots shown in Figure 18 below show typical DNL and INL plots for the AD7864.

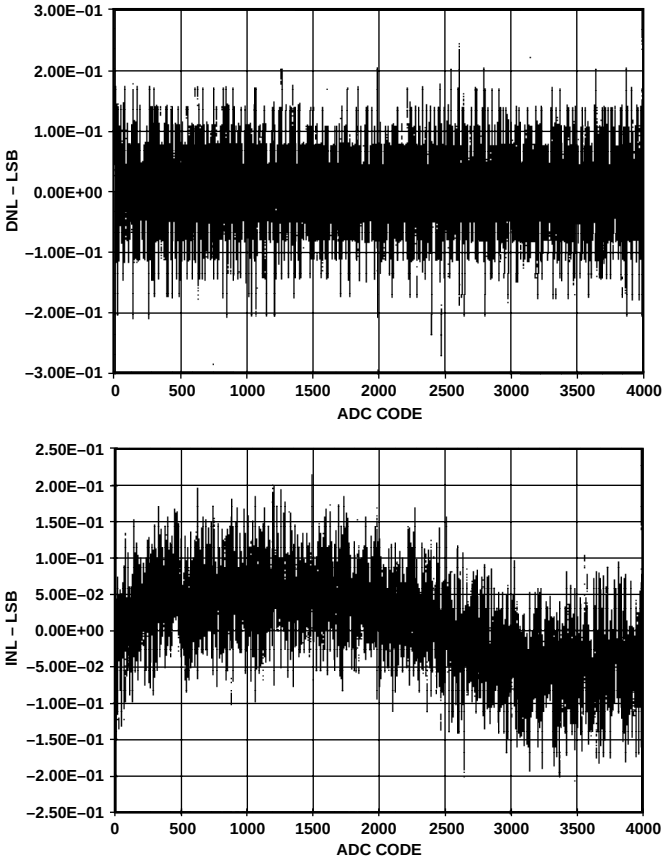


Figure 18. Typical DNL and INL Plots

Measuring Aperture Jitter

A convenient way to measure aperture jitter is to use the relationship it is known to have with SNR (Signal to Noise plus distortion) given below:

$$SNR_{JITTER} = 20 \times \log_{10}\left(\frac{1}{(2 \times \pi \times f_{IN} \times \sigma)}\right), \textit{ where} \qquad (3)$$

SNR_{JITTER} = Signal to Noise due to the rms time jitter
σ = rms time jitter
f_{IN} = sinusoidal input frequency (1 MHz in this case)

From Equation 3 above it can be seen that the signal-to-noise ratio due to jitter degrades significantly with frequency. Therefore, at low input frequencies the measured SNR performance of the AD7864 is indicative of noise performance due to quantization noise and system noise only (72 dBs used as a typical figure here).

Therefore, by measuring the overall SNR performance (including noise due to jitter, system and quantization) of the AD7864 a good estimation of the jitter performance of the AD7864 can be calculated.

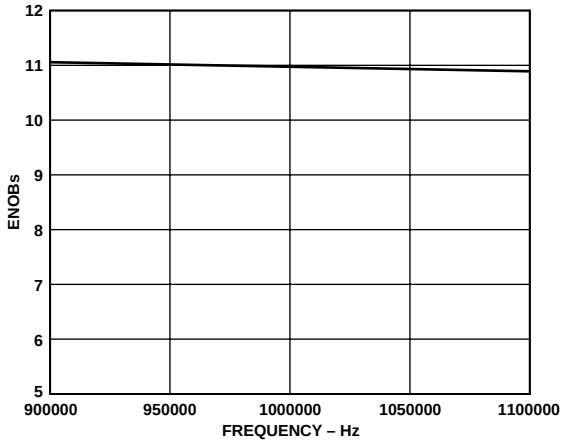


Figure 19. ENOBs of the AD7864 at 1 MHz

From Figure 19 above the ENOBs of the AD7864 at 1 MHz is approximately 11 bits. This is equivalent to 68 dBs SNR.

$SNR_{TOTAL} = SNR_{JITTER} + SNR_{QUANT} = 68$ dBs
68 dBs = SNR_{JITTER} + 72 dBs (at 100 kHz)
$SNR_{JITTER} = 70.2$ dBs

From (3) above
70.2 dBs = $20 \times \log_{10} [1/(2 \times \pi \times 1 \text{ MHz} \times \sigma)]$
σ = 49 ps where σ is the rms jitter of the AD7864

MICROPROCESSOR INTERFACING

The high speed parallel interface of the AD7864 allows easy interfacing to most DSP processors and microprocessors. The ADC7864 interface of the AD7864 consists of the data lines (DB0–DB11), $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, $\overline{EOC}$ and BUSY.

AD7864–ADSP-2100/ADSP-2101/ADSP-2102 Interface

Figure 20 shows an interface between the AD7864 and the ADSP-2100. The $\overline{CONVST}$ signal can be generated by the ADSP-2100 or from some other external source. Figure 20 shows the $\overline{CS}$ being generated by a combination of the $\overline{DMS}$ signal and the address bus of the ADSP-2100. In this way the AD7864 is mapped into the data memory space of the ADSP-2100.

The AD7864 BUSY line provides an interrupt to the ADSP-2100 when the conversion sequence is complete on all the selected channels. The conversion results can then be read from the AD7864 using successive read operations. Alternately, one can use the $\overline{EOC}$ pulse to interrupt the ADSP-2100 when the conversion on each channel is complete when reading between each conversion in the conversion sequence (Figure 7). The AD7864 is read using the following instruction

MR0 = DM(ADC)

where MR0 is the ADSP-2100 MR0 register and ADC is the AD7864 address.

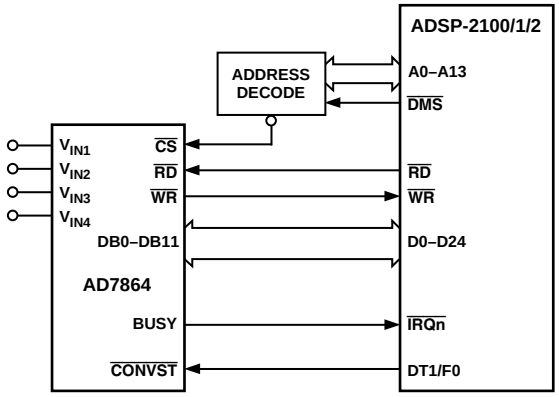


Figure 20. AD7864–ADSP-2100 Interface

AD7864–TMS320C5x Interface

Figure 21 shows an interface between the AD7864 and the TMS320C5x. As with the previous interfaces, conversion can be initiated from the TMS320C5x or from an external source and the processor is interrupted when the conversion sequence is completed. The $\overline{CS}$ signal to the AD7864 is derived from the DS signal and a decode of the address bus. This maps the AD7864 into external data memory. The $\overline{RD}$ signal from the TMS320 is used to enable the ADC data onto the data bus. The AD7864 has a fast parallel bus so there are no wait state requirements. The following instruction is used to read the conversion results from the AD7864:

IN D,ADC

where D is Data Memory address and ADC is the AD7864 address.

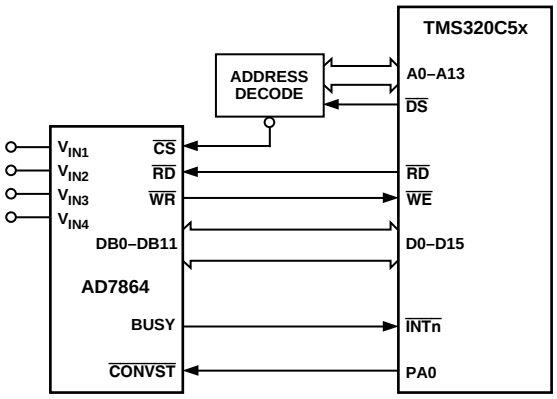


Figure 21. AD7864–TMS320C5x Interface

AD7864–MC68000 Interface

An interface between the AD7864 and the MC68000 is shown in Figure 22. The conversion can be initiated from the MC68000 or from an external source. The AD7864 BUSY line can be used to interrupt the processor or, alternatively, software delays can ensure that conversion has been completed before a read to the AD7864 is attempted. Because of the nature of its interrupts, the 68000 requires additional logic (not shown in Figure 22) to allow it to be interrupted correctly. For further information on 68000 interrupts, consult the 68000 Users Manual.

The MC68000 $\overline{AS}$ and R/$\overline{W}$ outputs are used to generate a separate $\overline{RD}$ input signal for the AD7864. $\overline{RD}$ is used to drive the 68000 $\overline{DTACK}$ input to allow the processor to execute a normal read operation to the AD7864. The conversion results are read using the following 68000 instruction:

MOVE.W ADC,D0

where D0 is the 68000 D0 register and ADC is the AD7864 address.

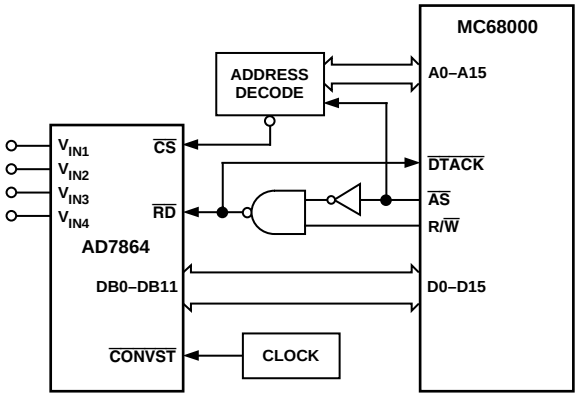


Figure 22. AD7864–MC68000 Interface

Vector Motor Control

The current drawn by a motor can be split into two components: one produces torque and the other produces magnetic flux. For optimal performance of the motor, these two components should be controlled independently. In conventional methods of controlling a three-phase motor, the current (or voltage) supplied to the motor and the frequency of the drive are the basic control variables. However, both the torque and flux are functions of current (or voltage) and frequency. This coupling effect can reduce the performance of the motor because, for example, if the torque is increased by increasing the frequency, the flux tends to decrease.

Vector control of an ac motor involves controlling phase in addition to drive and current frequency. Controlling the phase of the motor requires feedback information on the position of the rotor relative to the rotating magnetic field in the motor. Using this information, a vector controller mathematically transforms the three phase drive currents into separate torque and flux components. The AD7864, with its four-channel simultaneous sampling capability, is ideally suited for use in vector motor control applications.

A block diagram of a vector motor control application using the AD7864 is shown in Figure 23. The position of the field is derived by determining the current in each phase of the motor. Only two phase currents need to be measured because the third can be calculated if two phases are known. V_{IN1} and V_{IN2} of the AD7864 are used to digitize this information.

Simultaneous sampling is critical to maintain the relative phase information between the two channels. A current sensing isolation amplifier, transformer or Hall effect sensor is used between the motor and the AD7864. Rotor information is obtained by measuring the voltage from two of the inputs to the motor. V_{IN3} and V_{IN4} of the AD7864 are used to obtain this information. Once again the relative phase of the two channels is important. A DSP microprocessor is used to perform the mathematical transformations and control loop calculations on the information fed back by the AD7864.

MULTIPLE AD7864s IN A SYSTEM

Figure 24 shows a system where a number of AD7864s can be configured to handle multiple input channels. This type of configuration is common in applications such as sonar, radar, etc. The AD7864 is specified with maximum limits on aperture delay match. This means that the user knows the difference in the sampling instant between all channels. This allows the user to maintain relative phase information between the different channels. The AD7864 has a maximum aperture delay matching of 4 ns.

All AD7864s use the same external SAR clock (5 MHz). Therefore, the conversion time for all devices will be the same and so all devices may be read simultaneously. The example shown in Figure 24 the data outputs of two AD7864s are enabled onto a 32-bit wide data bus when $\overline{EOC}$ goes low.

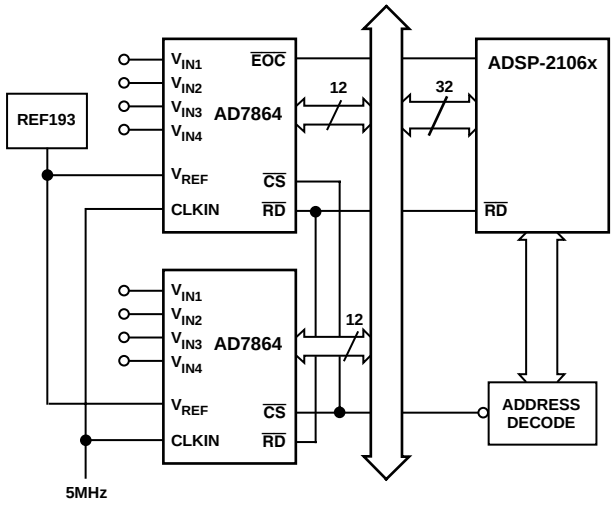


Figure 24. Multiple AD7864s in Multichannel System

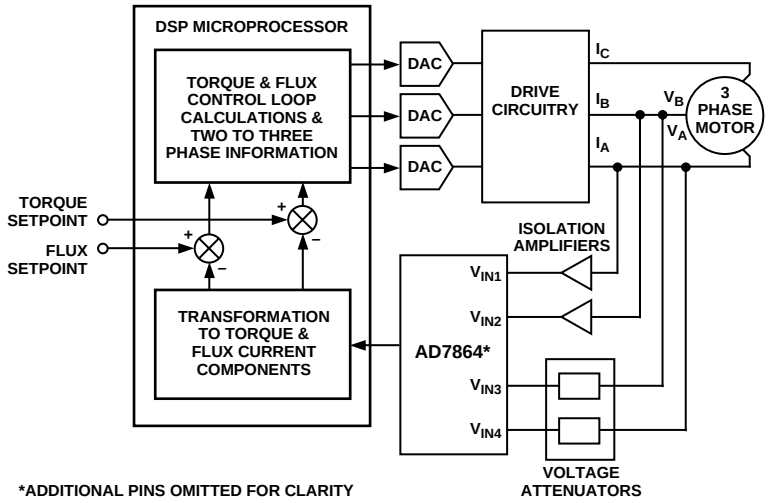
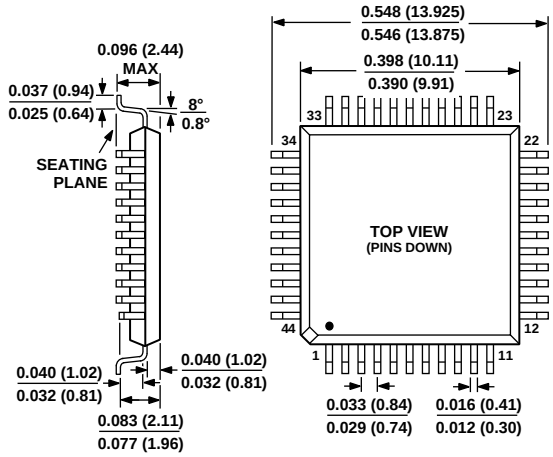


Figure 23. Vector Motor Control Using the AD7864

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

44-Lead Plastic Quad Flatpack
(S-44)



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