Low Power, 16-/24-Bit, Sigma-Delta ADCs

AD7788/AD7789

FEATURES

- AD7788: 16-bit resolution
- AD7789: 24-bit resolution
- Power
  - Supply: 2.5 V to 5.25 V operation
  - Normal: 75 µA maximum
  - Power-down: 1 µA maximum
- RMS noise: 1.5 µV
- AD7788: 16-bit p-p resolution
- AD7789: 19-bit p-p resolution (21.5 bits effective)
- Integral nonlinearity: 3.5 ppm typical
- Simultaneous 50 Hz and 60 Hz rejection
- Internal clock oscillator
- V_{DD} monitor channel
- 10-lead MSOP

INTERFACE

- 3-wire serial
- SPI®-, QSPI™-, MICROWIRE™-, and DSP-compatible
- Schmitt trigger on SCLK

APPLICATIONS

- Smart transmitters
- Battery applications
- Portable instrumentation
- Sensor measurement
- Temperature measurement
- Pressure measurement
- Weigh scales
- 4 to 20 mA loops

FUNCTIONAL BLOCK DIAGRAM

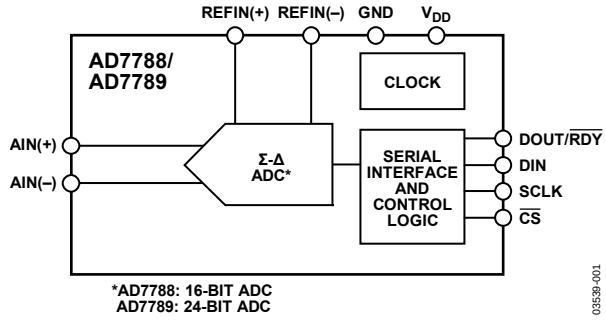


Figure 1.

GENERAL DESCRIPTION

The AD7788/AD7789 are low power, low noise, analog front ends for low frequency measurement applications. The AD7789 contains a low noise, 24-bit, Σ-Δ ADC with one differential input. The AD7788 is a 16-bit version of the AD7789.

The devices operate from an internal clock. Therefore, the user does not have to supply a clock source to the devices. The output data rate is 16.6 Hz, which gives simultaneous 50 Hz/60 Hz rejection.

The parts operate with a single power supply from 2.5 V to 5.25 V. When operating from a 3 V supply, the power dissipation for the part is 225 µW maximum. The AD7788/AD7789 are available in a 10-lead MSOP.

Rev. B

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REVISION HISTORY

3/06—Rev. A to Rev. B

Changes to Ordering Guide ... 19

11/04—Rev. 0 to Rev. A

Updated Format ... Universal
Added Footnote 2 to Integral Nonlinearity A Grade ... 4
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Updated Outline Dimensions ... 19
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8/03—Revision 0: Initial Version

SPECIFICATIONS

AD7789

V_{DD} = 2.5 V to 5.25 V; REFIN(+) = 2.5 V; REFIN(−) = GND; GND = 0 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter[1]	AD7789B	Unit	Test Conditions/Comments
ADC CHANNEL SPECIFICATION			
Output Update Rate	16.6	Hz nom	
ADC CHANNEL			
No Missing Codes[2]	24	Bits min	
Resolution	19	Bits p-p	
Output Noise	1.5	µV rms typ	
Integral Nonlinearity	±15	ppm of FSR max	
Offset Error	±3	µV typ	
Offset Error Drift vs. Temperature	±10	nV/°C typ	
Full-Scale Error[3]	±10	µV typ	
Gain Drift vs. Temperature	±0.5	ppm/°C typ	
Power Supply Rejection	90	dB min	100 dB typ, AIN = 1 V
ANALOG INPUTS			
Differential Input Voltage Ranges	±REFIN	V nom	REFIN = REFIN(+) − REFIN(−)
Absolute AIN Voltage Limits[2]	GND − 30 mV	V min	
	V_{DD} + 30 mV	V max	
Analog Input Current			Input current varies with input voltage
Average Input Current[2]	±400	nA/V typ	
Average Input Current Drift	±50	pA/V/°C typ	
Normal-Mode Rejection[2]			
@ 50 Hz, 60 Hz	65	dB min	50 Hz ± 1 Hz, 60 Hz ± 1 Hz
Common-Mode Rejection			AIN = 1 V
@ DC	90	dB min	100 dB typ
@ 50 Hz, 60 Hz[2]	100	dB min	50 Hz ± 1 Hz, 60 Hz ± 1 Hz
REFERENCE INPUT			
REFIN Voltage	2.5	V nom	REFIN = REFIN(+) − REFIN(−)
Reference Voltage Range[2]	0.1	V min	
	V_{DD}	V max	
Absolute REFIN Voltage Limits[2]	GND − 30 mV	V min	
	V_{DD} + 30 mV	V max	
Average Reference Input Current	0.5	µA/V typ	
Average Reference Input Current Drift	±0.03	nA/V/°C typ	
Normal-Mode Rejection[2]			
@ 50 Hz, 60 Hz	65	dB min	50 Hz ± 1 Hz, 60 Hz ± 1 Hz
Common-Mode Rejection			AIN = 1 V
@ DC	110	dB typ	
@ 50 Hz, 60 Hz	110	dB typ	50 Hz ± 1 Hz, 60 Hz ± 1 Hz

[1] Temperature range: −40°C to +105°C.
[2] Specification is not production tested but is supported by characterization data at initial product release.
[3] Full-scale error applies to both positive and negative full scale and applies at the factory calibration conditions (V_{DD} = 4 V).

AD7788

V_{DD} = 2.5 V to 5.25 V (B grade); V_{DD} = 2.7 V to 5.25 V (A grade); REFIN(+) = 2.5 V; REFIN(−) = GND; GND = 0 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	AD7788 A, AD7788B	Unit	Test Conditions/Comments
ADC CHANNEL SPECIFICATION			
Output Update Rate	16.6	Hz nom	
ADC CHANNEL			
No Missing Codes[2]	16	Bits min	
Resolution	16	Bits p-p	
Output Noise	1.5	µV rms typ	
Integral Nonlinearity	±15	ppm of FSR max	B grade
	±50	ppm of FSR max	A grade[2]
Offset Error	±3	µV typ	
Offset Error Drift vs. Temperature	±10	nV/°C typ	
Full-Scale Error[3]	±10	µV typ	
Gain Drift vs. Temperature	±0.5	ppm/°C typ	
Power Supply Rejection	90	dB min	B grade
	90	dB typ	A grade
ANALOG INPUTS			
Differential Input Voltage Ranges	±REFIN	V nom	REFIN = REFIN(+) − REFIN(−)
Absolute AIN Voltage Limits[2]	GND − 30 mV	V min	
	V_{DD} + 30 mV	V max	
Analog Input Current			Input current varies with input voltage
Average Input Current[2]	±400	nA/V typ	
Average Input Current Drift	±50	pA/V/°C typ	
Normal-Mode Rejection[2]			
@ 50 Hz, 60 Hz	65	dB min	B grade, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
	60	dB min	A grade, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
Common-Mode Rejection			AIN = 1 V
@ DC	90	dB min	B grade, 100 dB typ
	90	dB typ	A grade
@ 50 Hz, 60 Hz[2]	100	dB min	B grade, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
	100	dB typ	A grade, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
REFERENCE INPUT			
REFIN Voltage	2.5	V nom	REFIN = REFIN(+) − REFIN(−)
Reference Voltage Range[2]	0.1	V min	
	V_{DD}	V max	
Absolute REFIN Voltage Limits[2]	GND − 30 mV	V min	
	V_{DD} + 30 mV	V max	
Average Reference Input Current	0.5	µA/V typ	
Average Reference Input Current Drift	±0.03	nA/V/°C typ	
Normal-Mode Rejection[2]			
@ 50 Hz, 60 Hz	65	dB min	B grade, 50 Hz ± 1 Hz, 60 Hz ± 1 Hz
	60	dB min	A grade
Common-Mode Rejection			AIN = 1 V
@ DC	100	dB typ	
@ 50 Hz, 60 Hz	110	dB typ	50 Hz ± 1 Hz, 60 Hz ± 1 Hz

[1] Temperature range: B grade: −40°C to +105°C; A grade: −40°C to +85°C.
[2] Specification is not production tested but is supported by characterization data at initial product release.
[3] Full-scale error applies to both positive and negative full scale and applies at the factory calibration conditions (V_{DD} = 4 V).

AD7788/AD7789

Table 3.

Parameter	AD7788A, AD7788B/AD7789B	Unit	Test Conditions/Comments
LOGIC INPUTS			
All Inputs Except SCLK[1]			
V_{INL}, Input Low Voltage	0.8	V max	V_{DD} = 5 V
	0.4	V max	V_{DD} = 3 V
V_{INH}, Input High Voltage	2.0	V min	V_{DD} = 3 V or 5 V
SCLK Only (Schmitt-Triggered Input)[1]			
$V_T(+)$	1.4/2	V min/V max	V_{DD} = 5 V
$V_T(-)$	0.8/1.4	V min/V max	V_{DD} = 5 V
$V_T(+) - V_T(-)$	0.3/0.85	V min/V max	V_{DD} = 5 V
$V_T(+)$	0.9/2	V min/V max	V_{DD} = 3 V
$V_T(-)$	0.4/1.1	V min/V max	V_{DD} = 3 V
$V_T(+) - V_T(-)$	0.3/0.85	V min/V max	V_{DD} = 3 V
Input Currents	±1	μA max	$V_{IN} = V_{DD}$
Input Capacitance	10	pF typ	All digital inputs
LOGIC OUTPUTS			
V_{OH}, Output High Voltage[1]	V_{DD} − 0.6	V min	V_{DD} = 3 V, I_{SOURCE} = 100 μA
V_{OL}, Output Low Voltage[1]	0.4	V max	V_{DD} = 3 V, I_{SINK} = 100 μA
V_{OH}, Output High Voltage[1]	4	V min	V_{DD} = 5 V, I_{SOURCE} = 200 μA
V_{OL}, Output Low Voltage[1]	0.4	V max	V_{DD} = 5 V, I_{SINK} = 1.6 mA
Floating-State Leakage Current	±1	μA max	
Floating-State Output Capacitance	10	pF typ	
Data Output Coding	Offset binary		
POWER REQUIREMENTS[2]			
Power Supply Voltage			
V_{DD} − GND	2.5/5.25	V min/max	AD7789, AD7788 B grade
	2.7/5.25	V min/max	AD7788 A grade
Power Supply Currents			
I_{DD} Current	75	μA max	65 μA typ, V_{DD} = 3.6 V
	80	μA max	73 μA typ, V_{DD} = 5.25 V
I_{DD} (Power-Down Mode)	1	μA max	

[1] Specification is not production tested but is supported by characterization data at initial product release.
[2] Digital inputs equal to V_{DD} or GND.

TIMING CHARACTERISTICS

V_{DD} = 2.5 V to 5.25 V (AD7788B and AD7789); V_{DD} = 2.7 V to 5.25 V (AD7788A); GND = 0 V; REFIN(+) = 2.5 V; REFIN(−) = GND; Input Logic 0 = 0 V; Input Logic 1 = V_{DD}, unless otherwise noted.

Table 4.

Parameter[1, 2]	Limit at T_{MIN}, T_{MAX} (B Version)	Unit	Description
t_3	100	ns min	SCLK high pulse width
t_4	100	ns min	SCLK low pulse width
Read Operation			
t_1	0	ns min	$\overline{CS}$ falling edge to DOUT/$\overline{RDY}$ active time
	60	ns max	V_{DD} = 4.75 V to 5.25 V
	80	ns max	V_{DD} = 2.7 V to 3.6 V
t_2[3]	0	ns min	SCLK active edge to data valid delay[4]
	60	ns max	V_{DD} = 4.75 V to 5.25 V
	80	ns max	V_{DD} = 2.7 V to 3.6 V
t_5[5, 6]	10	ns min	Bus relinquish time after $\overline{CS}$ inactive edge
	80	ns max	
t_6	0	ns min	SCLK inactive edge to $\overline{CS}$ inactive edge
t_7	10	ns min	SCLK inactive edge to DOUT/$\overline{RDY}$ high
Write Operation			
t_8	0	ns min	$\overline{CS}$ falling edge to SCLK active edge setup time[4]
t_9	30	ns min	Data valid to SCLK edge setup time
t_{10}	25	ns min	Data valid to SCLK edge hold time
t_{11}	0	ns min	$\overline{CS}$ rising edge to SCLK edge hold time

[1] Sample tested during initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.
[2] See Figure 3 and Figure 4.
[3] These numbers are measured with the load circuit of, and defined as, the time required for the output to cross the V_{OL} or V_{OH} limits.
[4] SCLK active edge is the falling edge of SCLK.
[5] These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the Timing Characteristics are the true bus relinquish times of the part and, as such, are independent of external bus loading capacitances.
[6] $\overline{RDY}$ returns high after a read of the ADC. In single-conversion mode and continuous-conversion mode, the same data can be read again, if required, while $\overline{RDY}$ is high, although care should be taken to ensure that subsequent reads do not occur close to the next output update. In continuous read mode, the digital word can be read only once.

TIMING DIAGRAMS

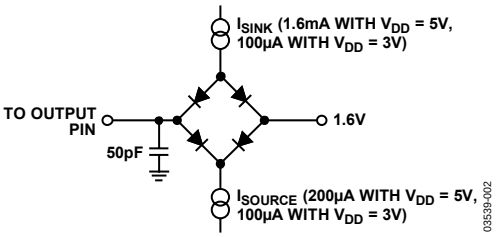


Figure 2. Load Circuit for Timing Characterization

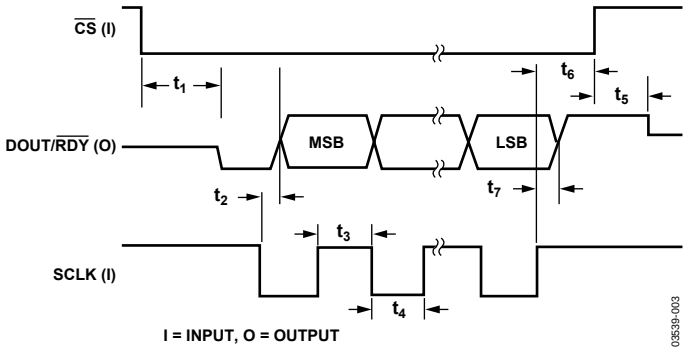


Figure 3. Read Cycle Timing Diagram

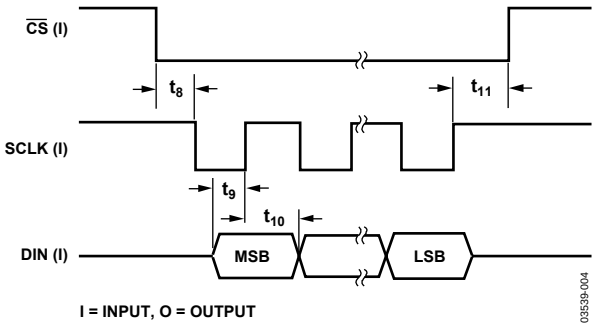


Figure 4. Write Cycle Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Total AIN/REFIN Current (Indefinite)	30 mA
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
B Grade	−40°C to +105°C
A Grade	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
10-Lead MSOP	
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

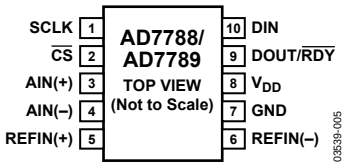


Figure 5. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCLK	Serial Clock Input for Data Transfers to and from the ADC. The SCLK has a Schmitt-triggered input, making the interface suitable for opto-isolated applications. The serial clock can be continuous, with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to or from the ADC in smaller batches of data.
2	$\overline{CS}$	Chip Select Input. This is an active low logic input used to select the ADC. $\overline{CS}$ can be used to select the ADC in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the device. $\overline{CS}$ can be hardwired low, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT/$\overline{RDY}$ used to interface with the device.
3	AIN(+)	Analog Input. AIN(+) is the positive terminal of the fully differential analog input.
4	AIN(–)	Analog Input. AIN(–) is the negative terminal of the fully differential analog input.
5	REFIN(+)	Positive Reference Input. REFIN(+) can lie anywhere between V_{DD} and GND + 0.1 V. The nominal reference voltage (REFIN(+) − REFIN(–)) is 2.5 V, but the part functions with a reference from 0.1 V to V_{DD}.
6	REFIN(–)	Negative Reference Input. This reference input can lie anywhere between GND and V_{DD} − 0.1 V.
7	GND	Ground Reference Point.
8	V_{DD}	Supply Voltage. 3 V or 5 V nominal.
9	DOUT/$\overline{RDY}$	The DOUT/$\overline{RDY}$ falling edge can be used as an interrupt to a processor, indicating that valid data is available. With an external serial clock, the data can be read using the DOUT/$\overline{RDY}$ pin. With $\overline{CS}$ low, the data/control word information is placed on the DOUT/$\overline{RDY}$ pin on the SCLK falling edge and is valid on the SCLK rising edge. The end of a conversion is also indicated by the $\overline{RDY}$ bit in the status register. When $\overline{CS}$ is high, the DOUT/$\overline{RDY}$ pin is three-stated, but the $\overline{RDY}$ bit remains active.
10	DIN	Serial Data Input to the Input Shift Register on the ADC. Data in this shift register is transferred to the control registers within the ADC; the register selection bits of the communications register identify the appropriate register.

TYPICAL PERFORMANCE CHARACTERISTICS

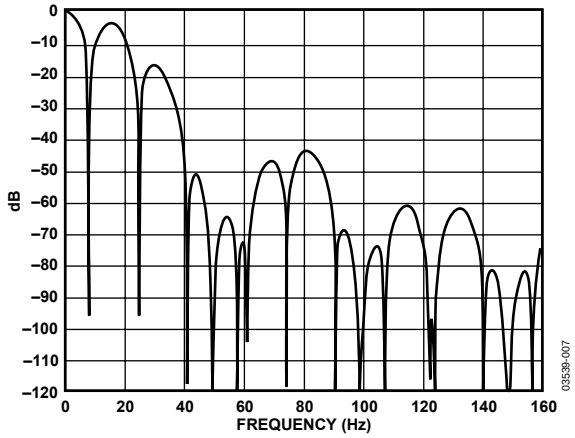


Figure 6. Frequency Response with 16.6 Hz Update Rate

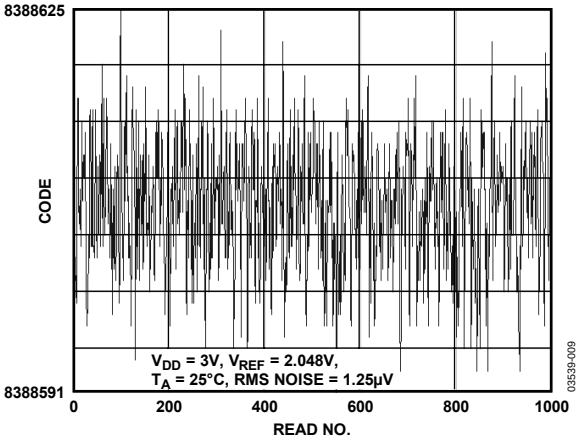


Figure 8. AD7789 Noise Plot

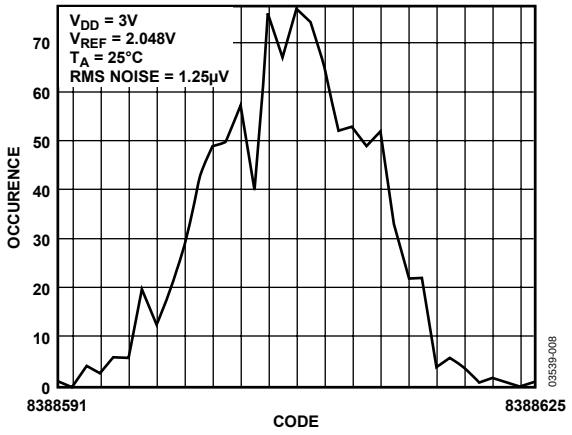


Figure 7. AD7789 Noise Histogram

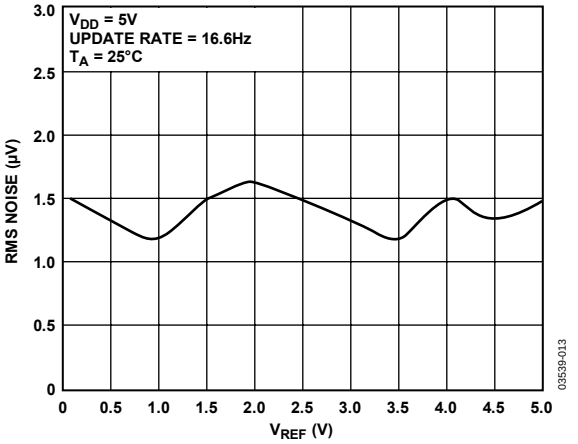


Figure 9. AD7788/AD7789 Noise vs. V_{REF}

ON-CHIP REGISTERS

The ADC is controlled and configured via a number of on-chip registers, which are described on the following pages. In the following descriptions, set implies a Logic 1 state and cleared implies a Logic 0 state, unless otherwise stated.

COMMUNICATIONS REGISTER

(RS1, RS0 = 0, 0)

The communications register is an 8-bit, write only register. All communications to the part must start with a write operation to the communications register. The data written to the communications register determines whether the next operation is a read or write operation, and to which register this operation takes place.

For read or write operations, once the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the communications register. This is the default state of the interface and, on power-up or after a reset, the ADC is in this default state waiting for a write operation to the communications register. In situations where the interface sequence is lost, a write operation of at least 32 serial clock cycles with DIN high returns the ADC to this default state by resetting the entire part. Table 7 outlines the bit designations for the communications register. CR0 through CR7 indicate the bit location, CR denoting the bits are in the communications register. CR7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit.

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
$\overline{\text{WEN}}$[0]	0[0]	RS1[0]	RS0[0]	R/$\overline{\text{W}}$[0]	CREAD[0]	CH1[0]	CH0[0]

Table 7. Communications Register Bit Designations

Bit Location	Bit Name	Description
CR7	$\overline{\text{WEN}}$	Write Enable Bit. A 0 must be written to this bit so that the write to the communications register actually occurs. If a 1 is the first bit written, the part does not clock on to subsequent bits in the register. It stays at this bit location until a 0 is written to this bit. Once a 0 is written to the $\overline{\text{WEN}}$ bit, the next seven bits are loaded to the communications register.
CR6	0	This bit must be programmed with a Logic 0 for correct operation.
CR5 to CR4	RS1 to RS0	Register Address Bits. These address bits are used to select which of the ADC registers are being selected during this serial interface communication (see Table 8).
CR3	R/$\overline{\text{W}}$	A 0 in this bit location indicates that the next operation is a write to a specified register. A 1 in this position indicates that the next operation is a read from the designated register.
CR2	CREAD	Continuous Read of the Data Register. When this bit is set to 1 (and the data register is selected), the serial interface is configured so that the data register can be continuously read, that is, the contents of the data register are placed on the DOUT/$\overline{\text{RDY}}$ pin automatically when the SCLK pulses are applied. The communications register does not have to be written to for data reads. To enable continuous read mode, the instruction 001111XX must be written to the communications register. To exit the continuous read mode, the instruction 001110XX must be written to the communications register while the DOUT/$\overline{\text{RDY}}$ pin is low. While in continuous read mode, the ADC monitors activity on the DIN line so that it can receive the instruction to exit continuous read mode. Additionally, a reset occurs if 32 consecutive 1s are seen on DIN. Therefore, DIN should be held low in continuous read mode until an instruction is to be written to the device.
CR1 to CR0	CH1 to CH0	These bits are used to select the analog input channel. The differential channel can be selected AIN(+)/AIN(−) or an internal short AIN(−)/AIN(−) can be selected. Alternatively, the power supply can be selected, that is, the ADC can measure the voltage on the power supply, which is useful for monitoring power supply variation. The power supply voltage is divided by 5 and then applied to the modulator for conversion. The ADC uses a 1.17 V ± 5% on-chip reference as the reference source for the analog-to-digital conversion. Any change in channel resets the filter and a new conversion is started.

Table 8. Register Selection

RS1	RS0	Register	Register Size
0	0	Communications register during a write operation	8-bit
0	0	Status register during a read operation	8-bit
0	1	Mode register	8-bit
1	0	Reserved	8-bit
1	1	Data register	16-bit (AD7788) 24-bit (AD7789)

Table 9. Channel Selection

CH1	CH0	Channel
0	0	AIN(+) – AIN(–)
0	1	Reserved
1	0	AIN(–) – AIN(–)
1	1	V_{DD} monitor

STATUS REGISTER

(RS1, RS0 = 0, 0; Power-On/Reset = 0x88 for AD7788 and 0x8C for AD7789)

The status register is an 8-bit, read only register. To access the ADC status register, the user must write to the communications register, select the next operation to be a read, and load Bit RS1 and Bit RS0 with 0. Table 10 outlines the bit designations for the status register. SR0 through SR7 indicate the bit locations, SR denoting the bits are in the status register. SR7 denotes the first bit of the data stream. The number(s) in brackets indicates the power-on/reset default status of that bit.

MSB **LSB**

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
$\overline{\text{RDY}}$[1]	ERR[0]	0[0]	0[0]	1[1]	WL[1/0]	CH1[0]	CH0[0]

Table 10. Status Register Bit Designations

Bit Location	Bit Name	Description
SR7	$\overline{\text{RDY}}$	Ready Bit for ADC. Cleared when data is written to the ADC data register. The $\overline{\text{RDY}}$ bit is set automatically after the ADC data register has been read or a period of time before the data register is updated with a new conversion result to tell the user not to read the conversion data. It is also set when the part is placed in power-down mode. The end of a conversion is indicated by the DOUT/$\overline{\text{RDY}}$ pin. This pin can be used as an alternative to the status register for monitoring the ADC for conversion data.
SR6	ERR	ADC Error Bit. This bit is written to at the same time as the $\overline{\text{RDY}}$ bit. Set to indicate that the result written to the ADC data register has been clamped to all 0s or all 1s. Error sources include overrange, under-range. Cleared by a write operation to start a conversion.
SR5	0	This bit is cleared automatically.
SR4	0	This bit is cleared automatically.
SR3	1	This bit is set automatically.
SR2	WL	AD7788/AD7789 Identifier. This bit is cleared automatically if the device is an AD7788 and it is set automatically if the device is an AD7789. This bit is used to distinguish between the AD7788 and AD7789.
SR1 to SR0	CH1 to CH0	These bits indicate which channel is being converted by the ADC.

MODE REGISTER

(RS1, RS0 = 0, 1; Power-On/Reset = 0x02)

The mode register is an 8-bit register from which data can be read from or written to. This register is used to configure the ADC for range, to set unipolar or bipolar mode, to enable or disable the buffer, or to place the device into power-down mode. Table 11 outlines the bit designations for the mode register. MR0 through MR7 indicate the bit locations, MR denoting the bits are in the mode register. MR7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit. Any write to the setup register resets the modulator and filter, and sets the $\overline{RDY}$ bit.

MSB **LSB**

MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
MD1[0]	MD0[0]	0[0]	0[0]	0[0]	U/$\overline{B}$[0]	1[1]	0[0]

Table 11. Mode Register Bit Designations

Bit Location	Bit Name	Description
MR7 to MR6	MD1 to MD0	Mode Select Bits. These bits select between continuous conversion mode, single conversion mode, and standby mode. In continuous conversion mode, the ADC continuously performs conversions and places the result in the data register. DOUT/ $\overline{RDY}$ goes low when a conversion is complete. The user can read these conversions by placing the device in continuous read mode whereby the conversions are automatically placed on the DOUT/ $\overline{RDY}$ line when SCLK pulses are applied. Alternatively, the user can instruct the ADC to output the conversion by writing to the communications register. After power-on, the first conversion is available after a period 2/ f_{ADC} while subsequent conversions are available at a frequency of f_{ADC}. In single conversion mode, the ADC is placed in power-down mode when conversions are not being performed. When single conversion mode is selected, the ADC powers up (which takes 1 ms) and performs a single conversion, requiring a duration of 2/f_{ADC}. The conversion result is placed in the data register, DOUT/ $\overline{RDY}$ goes low, and the ADC returns to power-down mode. The conversion remains in the data register and DOUT/ $\overline{RDY}$ remains active (low) until the data is read or another conversion is performed (see Table 12).
MR5 to MR3	0	These bits must be programmed with a Logic 0 for correct operation.
MR2	U/$\overline{B}$	Unipolar/Bipolar Bit. Set by user to enable unipolar coding; that is, zero differential input results in 000…000 output, and a full-scale differential input results in 111…111 output. Cleared by the user to enable bipolar coding. Negative full-scale differential input results in an output code of 000…000, zero differential input results in an output code of 100…000, and a positive full-scale differential input results in an output code of 111…111.
MR1	1	This bit must be programmed with a Logic 1 for correct operation.
MR0	0	This bit must be programmed with a Logic 0 for correct operation.

Table 12. Operating Modes

MD1	MD0	Mode
0	0	Continuous conversion mode (default)
0	1	Reserved
1	0	Single conversion mode
1	1	Power-down mode

DATA REGISTER

(RS1, RS0 = 1, 1; Power-On/Reset = 0x0000 for the AD7788 and 0x000000 for the AD7789)

The conversion result from the ADC is stored in this data register. This is a read only register. On completion of a read operation from this register, the $\overline{RDY}$ bit/pin is set.

ADC CIRCUIT INFORMATION

The AD7788/AD7789 are low power ADCs that incorporate a Σ-Δ modulator and on-chip digital filtering intended for the measurement of wide dynamic range, low frequency signals, such as those in pressure transducers, weigh scales, and temperature measurement applications. The part has one unbuffered differential input. The device requires an external reference voltage between 0.1 V and V_{DD}. Figure 10 shows the basic connections required to operate the part.

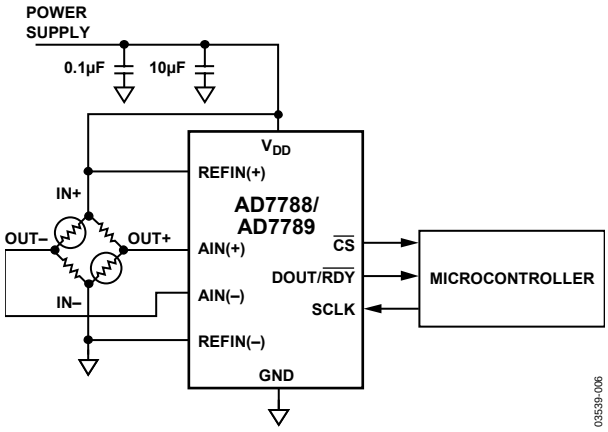


Figure 10. Basic Connection Diagram

The output rate of the AD7788/AD7789 (f_{ADC}) is 16.6 Hz with the settling time equal to $2 \times t_{ADC}$ (120.4 ms). Normal-mode rejection is the major function of the digital filter. Simultaneous 50 Hz and 60 Hz rejection is optimized as notches are placed at both 50 Hz and 60 Hz with this update rate (see Figure 6).

NOISE PERFORMANCE

Typically, the devices have an rms noise of 1.5 µV rms that corresponds to a peak-to-peak resolution of 16 bits for the AD7788 and 19 bits (equivalent to an effective resolution of 21.5 bits) for the AD7789. These numbers are for the bipolar input range with a reference of 2.5 V. The noise was measured with a differential input voltage of 0 V. The peak-to-peak resolution figures represent the resolution for which there is no code flicker within a six-sigma limit. The output noise comes from two sources. The first is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. The second is quantization noise, added when the analog input is converted into the digital domain.

DIGITAL INTERFACE

As previously outlined, the AD7788/AD7789 programmable functions are controlled using a set of on-chip registers. Data is written to these registers via the serial interface and read access to the on-chip registers is also provided by this interface. All communications with the devices must start with a write to the communications register. After power-on or reset, the devices expect a write to the communications register. The data written to this register determines whether the next operation is a read operation or a write operation, and also determines to which register this read or write operation occurs. Therefore, write access to any of the other registers on the devices begins with a write operation to the communications register followed by a write to the selected register. A read operation from any other register (except when continuous read mode is selected) starts with a write to the communications register followed by a read operation from the selected register.

The AD7788/AD7789 serial interface consists of four signals: $\overline{CS}$, DIN, SCLK, and DOUT/$\overline{RDY}$. The DIN line is used to transfer data into the on-chip registers and DOUT/$\overline{RDY}$ is used for accessing data from the on-chip registers. SCLK is the serial clock input for the device, and all data transfers (either on DIN or DOUT/$\overline{RDY}$) occur with respect to the SCLK signal. The DOUT/ $\overline{RDY}$ pin operates as a data ready signal also, the line goes low when a new data-word is available in the output register. It is reset high when a read operation from the data register is complete. It also goes high prior to the data register update to indicate when not to read from the device; this ensures that a data read is not attempted while the register is being updated. $\overline{CS}$ is used to select a device. It can be used to decode the AD7788/AD7789 in systems where several components are connected to the serial bus.

Figure 3 and Figure 4 show timing diagrams for interfacing to the AD7788/AD7789 with $\overline{CS}$ being used to decode the devices. Figure 3 shows the timing for a read operation from the output shift register, while Figure 4 shows the timing for a write operation to the input shift register. In all modes except continuous read mode, it is possible to read the same word from the data register several times even though the DOUT/$\overline{RDY}$ line returns high after the first read operation. However, care must be taken to ensure that the read operations have been completed before the next output update occurs. In continuous read mode, the data register can be read only once.

The serial interface can operate in 3-wire mode by tying $\overline{CS}$ low. In this case, the SCLK, DIN, and DOUT/$\overline{RDY}$ lines are used to communicate with the AD7788/AD7789. The end of conversion can be monitored using the $\overline{RDY}$ bit in the status register. This scheme is suitable for interfacing to microcontrollers. If $\overline{CS}$ is required as a decoding signal, it can be generated from a port pin. For microcontroller interfaces, it is recommended that SCLK idles high between data transfers.

The AD7788/AD7789 can operate with $\overline{CS}$ being used as a frame synchronization signal. This scheme is useful for DSP interfaces. In this case, the first bit (MSB) is effectively clocked out by $\overline{CS}$, because $\overline{CS}$ normally occurs after the falling edge of SCLK in DSPs. The SCLK can continue to run between data transfers, provided the timing numbers are obeyed.

The serial interface can be reset by writing a series of 1s on the DIN input. If a Logic 1 is written to the AD7788/AD7789 for at least 32 serial clock cycles, the serial interface is reset. This ensures that the interface can be reset to a known state if the interface gets lost due to a software error or a glitch in the system. Reset returns the interface to the state in which it is expecting a write to the communications register. This operation resets the contents of all registers to their power-on values.

The AD7788/AD7789 can be configured to continuously convert or to perform a single conversion. See Figure 11 through Figure 13.

Single Conversion Mode

In single-conversion mode, the AD7788/AD7789 are placed in power-down mode between conversions. When a single conversion is initiated by setting MD1 to 1 and MD0 to 0 in the mode register, the AD7788/AD7789 power up, perform a single conversion, and then return to power-down mode. The devices require 1 ms to power up and settle. The AD7788/AD7789 then perform a conversion, requiring a time period of $2 \times t_{ADC}$. DOUT/$\overline{RDY}$ goes low to indicate the completion of a conversion.

When the data-word has been read from the data register, DOUT/$\overline{RDY}$ goes high. If $\overline{CS}$ is low, DOUT/$\overline{RDY}$ remains high until another conversion is initiated and completed. The data register can be read several times, if required, even when DOUT/ $\overline{RDY}$ has gone high.

Continuous Conversion Mode

This is the default power-up mode. The AD7788/AD7789 continuously convert, the $\overline{RDY}$ pin in the status register going low each time a conversion is complete. If $\overline{CS}$ is low, the DOUT/$\overline{RDY}$ line also goes low when a conversion is complete. To read a conversion, the user can write to the communications register, indicating that the next operation is a read of the data register. The digital conversion is placed on the DOUT/$\overline{RDY}$ pin as soon as SCLK pulses are applied to the ADC. DOUT/ $\overline{RDY}$ returns high when the conversion is read. The user can read this register additional times, if required. However, the user must ensure that the data register is not being accessed at the completion of the next conversion or else the new conversion word is lost.

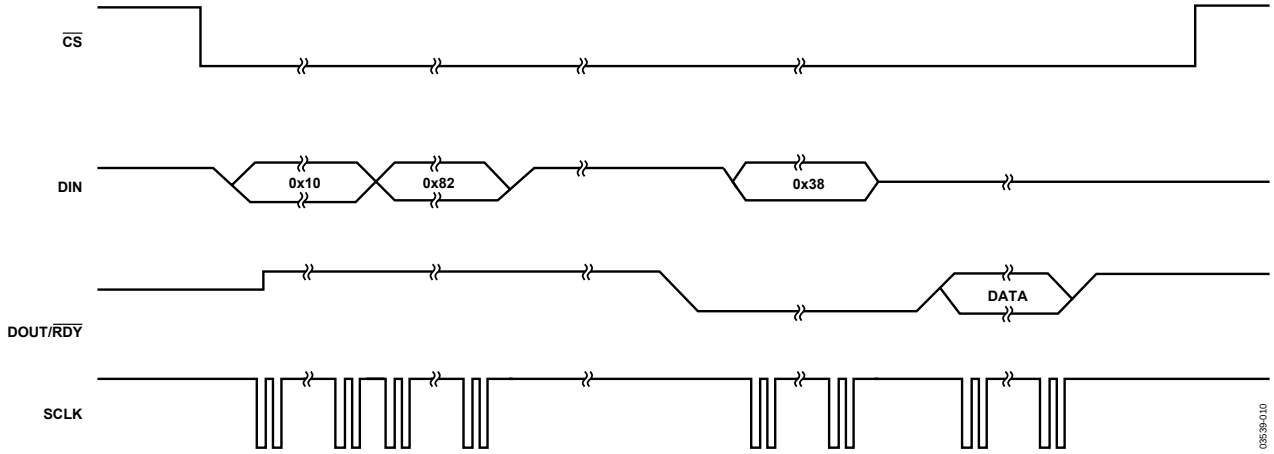


Figure 11. Single Conversion

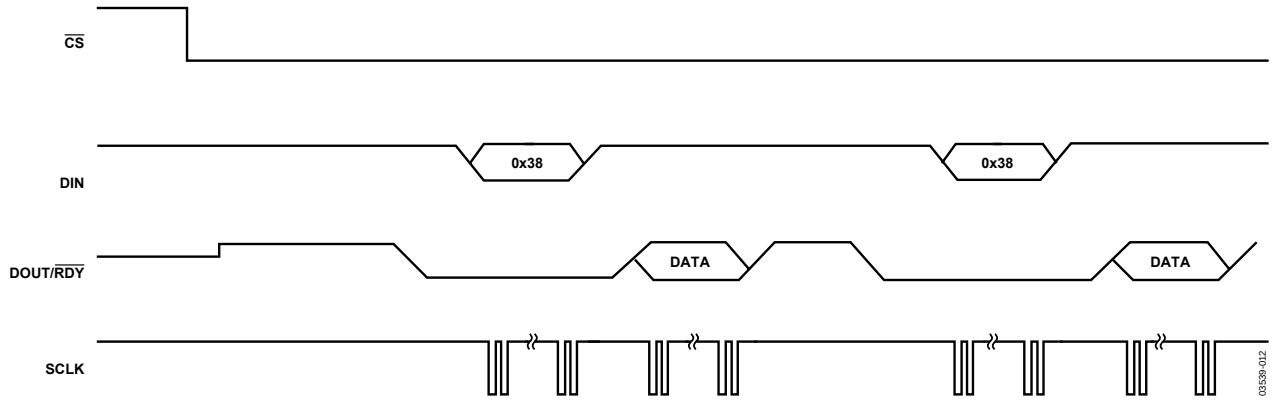


Figure 12. Continuous-Conversion Mode

Continuous Read Mode

Rather than write to the communications register each time a conversion is complete to access the data, the AD7788/AD7789 can be placed in continuous read mode. By writing 001111XX to the communications register, the user needs only to apply the appropriate number of SCLK cycles to the ADC and the data-word is automatically placed on the DOUT/$\overline{\text{RDY}}$ line when a conversion is complete.

When DOUT/$\overline{\text{RDY}}$ goes low to indicate the end of a conversion, sufficient SCLK cycles must be applied to the ADC and the data conversion is placed on the DOUT/$\overline{\text{RDY}}$ line. When the conversion is read, DOUT/$\overline{\text{RDY}}$ returns high until the next conversion is available. In this mode, the data can be read only once. Also, the user must ensure that the data-word is read before the next conversion is complete.

If the data-word has not read the conversion before the completion of the next conversion, or if insufficient serial clocks are applied to the AD7788/AD7789 to read the word, the serial output register is reset when the next conversion is complete and the new conversion is placed in the output serial register.

To exit continuous read mode, the instruction 001110XX must be written to the communications register while the DOUT/$\overline{\text{RDY}}$ pin is low. While in continuous read mode, the ADC monitors activity on the DIN line so that it can receive the instruction to exit continuous read mode. Additionally, a reset occurs if 32 consecutive 1s are seen on DIN. Therefore, DIN should be held low in continuous read mode until an instruction is to be written to the device.

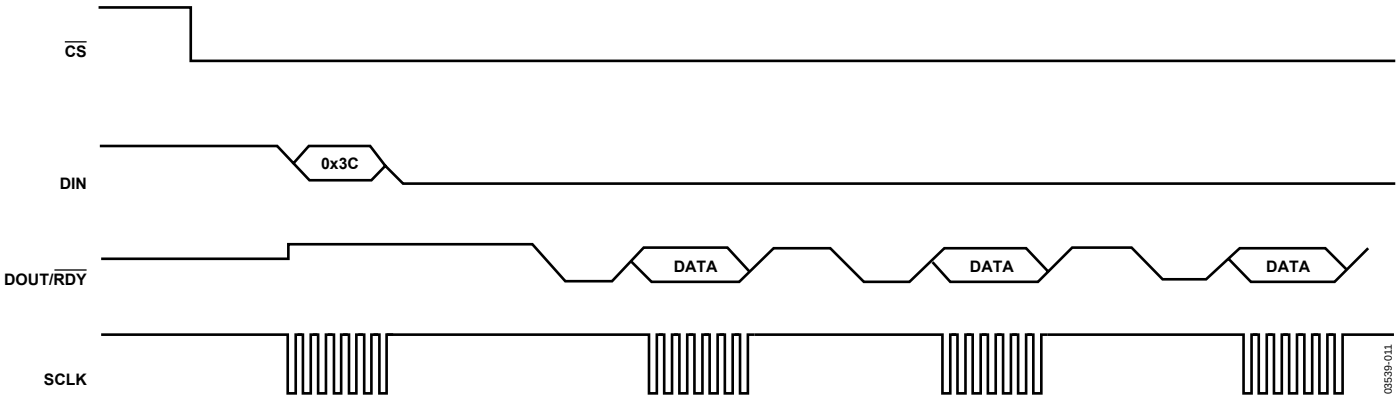


Figure 13. Continuous-Read Mode

CIRCUIT DESCRIPTION

ANALOG INPUT CHANNEL

The AD7788/AD7789 have one differential analog input channel that is connected to the modulator, thus, the input is unbuffered. Note that this unbuffered input path provides a dynamic load to the driving source. Therefore, resistor/capacitor combinations on the input pins can cause dc gain errors, depending on the output impedance of the source that is driving the ADC input. Table 13 shows the allowable external resistance/capacitance values such that no gain error at the 16-bit level is introduced (AD7788). Table 14 shows the allowable external resistance/capacitance values such that no gain error at the 20-bit level is introduced (AD7789).

Table 13. External R-C Combination for No 16-Bit Gain Error (AD7788)

C (pF)	R (Ω)
50	22.8 k
100	13.1 k
500	3.3 k
1000	1.8 k
5000	360

Table 14. External R-C Combination for No 20-Bit Gain Error (AD7789)

C (pF)	R (Ω)
50	16.7 k
100	9.6 k
500	2.2 k
1000	1.1 k
5000	160

The absolute input voltage includes the range between GND − 30 mV and V_{DD} + 30 mV. The negative absolute input voltage limit does allow the possibility of monitoring small true bipolar signals with respect to GND.

BIPOLAR/UNIPOLAR CONFIGURATION

The analog input to the devices can accept either unipolar or bipolar input voltage ranges. A bipolar input range does not imply that the parts can tolerate large negative voltages with respect to system GND. Unipolar and bipolar signals on the AIN(+) input are referenced to the voltage on the AIN(−) input. For example, if AIN(−) is 2.5 V and the ADC is configured for unipolar mode, the input voltage range on the AIN(+) pin is 2.5 V to 5 V. If the ADC is configured for bipolar mode, the analog input range on the AIN(+) input is 0 V to 5 V. The bipolar/unipolar option is chosen by programming the U/$\overline{B}$ bit in the mode register.

DATA OUTPUT CODING

When the ADC is configured for unipolar operation, the output code is natural (straight) binary with a zero differential input voltage resulting in a code of 000...000, a midscale voltage resulting in a code of 100...000, and a full-scale input voltage resulting in a code of 111...111. The output code for any analog input voltage can be represented as

$$Code = 2^N \times (AIN/V_{REF})$$

When the ADC is configured for bipolar operation, the output code is offset binary with a negative full-scale voltage resulting in a code of 000...000, a zero differential input voltage resulting in a code of 100...000, and a positive full-scale input voltage resulting in a code of 111...111. The output code for any analog input voltage can be represented as

$$Code = 2^{N-1} \times [(AIN/V_{REF}) + 1]$$

where:
AIN is the analog input voltage.
N = 16 for the AD7788, 24 for the AD7789.

REFERENCE INPUT

The AD7788/AD7789 have a fully differential input capability for the channel. The common-mode range for these differential inputs is from GND to V_{DD}. The reference input is unbuffered and, therefore, excessive R-C source impedances introduce gain errors. The reference voltage REFIN [REFIN(+) − REFIN(−)] is 2.5 V nominal, but the AD7788/AD7789 are functional with reference voltages from 0.1 V to V_{DD}. In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference voltage for the parts, the effect of the low frequency noise in the excitation source is removed because the application is ratiometric. If the AD7788/AD7789 are used in a nonratiometric application, a low noise reference should be used.

Recommended 2.5 V reference voltage sources for the AD7788/AD7789 include the ADR381 and ADR391, because they are low noise, low power references. If the analog circuitry uses a 2.5 V power supply, the reference voltage source requires some headroom. In this case, a 2.048 V reference such as the ADR380 or ADR390 can be used. Again, these are low power, low noise references. Also note that the reference inputs provide a high impedance, dynamic load. Because the input impedance of each reference input is dynamic, resistor/capacitor combinations on these inputs can cause dc gain errors, depending on the output impedance of the source that is driving the reference inputs.

Reference voltage sources like those recommended in the previous section (for example, ADR391) typically have low output impedances and are, therefore, tolerant to having decoupling capacitors on REFIN(+) without introducing gain errors in the system. Deriving the reference input voltage across an external resistor means that the reference input sees a significant external source impedance. External decoupling on the REFIN pins is not recommended in this type of circuit configuration.

V_{DD} MONITOR

Along with converting external voltages, the analog input channel can be used to monitor the voltage on the V_{DD} pin. When Bit CH1 and Bit CH0 in the communications register are set to 1, the voltage on the V_{DD} pin is internally attenuated by 5 and the resultant voltage is applied to the Σ-Δ modulator using an internal 1.17 V reference for analog-to-digital conversion. This is useful because variations in the power supply voltage can be monitored.

GROUNDING AND LAYOUT

Because the analog inputs and reference inputs of the ADC are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent common-mode rejection of the part removes common-mode noise on these inputs. The digital filter provides rejection of broadband noise on the power supply, except at integer multiples of the modulator sampling frequency. The digital filter also removes noise from the analog and reference inputs, provided that these noise sources do not saturate the analog modulator. As a result, the AD7788/AD7789 are more immune to noise interference than conventional high resolution converters. However, because the resolution of the AD7788/AD7789 is so high, and the noise levels from the AD7788/AD7789 are so low, care must be taken with regard to grounding and layout.

The printed circuit board that houses the AD7788/AD7789 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. A minimum etch technique is generally best for ground planes because it gives the best shielding.

It is recommended that the AD7788/AD7789 GND pins be tied to the AGND plane of the system. In any layout, it is important that the user consider the flow of currents in the system, ensuring that the return paths for all currents are as close as possible to the paths the currents took to reach their destinations. Avoid forcing digital currents to flow through the AGND sections of the layout.

The AD7788/AD7789 ground plane should be allowed to run under the devices to prevent noise coupling. The power supply lines to the AD7788/AD7789 should use as wide a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but it is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, with signals placed on the solder side.

Good decoupling is important when using high resolution ADCs. V_{DD} should be decoupled with a 10 µF tantalum in parallel with 0.1 µF capacitors to GND. To achieve the best from these decoupling components, they should be placed as close as possible to the device, ideally right up against the device. All logic chips should be decoupled with 0.1 µF ceramic capacitors to DGND.

OUTLINE DIMENSIONS

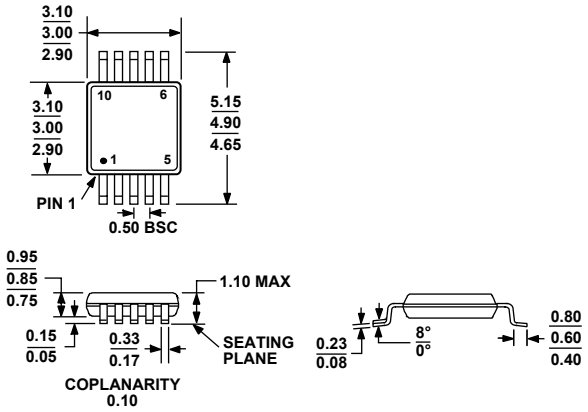


Figure 14. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD7788BRM	−40°C to +105°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	COX
AD7788BRM-REEL	−40°C to +105°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	COX
AD7788BRMZ[1]	−40°C to +105°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	C3G
AD7788BRMZ-REEL[1]	−40°C to +105°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	C3G
AD7788ARM	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	COZ
AD7788ARM-REEL	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	COZ
AD7788ARMZ[1]	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	C4T
AD7789BRM	−40°C to +105°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	COY
AD7789BRM-REEL	−40°C to +105°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	COY
AD7789BRMZ[1]	−40°C to +105°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	C43
AD7789BRMZ-REEL[1]	−40°C to +105°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	C43
EVAL-AD7788EB		Evaluation Board		
EVAL-AD7789EB		Evaluation Board		

[1] Z = Pb-free part.

NOTES

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