# Low Power, 2-Channel 24-Bit Sigma-Delta ADC

Data Sheet **AD7787**

## FEATURES

**Power**
- **Supply: 2.5 V to 5.25 V operation**
- **Normal mode: 75 µA max**
- **Power-down mode: 1 µA max**

**RMS noise: 1.1 µV at 9.5 Hz update rate**
**19.5-bit p-p resolution (22 bits effective resolution)**
**Integral nonlinearity: 3.5 ppm typical**
**Simultaneous 50 Hz and 60 Hz rejection**
**Internal clock oscillator**
**Rail-to-rail input buffer**
**VDD monitor channel**
**Temperature range: −40°C to +105°C**
**10-lead MSOP**

## INTERFACE

**3-wire serial**
**SPI®, QSPI™, MICROWIRE™, and DSP compatible**
**Schmitt trigger on SCLK**

## APPLICATIONS

**Smart transmitters**
**Battery applications**
**Portable instrumentation**
**Sensor measurement**
**Temperature measurement**
**Pressure measurement**
**Weigh scales**
**4 to 20 mA loops**

## GENERAL DESCRIPTION

The AD7787 is a low power, complete analog front end for low frequency measurement applications. It contains a low noise 24-bit Σ-Δ ADC with one differential input and one single-ended input that can be buffered or unbuffered.

The device operates from an internal clock. Therefore, the user does not have to supply a clock source to the device. The output data rate from the part is software programmable and can be varied from 9.5 Hz to 120 Hz, with the rms noise equal to 1.1 µV at the lower update rate. The internal clock frequency can be divided by a factor of 2, 4, or 8, which leads to a reduction in the current consumption. The update rate, cutoff frequency, and settling time scales with the clock frequency.

The part operates with a power supply from 2.5 V to 5.25 V. When operating from a 3 V supply, the power dissipation for the part is 225 µW maximum. It is housed in a 10-lead MSOP.

## FUNCTIONAL BLOCK DIAGRAM

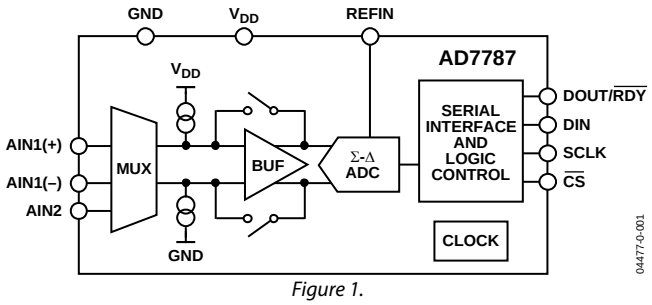



*Figure 1.*


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## REVISION HISTORY

**3/13—Rev. 0 to Rev. A**

Changes to Figure 13 ... 15
Change to Reference Input Section ... 18
Updated Outline Dimensions ... 20
Changes to Ordering Guide ... 20

**4/04—Revision 0: Initial Version**

# SPECIFICATIONS

Temperature range is −40°C to +105°C. $V_{DD}$ = 2.5 V to 5.25 V; REFIN = 2.5 V; GND = 0 V; CDIV1 = CDIV0 = 0; all specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 1.**

| Parameter | AD7787B | Unit | Test Conditions/Comments |
|---|---|---|---|
| ADC CHANNEL SPECIFICATION | | | |
| Output Update Rate | 9.5 | Hz min nom | |
| | 120 | Hz max nom | |
| ADC CHANNEL | | | |
| No Missing Codes[1] | 24 | Bits min | Update rate ≤ 20 Hz. |
| Resolution | 19.5 | Bits p-p | 9.5 Hz update rate. |
| Output Noise | 1.1 | µV rms typ | |
| Integral Nonlinearity | ±15 | ppm of FSR max | 3.5 ppm typ. |
| Offset Error | ±3 | µV typ | |
| Offset Error Drift vs. Temperature | ±10 | nV/°C typ | |
| Full-Scale Error[2] | ±10 | µV typ | |
| Gain Drift vs. Temperature | ±0.5 | ppm/°C typ | |
| Power Supply Rejection | 90 | dB min | 100 dB typ, AIN = 1 V. |
| ANALOG INPUTS | | | |
| Bipolar Input Voltage Range | ±REFIN | V nom | Because AIN2 is single-ended, it can have a negative voltage of 100 mV minimum (see Page 18). |
| Unipolar Voltage Range | 0 to REFIN | V nom | |
| Absolute AIN Voltage Limits[1] | GND + 100 mV | V min | Buffered mode. |
| | $V_{DD}$ − 100 mV | V max | |
| Analog Input Current | | | Buffered mode. |
| Average Input Current[1] | ±1 | nA max | |
| Average Input Current Drift | ±5 | pA/°C typ | |
| Absolute AIN Voltage Limits[1, 3] | GND − 100 mV | V min | Unbuffered mode. |
| | $V_{DD}$ + 30 mV | V max | |
| Analog Input Current | | | Unbuffered mode. Current varies with input voltage. |
| Average Input Current | ±400 | nA/V typ | |
| Average Input Current Drift | ±50 | pA/V/°C typ | |
| Normal Mode Rejection[1] | | | |
| @ 50 Hz, 60 Hz | 65 | dB min | 73 dB typ, 50 ± 1 Hz, 60 ± 1 Hz, FS[2:0] = 100[4]. |
| @ 50 Hz | 80 | dB min | 90 dB typ, 50 ± 1 Hz, FS[2:0] = 101[4]. |
| @ 60 Hz | 80 | dB min | 90 dB typ, 60 ± 1 Hz, FS[2:0] = 011[4]. |
| Common-Mode Rejection (AIN1) | | | AIN = 1 V. |
| @ DC | 90 | dB min | 100 dB typ. |
| @ 50 Hz, 60 Hz[1] | 100 | dB min | 50 ± 1 Hz (FS[2:0] = 101[4]), 60 ± 1 Hz (FS[2:0] = 011[4]). |
| REFERENCE INPUT | | | |
| REFIN Voltage | 2.5 | V nom | |
| Reference Voltage Range[1] | 0.1 | V min | |
| | $V_{DD}$ | V max | |
| Average Reference Input Current | 0.5 | µA/V typ | |
| Average Reference Input Current Drift | ±0.03 | nA/V/°C typ | |
| Normal Mode Rejection[1] | | | |
| @ 50 Hz, 60 Hz | 65 | dB min | 73 dB typ, 50 ± 1 Hz, 60 ± 1 Hz, FS[2:0] = 100[4]. |
| @ 50 Hz | 80 | dB min | 90 dB typ, 50 ± 1 Hz, FS[2:0] = 101[4]. |
| @ 60 Hz | 80 | dB min | 90 dB typ, 60 ± 1 Hz, FS[2:0] = 011[4]. |

| Parameter | AD7787B | Unit | Test Conditions/Comments |
|---|---|---|---|
| LOGIC INPUTS | | | |
| All Inputs Except SCLK[1] | | | |
| $V_{INL}$, Input Low Voltage | 0.8 | V max | $V_{DD}$ = 5 V. |
| | 0.4 | V max | $V_{DD}$ = 3 V. |
| $V_{INH}$, Input High Voltage | 2.0 | V min | $V_{DD}$ = 3 V or 5 V. |
| SCLK Only (Schmitt-Triggered Input)[1] | | | |
| $V_T(+)$ | 1.4/2 | V min/V max | $V_{DD}$ = 5 V. |
| $V_T(-)$ | 0.8/1.4 | V min/V max | $V_{DD}$ = 5 V. |
| $V_T(+) - V_T(-)$ | 0.3/0.85 | V min/V max | $V_{DD}$ = 5 V. |
| $V_T(+)$ | 0.9/2 | V min/V max | $V_{DD}$ = 3 V. |
| $V_T(-)$ | 0.4/1.1 | V min/V max | $V_{DD}$ = 3 V. |
| $V_T(+) - V_T(-)$ | 0.3/0.85 | V min/V max | $V_{DD}$ = 3 V. |
| Input Currents | ±1 | µA max | $V_{IN} = V_{DD}$ or GND. |
| Input Capacitance | 10 | pF typ | All Digital Inputs. |
| LOGIC OUTPUTS | | | |
| $V_{OH}$, Output High Voltage[1] | $V_{DD}$ − 0.6 | V min | $V_{DD}$ = 3 V, $I_{SOURCE}$ = 100 µA. |
| $V_{OL}$, Output Low Voltage[1] | 0.4 | V max | $V_{DD}$ = 3 V, $I_{SINK}$ = 100 µA. |
| $V_{OH}$, Output High Voltage[1] | 4 | V min | $V_{DD}$ = 5 V, $I_{SOURCE}$ = 200 µA. |
| $V_{OL}$, Output Low Voltage[1] | 0.4 | V max | $V_{DD}$ = 5 V, $I_{SINK}$ = 1.6 mA. |
| Floating-State Leakage Current | ±1 | µA max | |
| Floating-State Output Capacitance | 10 | pF typ | |
| Data Output Coding | Offset Binary | | |
| POWER REQUIREMENTS[5] | | | |
| Power Supply Voltage | | | |
| $V_{DD}$ − GND | 2.5/5.25 | V min/max | |
| Power Supply Currents | | | |
| $I_{DD}$ Current[6] | 75 | µA max | 65 µA typ, $V_{DD}$ = 3.6 V, unbuffered mode. |
| | 145 | µA max | 130 µA typ, $V_{DD}$ = 3.6 V, buffered mode. |
| | 80 | µA max | 73 µA typ, $V_{DD}$ = 5.25 V, unbuffered mode. |
| | 160 | µA max | 145 µA typ, $V_{DD}$ = 5.25 V, buffered mode. |
| $I_{DD}$ (Power-Down Mode) | 1 | µA max | |

[1] Specification is not production tested but is supported by characterization data at initial product release.
[2] Full-scale error applies to both positive and negative full scale and applies at the factory calibration conditions ($V_{DD}$ = 4 V).
[3] The AD7787 can tolerate absolute analog input voltages down to GND − 200 mV but the leakage current will increase.
[4] FS[2:0] are the three bits used in the filter register to select the output word rate.
[5] Digital inputs equal to $V_{DD}$ or GND.
[6] The current consumption can be further reduced by using the ADC in one of the low power modes (see Table 14).

# TIMING CHARACTERISTICS

Sample tested during initial release to ensure compliance. All input signals are specified with $t_R = t_F = 5$ ns (10% to 90% of $V_{DD}$) and timed from a voltage level of 1.6 V (see Figure 3 and Figure 4).

$V_{DD}$ = 2.5 V to 5.25 V; GND = 0 V, REFIN = 2.5 V, CDIV1 = CDIV0 = 0, Input Logic 0 = 0 V, Input Logic 1 = $V_{DD}$, unless otherwise noted.

**Table 2.**

| Parameter | Limit at $T_{MIN}$, $T_{MAX}$ (B Version) | Unit | Conditions/Comments |
|---|---|---|---|
| $t_3$ | 100 | ns min | SCLK High Pulse Width |
| $t_4$ | 100 | ns min | SCLK Low Pulse Width |
| Read Operation | | | |
| $t_1$ | 0 | ns min | $\overline{CS}$ Falling Edge to DOUT/$\overline{RDY}$ Active Time |
| | 60 | ns max | $V_{DD}$ = 4.75 V to 5.25 V |
| | 80 | ns max | $V_{DD}$ = 2.5 V to 3.6 V |
| $t_2$[1] | 0 | ns min | SCLK Active Edge to Data Valid Delay[2] |
| | 60 | ns max | $V_{DD}$ = 4.75 V to 5.25 V |
| | 80 | ns max | $V_{DD}$ = 2.5 V to 3.6 V |
| $t_5$[3, 4] | 10 | ns min | Bus Relinquish Time after $\overline{CS}$ Inactive Edge |
| | 80 | ns max | |
| $t_6$ | 100 | ns max | SCLK Inactive Edge to $\overline{CS}$ Inactive Edge |
| $t_7$ | 10 | ns min | SCLK Inactive Edge to DOUT/$\overline{RDY}$ High |
| Write Operation | | | |
| $t_8$ | 0 | ns min | $\overline{CS}$ Falling Edge to SCLK Active Edge Setup Time[2] |
| $t_9$ | 30 | ns min | Data Valid to SCLK Edge Setup Time |
| $t_{10}$ | 25 | ns min | Data Valid to SCLK Edge Hold Time |
| $t_{11}$ | 0 | ns min | $\overline{CS}$ Rising Edge to SCLK Edge Hold Time |

[1] These numbers are measured with the load circuit of Figure 2 and defined as the time required for the output to cross the $V_{OL}$ or $V_{OH}$ limits.
[2] The SCLK active edge is the falling edge of SCLK.
[3] These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and, as such, are independent of external bus loading capacitances.
[4] $\overline{RDY}$ returns high after a read of the ADC. In single conversion mode and continuous conversion mode, the same data can be read again, if required, while $\overline{RDY}$ is high, although care should be taken to ensure that subsequent reads do not occur close to the next output update. In continuous read mode, the digital word can be read only once.

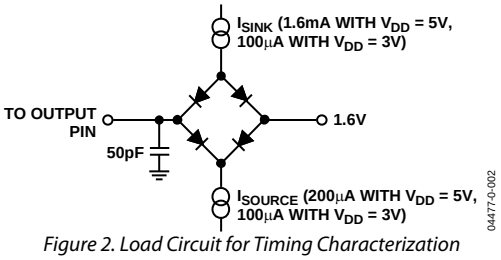



*Figure 2. Load Circuit for Timing Characterization*

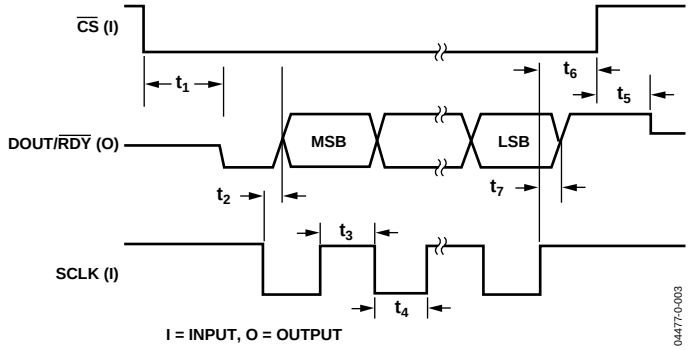



*Figure 3. Read Cycle Timing Diagram*

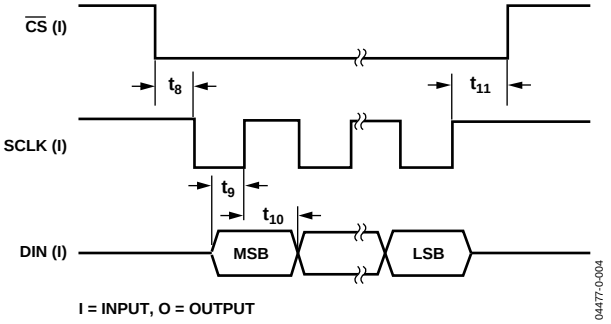



*Figure 4. Write Cycle Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 3.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to GND | −0.3 V to +7 V |
| Analog Input Voltage to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Reference Input Voltage to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Total AIN/REFIN Current (Indefinite) | 30 mA |
| Digital Input Voltage to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Digital Output Voltage to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Operating Temperature Range | −40°C to +105°C |
| Storage Temperature Range | −65°C to +150°C |
| Maximum Junction Temperature | 150°C |
| MSOP | |
| $\theta_{JA}$ Thermal Impedance | 206°C/W |
| $\theta_{JC}$ Thermal Impedance | 44°C/W |
| Lead Temperature, Soldering (10 sec) | 300°C |
| IR Reflow, Peak Temperature | 220°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

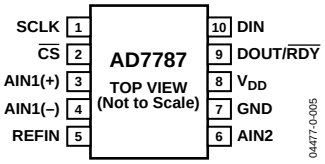



*Figure 5. Pin Configuration*

**Table 4. Pin Function Descriptions**

| Pin No. | Mnemonic | Function |
|---|---|---|
| 1 | SCLK | Serial Clock Input for Data Transfers to and from the ADC. The SCLK has a Schmitt-triggered input, making the interface suitable for opto-isolated applications. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to or from the ADC in smaller batches of data. |
| 2 | $\overline{CS}$ | Chip Select Input. This is an active low logic input used to select the ADC. $\overline{CS}$ can be used to select the ADC in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the device. $\overline{CS}$ can be hardwired low, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT used to interface with the device. |
| 3 | AIN1(+) | Analog Input. AIN1(+) is the positive terminal of the differential analog input pair AIN1(+)/AIN1(–). |
| 4 | AIN1(–) | Analog Input. AIN1(–) is the negative terminal of the differential analog input pair AIN1(+)/AIN1(–). |
| 5 | REFIN | Reference Input. REFIN can be anywhere between $V_{DD}$ and GND + 0.1 V. The nominal reference voltage is 2.5 V, but the part functions with a reference from 0.1 V to $V_{DD}$. |
| 6 | AIN2 | Analog Input. AIN2 is a single-ended analog input. |
| 7 | GND | Ground Reference Point. |
| 8 | $V_{DD}$ | Supply Voltage, 2.5 V to 5.25 V. |
| 9 | DOUT/$\overline{RDY}$ | Serial Data Output/Data Ready Output. DOUT/$\overline{RDY}$ serves a dual purpose. It functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. In addition, DOUT/$\overline{RDY}$ operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin will go high before the next update occurs. The DOUT/$\overline{RDY}$ falling edge can be used as an interrupt to a processor, indicating that valid data is available. With an external serial clock, the data can be read using the DOUT/$\overline{RDY}$ pin. With $\overline{CS}$ low, the data/control word information is placed on the DOUT/$\overline{RDY}$ pin on the SCLK falling edge and is valid on the SCLK rising edge. The end of a conversion is also indicated by the $\overline{RDY}$ bit in the status register. When $\overline{CS}$ is high, the DOUT/$\overline{RDY}$ pin is three-stated, but the $\overline{RDY}$ bit remains active. |
| 10 | DIN | Serial Data Input to the Input Shift Register on the ADC. Data in this shift register is transferred to the control registers within the ADC; the register selection bits of the communications register identifying the appropriate register. |

# TYPICAL PERFORMANCE CHARACTERISTICS

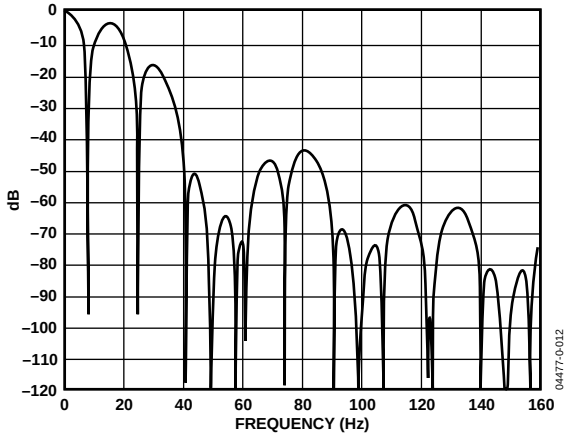



Figure 6. Frequency Response with 16.6 Hz Update Rate

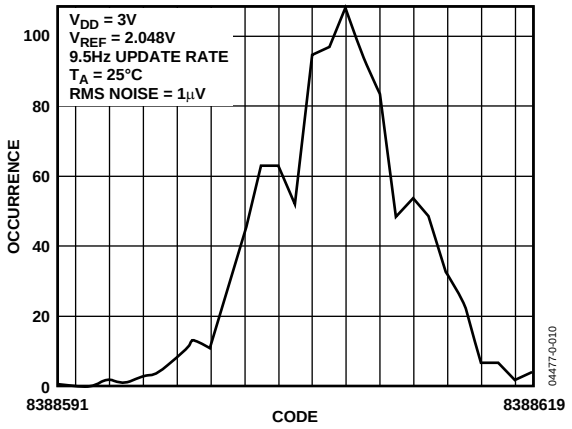



Figure 7. Noise Distribution Histogram (CDIV1 = CDIV0 = 0)

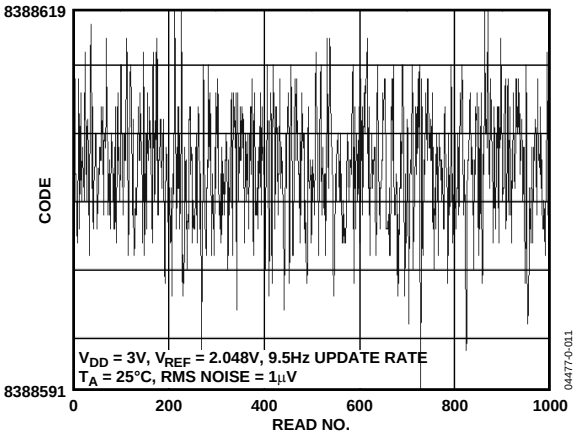



Figure 8. Typical Noise Plot with 16.6 Hz Update Rate (CDIV1 = CD1V0 = 0)

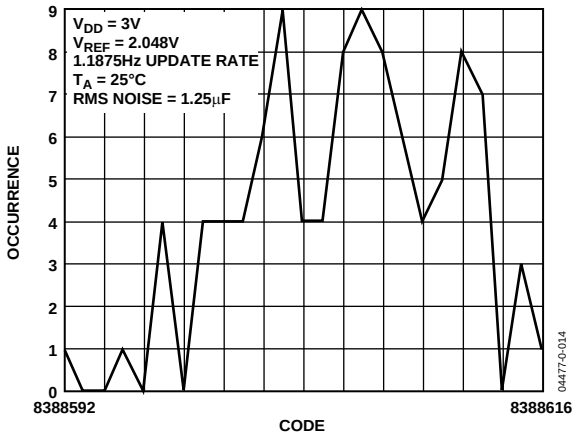



Figure 9. Noise Histogram for Clock Divide-by-8 Mode (CDIV0 = CDIV1 = 1)

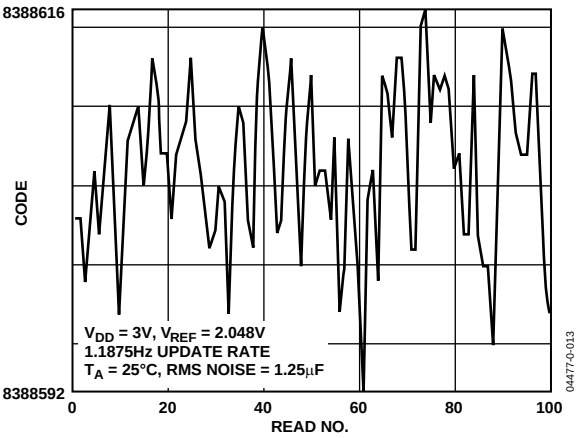



Figure 10. Noise Plot in Clock Divide-by-8 Mode (CDIV0 = CDIV1 = 1)

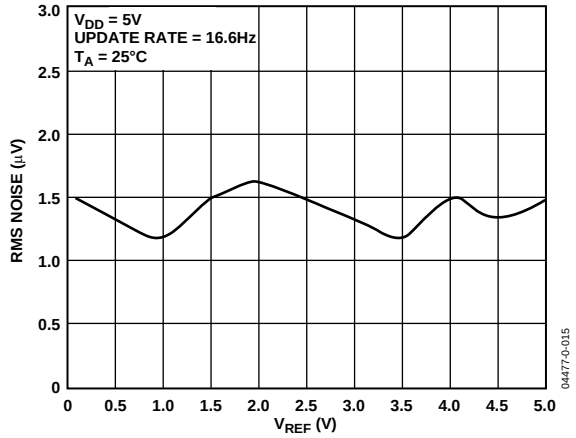



Figure 11. RMS Noise vs. Reference Voltage

# ON-CHIP REGISTERS

The ADC is controlled and configured via a number of on-chip registers, which are described on the following pages. In the following descriptions, *set* implies a Logic 1 state and *cleared* implies a Logic 0 state, unless otherwise noted.

## COMMUNICATIONS REGISTER (RS1, RS0 = 0, 0)

The communications register is an 8-bit write-only register. All communications to the part must start with a write operation to the communications register. The data written to the communications register determines whether the next operation is a read or write operation and to which register this operation takes place. For read or write operations, once the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the communications register. This is the default state of the interface and, on power-up or after a reset, the ADC is in this default state waiting for a write operation to the communications register. In situations where the interface sequence is lost, a write operation of at least 32 serial clock cycles with DIN high returns the ADC to this default state by resetting the entire part.

Table 5 outlines the bit designations for the communications register. CR0 through CR7 indicate the bit location, CR denoting the bits are in the communications register. CR7 denotes the first bit of the data stream. The number in the parenthesis indicates the power-on/reset default status of that bit.

| CR7 | CR6 | CR5 | CR4 | CR3 | CR2 | CR1 | CR0 |
|---|---|---|---|---|---|---|---|
| $\overline{\text{WEN}}$ (0) | 0 (0) | RS1 (0) | RS0 (0) | R/$\overline{\text{W}}$ (0) | CREAD (0) | CH1 (0) | CH0 (0) |

**Table 5. Communications Register Bit Designations**

| Bit Location | Bit Name | Description |
|---|---|---|
| CR7 | $\overline{\text{WEN}}$ | Write Enable Bit. A 0 must be written to this bit so that the write to the communications register actually occurs. If a 1 is the first bit written, the part does not clock on to subsequent bits in the register. It stays at this bit location until a 0 is written to this bit. Once a 0 is written to the WEN bit, the next seven bits are loaded to the communications register. |
| CR6 | 0 | This bit must be programmed to Logic 0 for correct operation. |
| CR5 to CR4 | RS1 to RS0 | Register Address Bits. These address bits are used to select which of the ADC's registers are being selected during this serial interface communication (see Table 6). |
| CR3 | R/$\overline{\text{W}}$ | A 0 in this bit location indicates that the next operation is a write to a specified register. A 1 in this position indicates that the next operation is a read from the designated register. |
| CR2 | CREAD | Continuous Read of the Data Register. When this bit is set to 1 (and the data register is selected), the serial interface is configured so that the data register can be continuously read, i.e., the contents of the data register are placed on the DOUT pin automatically when the SCLK pulses are applied. The communications register does not have to be written to for data reads. To enable continuous read mode, the instruction 00111100 (Channel AIN1) or 00111101 (Channel AIN2) must be written to the communications register. To exit the continuous read mode, the instruction 001110XX must be written to the communications register while the $\overline{\text{RDY}}$ pin is low. While in continuous read mode, the ADC monitors activity on the DIN line so that it can receive the instruction to exit continuous read mode. Additionally, a reset occurs if 32 consecutive 1s are seen on DIN. Therefore, DIN should be held low in continuous read mode until an instruction is to be written to the device. |
| CR1 to CR0 | CH1 to CH0 | These bits are used to select the analog input channel. Channel AIN1 or AIN2 can be selected or an internal short (AIN1(–)/AIN1(–)) can be selected. Alternatively, the power supply can be selected, i.e., the ADC can measure the voltage on the power supply, which is useful for monitoring power supply variation. To perform this measurement, the power supply voltage is divided by 5 and then applied to the modulator for conversion. The ADC uses a 1.17 V ± 5% on-chip reference as the reference source when this channel is selected. Any change in channel resets the filter and a new conversion is started. |

**Table 6. Register Selection**

| RS1 | RS0 | Register | Register Size |
|---|---|---|---|
| 0 | 0 | Communications Register during a Write Operation | 8-Bit |
| 0 | 0 | Status Register during a Read Operation | 8-Bit |
| 0 | 1 | Mode Register | 8-Bit |
| 1 | 0 | Filter Register | 8-Bit |
| 1 | 1 | Data Register | 24-Bit |

**Table 7. Channel Selection**

| CH1 | CH0 | Channel |
|---|---|---|
| 0 | 0 | AIN1(+) – AIN1(–) |
| 0 | 1 | AIN2 |
| 1 | 0 | AIN1(–) – AIN1(–) |
| 1 | 1 | $V_{DD}$ Monitor |

## STATUS REGISTER (RS1, RS0 = 0, 0; POWER-ON/RESET = 0×8C)

The status register is an 8-bit read-only register. To access the ADC status register, the user must write to the communications register, select the next operation to be a read, and load Bits RS1 and RS0 with 0s. Table 8 outlines the bit designations for the status register. SR0 through SR7 indicate the bit locations, SR denoting the bits are in the status register. SR7 denotes the first bit of the data stream. The number in the parenthesis indicates the power-on/reset default status of that bit.

| SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 |
|---|---|---|---|---|---|---|---|
| $\overline{\text{RDY}}$ (1) | ERR (0) | 0 (0) | 0 (0) | 1 (1) | 1 (1) | CH1 (0) | CH0 (0) |

**Table 8. Status Register Bit Designations**

| Bit Location | Bit Name | Description |
|---|---|---|
| SR7 | $\overline{\text{RDY}}$ | Ready Bit for ADC. *Cleared* when data is written to the ADC data register. The $\overline{\text{RDY}}$ bit is *set* automatically after the ADC data register has been read or a period of time before the data register is updated with a new conversion result to indicate to the user not to read the conversion data. It is also *set* when the part is placed in power-down mode. The end of a conversion is indicated by the DOUT/$\overline{\text{RDY}}$ pin also. This pin can be used as an alternative to the status register for monitoring the ADC for conversion data. |
| SR6 | ERR | ADC Error Bit. This bit is written to at the same time as the $\overline{\text{RDY}}$ bit. Set to indicate that the result written to the ADC data register has been clamped to all 0s or all 1s. Error sources include overrange, underrange. *Cleared* by a write operation to start a conversion. |
| SR5 to SR4 | 0 | These bits are automatically *cleared*. |
| SR3 to SR2 | 1 | These bits are automatically *set*. |
| SR1 to SR0 | CH1 to CH0 | These bits indicate which channel is being converted by the ADC. |

## MODE REGISTER (RS1, RS0 = 0, 1; POWER-ON/RESET = 0×02)

The mode register is an 8-bit register from which data can be read or to which data can be written. This register is used to configure the ADC for unipolar or bipolar mode, to enable or disable the buffer, or to place the device into power-down mode. Table 9 outlines the bit designations for the mode register. MR0 through MR7 indicate the bit locations, MR denoting the bits are in the mode register. MR7 denotes the first bit of the data stream. The number in the parenthesis indicates the power-on/reset default status of that bit. Any write to the setup register resets the modulator and filter and sets the $\overline{RDY}$ bit.

| MR7 | MR6 | MR5 | MR4 | MR3 | MR2 | MR1 | MR0 |
|---|---|---|---|---|---|---|---|
| MD1 (0) | MD0 (0) | 0 (0) | 0 (0) | BO (0) | U/$\overline{B}$ (0) | BUF (1) | 0 (0) |

**Table 9. Mode Register Bit Designations**

| Bit Location | Bit Name | Description |
|---|---|---|
| MR7 to MR6 | MD1 to MD0 | Mode Select Bits. These bits select between continuous conversion mode, single conversion mode, and standby mode. In continuous conversion mode, the ADC continuously performs conversions and places the result in the data register. $\overline{RDY}$ goes low when a conversion is complete. The user can read these conversions by placing the device in continuous read mode whereby the conversions are automatically placed on the DOUT line when SCLK pulses are applied. Alternatively, the user can instruct the ADC to output the conversion by writing to the communications register. After power-on, the first conversion is available after a period $2/f_{ADC}$ while subsequent conversions are available at a frequency of $f_{ADC}$. In single conversion mode, the ADC is placed in power-down mode when conversions are not being performed. When single conversion mode is selected, the ADC powers up and performs a single conversion, which occurs after a period $2/f_{ADC}$. The conversion result is placed in the data register, $\overline{RDY}$ goes low, and the ADC returns to power-down mode. The conversion remains in the data register and $\overline{RDY}$ remains active (low) until the data is read or another conversion is performed (see Table 10). |
| MR5 to MR4 | 0 | These bits must be programmed with a Logic 0 for correct operation. |
| MR3 | BO | Burnout Current Enable Bit. When this bit is set to 1 by the user, the 100 nA current sources in the signal path are enabled. When BO = 0, the burnout currents are disabled. The burnout currents can be enabled only when the buffer is active. |
| MR2 | U/$\overline{B}$ | Unipolar/Bipolar Bit. *Set* by user to enable unipolar coding, i.e., zero differential input results in 0x000000 output and a full-scale differential input results in 0xFFFFFF output. *Cleared* by the user to enable bipolar coding. Negative full-scale differential input results in an output code of 0x000000, zero differential input results in an output code of 0x800000, and a positive full-scale differential input will result in an output code of 0xFFFFFF. |
| MR1 | BUF | Configures the AD7787 for buffered or unbuffered mode of operation. If *cleared*, the ADC operates in unbuffered mode, lowering the power consumption of the device. If set, the device operates in buffered mode, allowing the user to place source impedances on the front end without contributing gain errors to the system. |
| MR0 | 0 | This bit must be programmed with a Logic 0 for correct operation. |

**Table 10. Operating Modes**

| MD1 | MD0 | Mode |
|---|---|---|
| 0 | 0 | Continuous Conversion Mode (Default) |
| 0 | 1 | Reserved |
| 1 | 0 | Single Conversion Mode |
| 1 | 1 | Power-Down Mode |

## FILTER REGISTER (RS1, RS0 = 1, 0; POWER-ON/RESET = 0×04)

The filter register is an 8-bit register from which data can be read or to which data can be written. This register is used to set the output word rate. Table 11 outlines the bit designations for the filter register. FR0 through FR7 indicate the bit locations, FR denoting the bits are in the filter register. FR7 denotes the first bit of the data stream. The number in the parenthesis indicates the power-on/reset default status of that bit.

| FR7 | FR6 | FR5 | FR4 | FR3 | FR2 | FR1 | FR0 |
|---|---|---|---|---|---|---|---|
| 0 (0) | 0 (0) | CDIV1 (0) | CDIV0 (0) | 0 (0) | FS2 (1) | FS1 (0) | FS0 (0) |

**Table 11. Filter Register Bit Designations**

| Bit Location | Bit Name | Description |
|---|---|---|
| FR7 to FR6 | 0 | These bits must be programmed with a Logic 0 for correct operation. |
| FR5 to FR4 | CLKDIV1 to CDIV0 | These bits are used to operate the AD7787 in the lower power modes. The clock is internally divided and the power is reduced. In the low power modes, the update rates will scale with the clock frequency so that dividing the clock by 2 causes the update rate to be reduced by a factor of 2 also.<br>00 Normal Mode<br>01 Clock Divided by 2<br>10 Clock Divided by 4<br>11 Clock Divided by 8 |
| FR3 | 0 | This bit must be programmed with a Logic 0 for correct operation. |
| FR2 to FR0 | FS2 to FS0 | These bits set the output word rate of the ADC. The update rate influences the 50 Hz/60 Hz rejection and the noise. Table 12 shows the allowable update rates when normal power mode is used. In the low power modes, the update rate is scaled with the clock frequency. For example, if the internal clock is divided by a factor of 2, the corresponding update rates are divided by 2 also. |

**Table 12. Update Rates**

| FS2 | FS1 | FS0 | $f_{ADC}$ (Hz) | f3dB (Hz) | RMS Noise (μV) | Rejection |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 120 | 28 | 40 | 25 dB @ 60 Hz |
| 0 | 0 | 1 | 100 | 24 | 25 | 25 dB @ 50 Hz |
| 0 | 1 | 0 | 33.3 | 8 | 3.36 | |
| 0 | 1 | 1 | 20 | 4.7 | 1.6 | 80 dB @ 60 Hz |
| **1** | **0** | **0** | **16.6** | **4** | **1.5** | **65 dB @ 50 Hz/60 Hz (Default Setting)** |
| 1 | 0 | 1 | 16.7 | 4 | 1.5 | 80 dB @ 50 Hz |
| 1 | 1 | 0 | 13.3 | 3.2 | 1.2 | |
| 1 | 1 | 1 | 9.5 | 2.3 | 1.1 | 67 dB @ 50 Hz/60 Hz |

## DATA REGISTER (RS1, RS0 = 1, 1; POWER-ON/RESET = 0×000000)

The conversion result from the ADC is stored in this data register. This is a read-only register. On completion of a read operation from this register, the $\overline{RDY}$ bit/pin is set.

# ADC CIRCUIT INFORMATION

## OVERVIEW

The AD7787 is a low power ADC that incorporates an Σ-Δ modulator, a buffer, and an on-chip digital filter intended for the measurement of wide dynamic range, low frequency signals, such as those in pressure transducers, weigh scales, and temperature measurement applications.

The part has one differential input and one single-ended input. The inputs can be operated in buffered or unbuffered mode. Buffering the input channel means that the part can accommodate significant source impedances on the analog input .The device requires an external reference of 2.5 nominal. Figure 12 shows the basic connections required to operate the part.

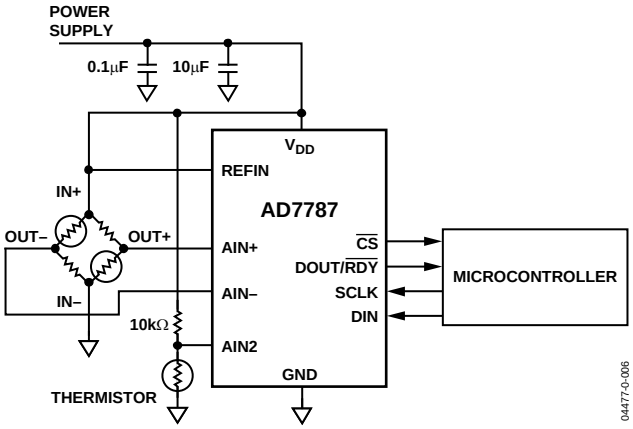



*Figure 12. Basic Connection Diagram*

The output rate of the AD7787 ($f_{ADC}$) is user programmable with the settling time equal to $2 \times t_{ADC}$. Normal mode rejection is the major function of the digital filter. Table 12 lists the available update rates from the AD7787. Simultaneous 50 Hz and 60 Hz rejection is optimized when the update rate equals 16.6 Hz as notches are placed at both 50 Hz and 60 Hz with this update rate (see Figure 6).

## NOISE PERFORMANCE

Table 13 shows the output rms noise, rms resolution, and peak-to-peak resolution (rounded to the nearest 0.5 LSB) for the different update rates and input ranges for the AD7787. The numbers given are for the bipolar input range with a reference of 2.5 V. These numbers are typical and generated with a differential input voltage of 0 V. The peak-to-peak resolution figures represent the resolution for which there is no code flicker within a six-sigma limit. The output noise comes from two sources. The first is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. The second is quantization noise, which is added when the analog input is converted into the digital domain. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source.

**Table 13. Typical Peak-to-Peak Resolution (Effective Resolution) vs. Update Rate**

| Update Rate | Peak-to-Peak Resolution | Effective Resolution |
|---|---|---|
| 9.5 | 19.5 | 22 |
| 13.3 | 19 | 21.5 |
| 16.7 | 19 | 21.5 |
| 16.6 | 19 | 21.5 |
| 20 | 18.5 | 21 |
| 33.3 | 17.5 | 20 |
| 100 | 14.5 | 17 |
| 120 | 14 | 16.5 |

## REDUCED CURRENT MODES

The AD7787 has a current consumption of 160 µA maximum when operated with a 5 V power supply, the buffer enabled, and the clock operating at its maximum speed. The clock frequency can be divided by a factor of 2, 4, or 8 before being applied to the modulator and filter, resulting in a reduction in the current consumption of the AD7787. Bits CDIV1 and CDIV0 in the filter register are used to enter these low power modes (see Table 14).

When the internal clock is reduced, the update rate is also reduced. For example, if the filter bits are set to give an update rate of 16.6 Hz when the AD7787 is operated in full power mode, the update rate equals 8.3 Hz in divide-by-2 mode. In the low power modes, there may be some degradation in the ADC performance.

**Table 14. Low Power Mode Selection**

| CDIV[1:0] | Clock | Typ Current, Buffered (µA) | Typ Current, Unbuffered (µA) | 50 Hz/60 Hz Rejection (dB) |
|---|---|---|---|---|
| 00 | 1 | 146 | 75 | 65 |
| 10 | 1/2 | 87 | 45 | 64 |
| 10 | 1/4 | 56 | 30 | 75 |
| 11 | 1/8 | 41 | 25 | 86 |

## DIGITAL INTERFACE

As previously outlined, the AD7787's programmable functions are controlled using a set of on-chip registers. Data is written to these registers via the part's serial interface and read access to the on-chip registers is also provided by this interface. All communications with the part must start with a write to the communications register. After power-on or reset, the device expects a write to its communications register. The data written to this register determines whether the next operation is a read operation or a write operation and also determines to which register this read or write operation occurs. Therefore, write access to any of the other registers on the part begins with a write operation to the communications register followed by a write to the selected register. A read operation from any other register (except when continuous read mode is selected) starts with a write to the communications register followed by a read operation from the selected register.

The AD7787's serial interface consists of four signals: $\overline{CS}$, DIN, SCLK, and DOUT/$\overline{RDY}$. The DIN line is used to transfer data into the on-chip registers while DOUT/$\overline{RDY}$ is used for accessing data from the on-chip registers. SCLK is the serial clock input for the device and all data transfers (either on DIN or DOUT/$\overline{RDY}$) occur with respect to the SCLK signal.

The DOUT/ $\overline{RDY}$ pin operates as a data-ready signal as well as a DOUT pin. Each time a conversion is available in the output register, DOUT/$\overline{RDY}$ goes low. DOUT/$\overline{RDY}$ resets high when a read operation from the data register is completed. It also goes high prior to the updating of the data register to indicate when not to read from the device to ensure that a data read is not attempted while the register is being updated. $\overline{CS}$ is used to select a device. It can be used to decode the AD7787 in systems where several components are connected to the serial bus.

Figure 3 and Figure 4 show timing diagrams for interfacing to the AD7787 with $\overline{CS}$ being used to decode the part. Figure 3 shows the timing for a read operation from the AD7787's output shift register, while Figure 4 shows the timing for a write operation to the input shift register. In all modes, except continuous read mode, it is possible to read the same word from the data register several times even though the DOUT/$\overline{RDY}$ line returns high after the first read operation. However, care must be taken to ensure that the read operations have been completed before the next output update occurs. In continuous read mode, the data register can only be read once.

The serial interface can operate in 3-wire mode by tying $\overline{CS}$ low. In this case, the SCLK, DIN, and DOUT/$\overline{RDY}$ lines are used to communicate with the AD7787. The end of the conversion can be monitored using the $\overline{RDY}$ bit in the status register. This scheme is suitable for interfacing to microcontrollers. If $\overline{CS}$ is required as a decoding signal, it can be generated from a port pin. For microcontroller interfaces, it is recommended that SCLK idle high between data transfers.

The AD7787 can be operated with $\overline{CS}$ being used as a frame synchronization signal. This scheme is useful for DSP interfaces. In this case, the first bit (MSB) is effectively clocked out by $\overline{CS}$, because $\overline{CS}$ would normally occur after the falling edge of SCLK in DSPs. The SCLK can continue to run between data transfers, provided the timing numbers are obeyed.

The serial interface can be reset by writing a series of 1s to the DIN input. If a Logic 1 is written to the AD7787 line for at least 32 serial clock cycles, the serial interface is reset. In 3-wire systems, this ensures that the interface can be reset to a known state if the interface gets lost due to a software error or some glitch in the system. Reset returns the interface to the state in which it is expecting a write to the communications register. This operation resets the contents of all registers to their power-on values.

The AD7787 can be configured to continuously convert or to perform a single conversion (see Figure 13 through Figure 15).

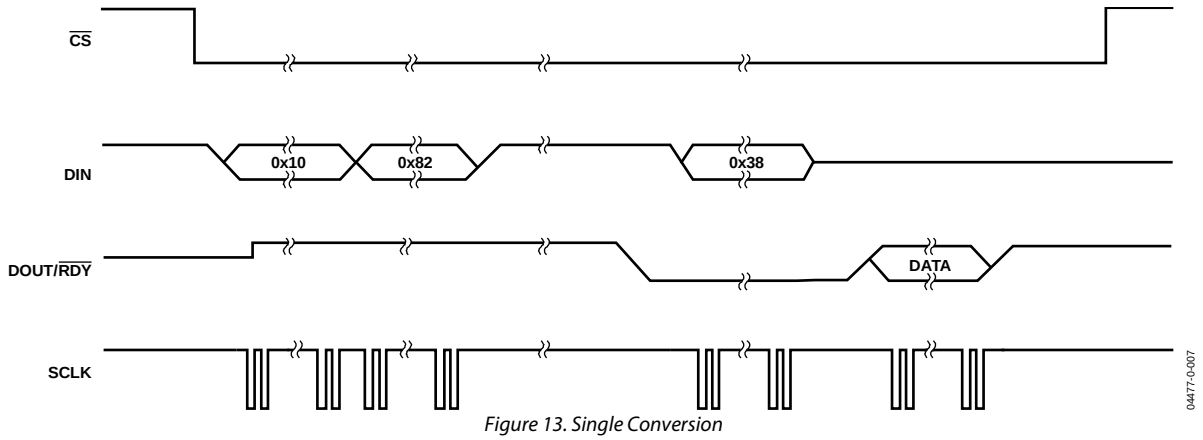



*Figure 13. Single Conversion*

### Single Conversion Mode

In single conversion mode, the AD7787 is placed in shutdown mode between conversions. When a single conversion is initiated by setting MD1 to 1 and MD0 to 0 in the mode register, the AD7787 powers up, performs a single conversion, and then returns to shutdown mode. When a single conversion is initiated, the AD7787's oscillator requires 1 ms to power up and settle. The AD7787 then performs a conversion which requires $2 \times t_{ADC}$. DOUT/$\overline{RDY}$ is high while the conversion is being performed and goes low to indicate the completion of the conversion. When the data word has been read from the data register, DOUT/$\overline{RDY}$ goes high. If $\overline{CS}$ is low, DOUT/$\overline{RDY}$ remains high until another conversion is initiated and completed. The data register can be read several times, if required, even when DOUT/$\overline{RDY}$ has gone high.

### Continuous Conversion Mode

This is the default power-up mode. The AD7787 will continuously converts with the $\overline{RDY}$ pin in the status register going low each time a conversion is complete. If $\overline{CS}$ is low, the DOUT/$\overline{RDY}$ line also goes low when a conversion is complete. To read a conversion, the user can write to the communications register, indicating that the next operation is a read of the data register. The digital conversion is placed on the DOUT/$\overline{RDY}$ pin as soon as SCLK pulses are applied to the ADC. DOUT/$\overline{RDY}$ returns high when the conversion is read. The user can read this register additional times, if required. However, the user must ensure that the data register is not being accessed at the completion of the next conversion or the new conversion word is lost.

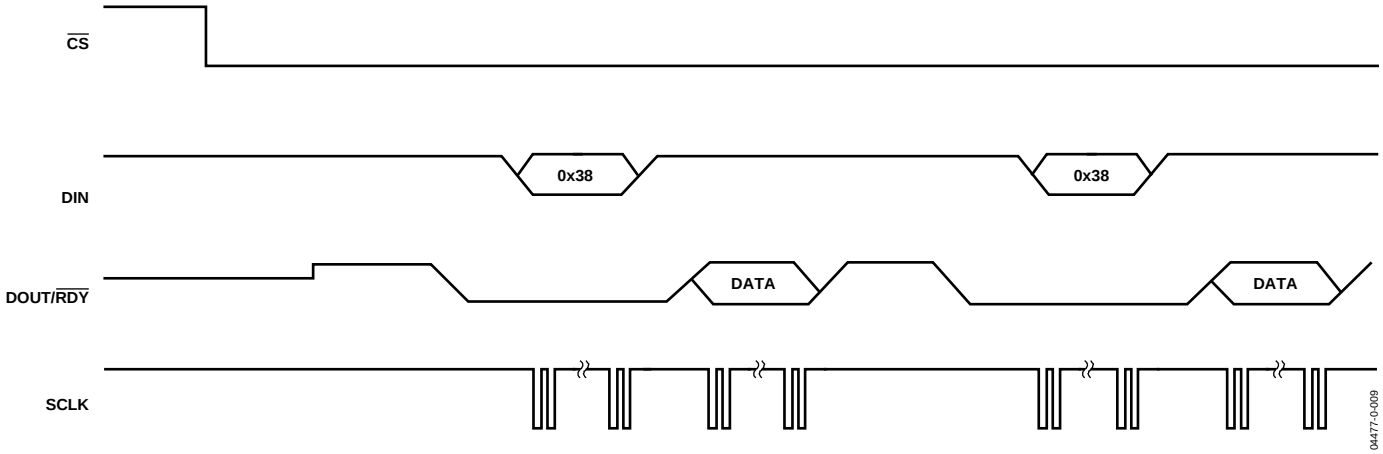



*Figure 14. Continuous Conversion*

### *Continuous Read Mode*

Rather than write to the communications register each time a conversion is complete to access the data, the AD7787 can be placed in continuous read mode. By writing 00111100 (Channel AIN1) or 00111101 (Channel AIN2) to the communications register, the user only needs to apply the appropriate number of SCLK cycles to the ADC, and the 24-bit word is automatically placed on the DOUT/$\overline{\text{RDY}}$ line when a conversion is complete.

When DOUT/$\overline{\text{RDY}}$ goes low to indicate the end of a conversion, sufficient SCLK cycles must be applied to the ADC, and the data conversion is placed on the DOUT/$\overline{\text{RDY}}$ line. When the conversion is read, DOUT/$\overline{\text{RDY}}$ returns high until the next conversion is available. In this mode, the data can only be read once. Also, the user must ensure that the data-word is read before the next conversion is complete. If the user has not read the conversion before the completion of the next conversion, or if insufficient serial clocks are applied to the AD7787 to read the word, the serial output register is reset when the next conversion is complete, and the new conversion is placed in the output serial register.

To exit the continuous read mode, the instruction 001110XX must be written to the communications register while the $\overline{\text{RDY}}$ pin is low. While in the continuous read mode, the ADC monitors activity on the DIN line so that it can receive the instruction to exit the continuous read mode. Additionally, a reset occurs if 32 consecutive 1s are seen on DIN. Therefore, DIN should be held low in continuous read mode until an instruction is written to the device.

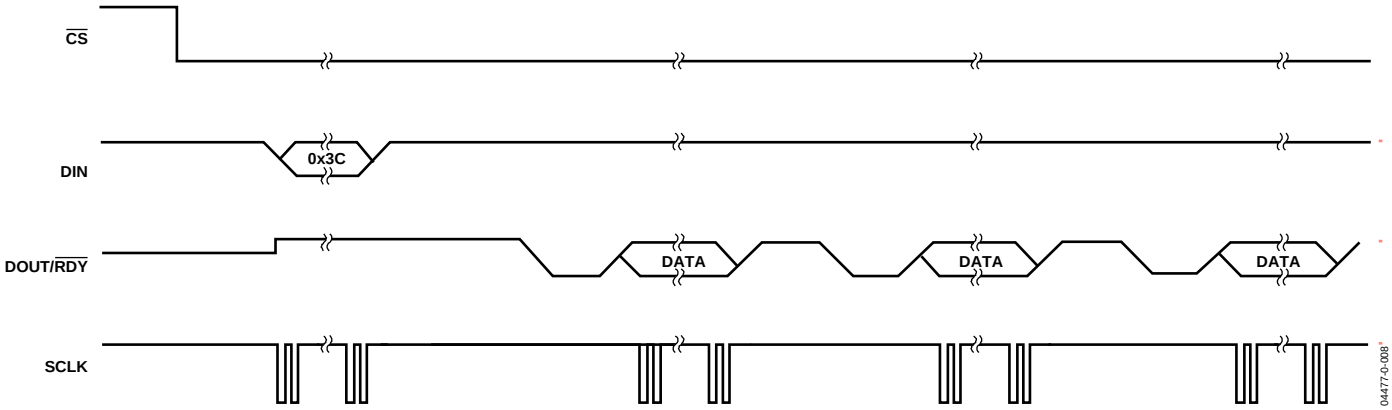



*Figure 15. Continuous Read*

# CIRCUIT DESCRIPTION

## ANALOG INPUT CHANNEL

The AD7787 has two analog input channels that are connected to the on-chip buffer amplifier when the device is operated in buffered mode and directly to the modulator when the device is operated in unbuffered mode. In buffered mode (the BUF bit in the mode register is set to 1), the input channel feeds into a high impedance input stage of the buffer amplifier. Therefore, the input can tolerate significant source impedances and is tailored for direct connection to external resistive-type sensors, such as strain gauges or resistance temperature detectors (RTDs).

When BUF = 0, the part is operated in unbuffered mode. This results in a higher analog input current. Note that this unbuffered input path provides a dynamic load to the driving source. Therefore, resistor/capacitor combinations on the input pins can cause dc gain errors, depending on the output impedance of the source that is driving the ADC input. Table 15 shows the allowable external resistance/capacitance values for the unbuffered mode such that no gain error at the 20-bit level is introduced.

**Table 15. External R-C Combination for No 20-Bit Gain Error**

| C (pF) | R (Ω) |
|---|---|
| 50 | 16.7 k |
| 100 | 9.6 k |
| 500 | 2.2 k |
| 1000 | 1.1 k |
| 5000 | 160 |

The absolute input voltage range in buffered mode is restricted to a range between GND + 100 mV and $V_{DD}$ − 100 mV. Care must be taken in setting up the common-mode voltage so that these limits are not exceeded. Otherwise, there is degradation in linearity and noise performance.

The absolute input voltage in unbuffered mode includes the range between GND − 100 mV and $V_{DD}$ + 30 mV resulting from being unbuffered. The negative absolute input voltage limit does allow the possibility of monitoring small true bipolar signals with respect to GND.

## BIPOLAR/UNIPOLAR CONFIGURATION

The analog input to the AD7787 can accept either unipolar or bipolar input voltage ranges. Unipolar and bipolar signals on the AIN1(+) input are referenced to the voltage on the AIN(−) input. For example, if AIN1(−) is 2.5 V and the ADC is configured for unipolar mode, the input voltage range on the AIN1(+) pin is 2.5 V to 5 V when REFIN = 2.5 V. If the ADC is configured for bipolar mode, the analog input range on the AIN1(+) input is 0 V to 5 V.

The voltage on AIN2 is referenced to GND. Therefore, when bipolar mode is selected and the part is operated in unbuffered mode, the voltage on AIN2 can vary from GND − 100 mV to +2.5 V. In unipolar mode, the voltage on AIN2 can vary from 0 V to 2.5 V. The bipolar/unipolar option is chosen by programming the U/$\overline{B}$ bit in the mode register.

## DATA OUTPUT CODING

When the ADC is configured for unipolar operation, the output code is natural (straight) binary with a zero differential input voltage resulting in a code of 00...00, a midscale voltage resulting in a code of 100...000, and a full-scale input voltage resulting in a code of 111...111. The output code for any analog input voltage can be represented as

$$Code = 2^{N} \times (AIN / V_{REF})$$

When the ADC is configured for bipolar operation, the output code is offset binary with a negative full-scale voltage resulting in a code of 000...000, a zero differential input voltage resulting in a code of 100...000, and a positive full-scale input voltage resulting in a code of 111...111. The output code for any analog input voltage can be represented as

$$Code = 2^{N-1} \times [(AIN / V_{REF}) + 1]$$

where *AIN* is the analog input voltage and $N = 24$.

## REFERENCE INPUT

The AD7787 has a single-ended reference that is 2.5 V nominal, but the AD7787 is functional with reference voltages from 0.1 V to $V_{DD}$. In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference voltage for the part, the effect of the low frequency noise in the excitation source is removed because the application is ratiometric. If the AD7787 is used in a nonratiometric application, a low noise reference should be used.

Recommended 2.5 V reference voltage sources for the AD7787 include the ADR381 and ADR391, which are low noise, low power references. In a system that operates from a 2.5 V power supply, the reference voltage source requires some headroom. In this case, a 2.048 V reference, such as the ADR380, can be used, requiring only 300 mV of headroom. Also note that the reference input provides a high impedance, dynamic load. Because the input impedance of the reference input is dynamic, resistor/capacitor combinations on this input can cause dc gain errors, depending on the output impedance of the source driving the reference inputs.

Reference voltage sources like those previously recommended, e.g., ADR391, will typically have low output impedances and are, therefore, tolerant to having decoupling capacitors on REFIN without introducing gain errors in the system. Deriving the reference input voltage across an external resistor means that the reference input sees a significant external source impedance. External decoupling on the REFIN pin is not recommended in this type of circuit configuration.

## $V_{DD}$ MONITOR

Along with converting external voltages, the AD7787 can monitor the voltage on the $V_{DD}$ pin. When the CH1 and CH0 bits in the communications register are set to 1, the voltage on the $V_{DD}$ pin is internally attenuated by 5 and the resultant voltage is applied to the Σ-Δ modulator using an internal 1.17 V reference for the analog-to-digital conversion. This is useful because variations in the power supply voltage can be monitored.

## GROUNDING AND LAYOUT

The digital filter provides rejection of broadband noise on the power supply, except at integer multiples of the modulator sampling frequency. The digital filter also removes noise from the analog and reference inputs, provided that these noise sources do not saturate the analog modulator. As a result, the AD7787 is more immune to noise interference than a conventional high resolution converter. However, because the resolution of the AD7787 is so high, and the noise levels from the AD7787 are so low, care must be taken with regard to grounding and layout.

The printed circuit board that houses the AD7787 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. A minimum etch technique is generally best for ground planes because it gives the best shielding.

It is recommended that the AD7787's GND pin be tied to the AGND plane of the system. In any layout, it is important that the user keep in mind the flow of currents in the system, ensuring that the return paths for all currents are as close as possible to the paths the currents took to reach their destinations. Avoid forcing digital currents to flow through the AGND sections of the layout.

The AD7787's ground plane should be allowed to run under the AD7787 to prevent noise coupling. The power supply lines to the AD7787 should use as wide a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but it is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. $V_{DD}$ should be decoupled with 10 µF tantalum in parallel with 0.1 µF capacitors to GND. To achieve the best from these decoupling components, they should be placed as close as possible to the device, ideally right up against the device. All logic chips should be decoupled with 0.1 µF ceramic capacitors to DGND.

## APPLICATIONS

### *Battery Monitoring*

In battery monitoring, the battery current and voltage are measured. The current is passed through a 100 µΩ resistor. Because the current is from −200 A to +2000 A, the result is a voltage from −20 mV to +200 mV. Channel AIN1 of the AD7787 can be connected directly to the shunt resistor to measure this current. The battery voltage can vary from 12 V to 42 V with peaks up to 60 V. This voltage is attenuated using an external resistor network before being applied to the AD7787. The buffers onboard the AD7787 mean that channel AIN2 can be connected directly to the high impedance attenuator circuit without introducing gain errors.

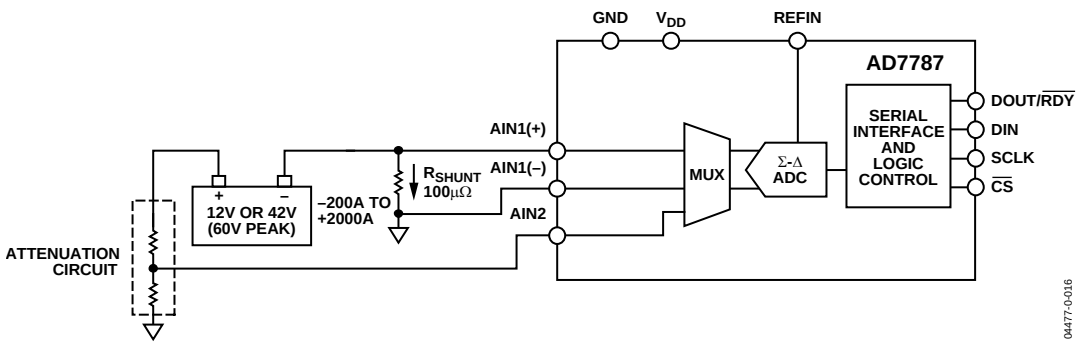
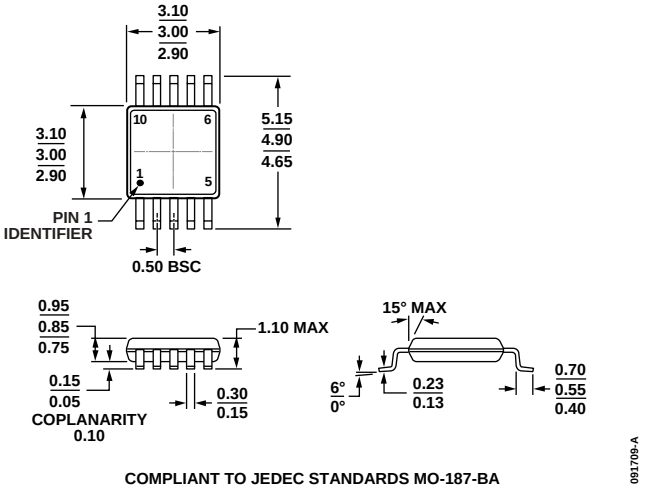



*Figure 16. Battery Monitoring*

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MO-187-BA

*Figure 17. 10-Lead Mini Small Outline Package [MSOP]*
*(RM-10)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Models[1] | Temperature Range | Package Description | Package Option | Branding |
|---|---|---|---|---|
| AD7787BRM | −40°C to +105°C | 10-Lead Mini Small Outline Package (MSOP) | RM-10 | C1T |
| AD7787BRMZ | −40°C to +105°C | 10-Lead Mini Small Outline Package (MSOP) | RM-10 | C42 |
| AD7787BRM-REEL | −40°C to +105°C | 10-Lead Mini Small Outline Package (MSOP) | RM-10 | C1T |
| AD7787BRMZ-RL | −40°C to +105°C | 10-Lead Mini Small Outline Package (MSOP) | RM-10 | C42 |
| EVAL-AD7787EB | | Evaluation Board | | |

[1] Z = RoHS Compliant Part.

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