# 4-Channel, ±10 V Input Range, High Throughput, 24-Bit Sigma-Delta ADC

Data Sheet **AD7734**

## FEATURES

**High resolution analog-to-digital converter (ADC)**
- **24 bits no missing codes**
- **±0.0025% nonlinearity**

**Optimized for fast channel switching**
- **18-bit p-p resolution (21 bits effective) at 500 Hz**
- **16-bit p-p resolution (19 bits effective) at 2 kHz**
- **14-bit p-p resolution (18 bits effective) at 15 kHz**
- **On-chip per channel system calibration**

**4 single-ended analog inputs**
- **Input ranges +5 V, ±5 V, +10 V, ±10 V**
- **Overvoltage tolerant**
- **Up to ±16.5 V not affecting adjacent channel**
- **Up to ±50 V absolute maximum**

**3-wire serial interface**
- **SPI, QSPI™, MICROWIRE, and DSP compatible**
- **Schmitt trigger on logic inputs**

**Single-supply operation**
- **5 V analog supply**
- **3 V or 5 V digital supply**

**Package: 28-lead TSSOP**

## APPLICATIONS

**PLCs/DCS**
**Multiplexing applications**
**Process control**
**Industrial instrumentation**

## FUNCTIONAL BLOCK DIAGRAM

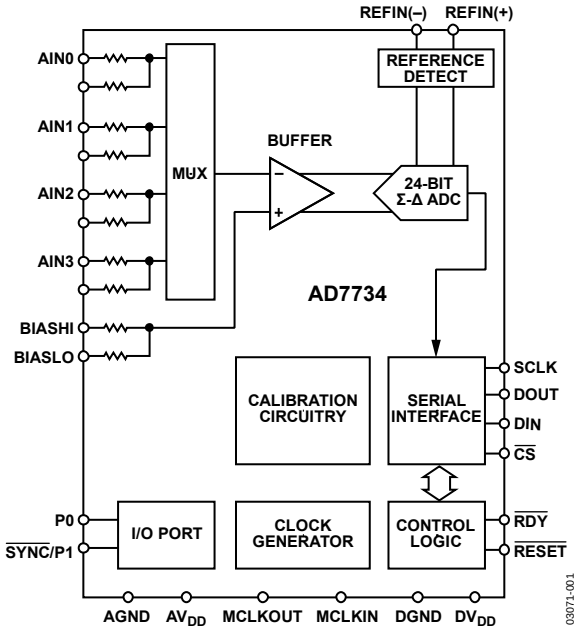


*Figure 1.*

## GENERAL DESCRIPTION

The AD7734 is a high precision, high throughput analog front end. True 16-bit p-p resolution is achievable with a total conversion time of 500 µs (2 kHz channel switching), making it ideally suitable for high resolution multiplexing applications.

The device can be configured via a simple digital interface, which allows users to balance the noise performance against data throughput up to 15.4 kHz.

The analog front end features four single-ended input channels with unipolar or true bipolar input ranges to ±10 V while operating from a single +5 V analog supply. The device has an overrange and underrange detection capability and accepts an analog input overvoltage to ±16.5 V without degrading the performance of the adjacent channels.

The differential reference input features "No-Reference" detect capability. The ADC also supports per channel system calibration options. The digital serial interface can be configured for 3-wire operation and is compatible with microcontrollers and digital signal processors. All interface inputs are Schmitt triggered.

The device is specified for operation over the extended industrial temperature range of −40°C to +105°C.

Other devices in the AD7734 family are the AD7732 and the AD7738.

The AD7732 is similar to the AD7734, but its analog front end features two fully differential input channels.

The AD7738 analog front end is configurable for four fully differential or eight single-ended input channels, features 0.625 V to 2.5 V bipolar/unipolar input ranges, and accepts a common-mode input voltage from 200 mV to AVDD − 300 mV. The AD7738 multiplexer output is pinned out externally, allowing the user to implement programmable gain or signal conditioning before being applied to the ADC.

**Rev. B** **Document Feedback**
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## REVISION HISTORY

**9/15—Rev. A to Rev. B**

Change to Figure 14 ... 22
Changes to Figure 28 ... 29
Changes to Ordering Guide ... 32

**7/12—Rev. 0 to Rev. A**

Changes to ADC Performance Chop Enabled Parameter ... 3
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**2/03—Revision 0: Initial Version**

# SPECIFICATIONS

−40°C to +105°C; $AV_{DD}$ = 5 V ± 5%; $DV_{DD}$ = 2.7 V to 3.6 V, or 5 V ± 5%; BIAS0 to BIAS3, BIASHI, REFIN(+) = 2.5 V; BIASLO, REFIN(−) = AGND; AIN Range = ±10 V; $f_{MCLKIN}$ = 6.144 MHz; unless otherwise noted.

**Table 1.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| ADC PERFORMANCE | | | | | |
| CHOPPING ENABLED | | | | | |
| Conversion Time Rate | 372 | | 12190 | Hz | Configure via Conv. Time Register |
| No Missing Codes[1, 2] | 24 | | | Bits | FW ≥ 6 (Conversion Time ≥ 165 µs) |
| Output Noise | | See Table 4 | | | |
| Resolution | | See Table 5 and Table 6 | | | |
| Integral Nonlinearity (INL)[1, 2] | | ±0.0010 | ±0.0030 | % of FSR | $f_{MCLKIN}$ = 2.5 MHz |
| Integral Nonlinearity (INL)[2] | | ±0.0025 | ±0.0060 | % of FSR | $f_{MCLKIN}$ = 6.144 MHz |
| Offset Error (Unipolar, Bipolar)[3] | | | ±13 | mV | Before Calibration |
| Offset Drift vs. Temperature[1] | | ±2.5 | | µV/°C | |
| Gain Error[3] | | | ±0.45 | % | Before Calibration |
| Gain Drift vs. Temperature[1] | | | ±3.2 | ppm of FS/°C | |
| Positive Full-Scale Error[3] | | | ±0.5 | % of FSR | Before Calibration |
| Positive Full-Scale Drift vs. Temp.[1] | | ±3 | | ppm of FS/°C | |
| Bipolar Negative Full-Scale Error[4] | | ±0.0050 | | % of FSR | After Calibration |
| Power Supply Sensitivity | | ±4 | ±10 | $LSB_{16}$ | At DC, AIN = 7 V, $AV_{DD}$ = 5 V ± 5% |
| Channel-to-Channel Isolation | | 110 | | dB | At DC, Maximum ±16.5 V AIN Voltage |
| ADC PERFORMANCE | | | | | |
| CHOPPING DISABLED | | | | | |
| Conversion Time Rate | 737 | | 15437 | Hz | Configure via Conv. Time Register |
| No Missing Codes[1, 2] | 24 | | | Bits | FW ≥ 8 (Conversion Time ≥ 117 µs) |
| Output Noise | | See Table 7 | | | |
| Resolution | | See Table 8 and Table 9 | | | |
| Integral Nonlinearity (INL)[2] | | ±0.0025 | | % of FSR | |
| Offset Error (Unipolar, Bipolar)[5] | | ±15 | | mV | Before Calibration |
| Offset Drift vs. Temperature | | ±25 | | µV/°C | |
| Gain Error[3] | | ±0.1 | | % | Before Calibration |
| Gain Drift vs. Temperature | | ±5.3 | | ppm of FS/°C | |
| Positive Full-Scale Error[3] | | ±0.2 | | % of FSR | Before Calibration |
| Positive Full-Scale Drift vs. Temp. | | ±4 | | ppm of FS/°C | |
| Bipolar Negative Full-Scale Error[4] | | ±0.0050 | | % of FSR | After Calibration |
| Power Supply Sensitivity | | ±4 | | $LSB_{16}$ | At DC, AIN = 7 V, $AV_{DD}$ = 5 V ± 5% |
| Channel-to-Channel Isolation | | 110 | | dB | At DC, Maximum ±16.5 V AIN Voltage |
| ANALOG INPUTS | | | | | |
| Analog Input Voltage[1, 6, 7] | | | | | |
| ±10 V Range | | ±10 | | V | |
| 0 V to +10 V Range | | 0 to +10 | | V | |
| ±5 V Range | | ±5 | | V | |
| 0 V to +5 V Range | | 0 to +5 | | V | |
| BIASLO Voltage | | 0 | | V | |
| BIAS0 to 3, BIASHI Voltage | | 2.5 | | V | |
| AIN Impedance[1, 8] | 100 | 124 | | kΩ | |
| AIN Pin, BIASLO Pin Impedance[1, 8] | 87.5 | 108.5 | | kΩ | |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| BIAS0 to 3, BIASHI Pin Impedance[1, 8] | 12.5 | 15.5 | | kΩ | |
| Input Resistor Matching | | 0.2 | | % | |
| Input Resistor Temp. Coefficient | | –30 | | ppm/°C | |
| REFERENCE INPUTS | | | | | |
| REFIN(+) to REFIN(–) Voltage[1, 9] | 2.475 | 2.5 | 2.525 | V | |
| NOREF Trigger Voltage | | 0.5 | | V | NOREF Bit in Channel Status Register |
| REFIN(+), REFIN(–) | | | | | |
| Common-Mode Voltage[1] | 0 | | $AV_{DD}$ | V | |
| Reference Input DC Current[10] | | | 400 | µA | |
| SYSTEM CALIBRATION[1, 11] | | | | | |
| Full-Scale Calibration Limit | | | +1.05 × FS | V | |
| Zero-Scale Calibration Limit | –1.05 × FS | | | V | |
| Input Span | 0.8 × FS | | 2.1 × FS | V | |
| LOGIC INPUTS | | | | | |
| Input Current | | | ±1 | µA | |
| Input Current $\overline{CS}$ | | | ±10 | µA | $\overline{CS}$ = $DV_{DD}$ |
| | | | –40 | µA | $\overline{CS}$ = DGND, Internal Pull-Up Resistor |
| Input Capacitance | | 5 | | pF | |
| $V_{T+}$[1] | 1.4 | | 2 | V | $DV_{DD}$ = 5 V |
| $V_{T-}$[1] | 0.8 | | 1.4 | V | $DV_{DD}$ = 5 V |
| $V_{T+} – V_{T-}$[1] | 0.3 | | 0.85 | V | $DV_{DD}$ = 5 V |
| $V_{T+}$[1] | 0.95 | | 2 | V | $DV_{DD}$ = 3 V |
| $V_{T-}$[1] | 0.4 | | 1.1 | V | $DV_{DD}$ = 3 V |
| $V_{T+} – V_{T-}$[1] | 0.3 | | 0.85 | V | $DV_{DD}$ = 3 V |
| MCLK IN ONLY | | | | | |
| Input Current | | | ±10 | µA | |
| Input Capacitance | | 5 | | pF | |
| $V_{INL}$ Input Low Voltage | | | 0.8 | V | $DV_{DD}$ = 5 V |
| $V_{INH}$ Input High Voltage | 3.5 | | | V | $DV_{DD}$ = 5 V |
| $V_{INL}$ Input Low Voltage | | | 0.4 | V | $DV_{DD}$ = 3 V |
| $V_{INH}$ Input High Voltage | 2.5 | | | V | $DV_{DD}$ = 3 V |
| LOGIC OUTPUTS[12] | | | | | |
| $V_{OL}$ Output Low Voltage | | | 0.4 | V | $I_{SINK}$ = 800 µA, $DV_{DD}$ = 5 V |
| $V_{OH}$ Output High Voltage | 4.0 | | | V | $I_{SOURCE}$ = 200 µA, $DV_{DD}$ = 5 V |
| $V_{OL}$ Output Low Voltage | | | 0.4 | V | $I_{SINK}$ = 100 µA, $DV_{DD}$ = 3 V |
| $V_{OH}$ Output High Voltage | $DV_{DD}$ – 0.6 | | | V | $I_{SOURCE}$ = 100 µA, $DV_{DD}$ = 3 V |
| Floating State Leakage Current | | | ±1 | µA | |
| Floating State Leakage Capacitance | | 3 | | pF | |
| P0, P1 INPUTS/OUTPUTS | | | | | Levels Referenced to Analog Supplies |
| Input Current | | | ±10 | µA | |
| $V_{INL}$ Input Low Voltage | | | 0.8 | V | $AV_{DD}$ = 5 V |
| $V_{INH}$ Input High Voltage | 3.5 | | | V | $AV_{DD}$ = 5 V |
| $V_{OL}$ Output Low Voltage | | | 0.4 | V | $I_{SINK}$ = 7 mA, See Absolute Maximum Ratings Section |
| $V_{OH}$ Output High Voltage | 4.0 | | | V | $I_{SOURCE}$ = 200 µA, $AV_{DD}$ = 5 V |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| POWER REQUIREMENTS | | | | | |
| $AV_{DD}$–AGND Voltage | 4.75 | | 5.25 | V | |
| $DV_{DD}$–DGND Voltage | 4.75 | | 5.25 | V | |
| | 2.70 | | 3.60 | V | |
| $AV_{DD}$ Current (Normal Mode) | | 13.5 | 15.9 | mA | $AV_{DD}$ = 5 V |
| $DV_{DD}$ Current (Normal Mode) [13] | | 2.8 | 3.1 | mA | $DV_{DD}$ = 5 V |
| $DV_{DD}$ Current (Normal Mode)[13] | | 1.0 | 1.5 | mA | $DV_{DD}$ = 3 V |
| Power Dissipation (Normal Mode)[13] | | 85 | 100 | mW | |
| $AV_{DD}$+$DV_{DD}$ Current (Standby Mode)[14] | | 100 | | µA | |
| Power Dissipation (Standby Mode)[14] | | 525 | | µW | |

[1] Specifications are not production tested but guaranteed by design and/or characterization data at initial product release.
[2] See Typical Performance Characteristics.
[3] Specifications before calibration. Channel system calibration reduces these errors to the order of the noise.
[4] Applies after the zero-scale and full-scale calibration. The negative full-scale error represents the remaining error after removing the offset and gain error.
[5] ADC zero-scale self-calibration reduces this error to ±10 mV. Channel zero-scale system calibration reduces this error to the order of the noise.
[6] For specified performance. The output data span corresponds to the specified nominal input voltage range. The ADC is functional outside the nominal input voltage range, but the performance might degrade. Outside the nominal input voltage range, the OVR bit in the channel status register is set and the channel data register value depends on the CLAMP bit in the mode register. See the register and circuit descriptions for more details.
[7] The adjacent channels are not affected by AIN voltage up to ±16.5 V.
[8] Pin impedance is from the pin to the internal node. In normal circuit configuration, the analog input total impedance is typically 108.5 kΩ + 15.5 kΩ = 124 kΩ.
[9] For specified performance. Device is functional with lower $V_{REF}$.
[10] Dynamic current charging the Σ-Δ modulator input switching capacitor.
[11] Outside the specified calibration range, calibration is possible but the performance may degrade.
[12] These logic output levels apply to the MCLK OUT output when it is loaded with a single CMOS load.
[13] With external MCLK, MCLKOUT disabled (CLKDIS bit set in the mode register).
[14] External MCLKIN = 0 V or $DV_{DD}$, digital inputs = 0 V or $DV_{DD}$, P0 and P1 = 0 V or $AV_{DD}$.

## TIMING SPECIFICATIONS

$AV_{DD}$ = 5 V ± 5%; $DV_{DD}$ = 2.7 V to 3.6 V, or 5 V ± 5%; Input Logic 0 = 0 V; Logic 1 = $DV_{DD}$; unless otherwise noted. Sample tested during initial release to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of $DV_{DD}$) and timed from a voltage level of 1.6 V. See Figure 2 and Figure 3.

**Table 2.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| Master Clock Range | 1 | | 6.144 | MHz | |
| $t_1$ | 50 | | | ns | $\overline{SYNC}$ Pulse Width |
| $t_2$ | 500 | | | ns | $\overline{RESET}$ Pulse Width |
| Read Operation | | | | | |
| $t_4$ | 0 | | | ns | $\overline{CS}$ Falling Edge to SCLK Falling Edge Setup Time |
| $t_5$[1] | | | | | SCLK Falling Edge to Data Valid Delay |
| | 0 | | 60 | ns | $DV_{DD}$ of 4.75 V to 5.25 V |
| | 0 | | 80 | ns | $DV_{DD}$ of 2.7 V to 3.3 V |
| $t_{5A}$[2] | | | | | $\overline{CS}$ Falling Edge to Data Valid Delay |
| | 0 | | 60 | ns | $DV_{DD}$ of 4.75 V to 5.25 V |
| | 0 | | 80 | ns | $DV_{DD}$ of 2.7 V to 3.3 V |
| $t_6$ | 50 | | | ns | SCLK High Pulse Width |
| $t_7$ | 50 | | | ns | SCLK Low Pulse Width |
| $t_8$ | 0 | | | ns | $\overline{CS}$ Rising Edge after SCLK Rising Edge Hold Time |
| $t_9$[3] | 10 | | 80 | ns | Bus Relinquish Time after SCLK Rising Edge |
| Write Operation | | | | | |
| $t_{11}$ | 0 | | | ns | $\overline{CS}$ Falling Edge to SCLK Falling Edge Setup |
| $t_{12}$ | 30 | | | ns | Data Valid to SCLK Rising Edge Setup Time |
| $t_{13}$ | 25 | | | ns | Data Valid after SCLK Rising Edge Hold Time |
| $t_{14}$ | 50 | | | ns | SCLK High Pulse Width |
| $t_{15}$ | 50 | | | ns | SCLK Low Pulse Width |
| $t_{16}$ | 0 | | | ns | $\overline{CS}$ Rising Edge after SCLK Rising Edge Hold Time |

[1] These numbers are measured with the load circuit of Figure 4 and defined as the time required for the output to cross the $V_{OL}$ or $V_{OH}$ limits.
[2] This specification is relevant only if $\overline{CS}$ goes low while SCLK is low.
[3] These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 4. The measured number is then extrapolated back to remove effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the Timing Characteristics are the true bus relinquish times of the device and as such are independent of external bus loading capacitances.

### *Timing Diagrams*

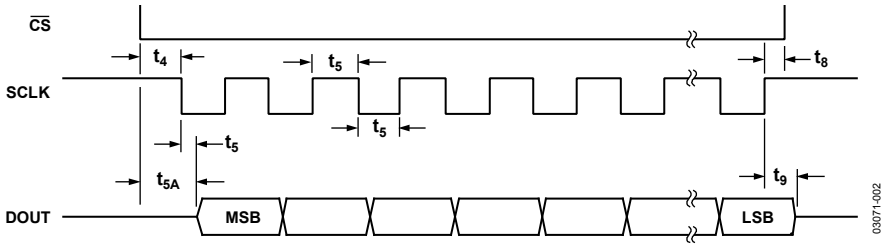


*Figure 2. Read Cycle Timing Diagram*

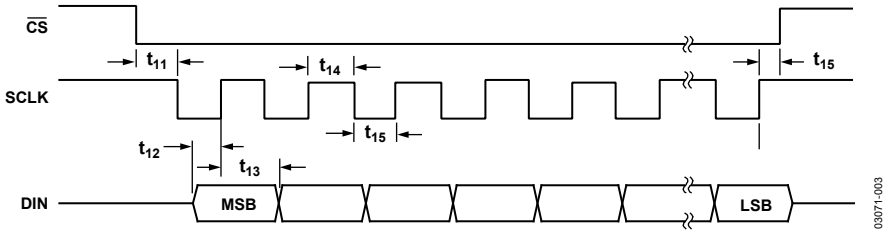


*Figure 3. Write Cycle Timing Diagram*

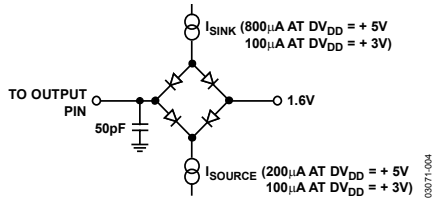


*Figure 4. Load Circuit for Access Time and Bus Relinquish Time*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 3.**

| Parameter | Rating |
|---|---|
| $AV_{DD}$ to AGND, $DV_{DD}$ to DGND | −0.3 V to +7 V |
| AGND to DGND | −0.3 V to +0.3 V |
| $AV_{DD}$ to $DV_{DD}$ | −5 V to +5 V |
| AIN to AGND | −50 V to +50 V |
| BIAS to AGND | −0.3 V to $AV_{DD}$ + 0.3 V |
| REFIN+, REFIN− to AGND | −0.3 V to $AV_{DD}$ + 0.3 V |
| MUX0, INTBIAS to AGND | −0.3 V to $AV_{DD}$ + 0.3 V |
| P0, P1 Voltage to AGND | −0.3 V to $AV_{DD}$ + 0.3 V |
| P0, P1 Current ($T_{MAX}$ = 70°C) | 8 mA |
| P0, P1 Current ($T_{MAX}$ = 85°C) | 5 mA |
| P0, P1 Current ($T_{MAX}$ = 105°C) | 2.5 mA |
| Digital Input Voltage to DGND | −0.3 V to $DV_{DD}$ + 0.3 V |
| Digital Output Voltage to DGND | −0.3 V to $DV_{DD}$ + 0.3 V |
| Operating Temperature Range | −40°C to +105°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| TSSOP, Power Dissipation | 660 mW |
| $\theta_{JA}$ Thermal Impedance | 97.9°C/W |
| Lead Temperature, Soldering | |
| Vapor Phase (60 sec) | 215°C |
| Infrared (15 sec) | 220°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# TYPICAL PERFORMANCE CHARACTERISTICS

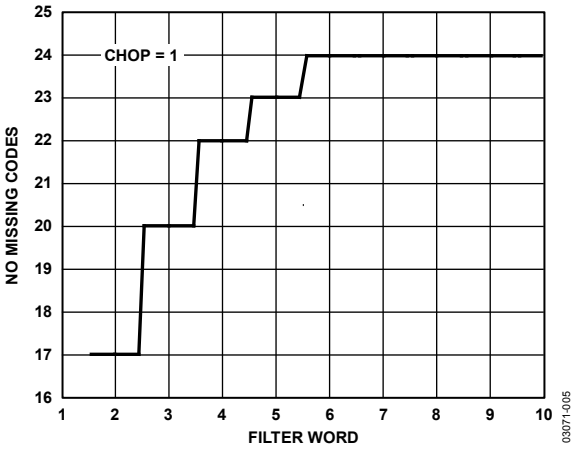


*Figure 5. No Missing Codes Performance, Chopping Enabled*

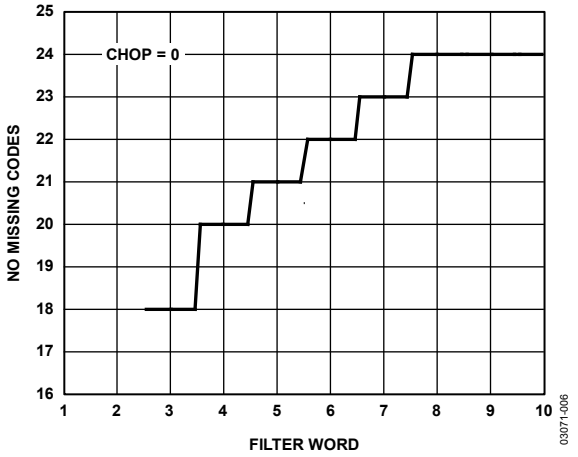


*Figure 6. No Missing Codes Performance, Chopping Disabled*

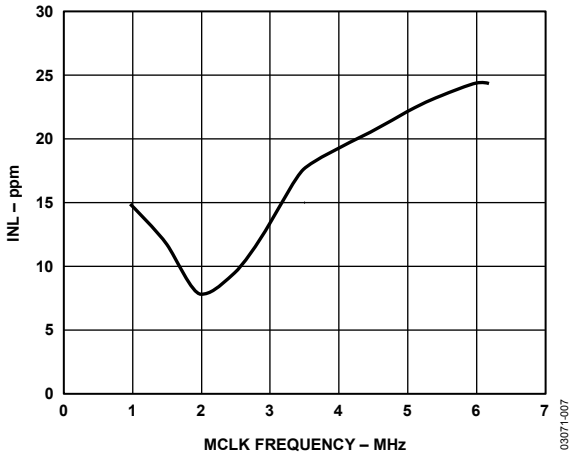


*Figure 7. Typical INL vs. MCLK Frequency, AIN = ±10 V, BIAS0 to BIAS3, BIASHI = 2.5 V, BIASLO = 0 V*

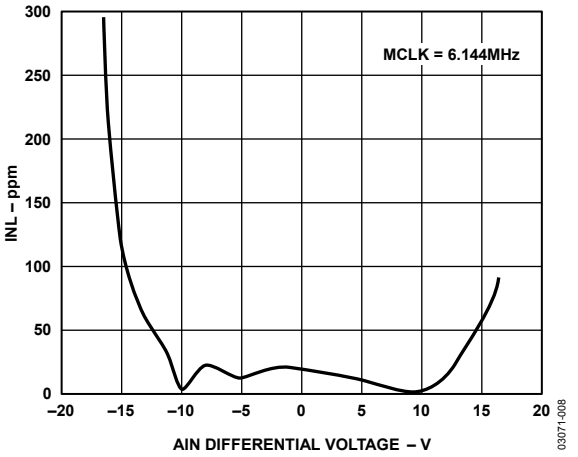


*Figure 8. Typical INL vs. AIN Voltage, AIN Range =±10 V, BIAS0 to BIAS3, BIASHI = 2.5 V, BIASLO = O V*

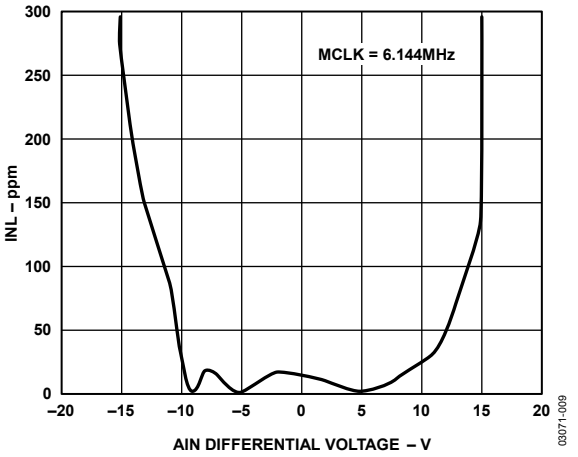


*Figure 9. Typical INL vs. AIN Voltage, AIN Range = ±10 V, BIAS0 to BIAS3, BIASHI = 2.5 V, BIASLO = 0 V*

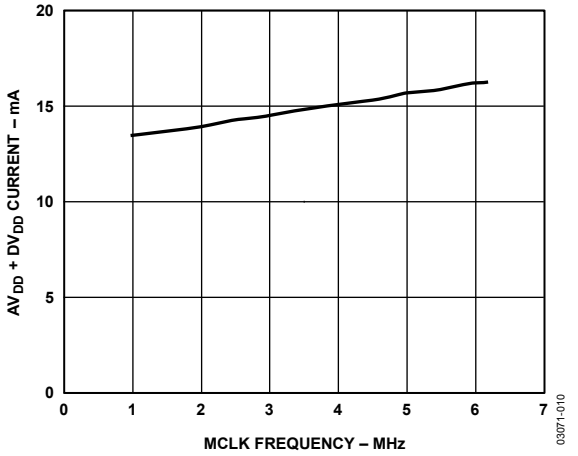


*Figure 10. Typical Supply Current vs. MCLK Frequency, Normal Operation, Converting*

# OUTPUT NOISE AND RESOLUTION SPECIFICATION

The AD7734 can be operated with chopping enabled or disabled, allowing the ADC to be programmed either to optimize the throughput rate and channel switching time or to optimize the offset drift performance. Noise tables for these two primary modes of operation are outlined below for a selection of output rates and settling times.

The AD7734 noise performance depends on the selected chopping mode, the filter word (FW) value, and the selected analog input range. The AD7734 noise will not vary significantly with MCLK frequency.

## CHOPPING ENABLED

The first mode, in which the AD7734 is configured with chopping enabled (CHOP = 1), provides very low noise with lower output rates. Table 4 to Table 6 show the –3 dB frequencies and typical performance versus the channel conversion time and equivalent output data rate, respectively.

Table 4 shows the typical output rms noise. Table 5 shows the typical effective resolution based on rms noise. Table 6 shows the typical output peak-to-peak resolution, representing values for which there will be no code flicker within a 6 Σ limit. The peak-to-peak resolutions are not calculated based on rms noise but on peak-to-peak noise.

These typical numbers are generated from 4096 data samples acquired in continuous conversion mode with an analog input voltage set to 0 V and MCLK = 6.144 MHz. The conversion time is selected via the channel conversion time register.

**Table 4. Typical Output RMS Noise in µV vs. Conversion Time and Input Range with Chopping Enabled**

| FW | Conversion Time Register | Conversion Time (µs) | Output Data Rate (Hz) | –3 dB Frequency (Hz) | RMS Noise (µV) |
|---|---|---|---|---|---|
| 127 | FFh | 2686 | 372 | 200 | 9.6 |
| 46 | AEh | 999 | 1001 | 520 | 15.5 |
| 22 | 96h | 499 | 2005 | 1040 | 22.7 |
| 17 | 91h | 395 | 2534 | 1300 | 26.1 |
| 8 | 88h | 207 | 4826 | 2500 | 39.2 |
| 6 | 86h | 166 | 6041 | 3100 | 46.0 |
| 2 | 82h | 82 | 12166 | 6300 | 120.0 |

**Table 5. Typical Effective Resolution in Bits vs. Conversion Time and Input Range with Chopping Enabled**

| FW | Conversion Time Register | Conversion Time (µs) | Output Data Rate (Hz) | –3 dB Frequency (Hz) | Input Range/Effective Resolution (Bits) | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | ±10 V | 0 V to +10 V | ±5 V | 0 V to +5 V |
| 127 | FFh | 2686 | 372 | 200 | 21.0 | 20.0 | 20.0 | 19.0 |
| 46 | AEh | 999 | 1001 | 520 | 20.3 | 19.3 | 19.3 | 18.3 |
| 22 | 96h | 499 | 2005 | 1040 | 19.7 | 18.7 | 18.7 | 17.7 |
| 17 | 91h | 395 | 2534 | 1300 | 19.5 | 18.5 | 18.5 | 17.5 |
| 8 | 88h | 207 | 4826 | 2500 | 19.0 | 18.0 | 18.0 | 17.0 |
| 6 | 86h | 166 | 6041 | 3100 | 18.7 | 17.7 | 17.7 | 16.7 |
| 2 | 82h | 82 | 12166 | 6300 | 17.3 | 16.3 | 16.3 | 15.3 |

**Table 6. Typical Peak-to-Peak Resolution in Bits vs. Conversion Time and Input Range with Chopping Enabled**

| FW | Conversion Time Register | Conversion Time (µs) | Output Data Rate (Hz) | –3 dB Frequency (Hz) | Input Range/Peak-to-Peak Resolution (Bits) | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | ±10 V | 0 V to +10 V | ±5 V | 0 V to +5 V |
| 127 | FFh | 2686 | 372 | 200 | 18.1 | 17.1 | 17.1 | 16.1 |
| 46 | AEh | 999 | 1001 | 520 | 17.4 | 16.4 | 16.4 | 15.4 |
| 22 | 96h | 499 | 2005 | 1040 | 16.9 | 15.9 | 15.9 | 14.9 |
| 17 | 91h | 395 | 2534 | 1300 | 16.7 | 15.7 | 15.7 | 14.7 |
| 8 | 88h | 207 | 4826 | 2500 | 16.2 | 15.2 | 15.2 | 14.2 |
| 6 | 86h | 166 | 6041 | 3100 | 15.8 | 14.8 | 14.8 | 13.8 |
| 2 | 82h | 82 | 12166 | 6300 | 15.0 | 13.4 | 13.4 | 12.4 |

## CHOPPING DISABLED

The second mode, in which the AD7734 is configured with chopping disabled (CHOP = 0), provides faster conversion time while still maintaining high resolution. Table 7 to Table 9 show the −3 dB frequencies and typical performance versus the channel conversion time and equivalent output data rate, respectively. Table 7 shows the typical output rms noise. Table 8 shows the typical effective resolution based on the rms noise. Table 9 shows the typical output peak-to-peak resolution, representing values for which there will be no code flicker within a 6 Σ limit. The peak-to-peak resolutions are not calculated based on rms noise but on peak-to-peak noise.

These typical numbers are generated from 4096 data samples acquired in continuous conversion mode with an analog input voltage set to 0 V and MCLK = 6.144 MHz. The conversion time is selected via the channel conversion time register.

**Table 7. Typical Output RMS Noise in µV vs. Conversion Time and Input Range with Chopping Disabled**

| FW | Conversion Time Register | Conversion Time (µs) | Output Data Rate (Hz) | −3 dB Frequency (Hz) | RMS Noise (µV) |
|---|---|---|---|---|---|
| 127 | 7Fh | 1357 | 737 | 670 | 13.2 |
| 92 | 5Ch | 992 | 1008 | 920 | 15.5 |
| 44 | 2Ch | 492 | 2032 | 1850 | 22.7 |
| 35 | 23h | 398 | 2511 | 2290 | 26.3 |
| 16 | 10h | 200 | 4991 | 2500 | 39.0 |
| 8 | 08h | 117 | 8545 | 7780 | 57.0 |
| 3 | 03h | 65 | 15398 | 14000 | 132 |

**Table 8. Typical Effective Resolution in Bits vs. Conversion Time and Input Range with Chopping Disabled**

| FW | Conversion Time Register | Conversion Time (µs) | Output Data Rate (Hz) | −3 dB Frequency (Hz) | Input Range/Effective Resolution (Bits) | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | ±10 V | 0 V to +10 V | ±5 V | 0 V to +5 V |
| 127 | 7Fh | 1357 | 737 | 670 | 20.5 | 19.5 | 19.5 | 18.5 |
| 92 | 5Ch | 992 | 1008 | 920 | 20.3 | 19.3 | 19.3 | 18.3 |
| 44 | 2Ch | 492 | 2032 | 1850 | 19.7 | 18.7 | 18.7 | 17.7 |
| 35 | 23h | 398 | 2511 | 2290 | 19.5 | 18.5 | 18.5 | 17.5 |
| 16 | 10h | 200 | 4991 | 2500 | 19.0 | 18.0 | 18.0 | 17.0 |
| 8 | 08h | 117 | 8545 | 7780 | 18.4 | 17.4 | 17.4 | 16.4 |
| 3 | 03h | 65 | 15398 | 14000 | 17.2 | 16.2 | 16.2 | 15.2 |

**Table 9. Typical Peak-to-Peak Resolution in Bits vs. Conversion Time and Input Range with Chopping Disabled**

| FW | Conversion Time Register | Conversion Time (µs) | Output Data Rate (Hz) | −3 dB Frequency (Hz) | Input Range/Peak-to-Peak Resolution (Bits) | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | ±10 V | 0 V to +10 V | ±5 V | 0 V to +5 V |
| 127 | 7Fh | 1357 | 737 | 670 | 17.6 | 16.6 | 16.6 | 15.6 |
| 92 | 5Ch | 992 | 1008 | 920 | 17.4 | 16.4 | 16.4 | 15.4 |
| 44 | 2Ch | 492 | 2032 | 1850 | 16.8 | 15.8 | 15.8 | 14.8 |
| 35 | 23h | 398 | 2511 | 2290 | 16.6 | 15.6 | 15.6 | 14.6 |
| 16 | 10h | 200 | 4991 | 2500 | 16.1 | 15.1 | 15.1 | 14.1 |
| 8 | 08h | 117 | 8545 | 7780 | 15.5 | 14.5 | 14.5 | 13.5 |
| 3 | 03h | 65 | 15398 | 14000 | 14.3 | 13.3 | 13.3 | 12.3 |

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

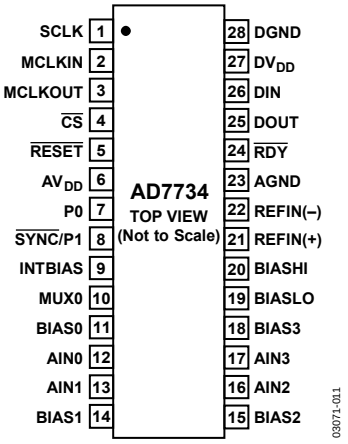


*Figure 11. 28-Lead TSSOP*

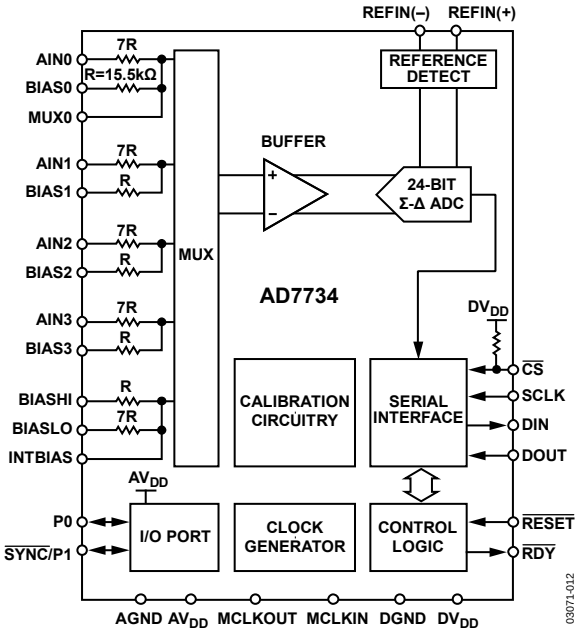


*Figure 12. Block Diagram*

**Table 10. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | SCLK | Serial Clock. Schmitt triggered logic input. An external serial clock is applied to this input to transfer serial data to or from the AD7734. |
| 2 | MCLKIN | Master Clock Signal for the ADC. This can be provided in the form of a crystal/resonator or external clock. A crystal/resonator can be tied across the MCLKIN and MCLKOUT pins. Alternatively, the MCLKIN pin can be driven with a CMOS compatible clock and MCLKOUT left unconnected. |
| 3 | MCLKOUT | When the master clock for the device is a crystal/resonator, the crystal/resonator is connected between MCLKIN and MCLKOUT. If an external clock is applied to the MCLKIN, MCLKOUT provides an inverted clock signal or can be switched off to reduce the device power consumption. MCLK OUT is capable of driving one CMOS load. |
| 4 | $\overline{CS}$ | Chip Select. Active low Schmitt triggered logic input with an internal pull-up resistor. With this input hardwired low, the AD7734 can operate in its 3-wire interface mode using SCLK, DIN, and DOUT. $\overline{CS}$ can be used to select the device in systems with more than one device on the serial bus. It can also be used as an 8-bit frame synchronization signal. |
| 5 | $\overline{RESET}$ | Schmitt Triggered Logic Input. Active low input that resets the control logic, interface logic, digital filter, analog modulator, and all on-chip registers of the device to power-on status. Effectively, everything on the device except the clock oscillator is reset when the $\overline{RESET}$ pin is exercised. |
| 6 | $AV_{DD}$ | Analog Positive Supply Voltage. 5 V to AGND nominal. |
| 7 | P0 | Digital Input/Output. The pin direction is determined by the P0 DIR bit; the digital value can be read/written as the P0 bit in the I/O port register. The digital voltage is referenced to analog supplies. When configured as an input, the pin should be tied high or low. |
| 8 | $\overline{SYNC}$/P1 | $\overline{SYNC}$/Digital Input/Digital Output. The pin direction is determined by the P1 DIR bit; the digital value can be read/written as the P1 bit in the I/O port register. When the SYNC bit in the I/O port register is set to 1, then the $\overline{SYNC}$/P1 pin can be used to synchronize the AD7734 modulator and digital filter with other devices in the system. The digital voltage is referenced to analog supplies. When configured as an input, the pin should be tied high or low. |
| 9 | INTBIAS | This pin provides direct access to the analog input's common node, bypassing the input resistor divider. In normal circuit configuration, this pin is left open circuit. |
| 10 | MUX0 | This pin provides direct access to the multiplexer input of Channel 0, bypassing the input resistor divider. The input voltage range is 0 V to +0.625 V, ±0.625 V, 0 V to +1.25 V, or ±1.25 V referenced to the INTBIAS pin. In normal circuit configuration, this pin is left open circuit. |
| 11, 14, 15, 18 | BIAS0 to BIAS3 | These inputs are used to level shift the analog inputs. These signals are used to ensure that the differential signal seen by the internal buffer amplifier is within its common-mode range. The BIAS0 to BIAS3 pins will normally be connected to 2.5 V. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 12, 13, 16, 17 | AIN0 to AIN3 | Analog Inputs. |
| 19 | BIASLO | BIASLO, in association with BIASHI, is used to set the analog input common-mode voltage. Assuming the BIAS0 to BIAS3 and BIASHI pins are connected to 2.5 V, the analog input voltages are referenced to the voltage at BIASLO. In normal circuit configuration, this pin should be connected to 0 V. |
| 20 | BIASHI | BIASHI, in association with BIASLO, is used to set the analog input common-mode voltage. In normal circuit configuration, this pin should be connected to 2.5 V. |
| 21 | REFIN(+) | Positive Terminal of the Differential Reference Input. REFIN(+) voltage potential can lie anywhere between $AV_{DD}$ and AGND. In normal circuit configuration, this pin should be connected to a 2.5 V reference voltage. |
| 22 | REFIN(–) | Negative Terminal of the Differential Reference Input. REFIN(–) voltage potential can lie anywhere between $AV_{DD}$ and AGND. In normal circuit configuration, this pin should be connected to a 0 V reference voltage. |
| 23 | AGND | Ground Reference Point for Analog Circuitry. |
| 24 | $\overline{RDY}$ | Logic Output. Used as a status output in both conversion mode and calibration mode. In conversion mode, a falling edge on this output indicates that either any channel or all channels have unread data available, according to the RDYFN bit in the I/O port register. In calibration mode, a falling edge on this output indicates that calibration is complete (see the Digital Interface Description section for more details). |
| 25 | DOUT | Serial data output with serial data being read from the output shift register on the device. This output shift register can contain information from any AD7734 register, depending on the address bits of the communications register. |
| 26 | DIN | Serial data input (Schmitt triggered) with serial data being written to the input shift register on the device. Data from this input shift register is transferred to any AD7734 register, depending on the address bits of the communications register. |
| 27 | $DV_{DD}$ | Digital Supply Voltage, 3 V or 5 V Nominal. |
| 28 | DGND | Ground Reference Point for Digital Circuitry. |

# REGISTER DESCRIPTION

**Table 11. Register Summary**

| Register | Addr | Dir | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| | (hex) | | Default Value | | | | | | | |
| Communications | 00 | W | 0 | R/$\overline{W}$ | 6-Bit Register Address | | | | | |
| | | | | | | | | | | |
| I/O Port | 01 | R/W | P0 | P1 | P0 DIR | P1 DIR | RDYFN | 0 | 0 | SYNC |
| | | | P0 Pin | P1 Pin | 1 | 1 | 0 | 0 | 0 | 0 |
| Revision | 02 | R | Chip Revision Code | | | | Chip Generic Code | | | |
| | | | x | x | x | x | 0 | 0 | 1 | 0 |
| Test | 03 | R/W | 24-Bit Manufacturing Test Register | | | | | | | |
| | | | | | | | | | | |
| ADC Status | 04 | R | | | | | RDY3 | RDY2 | RDY1 | RDY0 |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Checksum | 05 | R/W | 16-Bit Checksum Register | | | | | | | |
| | | | | | | | | | | |
| ADC Zero-Scale Calibration | 06 | R/W | 24-Bit ADC Zero-Scale Calibration Register | | | | | | | |
| | | | 800000h | | | | | | | |
| ADC Full-Scale | 07 | R/W | 24-Bit ADC Full-Scale Register | | | | | | | |
| | | | 800000h | | | | | | | |
| Channel Data[1] | 08 to 0B | R | 16-/24-Bit Data Registers | | | | | | | |
| | | | 8000h | | | | | | | |
| Channel Zero-Scale Cal.[1] | 10 to 13 | R/W | 24-Bit Channel Zero-Scale Calibration Registers | | | | | | | |
| | | | 800000h | | | | | | | |
| Channel Full-Scale Cal.[1] | 18 to 1B | R/W | 24-Bit Channel Full-Scale Calibration Registers | | | | | | | |
| | | | 200000h | | | | | | | |
| Channel Status[1] | 20 to 3 | R | 0 | CH1 | CH0 | 0/P0 | RDY/P1 | NOREF | SIGN | OVR |
| | | | Channel Number | | | 0 | 0 | 0 | 0 | 0 |
| Channel Setup[1] | 28 to 2B | R/W | 0 | 0 | 0 | Stat OPT | ENABLE | 0 | RNG1 | RNG0 |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Channel Conversion Time[1] | 30 to 33 | R/W | CHOP | FW (7-Bit Filter Word) | | | | | | |
| | | | 1 | 11h | | | | | | |
| Mode[2] | 38 to 3B | R/W | MD2 | MD1 | MD0 | CLKDIS | DUMP | Cont RD | 24/16 BIT | CLAMP |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

[1] The two LSBs of the register address, Bit 1 and Bit 0 in the communication register, specify the channel number of the register being accessed.
[2] There is only one mode register, although the mode register can be accessed in one of four address locations. The address used to write the mode register specifies the ADC channel on which the mode will be applied. Only address 38h must be used for reading from the mode register.

**Table 12. Operational Mode Summary**

| MD2 | MD1 | MD0 | Mode |
|---|---|---|---|
| 0 | 0 | 0 | Idle Mode |
| 0 | 0 | 1 | Continuous Conversion Mode |
| 0 | 1 | 0 | Single Conversion Mode |
| 0 | 1 | 1 | Power-Down (Standby) Mode |
| 1 | 0 | 0 | ADC Zero-Scale Self-Calibration |
| 1 | 0 | 1 | For Future Use |
| 1 | 1 | 0 | Channel Zero-Scale System Calibration |
| 1 | 1 | 1 | Channel Full-Scale System Calibration |

**Table 13. Input Range Summary**

| RNG1 | RNG0 | Nominal Input Voltage Range |
|---|---|---|
| 0 | 0 | ±10 V |
| 0 | 1 | 0 V to +10 V |
| 1 | 0 | ±5 V |
| 1 | 1 | 0 V to +5 V |

## REGISTER ACCESS

The AD7734 is configurable through a series of registers. Some of them configure and control general AD7734 features, while others are specific to each channel. The register data widths vary from 8 bits to 24 bits. All registers are accessed through the communications register, that is, any communication to the AD7734 must start with a write to the communications register specifying which register will subsequently be read or written.

## COMMUNICATIONS REGISTER

*8 Bits, Write-Only Register, Address 00h*

All communications to the device must start with a write operation to the communications register. The data written to the communications register determines whether the subsequent operation will be a read or write and to which register this operation will be directed. The digital interface defaults to expect write operation to the communications register after power-on, after reset, or after the subsequent read or write operation to the selected register is complete. If the interface sequence is lost, the device can be reset by writing at least 32 serial clock cycles with DIN high and $\overline{CS}$ low. (Note that all of the parts, including the modulator, filter, interface, and all registers are reset in this case.) Remember to keep DIN low while reading 32 bits or more either in continuous read mode or with the DUMP bit and "24/16" bit in the mode register set.

| Bit | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Mnemonic | 0 | R/$\overline{W}$ | 6-Bit Register Address | | | | | |

| Bit | Mnemonic | Description |
|---|---|---|
| 7 | 0 | This bit must be 0 for proper operation. |
| 6 | R/$\overline{W}$ | A 0 in this bit indicates that the next operation will be a write to a specified register. A 1 in this bit indicates that the next operation will be a read from a specified register. |
| 5 to 0 | Address | Address specifying to which register the read or write operation will be directed. For channel specific registers, two LSBs, Bit 1 and Bit 0, specify the channel number. When the subsequent operation writes to the Mode register, two LSBs specify the channel selected for operation determined by the mode register value (see Table 14). |

**Table 14.**

| Bit 2 | Bit 1 | Bit 0 | Channel | Input |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | AIN0 |
| 0 | 0 | 1 | 1 | AIN1 |
| 0 | 1 | 0 | 2 | AIN2 |
| 0 | 1 | 1 | 3 | AIN3 |

## I/O PORT REGISTER

*8 Bits, Read/Write Register, Address 01h, Default Value 30h + Digital Input Value × 40h*

The bits in this register are used to configure and access the digital I/O port on the AD7734.

| Bit | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Mnemonic | P0 | P1 | P0 DIR | P1 DIR | RDYFN | 0 | 0 | SYNC |
| Default | P0 Pin | P1 Pin | 1 | 1 | 0 | 0 | 0 | 0 |

| Bit | Mnemonic | Description |
|---|---|---|
| 7, 6 | P0, P1 | When the P0 and P1 pins are configured as outputs, the P0 and P1 bits determine the pins' output level. When the P0 and P1 pins are configured as inputs, the P0 and P1 bits reflect the current input level on the pins. |
| 5, 4 | P0 DIR, P1 DIR | These bits determine whether the P0 and P1 pins are configured as inputs or outputs. When set to 1, the corresponding pin will be an input; when reset to 0, the corresponding pin will be an output. |
| 3 | RDYFN | This bit is used to control the function of the $\overline{RDY}$ pin on the AD7734. When this bit is reset to 0, the $\overline{RDY}$ pin goes low when any channel has unread data. When this bit is set to 1, the $\overline{RDY}$ pin will only go low if all enabled channels have unread data. |
| 2, 1 | 0 | These bits must be 0 for proper operation. |
| 0 | SYNC | This bit enables the $\overline{SYNC}$ pin function. By default, this bit is 0 and $\overline{SYNC}$/P1 can be used as a digital I/O pin. When the SYNC bit is set to 1, the $\overline{SYNC}$ pin can be used to synchronize the AD7734 modulator and digital filter with other devices in the system. |

## REVISION REGISTER

*8 Bits, Read-Only Register, Address 02h, Default Value 02h + Chip Revision × 10h*

| Bit | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Mnemonic | Chip Revision Code | | | | Chip Generic Code | | | |
| Default | x | x | x | x | 0 | 0 | 1 | 0 |

| Bit | Mnemonic | Description |
|---|---|---|
| 7 to 4 | Chip Revision Code | 4-Bit Factory Chip Revision Code |
| 3 to 0 | Chip Generic Code | On the AD7734, these bits will read back as 02h. |

| Bit | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Mnemonic | | | | | RDY3 | RDY2 | RDY1 | RDY0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## TEST REGISTER

*24 Bits, Read/Write Register, Address 03h*

This register is used for testing the device in the manufacturing process. The user must not change the default configuration of this register.

## ADC STATUS REGISTER

*8 Bits, Read-Only Register, Address 04h, Default Value 00h*

In conversion modes, the register bits reflect the individual channel status. When a conversion is complete, the corresponding channel data register is updated and the corresponding RDY bit is set to 1.

When the channel data register is read, the corresponding bit is reset to 0. The bit is also reset to 0 when no read operation has taken place and the result of the next conversion is being updated to the channel data register. Writing to the mode register resets all the bits to 0.

In calibration modes, all the register bits are reset to 0 while a calibration is in progress; all the register bits are set to 1 when the calibration is complete.

The $\overline{RDY}$ pin output is related to the content of the ADC status register as defined by the RDYFN bit in the I/O port register. The RDY0 bit corresponds to Channel 0, the RDY1 bit corresponds to Channel 1, and so on.

## CHECKSUM REGISTER

*16 Bits, Read/Write Register, Address 05h*

This register is described in the AN-626 Application Note, *Using the AD7732/AD7734/AD7738/AD7739 Checksum Register*.

## ADC ZERO-SCALE CALIBRATION REGISTER

*24 Bits, Read/Write Register, Address 06h, Default Value 800000h*

The register holds the ADC zero-scale calibration coefficient. The value in this register is used in conjunction with the value in the ADC full-scale calibration register and the corresponding channel zero-scale and channel full-scale calibration registers to scale digitally all channels' conversion results. The value in this register is updated automatically following the execution of an ADC zero-scale self-calibration. Writing this register is possible in the idle mode only (see the Calibration section for more details).

## ADC FULL-SCALE REGISTER

*24 Bits, Read/Write Register, Address 07h, Default Value 800000h*

This register holds the ADC full-scale coefficient. The user is advised not to change the default configuration of this register.

## CHANNEL DATA REGISTERS

*16 Bit/24 Bit, Read-Only Registers, Address 08h–0Bh, Default Width 16 Bits, Default Value 8000h*

These registers contain the most up-to-date conversion results corresponding to each analog input channel. The 16-bit or 24-bit data width can be configured by setting the 24/16 bit in the mode register. The relevant RDY bit in the channel status register goes high when the result is updated. The RDY bit will return low once the data register reading has begun. The $\overline{\text{RDY}}$ pin can be configured to indicate when any channel has unread data or waits until all enabled channels have unread data. If any channel data register read operation is in progress when a new result is updated, no update of the data register will occur. This avoids having corrupted data. Reading the status registers can be associated with reading the data registers in the dump mode. Reading the status registers is always associated with reading the data registers in the continuous read mode (see the Digital Interface Description section for more details).

## CHANNEL ZERO-SCALE CALIBRATION REGISTERS

*24 Bits, Read/Write Registers, Address 10h–13h, Default Value 800000h*

These registers hold the particular channel zero-scale calibration coefficients. The value in these registers is used in conjunction with the value in the corresponding channel full-scale calibration register, the ADC zero-scale calibration register, and the ADC full-scale register to scale the particular channel conversion results digitally. The value in this register is updated automatically following the execution of a channel zero-scale system calibration.

The format of the channel zero-scale calibration register is a sign bit and 22 bits unsigned value. Writing this register is possible in the idle mode only (see the Calibration section for more details).

## CHANNEL FULL-SCALE CALIBRATION REGISTERS

*24 Bits, Read/Write Registers, Address 18h–1Bh, Default Value 200000h*

These registers hold the particular channel full-scale calibration coefficients. The value in these registers is used in conjunction with the value in the corresponding channel zero-scale calibration register, the ADC zero-scale calibration register, and the ADC full-scale register to scale the particular channel conversion results digitally. The value in this register is updated automatically following the execution of a channel full-scale system calibration. Writing this register is possible in the idle mode only (see the Calibration section for more details).

## CHANNEL STATUS REGISTERS

*8 Bits, Read-Only Register, Address 20h–23h, Default Value 20h × Channel Number*

These registers contain individual channel status information and some general AD7734 status information. Reading the status registers can be associated with reading the data registers in the dump mode. Reading the status registers is always associated with reading the data registers in the continuous read mode (see the Digital Interface Description section for more details).

| Bit | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Mnemonic | 0 | CH1 | CH0 | 0/P0 | RDY/P1 | NOREF | SIGN | OVR |
| Default | Channel Number | | | 0 | 0 | 0 | 0 | 0 |

| Bit | Mnemonic | Description |
|---|---|---|
| 7 to 5 | CH1 to CH0 | These bits reflect the channel number. This can be used for current channel identification and easier operation of the dump mode and continuous read mode. |
| 4 | 0/P0 | When the status option bit of the corresponding channel setup register is reset to 0, this bit is read as a zero. When the status option bit is set to 1, this bit reflects the state of the P0 pin, whether it is configured as an input or an output. |
| 3 | RDY/P1 | When the status option bit of the corresponding channel setup register is reset to 0, this bit reflects the selected channel RDY bit in the ADC status register. When the status option bit is set to 1, this bit reflects the state of the P1 pin, whether it is configured as an input or an output. |
| 2 | NOREF | This bit indicates the reference input status. If the voltage between the REFIN(+) and REFIN(–) pins is less than NOREF, the trigger voltage and a conversion is executed, then the NOREF bit goes to 1. |
| 1 | SIGN | The voltage polarity at the analog input. It will be 0 for a positive voltage and 1 for a negative voltage. |
| 0 | OVR | This bit reflects either the overrange or the underrange on the analog input. The bit is set to 1 when the analog input voltage goes over or under the nominal voltage range (see the Analog Input's Extended Voltage Range section). |

## CHANNEL SETUP REGISTERS

*8 Bits, Read/Write Register, Address 28h–2Bh, Default Value 00h*

These registers are used to configure the selected channel, to configure its input voltage range, and to set up the corresponding channel status register.

| Bit | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Mnemonic | 0 | 0 | 0 | Stat OPT | ENABLE | 0 | RNG1 | RNG0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Mnemonic | Description |
|---|---|---|
| 7 to 5 | 0 | These bits must be 0 for proper operation. |
| 4 | Stat OPT | Status Option. When this bit is set to 1, the P0 and P1 bits in the channel status register will reflect the state of the P0 and P1 pins. When this bit is reset to 0, the RDY bit in the channel status register will reflect the channel corresponding to the RDY bit in the ADC status register. |
| 3 | ENABLE | Channel Enable. Set this bit to 1 to enable the channel in the continuous conversion mode. A single conversion will take place regardless of this bit's value. |
| 2 | 0 | This bit must be 0 for proper operation. |
| 1 to 0 | RNG1–RNG0 | This is the channel input voltage range (see Table 15). |

**Table 15.**

| RNG1 | RNG0 | Nominal Input Voltage Range |
|---|---|---|
| 0 | 0 | ±10 V |
| 0 | 1 | 0 V to +10 V |
| 1 | 0 | ±5 V |
| 1 | 1 | 0 V to +5 V |

## CHANNEL CONVERSION TIME REGISTERS

*8 Bits, Read/Write Register, Address 30h–33h, Default Value 91h*

The conversion time registers enable or disable chopping and configure the digital filter for a particular channel. This register value affects the conversion time, frequency response, and noise performance of the ADC.

| Bit | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Mnemonic | CHOP | FW (7-Bit Filter Word) | | | | | | |
| Default | 1 | 11h | | | | | | |

| Bit | Mnemonic | Description |
|---|---|---|
| 7 | CHOP | Chopping Enable Bit. Set to 1 to apply chopping mode for a particular channel. |
| 6 to 0 | FW | CHOP = 1, single conversion or continuous conversion with one channel enabled.<br>Conversion Time (μs) = (FW × 128 + 248)/MCLK Frequency (MHz), the FW range is 2 to 127.<br>CHOP = 1, continuous conversion with two or more channels enabled.<br>Conversion Time (μs) = (FW × 128 + 249)/MCLK Frequency (MHz), the FW range is 2 to 127.<br>CHOP = 0, single conversion or continuous conversion with one channel enabled.<br>Conversion Time (μs) = (FW × 64 + 206)/MCLK Frequency (MHz), the FW range is 3 to 127.<br>CHOP = 0, continuous conversion with two or more channels enabled.<br>Conversion Time (μs) = (FW × 64 + 207)/MCLK Frequency (MHz), the FW range is 3 to 127. |

## MODE REGISTER

*8 Bits, Read/Write Register, Address 38h–3Bh, Default Value 00h*

The mode register configures the device and determines its operating mode. Writing to the mode register clears the ADC status register, sets the $\overline{RDY}$ pin to a logic high level, exits all current operations, and starts the mode specified by the mode bits.

The AD7734 contains only one mode register. The two LSBs of the address are used for writing to the mode register to specify the channel selected for the operation determined by the MD2 to MD0 bits. Only the address 38h must be used for reading from the mode register.

| Bit | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Mnemonic | MD2 | MD1 | MD0 | CLKDIS | DUMP | Cont RD | 24/16 BIT | CLAMP |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Mnemonic | Description |
|---|---|---|
| 7 to 5 | MD2–MD0 | Mode Bits. These three bits determine the AD7734 operation mode. Writing a new value to the mode bits will exit the device from the mode in which it has been operating and place it in the newly requested mode immediately. The function of the mode bits is described in more detail below. |
| 4 | CLKDIS | Master Clock Output Disable. When this bit is set to 1, the master clock is disabled from appearing at the MCLKOUT pin and the MCLKOUT pin is in a high impedance state. This allows turning off the MCLKOUT as a power saving feature. When using an external clock on MCLKIN, the AD7734 continues to have internal clocks and will convert normally regardless of the CLKDIS bit state. When using a crystal oscillator or ceramic resonator across the MCLKIN and MCLKOUT pins, the AD7734 clock is stopped and no conversions can take place when the CLKDIS bit is active. The AD7734 digital interface can still be accessed using the SCLK pin. |
| 3 | DUMP | DUMP Mode. When this bit is reset to 0, the channel status register and channel data register will be addressed and read separately. When the DUMP bit is set to 1, the channel status register will be followed immediately by a read of the channel data register regardless of whether the status or data register has been addressed through the communication register. The continuous read mode will always be dump mode reading of the channel status and data register, regardless of the dump bit value (see the Digital Interface Description section for more details). |
| 2 | Cont RD | When this bit is set to 1, the AD7734 will operate in the continuous read mode (see the Digital Interface Description section for more details). |
| 1 | 24/16 BIT | The Channel Data Register Data Width Selection Bit. When set to 1, the channel data registers will be 24 bits wide. When set to 0, the channel data registers will be 16 bits wide. |
| 0 | CLAMP | This bit determines the channel data register's value when the analog input voltage is outside the nominal input voltage range. When the CLAMP bit is set to 1, the channel data register will be digitally clamped either to all 0s or to all 1s when the analog input voltage goes outside the nominal input voltage range. When the CLAMP bit is reset to 0, the data registers reflect the analog input voltage even outside the nominal voltage range (see the Analog Input's Extended Voltage Range section). |

| MD2 | MD1 | MD0 | Mode | Address Used for Mode Register Write Specifies: |
|---|---|---|---|---|
| 0 | 0 | 0 | Idle Mode | |
| 0 | 0 | 1 | Continuous Conversion Mode | The First Channel to Start Converting |
| 0 | 1 | 0 | Single Conversion Mode | Channel to Convert |
| 0 | 1 | 1 | Power-Down (Standby) Mode | |
| 1 | 0 | 0 | ADC Zero-Scale Self-Calibration | Channel Conversion Time Used for the ADC Self-Calibration |
| 1 | 0 | 1 | For Future Use | |
| 1 | 1 | 0 | Channel Zero-Scale System Calibration | Channel to Calibrate |
| 1 | 1 | 1 | Channel Full-Scale System Calibration | Channel to Calibrate |

| MD2 | MD1 | MD0 | Operating Mode |
|---|---|---|---|
| 0 | 0 | 0 | Idle Mode<br>The default mode after power-on or reset.<br>The AD7734 automatically returns to this mode after any calibration or after a single conversion. |
| 0 | 0 | 1 | Continuous Conversion Mode<br>The AD7734 performs a conversion on the specified channel. After the conversion is complete, the relevant channel data register and channel status register are updated, the relevant RDY bit in the ADC status register is set, and the AD7734 continues converting on the next enabled channel. The devices will cycle through all enabled channels until it is put into another mode or reset. The cycle period will be the sum of all enabled channels' conversion times, set by the corresponding channel conversion time registers. |
| 0 | 1 | 0 | Single Conversion Mode<br>The AD7734 performs a conversion on the specified channel. After the conversion is complete, the relevant channel data register and channel status register are updated, the relevant RDY bit in the ADC status register is set, the $\overline{RDY}$ pin goes low, the MD2–MD0 bits are reset, and the AD7734 returns to idle mode. Requesting a single conversion ignores the channel setup register enable bits; a conversion will be performed even if that channel is disabled. |
| 0 | 1 | 1 | Power-Down (Standby) Mode<br>The ADC and the analog front end (internal buffer) go into the power-down mode.<br>The AD7734 digital interface can still be accessed. The CLKDIS bit works separately, and the MCLKOUT mode is not affected by the power-down (standby) mode. |
| 1 | 0 | 0 | ADC Zero-Scale Self-Calibration Mode<br>A zero-scale self-calibration is performed on internally shorted ADC inputs.<br>After the calibration is complete, the contents of the ADC zero-scale calibration register are updated, all RDY bits in the ADC status register are set, the $\overline{RDY}$ pin goes low, the MD2–MD0 bits are reset, and the AD7734 returns to idle mode. |
| 1 | 0 | 1 | For Future Use. |
| 1 | 1 | 0 | Channel Zero-Scale System Calibration Mode<br>A zero-scale system calibration is performed on the selected channel. An external system zero-scale voltage should be provided at the AD7734 analog input and this voltage should remain stable for the duration of the calibration. After the calibration is complete, the contents of the corresponding channel zero-scale calibration register are updated, all RDY bits in the ADC status register are set, the $\overline{RDY}$ pin goes low, the MD2–MD0 bits are reset, and the AD7734 returns to idle mode. |
| 1 | 1 | 1 | Channel Full-Scale System Calibration Mode<br>A full-scale system calibration is performed on the selected channel. An external system full-scale voltage should be provided at the AD7734 analog input and this voltage should remain stable for the duration of the calibration. After the calibration is complete, the contents of the corresponding channel full-scale calibration register are updated, all RDY bits in the ADC status register are set, the $\overline{RDY}$ pin goes low, the MD2–MD0 bits are reset, and the AD7734 returns to idle mode. |

# DIGITAL INTERFACE DESCRIPTION

## HARDWARE

The AD7734 serial interface can be connected to the host device via the serial interface in several different ways.

The $\overline{CS}$ pin can be used to select the AD7734 as one of several circuits connected to the host serial interface. When $\overline{CS}$ is high, the AD7734 ignores the SCLK and DIN signals and the DOUT pin goes to the high impedance state. When the $\overline{CS}$ signal is not used, connect the $\overline{CS}$ pin to DGND.

The $\overline{RDY}$ pin can be polled for high-to-low transition or can drive the host device interrupt input to indicate that the AD7734 has finished the selected operation and/or that new data from the AD7734 is available. The host system can also wait a designated time after a given command is written to the device before reading. Alternatively, the AD7734 status can be polled. When the $\overline{RDY}$ pin is not used in the system, it should be left as an open circuit. (Note that the $\overline{RDY}$ pin is always an active digital output. It never goes into a high impedance state.)

The $\overline{RESET}$ pin can be used to reset the AD7734. When not used, connect this pin to $DV_{DD}$.

The AD7734 interface can be reduced to just two wires connecting the DIN and DOUT pins to a single bidirectional data line. The second signal in this 2-wire configuration is the SCLK signal. The host system should change the data line direction with reference to the AD7734 timing specification (see the Bus Relinquish Time in Table 2). The AD7734 cannot operate in the continuous read mode in 2-wire serial interface configuration.

All the digital interface inputs are Schmitt-Triggered; therefore, the AD7734 interface features higher noise immunity and can be easily isolated from the host system via optocouplers. Figure 13, Figure 14, and Figure 15 outline some of the possible host device interfaces: SPI without using the $\overline{CS}$ signal (Figure 13), a DSP interface (Figure 14), and a 2-wire configuration (Figure 15).

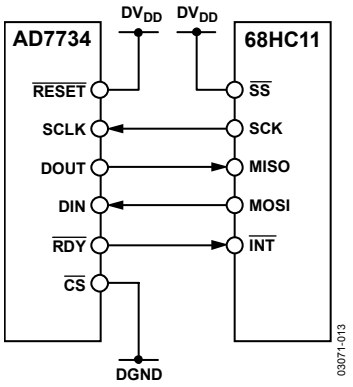


*Figure 13. AD7734 to Host Device Interface, SPI*

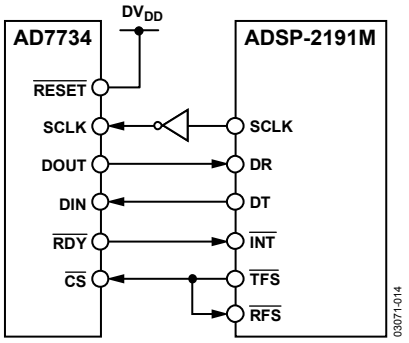


*Figure 14. AD7734 to Host Device Interface, DSP*

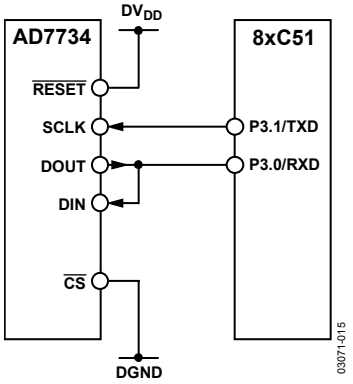


*Figure 15. AD7734 to Host Device Interface, 2-Wire Configuration*

## RESET

The AD7734 can be reset by the $\overline{\text{RESET}}$ pin or by writing a reset sequence to the AD7734 serial interface.

The reset sequence is N × 0 + 32 × 1, which could be the data sequence 00h + FFh + FFh + FFh + FFh in a byte-oriented interface. The AD7734 also features a power-on reset with a trip point of 2 V and goes to the defined default state after power-on.

It is the responsibility of the system designer to prevent an unwanted write operation to the AD7734. The unwanted write operation can happen when a spurious clock appears on the SCLK while the $\overline{\text{CS}}$ pin is low. It should be noted that on system power-on, if the AD7734 interface signals are floating or undefined, the device can inadvertently be configured into an unknown state. This can be overcome easily by initiating either a hardware reset event or a 32 ones reset sequence as the first step in the system configuration.

## ACCESS THE AD7734 REGISTERS

All communications to the device start with a write operation to the communications register followed by either reading or writing the addressed register.

In a simultaneous read-write interface (such as SPI), write 0 to the AD7734 while reading data.

Figure 16 shows the AD7734 interface read sequence for the ADC status register.

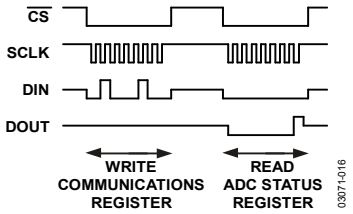


*Figure 16. Serial Interface Signals—Registers Access*

## SINGLE CONVERSION AND READING DATA

When the mode register is being written, the ADC status byte is cleared and the $\overline{\text{RDY}}$ pin goes high, regardless of its previous state. When the single conversion command is written to the mode register, the ADC starts the conversion on the channel selected by the address of the mode register. After the conversion is completed, the data register is updated, the mode register is changed to idle mode, the relevant RDY bit is set, and the $\overline{\text{RDY}}$ pin goes low. The RDY bit is reset and the $\overline{\text{RDY}}$ pin returns high when the relevant channel data register is being read.

Figure 17 shows the digital interface signals executing a single conversion on Channel 0, waiting for the $\overline{\text{RDY}}$ pin to go low, and reading the Channel 0 data register.

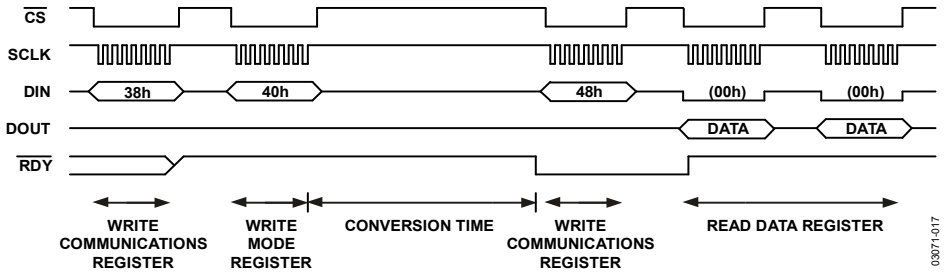


*Figure 17. Serial Interface Signals—Single Conversion Command and 16-Bits Data Reading*

## DUMP MODE

When the DUMP bit in the mode register is set to 1, the channel status register will be read immediately by a read of the channel data register, regardless of whether the status or the data register has been addressed through the communications register. The DIN pin should not be high while reading 24-bit data in dump mode; otherwise, the AD7734 will be reset.

Figure 18 shows the digital interface signals executing a single conversion on Channel 0, waiting for the $\overline{RDY}$ pin to go low, and reading the Channel 0 status register and data register in the dump mode.

## CONTINUOUS CONVERSION MODE

When the mode register is being written, the ADC status byte is cleared and the $\overline{RDY}$ pin goes high, regardless of its previous state. When the continuous conversion command is written to the mode register, the ADC starts conversion on the channel selected by the address of the mode register.

After the conversion is complete, the relevant channel data register and channel status register are updated, the relevant RDY bit in the ADC status register is set, and the AD7734 continues converting on the next enabled channel. The device will cycle through all enabled channels until put into another mode or reset. The cycle period will be the sum of all enabled channels' conversion times, set by the corresponding channel conversion time registers.

The RDY bit is reset when the relevant channel data register is being read. The behavior of the $\overline{RDY}$ pin depends on the RDYFN bit in the I/O port register. When the RDYFN bit is 0, the $\overline{RDY}$ pin goes low when any channel has unread data. When the RDYFN bit is set to 1, the $\overline{RDY}$ pin will only go low if all enabled channels have unread data.

If an ADC conversion result has not been read before a new ADC conversion is completed, the new result will overwrite the previous one. The relevant RDY bit goes low and the $\overline{RDY}$ pin goes high for at least 163 MCLK cycles (approximately 26.5 μs), indicating when the data register is updated, and the previous conversion data is lost.

If the data register is being read as an ADC conversion completes, the data register will not be updated with the new result (to avoid data corruption) and the new conversion data is lost.

Figure 19 shows the digital interface signal's sequence for the continuous conversion mode with Channels 0 and 1 enabled and the RDYFN bit set to 0. The $\overline{RDY}$ pin goes low and the data register is read after each conversion. Figure 20 shows a similar sequence but with the RDYFN bit set to 1. The $\overline{RDY}$ pin goes low and all data registers are read after all conversions are completed. Figure 21 shows the $\overline{RDY}$ pin when no data are read from the AD7734.

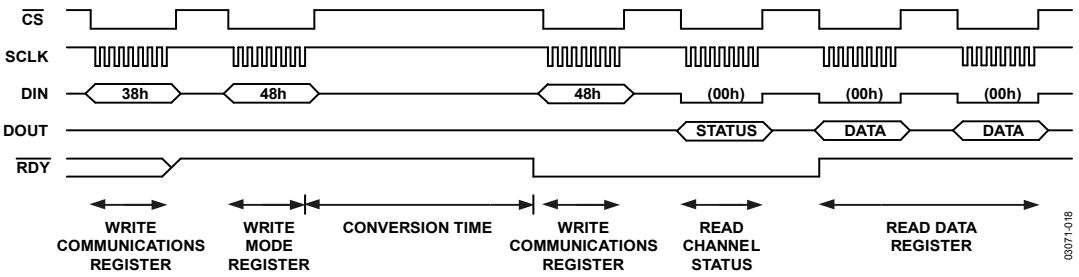


*Figure 18. Serial Interface Signals—Single Conversion Command, 16-Bits Data Reading, Dump Mode*

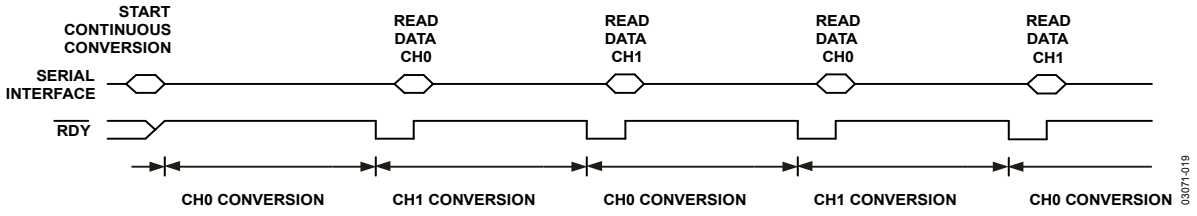


*Figure 19. Continuous Conversion, CH0 and CH1, RDYFN = 0*

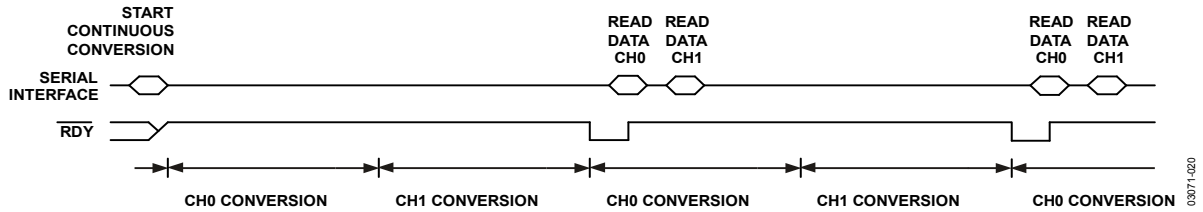


*Figure 20. Continuous Conversion, CH0 and CH1, RDYFN = 1*

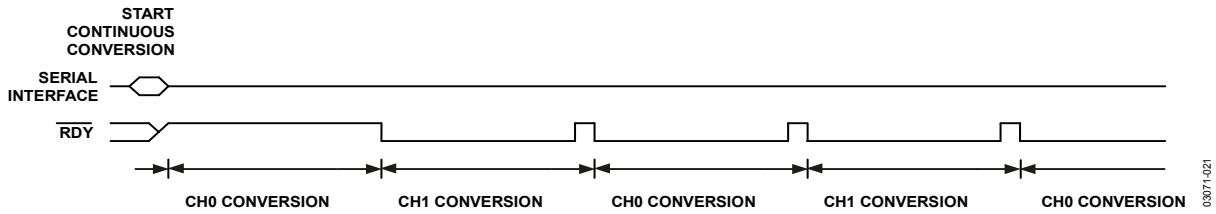


*Figure 21. Continuous Conversion, CH0 and CH1, No Data Read*

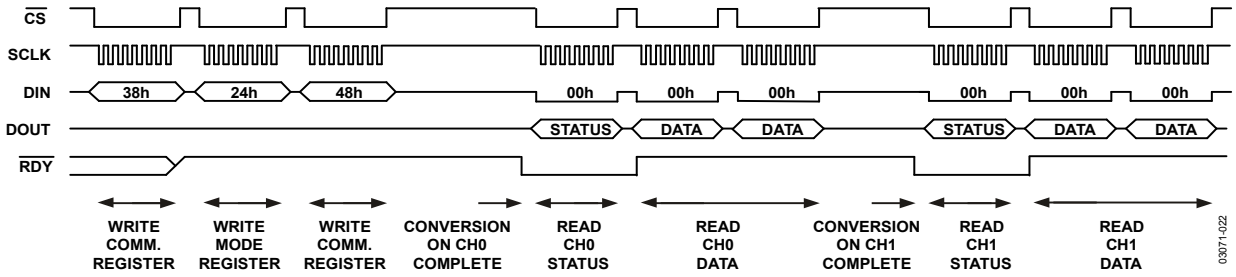


*Figure 22. Continuous Conversion, CH0 and CH1, Continuous Read*

## CONTINUOUS READ (CONTINUOUS CONVERSION) MODE

When the Cont RD bit in the mode register is set, the first write of 48h to the communications register starts the continuous read mode. As shown in Figure 22, subsequent accesses to the device sequentially read the channel status and data registers of the last completed conversion without any further configuration of the communications register being required.

Note that the continuous conversion bit in the mode register should be set when entering the continuous read mode.

Note that the continuous read mode is a dump mode reading of the channel status and data registers regardless of the dump bit value. Use the channel bits in the channel status register to check/recognize which channel data is actually being shifted out.

Note that the last completed conversion result is being read. Therefore, the RDYFN bit in the I/O port register should be 0, and reading the result should always start before the next conversion is completed.

The AD7734 will stay in continuous read mode as long as the DIN pin is low while the $\overline{CS}$ pin is low; therefore, write 0 to the AD7734 while reading in continuous read mode. To exit continuous read mode, take the DIN pin high for at least 100 ns after a read is complete. (Write 80h to the AD7734 to exit continuous reading.)

Taking the DIN pin high does not change the Cont RD bit in the mode register. Therefore, the next write of 48h starts the continuous read mode again. To stop the continuous read mode completely, write to the mode register to clear the Cont RD bit.

# CIRCUIT DESCRIPTION

The AD7734 is a Σ-Δ ADC that is intended for the measurement of wide dynamic range, low frequency signals in industrial process control, instrumentation, and PLC systems.

It contains thin film resistor dividers, a multiplexer, an input buffer, a Σ-Δ (or charge balancing) ADC, a digital filter, a clock oscillator, a digital I/O port, and a serial communications interface.

## ANALOG FRONT END

The AD7734 features four single-ended analog inputs. The on-chip thin film resistor dividers allow ±10 V, ±5 V, 0 V to +10 V, and 0 V to +5 V input signals to be connected directly to the analog input pins.

The resistor divider input stage is followed by the multiplexer and then by a wide bandwidth, fast settling time differential input buffer capable of driving the dynamic load of a high speed Σ-Δ modulator.

In normal circuit configuration, the BIAS0 to BIAS3 and BIASHI pins are connected to the 2.5 V (reference) voltage source and the BIASLO pin is connected to 0 V. This ensures that the differential signal seen by the internal input buffer is within its absolute/common-mode range of AGND + 200 mV to $AV_{DD}$ – 300 mV.

The AD7734 AIN voltage should be within the specified nominal (up to ±10 V) input range, otherwise the performance on channel might degrade (see the Analog Input's Extended Voltage Range section).

If the BIAS pins are in normal configuration, the AIN pin absolute voltage up to ±16.5 V does not degrade the adjacent channel's performance. An AIN absolute voltage over ±16.5 V results in current flowing through the internal protection diodes located behind the thin film resistors and the adjacent channel can be affected.

The AIN pins are overvoltage tolerant. However, the absolute maximum AIN voltage of ±50 V must never be exceeded.

Note that the OVR bit in the channel status register is generated digitally from the conversion result and indicates the Σ-Δ modulator (nominal) overrange. The OVR bit does not indicate exceeding the AIN pin absolute voltage limits.

Figure 23 shows the AD7734 analog input internal structure.

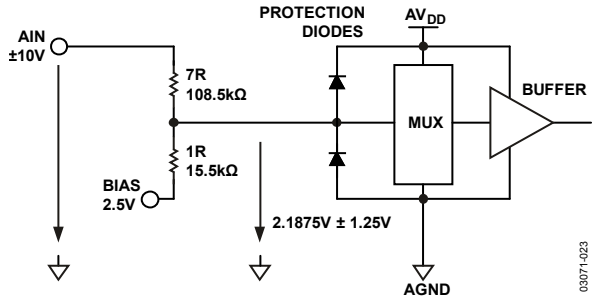


*Figure 23. Simplified Analog Input Internal Structure*

## ANALOG INPUT'S EXTENDED VOLTAGE RANGE

The AD7734 output data code span corresponds to the nominal input voltage range. The ADC is functional outside the nominal input voltage range, but the performance might degrade. The Σ-Δ modulator was designed to fully cover a ±11.6 V analog input voltage; outside this range, the performance might degrade more rapidly. The adjacent channels are not affected by up to ±16.5 V analog input voltage (Figure 8).

When the CLAMP bit in the mode register is set to 1, the channel data register will be digitally clamped to either all 0s or all 1s when the analog input voltage goes outside the nominal input voltage range.

As shown in Table 16 and Table 17, when CLAMP = 0, the data reflects the analog input voltage outside the nominal voltage range. In this case, the SIGN and OVR bits in the channel status register should be considered along with the data register value to decode the actual conversion result.

Note that the OVR bit in the channel status register is generated digitally from the conversion result and indicates the Σ-Δ modulator (nominal) overrange. The OVR bit does not indicate exceeding the absolute voltage limits of the AIN pin.

**Table 16. Extended Input Voltage Range, Nominal Voltage Range ±10 V, 16 Bits, CLAMP = 0**

| Input (V) | Data (hex) | SIGN | OVR |
|---|---|---|---|
| 11.60039 | 147B | 0 | 1 |
| 10.00061 | 0001 | 0 | 1 |
| 10.00031 | 0000 | 0 | 1 |
| 10.00000 | FFFF | 0 | 0 |
| 0.00031 | 8001 | 0 | 0 |
| 0.00000 | 8000 | 0 | 0 |
| –0.00031 | 7FFF | 1 | 0 |
| –10.00000 | 0000 | 1 | 0 |
| –10.00031 | FFFF | 1 | 1 |
| –10.00061 | FFFE | 1 | 1 |
| –11.60040 | EB85 | 1 | 1 |

**Table 17. Extended Input Voltage Range, Nominal Voltage Range 0 V to +10 V, 16 Bits, CLAMP = 0**

| Input (V) | Data (hex) | SIGN | OVR |
|---|---|---|---|
| 11.60006 | 28F5 | 0 | 1 |
| 10.00031 | 0001 | 0 | 1 |
| 10.00015 | 0000 | 0 | 1 |
| 10.00000 | FFFF | 0 | 0 |
| 0.00015 | 0001 | 0 | 0 |
| 0.00000 | 0000 | 0 | 0 |
| –0.00015 | 0000 | 1 | 1 |

## CHOPPING

With chopping enabled, the multiplexer repeatedly reverses the ADC inputs. Every output data result is then calculated as an average of two conversions, the first with the positive and the second with the negative offset term included. This effectively removes any offset error of the input buffer and Σ-Δ modulator.

However, chopping is applied only behind the input resistor divider stage; therefore, chopping does not eliminate the offset error and drifts caused by the resistors. Figure 24 shows the channel signal chain with chopping enabled.

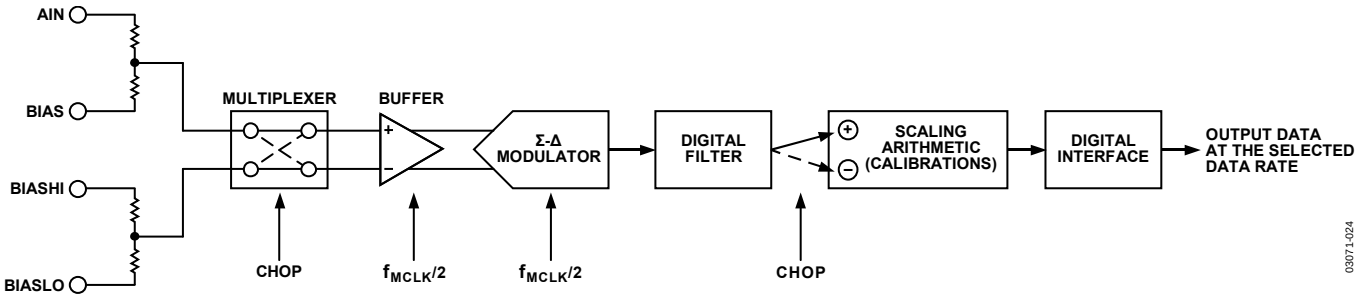


*Figure 24. Channel Signal Chain Diagram with Chopping Enabled*

## MULTIPLEXER, CONVERSION, AND DATA OUTPUT TIMING

The specified conversion time includes one or two settling and sampling periods and a scaling time.

With chopping enabled (Figure 25), a conversion cycle starts with a settling time of 43 MCLK cycles or 44 MCLK cycles (approximately 7 µs with a 6.144 MHz MCLK) to allow the circuits following the multiplexer to settle. The Σ-Δ modulator then samples the analog signals and the digital filter processes the digital data stream. The sampling time depends on FW, that is, on the channel conversion time register contents. After another settling of 42 MCLK cycles (approximately 6.8 µs), the sampling time is repeated with a reversed (chopped) analog input signal. Then, during the scaling time of 163 MCLK cycles (approximately 26.5 µs), the two results from the digital filter are averaged, scaled using the calibration registers, and written into the channel data register.

With chopping disabled (Figure 26), there is only one sampling time preceded by a settling time of 43 MCLK cycles or 44 MCLK cycles and followed by a scaling time of 163 MCLK cycles.

The $\overline{\text{RDY}}$ pin goes high during the scaling time, regardless of its previous state. The relevant RDY bit is set in the ADC status register and in the channel status register, and the $\overline{\text{RDY}}$ pin goes low when the channel data register is updated and the channel conversion cycle is finished. If in continuous conversion mode, the device will automatically continue with a conversion cycle on the next enabled channel.

Note that every channel can be configured independently for conversion time and chopping mode. The overall cycle and effective per channel data rates depend on all enabled channel settings.

## Σ-Δ ADC

The AD7734 core consists of a charge balancing Σ-Δ modulator and a digital filter. The architecture is optimized for fast, fully settled conversion. This allows for fast channel-to-channel switching while maintaining inherently excellent linearity, high resolution, and low noise.

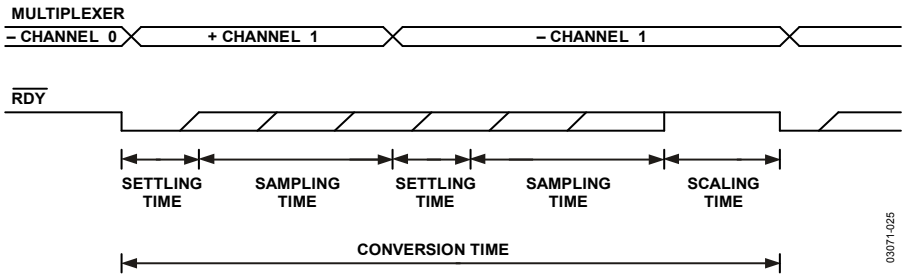


*Figure 25. Multiplexer and Conversion Timing—Continuous Conversion on Several Channels with Chopping Enabled*

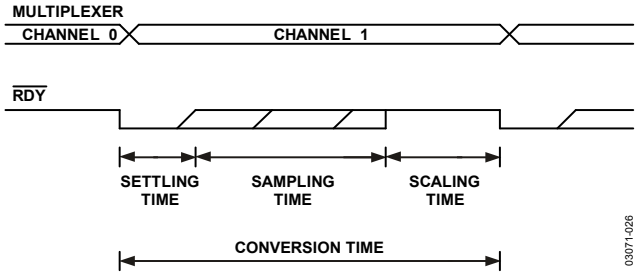


*Figure 26. Multiplexer and Conversion Timing—Continuous Conversion on Several Channels with Chopping Disabled*

## FREQUENCY RESPONSE

The Σ-Δ modulator runs at ½ the MCLK frequency, which is effectively the sampling frequency. Therefore, the Nyquist frequency is ¼ the MCLK frequency. The digital filter, in association with the modulator, features the frequency response of a first order low-pass filter. The –3 dB point is close to the frequency of 1/channel conversion time. The roll-off is –20 dB/dec up to the Nyquist frequency. If chopping is enabled, the input signal is resampled by chopping. Therefore, the overall frequency response features notches close to the frequency of 1/channel conversion time. The top envelope is again the ADC response of –20 dB/dec.

The typical frequency response plots are given in Figure 27 and Figure 28. The plots are normalized to 1/channel conversion time.

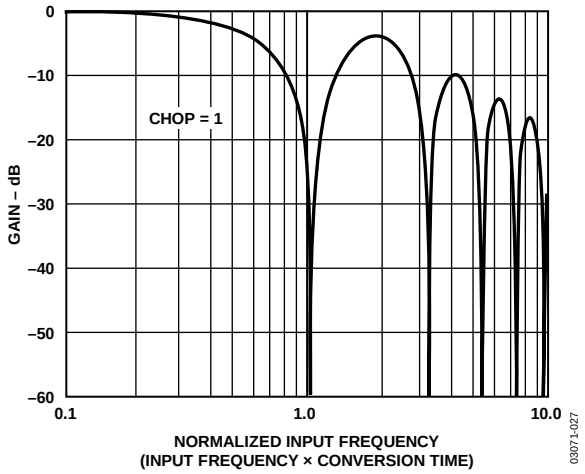


*Figure 27. Typical ADC Frequency Response, Chopping Enabled*

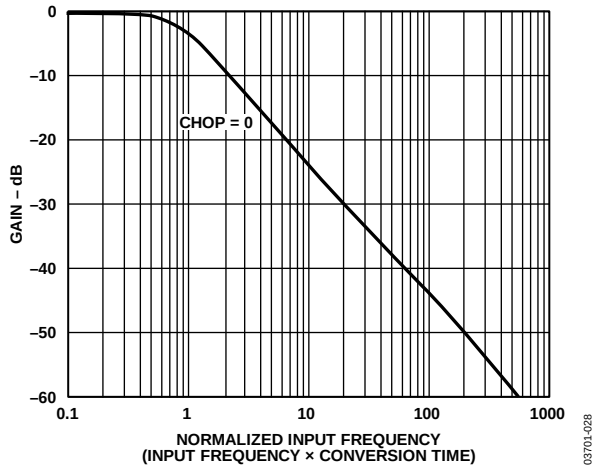


*Figure 28. Typical ADC Frequency Response, Chopping Disabled*

## VOLTAGE REFERENCE INPUTS

The AD7734 has a differential reference input, REF IN(+) and REF IN(–). The common-mode range for these inputs is from AGND to $AV_{DD}$. The nominal differential reference voltage for specified operation is 2.5 V. Both reference inputs feature dynamic load. Therefore, the reference inputs should be connected to a low impedance reference voltage source. External resistance/capacitance combinations may result in gain errors on the device.

The output noise performance outlined in Table 4 through Table 9 is for an analog input of 0 V and is unaffected by noise on the reference. To obtain the same noise performance as shown in the noise tables over the full input range requires a low noise reference source for the AD7734. If the reference noise in the bandwidth of interest is excessive, it will degrade the performance of the AD7734.

Recommended reference voltage sources for the AD7734 include the AD780, ADR421, REF43, and REF192. Note that in a typical connection, the voltage reference must be capable of sinking current flowing out of the BIAS pins through the internal resistors if a positive voltage is applied to the analog input. The AD780 meets this requirement. If the voltage reference used in an application is not capable of sinking current, an external resistor (5 kΩ) should be connected in parallel to the REFIN pins.

## REFERENCE DETECT

The AD7734 includes on-chip circuitry to detect if the device has a valid reference for conversions. If the voltage between the REFIN(+) and REFIN(–) pins goes below the NOREF trigger voltage (0.5 V typ.) and the AD7734 is performing a conversion, the NOREF bit in the channel status register is set.

## I/O PORT

The AD7734 P0 pin can be used as a general-purpose digital I/O pin. The P1 pin ($\overline{SYNC}$/P1) can be used as a general-purpose digital I/O pin or to synchronize the AD7734 with other devices in the system. When the SYNC bit in the I/O port register is set and the $\overline{SYNC}$ pin is low, the AD7734 does not process any conversion. If it is put into single conversion mode, continuous conversion mode, or any calibration mode, the AD7734 waits until the $\overline{SYNC}$ pin goes high and then starts operation. This allows conversion to start from a known point in time, that is, the rising edge of the $\overline{SYNC}$ pin.

The digital P0 and P1 voltage is referenced to the analog supplies. When configured as inputs, the pins should be tied high or low.

## CALIBRATION

The AD7734 provides zero-scale self-calibration, and zero-scale and full-scale system calibration capability that can effectively reduce the offset error and gain error to the order of the noise. After each conversion, the ADC conversion result is scaled using the ADC calibration registers and the relevant channel calibration registers before being written to the data register.

For unipolar ranges:

Data = ((ADC result − ADC ZS Cal. reg.) × ADC FS Reg./200000h − Ch. ZS Cal. reg.) × Ch. FS Cal. reg./200000h

For bipolar ranges:

Data = ((ADC result − ADC ZS Cal. reg.) × ADC FS Reg./400000h + 800000h − Ch. ZS Cal. reg.) × Ch. FS Cal. reg./200000h

Where the ADC result is in the range of 0 to FFFFFFh.

Note that the channel zero-scale calibration register has the format of a sign bit and a 22-bit channel offset value.

It is strongly recommended that the user not change the ADC full-scale register.

To start any calibration, write the relevant mode bits to the AD7734 mode register. After the calibration is complete, the contents of the corresponding calibration registers are updated, all RDY bits in the ADC status register are set, the $\overline{SYNC}$ pin goes low, and the AD7734 reverts to idle mode. The calibration duration is the same as the conversion time configured on the selected channel. A longer conversion time gives less noise and yields a more exact calibration; therefore, use at least the default conversion time to initiate any calibration.

## ADC ZERO-SCALE SELF-CALIBRATION

The ADC zero-scale self-calibration can reduce the offset error in the chopping disabled mode. If repeated after a temperature change, it can also reduce the offset drift error in the chopping disabled mode.

The zero-scale self-calibration is performed on internally shorted ADC inputs. The negative analog input terminal on the selected channel is used to set the ADC zero-scale calibration common mode. Therefore, either the negative terminal of the selected differential pair or the AINCOM on the single-ended channel configuration should be driven to a proper common-mode voltage.

It is strongly recommended that the ADC zero-scale calibration register should only be updated as part of a zero-scale self-calibration.

## PER CHANNEL SYSTEM CALIBRATION

If the per channel system calibrations are used, these should be initiated in the following order: a channel zero-scale system calibration, followed by a channel full-scale system calibration.

The system calibration is affected by the ADC zero-scale and full-scale calibration registers. Therefore, if both self-calibration and system calibration are used in the system, an ADC full-scale self-calibration should be performed first, followed by a system calibration cycle.

While executing a system calibration, the fully settled system zero-scale voltage signal or system full-scale voltage signal must be connected to the selected channel analog inputs.

The per channel calibration registers can be read, stored, or modified and written back to the AD7734. Note that when writing the calibration registers the AD7734 must be in idle mode. Note that outside the specified calibration range, calibration is possible but the performance may degrade (see the System Calibration parameter in Table 1).

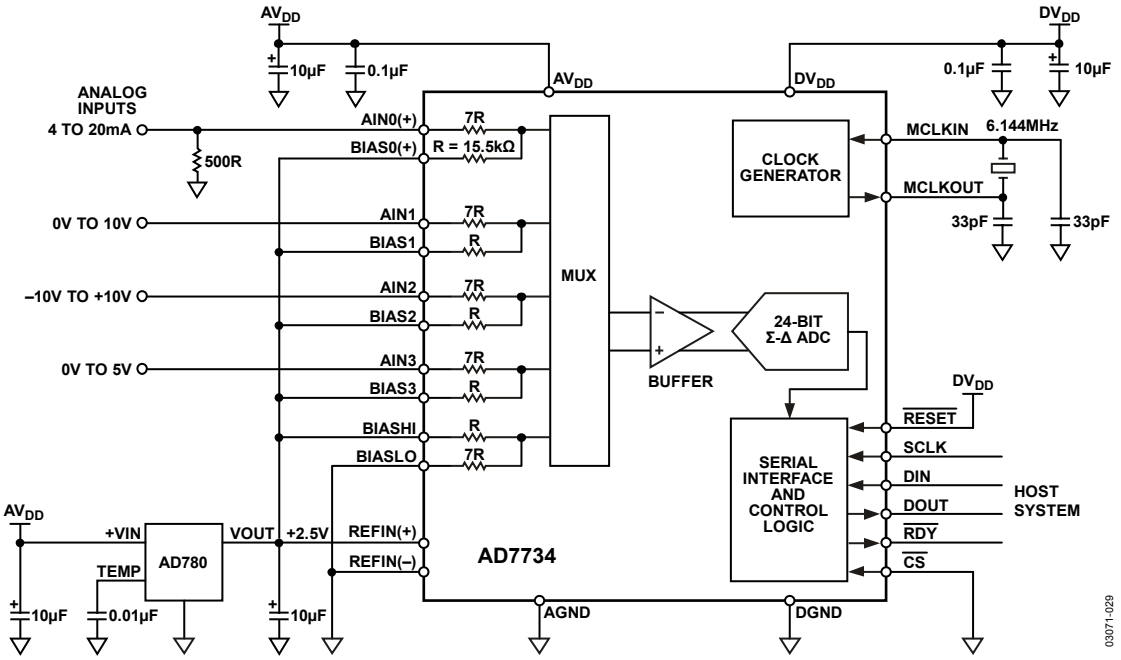


*Figure 29. Typical Connections for the AD7734 Application*

# OUTLINE DIMENSIONS

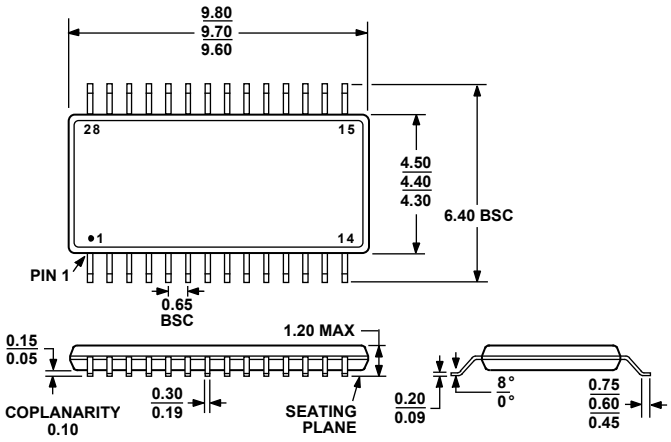


*Figure 30. 28-Lead Thin Shrink Small Outline Package [TSSOP]*
*(RU-28)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD7734BRU | –40°C to +105°C | 28-Lead Thin Shrink Small Outline Package [TSSOP] | RU-28 |
| AD7734BRUZ | –40°C to +105°C | 28-Lead Thin Shrink Small Outline Package [TSSOP] | RU-28 |
| AD7734BRUZ-REEL7 | –40°C to +105°C | 28-Lead Thin Shrink Small Outline Package [TSSOP] | RU-28 |
| EVAL-AD7734EBZ | | Evaluation Board | |

[1] Z = RoHS Compliant Part.

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