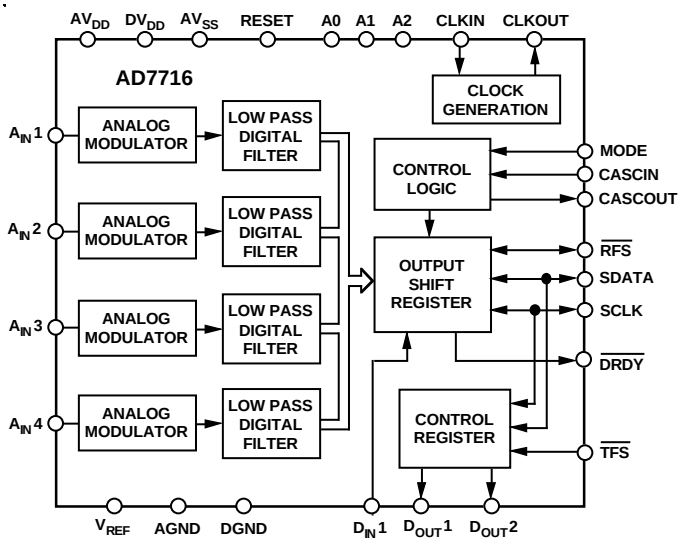
LC²MOS
22-Bit Data Acquisition System

AD7716

FEATURES
22-Bit Sigma-Delta ADC
Dynamic Range of 105 dB (146 Hz Input)
±0.003% Integral Nonlinearity
On-Chip Low-Pass Digital Filter
Cutoff Programmable from 584 Hz to 36.5 Hz
Linear Phase Response
Five Line Serial I/O
Twos Complement Coding
Easy Interface to DSPs and Microcomputers
Software Control of Filter Cutoff
±5 V Supply
Low Power Operation: 50 mW

APPLICATIONS
Biomedical Data Acquisition
ECG Machines
EEG Machines
Process Control
High Accuracy Instrumentation
Seismic Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7716 is a signal processing block for data acquisition systems. It is capable of processing four channels with bandwidths of up to 584 Hz. Resolution is 22 bits and the usable dynamic range varies from 111 dB with an input bandwidth of 36.5 Hz to 99 dB with an input bandwidth of 584 Hz.

The device consists of four separate A/D converter channels that are implemented using sigma-delta technology. Sigma-delta ADCs include on-chip digital filtering and, thus, the system filtering requirements are eased.

Three address pins program the device address. This allows a data acquisition system with up to 32 channels to be set up in a simple fashion. The output word from the device contains 32 bits of data. One bit is determined by the state of the $D_{IN}1$ input and may be used, for example, in an ECG system with an external pacemaker detect circuit to indicate that the output word is invalid because of the presence of a pacemaker pulse.

There are 22 bits of data corresponding to the analog input. Two bits contain the channel address and 3 bits are the device address. Thus, each channel in a 32-channel system would have a discrete 5-bit address. The device also has a CASCOUT pin and a CASCIN pin that allow simple networking of multiple devices.

The on-chip control register is programmed using the SCLK, SDATA and $\overline{TFS}$ pins. Three bits of the Control Register set the digital filter cutoff frequency for the device. Selectable frequencies are 584 Hz, 292 Hz, 146 Hz, 73 Hz and 36.5 Hz. A further 2 bits appear as outputs $D_{OUT}1$ and $D_{OUT}2$ and can be used for controlling calibration at the front end. The device is available in a 44-pin PQFP (Plastic Quad Flatpack) and 44-pin PLCC.

REV. A

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AD7716—SPECIFICATIONS[1, 2] (f_{CLKIN} = 8 MHz; MODE Pin Is High (Slave Mode Operation); AV_{DD} = DV_{DD} = +5 V ± 5%; AV_{SS} = –5 V ± 5%; AGND = DGND = 0 V; V_{REF} = 2.5 V; Filter Cutoff = 146 Hz; Noise Measurement Bandwidth = 146 Hz; A_{IN} Source Resistance = 750 Ω[2] with 1 nF to AGND at each A_{IN}. T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	B Version	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution	22	Bits	
Integral Linearity Error	0.003	% FSR typ	Guaranteed No Missed Codes to 21 Bits[3]
	0.006	% FSR max	
Gain Error	1	% FSR max	
Gain Match Between Channels	0.5	% FSR max	
Gain TC	30	μV/°C typ	
Offset Error	0.2	% FSR max	
Offset Match Between Channels	0.1	% FSR max	
Offset TC	4	μV/°C typ	
Noise	11	μV rms max	See Table I for Typical Noise Performance vs. Programmed Cutoff Frequency
DYNAMIC PERFORMANCE			
Sampling Rate	$f_{CLKIN}/14$		570 kHz for f_{CLKIN} = 8 MHz
Output Update Rate	$f_{CLKIN}/(14 \times 256 \times 2^N)$		N Is Decimal Equivalent of FC2, FC1, FC0 in Control Register
Filter Cutoff Frequency	$f_{CLKIN}/(3.81 \times 14 \times 256 \times 2^N)$		
Settling Time	$(3 \times 14 \times 256 \times 2^N/f_{CLKIN})$		
Usable Dynamic Range[4]	See Table I		
Total Harmonic Distortion	–90	dB typ	Input Frequency = 35 Hz
	–100	dB typ	A_{IN} = ±10 mV p-p
Absolute Group Delay[3]	$(3 \times 14 \times 256 \times 2^N)/2f_{CLKIN}$		
Differential Group Delay[3]	10	ns typ	
Channel-to-Channel Isolation	–85	dB typ	Feedthrough from Any One Channel to the Other Three, with 35 Hz Full-Scale Sine Wave Applied to that Channel
ANALOG INPUT			
Input Range	±2.5	Volts	
Input Capacitance	10	pF typ	
Input Bias Current	1	nA typ	
LOGIC INPUTS			
V_{INH}, Input High Voltage	2.4	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{IN}, Input Current			
SDATA, $\overline{RFS}$	+10/-130	μA max	Internal 50 kΩ Pull-Up Resistors
$\overline{TFS}$	+10/-650	μA max	Internal 10 kΩ Pull-Up Resistor
All Other Inputs	±10	μA max	
C_{IN}, Input Capacitance[3]	10	pF max	
LOGIC OUTPUTS			
V_{OH}, Output High Voltage	2.4	V min	$\|I_{OUT}\| \leq 40$ μA
V_{OL}, Output Low Voltage	0.4	V max	$\|I_{OUT}\| \leq 1.6$ mA
POWER SUPPLIES			
Reference Input	2.4/2.6	V min/V max	
AV_{DD}	4.75/5.25	V min/V max	
DV_{DD}	4.75/5.25	V min/V max	
AV_{SS}	–4.75/–5.25	V min/V max	
I_{DD}	7.5	mA max	4.8 mA typ
I_{SS}	2.5	mA max	1.8 mA typ
Power Consumption	50	mW max	35 mW typ
Power Supply Rejection[5]	–70	dB typ	

NOTES
[1]Operating temperature ranges as follows : B Version; –40°C to +85°C.
[2]The A_{IN} pins present a very high impedance dynamic load which varies with clock frequency.
[3]Guaranteed by design and characterization. Digital filter has linear phase.
[4]Usable dynamic range is guaranteed by measuring noise and relating this to the full-scale input range.
[5]100 mV p-p, 120 Hz sine wave applied to each supply.
Specifications subject to change without notice.

Table I. Typical Usable Dynamic Range, RMS Noise and Filter Settling Time vs. Filter Cutoff Frequency

N	Programmed Cutoff Frequency (Hz)	Output Update Rate (Hz)	Usable Dynamic Range (dB)	RMS Noise (μV)	Filter Settling Time to ±0.0007% FS (ms)	Absolute Group Delay (ms)
0	584	2232	99	21	1.35	0.675
1	292	1116	102	14	2.7	1.35
2	146	558	105	10	5.4	2.7
3	73	279	108	7	10.8	5.4
4	36.5	140	111	5	21.6	10.8

NOTE
Usable Dynamic Range is defined as the ratio of the rms full-scale reading (sine wave input) to the rms noise of the converter.

CONTROL REGISTER TIMING CHARACTERISTICS[1, 2] (AV_{DD} = DV_{DD} = +5 V ± 5%; AV_{SS} = –5 V ± 5%; AGND = DGND = 0 V; f_{CLKIN} = 8 MHz; Input Levels: Logic 0 = 0 V, Logic 1 = DV_{DD}; unless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Units	Conditions/Comments
t_1	$1/f_{CLKIN}$	ns min	SCLK Period
t_2	77	ns min	SCLK Width
t_3	30	ns min	$\overline{TFS}$ Setup Time
t_4	20	ns min	SDATA Setup Time
t_5	10	ns min	SDATA Hold Time
t_6	20	ns min	$\overline{TFS}$ Hold Time

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figure 2.
[3]CLKIN Duty Cycle range is 40% to 60%.

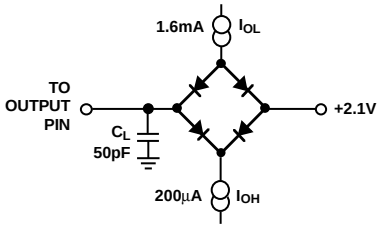


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

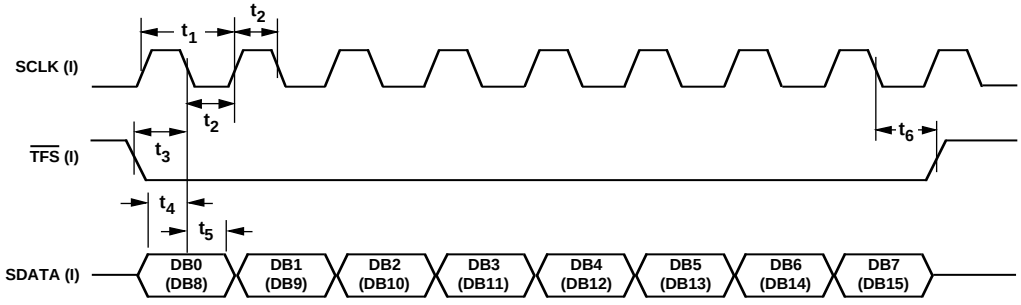


Figure 2. Control Register Timing Diagram

MASTER MODE TIMING CHARACTERISTICS[1, 2] (AV_{DD} = DV_{DD} = +5 V ± 5%; AV_{SS} = –5 V ± 5%; AGND = DGND = 0 V; f_{CLKIN} = 8 MHz; Input Levels: Logic 0 = 0 V, Logic 1 = DV_{DD}; unless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Units	Conditions/Comments
f_{CLKIN}[3, 4]	400	kHz min	CLKIN Frequency
	8	MHz max	
t_r[5]	40	ns max	Digital Output Rise Time. Typically 20 ns
t_f[5]	40	ns max	Digital Output Fall Time. Typically 20 ns
t_7	$1/f_{CLKIN}$	ns min	CASCIN Pulse Width
t_8	$1/f_{CLKIN}$	ns min	CASCIN to $\overline{DRDY}$ Setup Time
t_9	$1/2f_{CLKIN}$ + 30	ns max	$\overline{DRDY}$ Low to SCLK Low Delay
t_{10}	50	ns max	CLKIN High to $\overline{DRDY}$ Low, SCLK Active, $\overline{RFS}$ Active
t_{11}	40	ns max	CLKIN High to SCLK High Delay
t_{12}	50	ns min	SCLK Width
t_{13}	$1/f_{CLKIN}$	ns	SCLK Period
t_{14}	40	ns max	SCLK High to $\overline{RFS}$ High Delay
t_{15}	$1/f_{CLKIN}$	ns	$\overline{RFS}$ Pulse Width
t_{16}[6]	45	ns max	SCLK High to SDATA Valid Delay
t_{17}[7]	$1/2f_{CLKIN}$ + 50	ns max	SCLK Low to SDATA High Impedance Delay
	$1/2f_{CLKIN}$ + 10	ns min	
t_{18}	$1/2f_{CLKIN}$ + 60	ns max	CLKIN High to $\overline{DRDY}$ High Delay
t_{19}	50	ns max	CLKIN High to $\overline{RFS}$ High Impedance, SCLK High Impedance
	20	ns min	
t_{20}	$1/2f_{CLKIN}$ + 50	ns max	SCLK Low to CASCOUT High Delay
t_{21}	$2/f_{CLKIN}$	ns	CASCOUT Pulse Width

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figures 1 and 3.
[3]CLKIN duty cycle range is 40% to 60%.
[4]The AD7716 is production tested with f_{CLKIN} at 8 MHz in the slave mode. It is guaranteed by characterization to operate at 400 kHz and 8 MHz in master mode.
[5]Specified using 10% and 90% points on waveform of interest.
[6]t_{16} is measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[7]t_{17} is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time quoted in the timing characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

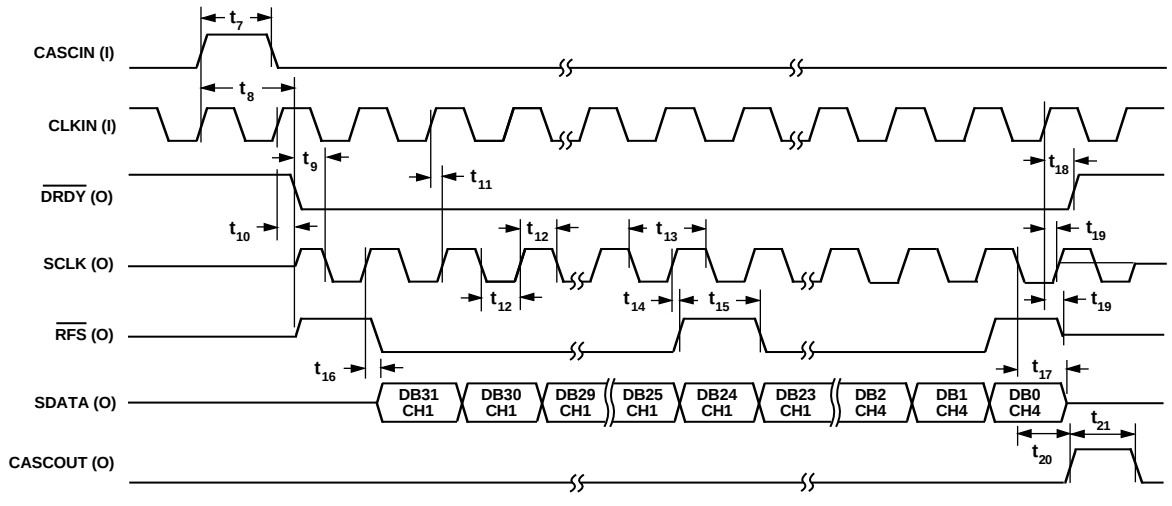


Figure 3. Master Mode Timing Diagram

SLAVE MODE TIMING CHARACTERISTICS[1, 2] (AV_{DD} = DV_{DD} = +5 V ± 5%; AV_{SS} = –5 V ± 5%; AGND = DGND = 0 V; f_{CLKIN} = 8 MHz; Input Levels: Logic 0 = 0 V, Logic 1 = DV_{DD}; unless otherwise noted)

Parameter	(B Version)	Units	Conditions/Comments
f_{CLKIN}[3, 4]	400	kHz min	CLKIN Frequency
	8	MHz max	
t_r[5]	40	ns max	Digital Output Rise Time. Typically 20 ns
t_f[5]	40	ns max	Digital Output Fall Time. Typically 20 ns
t_{23}	$1/f_{CLKIN}$	ns min	CASCIN Pulse Width
t_{24}	50	ns min	SCLK Width
t_{25}	125	ns min	SCLK Period
t_{26}	$1/f_{CLKIN}$ +30	ns min	CASCIN High to $\overline{RFS}$ Setup Time
t_{27}	30	ns min	$\overline{RFS}$ Low to SCLK High Setup Time
t_{28}[6]	50	ns max	SCLK High to SDATA Valid Delay
t_{29}	50	ns min	$\overline{RFS}$ Hold Time After SCLK High
t_{30}[7]	50	ns max	SCLK High to SDATA High Impedance Delay
	0	ns min	
t_{31}	60	ns max	SCLK High to CASCOUT High Delay.
t_{32}	$2/f_{CLKIN}$	ns max	CASCOUT Pulse Width

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figures 1 and 4.
[3]CLKIN duty cycle range is 40% to 60%.
[4]The AD7716 is production tested with f_{CLKIN} at 8 MHz in the slave mode. It is guaranteed by characterization to operate at 400 kHz.
[5]Specified using 10% and 90% points on waveform of interest.
[6]t_{28} is measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[7]t_{30} is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time quoted in the timing characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

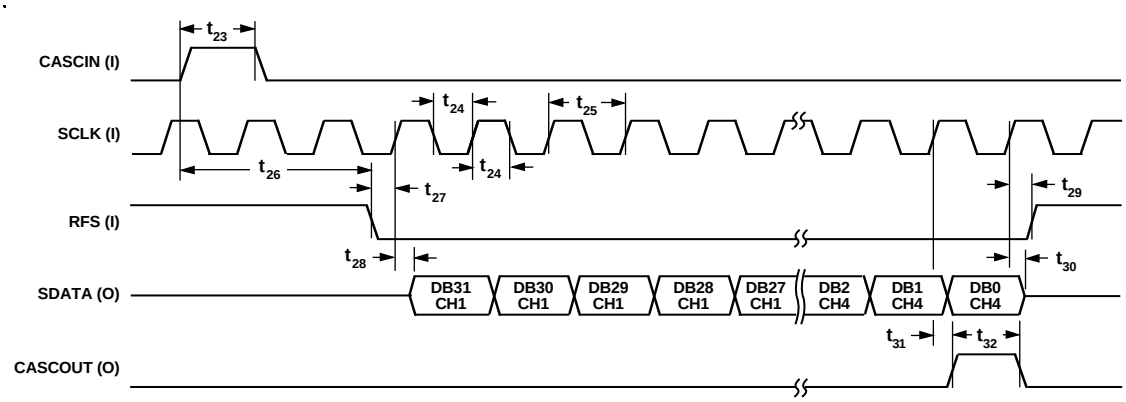


Figure 4. Slave Mode Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

AV_{DD} to AGND ..... –0.3 V to +7 V
AV_{SS} to AGND ..... +0.3 V to –7 V
AGND to DGND ..... –0.3 V to +0.3 V
AV_{DD} to DV_{DD} ..... –0.3 V to +0.3 V
Analog Inputs to AGND ..... AV_{SS} – 0.3 V to AV_{DD} + 0.3 V
V_{REF} to AGND ..... AV_{SS} – 0.3 V to AV_{DD} + 0.3 V
Digital Inputs to DGND[2] ..... –0.3 V to DV_{DD} + 0.3 V
Digital Outputs to DGND ..... –0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
Commercial Plastic (B Versions) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
PQFP Package, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... 95°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C
PLCC Package, Power Dissipation ..... 500 mW
θ_{JA} Thermal Impedance ..... 55°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

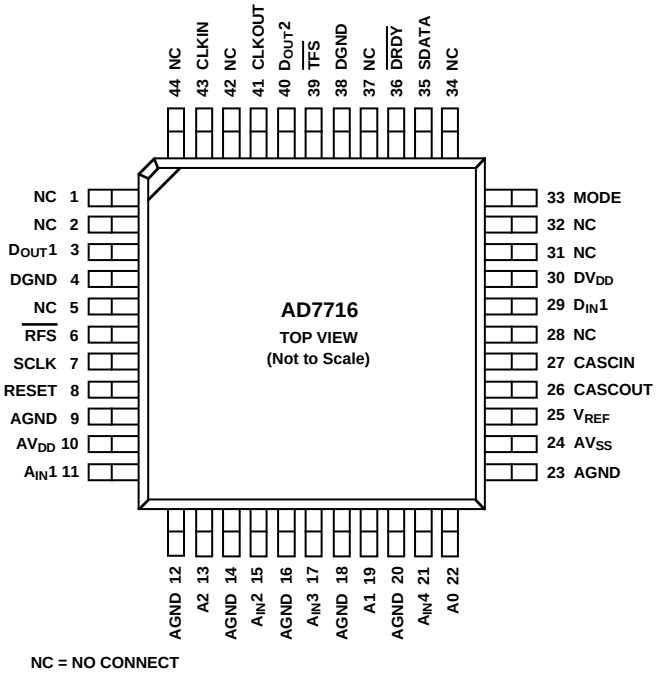
[2]Transient currents of up to 100 mA will not cause SCR latch-up.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

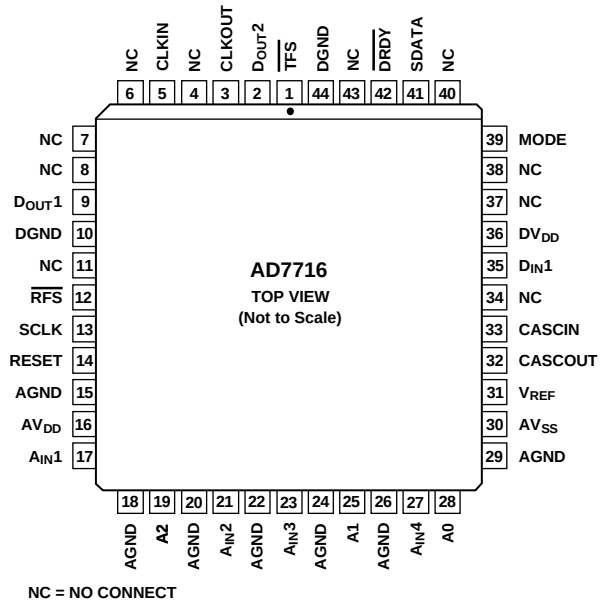


PQFP PINOUT



NC = NO CONNECT

PLCC PINOUT



NC = NO CONNECT

ORDERING GUIDE

Model	Temperature Range	Output Noise (Filter: 146 Hz)	Package Option*
AD7716BP	–40°C to +85°C	11 μV rms	P-44A
AD7716BS	–40°C to +85°C	11 μV rms	S-44

*P = PLCC (Plastic Leaded Chip Carrier); S = PQFP (Plastic Quad Flatpack).

PIN DESCRIPTION

Pin	Description
AV_{DD}	Analog Positive Supply, +5 V Nominal. This supplies +ve power to the analog modulators. AV_{DD} & DV_{DD} must be tied together externally.
DV_{DD}	Digital Positive Supply, +5 V Nominal. This supplies +ve power to the digital filter and input/output registers.
AV_{SS}	Analog Negative Supply, –5 V nominal. This supplies –ve power to the analog modulators.
RESET	A high pulse on this input pin synchronizes the sampling point on the four input channels. It can be used in a multichannel system to ensure simultaneous sampling. This also resets the digital interface to a known state.
A0–A2	The three address input pins, A0, A1 and A2 give the device a unique address. This information is contained in the output data stream from the device.
CLKIN	Clock Input for External Clock.
CLKOUT	Clock Output which is used to generate an internal master clock by connecting a crystal between CLKOUT and CLKIN. If an external clock is used then CLKOUT is not connected.
MODE	This digital input determines the device interface mode. If it is hardwired low, then the Master Mode interface is enabled whereas if it is high, the Slave Mode interface is enabled.
CASCIN	This is an active-high, level-triggered digital input which is used to enable the output data stream. This input may be used to cascade several devices in a multichannel system.
CASCOUT	Digital output which goes high at the end of a complete 4-channel data transfer. This can be connected to the CASCIN of the next device in a multichannel system to ensure proper control of the data transfer.
$\overline{RFS}$	Receive Frame Synchronization signal for the serial output data stream. This can be an input or output depending on the interface mode.
SDATA	Serial Data Input/Output Pin.
SCLK	Serial Clock Input/Output. The SCLK pin is configured as an input or output, depending on the state of the Mode pin.
$\overline{DRDY}$	Data Ready Output. A falling edge indicates that a new word is available for transmission. It will return high when 4, 32-bit words have been transmitted. It also goes high for one clock cycle, when a new word is being loaded into the output register. Data should not be read during this period.
$\overline{TFS}$	Transmit Frame Sync input for programming the on-chip Control Register.
$D_{IN}1$	Digital Data Input. This is contained in the digital data stream sent from the device.
$D_{OUT}1$, $D_{OUT}2$	Digital Outputs. These two digital outputs can be programmed from the on-chip Control Register. They can be used to control calibration signals at the front end.
V_{REF}	Reference Input, Nominally 2.5 V.
AGND	Analog Ground. Ground reference for analog circuitry.
DGND	Digital Ground. Ground return for digital circuitry.
$A_{IN}1$–$A_{IN}4$	Analog Input Pins. The analog input range is ±2.5 V.

TERMINOLOGY

LINEARITY ERROR
This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale (not to be confused with Bipolar Zero), a point 0.5 LSB below the first code transition (000 . . . 000 to 000 . . . 001) and full scale, a point 0.5 LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed as a percentage of full scale.

DIFFERENTIAL LINEARITY ERROR/NO MISSED CODES
This is the difference between any code's actual width and the ideal (1 LSB) width. Differential Linearity Error is expressed in LSBs. A differential linearity specification of ±1 LSB or less guarantees no missed codes to the full resolution of the device. The AD7716 has no missed codes guaranteed to 21 bits with a cutoff frequency of 146 Hz.

GAIN ERROR
Gain Error is the deviation of the last code transition (111 . . . 110 to 111 . . . 1) from the ideal (V_{REF} –3/2 LSBs). It is expressed as a percentage of full scale.

GAIN TC
This is the variation of gain error with temperature and is expressed in µV/°C.

OFFSET ERROR
Offset Error is the deviation of the first code transition from the ideal (–V_{REF} + 0.5 LSB). It is expressed as a percentage of full scale.

OFFSET TC
This is the variation of offset error with temperature and is expressed in µV/°C.

NOISE
This is the converter rms noise expressed in µV. Because of the digital filtering in the sigma delta converter, the noise performance is a function of the programmed filter cutoff.

SAMPLING RATE
This is the modulator sampling rate. For the AD7716, it is $f_{CLKIN}/14$.

OUTPUT UPDATE RATE
This is the rate at which the digital filter updates the output shift register. It is a function of the master clock frequency and the programmed filter cutoff frequency.

FILTER CUTOFF FREQUENCY
The digital filter of the AD7716 can be programmed, in binary steps, to 5 discrete cutoff frequencies, ranging from 584 Hz to 36.5 Hz (for a CLKIN frequency of 8 MHz).

SETTLING TIME
This is the settling time of the on-chip digital filter, to 0.0007% of FSR, in response to a full-scale step at the input of the ADC. It is proportional to the master clock frequency and the filter cutoff frequency.

USABLE DYNAMIC RANGE
The usable dynamic range is the ratio of the rms full-scale reading (sine wave input) to the rms noise of the converter, expressed in dBs. It determines the level to which it is possible to resolve the input signal. For example, at a bandwidth of 146 Hz, the rms noise of the converter is 11 µV. The full-scale rms is 1.77 volts. So, the usable dynamic range is 104 dB. Any signal below this level will be indistinguishable from noise unless extra post-filtering techniques are employed.

TOTAL HARMONIC DISTORTION
Total harmonic distortion (THD) is the ratio of the rms sum of the harmonics to the fundamental. For the AD7716, it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through sixth harmonics.

ABSOLUTE GROUP DELAY
Absolute group delay is the rate of change of phase versus frequency, $d\phi/df$ and is expressed in seconds. For the AD7716, it is dependent on master clock frequency and filter cutoff frequency.

DIFFERENTIAL GROUP DELAY
Differential group delay is the total variation in absolute group delay in the specified bandwidth. Since the digital filter in the AD7716 has perfectly linear phase, the differential group delay is almost zero. This is important in many signal processing applications where excessive differential group delay can cause phase distortion.

GENERAL DESCRIPTION

The AD7716 is a 4-channel 22-bit A/D converter with on-chip digital filtering, intended for the measurement of wide dynamic range, low frequency signals such as those representing ECG, EEG, chemical, physical or biological processes. It contains four sigma delta ADCs, a clock oscillator and a serial communications port.

Each of the analog input signals to the AD7716 is continuously sampled at a rate determined by the frequency of the master clock, CLKIN. Four sigma-delta modulators convert the sampled signals into digital pulse trains whose duty cycles contain the digital information. These are followed by low-pass filters to process the output of the modulators and update the output register at a maximum rate of 2.2 kHz. The output data can be read from the serial port at any rate up to this.

THEORY OF OPERATION

The general block diagram of a delta-sigma ADC is shown in Figure 5. It contains the following elements:

1. Continuously Sampling Integrator
2. A Differential Amplifier or Subtracter
3. A 1-Bit A/D Converter (Comparator)
4. A 1-Bit DAC
5. A Digital Low-Pass Filter

In operation, the sampled analog signal is fed to the subtracter, along with the output of the 1-bit DAC. The filtered difference signal is fed to the comparator, whose output samples the difference signal at a frequency many times that of the analog signal frequency (oversampling).

Oversampling is fundamental to the operation of delta-sigma ADCs. Using the quantization noise formula for an ADC:

$$SNR = (6.02 \times number\ of\ bits + 1.76)\ dB,$$

a 1-bit ADC or comparator yields an SNR of 7.78 dB.

When operating with a master clock of 8 MHz, the AD7716 samples the input signal at 570 kHz, which spreads the quantization noise from 0 kHz to 285 kHz. Since the specified analog input bandwidth of the AD7716 is only 584 Hz maximum (it can be programmed to be lower), the noise energy in this bandwidth would be only 1/488 of the total quantization noise, assuming that the noise energy was spread evenly throughout the spectrum. This very high sampling with respect to the input bandwidth is known as oversampling, and the ratio of 488:1 is called the oversampling ratio. The noise is reduced still further by analog filtering in the modulator loop, which shapes the quantization noise spectrum to move most of the noise energy to frequencies above 584 Hz. The SNR performance in the 0 Hz to 584 Hz range is conditioned to the 99 dB level in this fashion (see Table I). As the programmed bandwidth is reduced, the oversampling ratio increases and the usable dynamic range also increases. Thus, for example, with a programmed bandwidth of 73 Hz, the oversampling ratio is 3904:1, and the usable dynamic range is 108 dB which corresponds to greater than 17-bit resolution.

The output of the comparator provides the digital input for the 1-bit DAC, so the system functions as a negative feedback loop which minimizes the difference signal. The digital data that represents the analog input voltage is in the duty cycle of the pulse train appearing at the output of the comparator. It can be retrieved as a parallel binary data word using a digital filter.

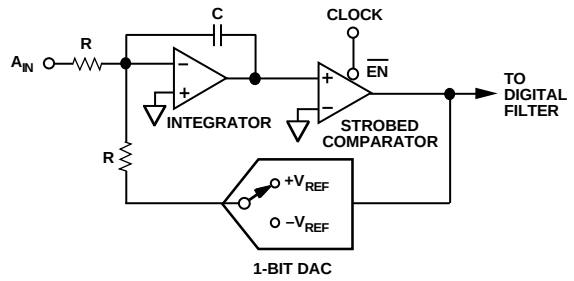


Figure 5. First Order Modulator

Sigma-delta ADCs are generally described by the order of the analog low-pass filter. A simple example of a first order sigma-delta ADC is shown in Figure 5. This contains only a first-order low-pass filter or integrator.

The AD7716 uses a second-order sigma-delta modulator and a digital filter that provides a rolling average of the sampled output. After power-up or if there is a step change in the input voltage, there is a settling time before valid data is obtained.

DIGITAL FILTERING

The AD7716's digital filter behaves like an analog filter, with a few minor differences.

First, since digital filtering occurs after the A-to-D conversion process, it can remove noise injected during the conversion process. Analog filtering cannot do this.

On the other hand, analog filtering can remove noise superimposed on the analog signal before it reaches the ADC. Digital filtering cannot do this and noise peaks riding on signals near full scale have the potential to saturate the analog modulator and digital filter, even though the average value of the signal is within limits. If noise signals cause the input signal to exceed the specified range, consideration should be given to analog input filtering, or to reducing the gain in the input channel to bring the combination of signal and noise spike within the specified input range.

Filter Characteristics

The cutoff frequency of the digital filter is determined by bits FC2, FC1 and FC0 in the control register (See Table IV). The cutoff frequency of the filter is $f_{CLKIN}/(3.81 \times 14 \times 256 \times 2N)$, where N is the decimal equivalent of FC2, FC1, FC0. At the maximum clock frequency of 8 MHz, with all 0s loaded to FC2, FC1, FC0, the cutoff frequency of the filter is 584 Hz and the data update rate is 2232 Hz.

Since the AD7716 contains low-pass filtering, there is a settling time associated with step function inputs, and data will be invalid after a step change until the settling time has elapsed. The

relationship between input bandwidth and settling is given in Table I. Because of this settling time, most sigma delta ADCs are unsuitable for high speed multiplexing, where channels are switched and converted sequentially at high rates, as switching between channels can cause a step change in the input. However, the AD7716 is a sigma-delta solution to multichannel applications, since it can process four channels simultaneously. In addition, it is easy to cascade several devices in order to increase the number of channels being processed.

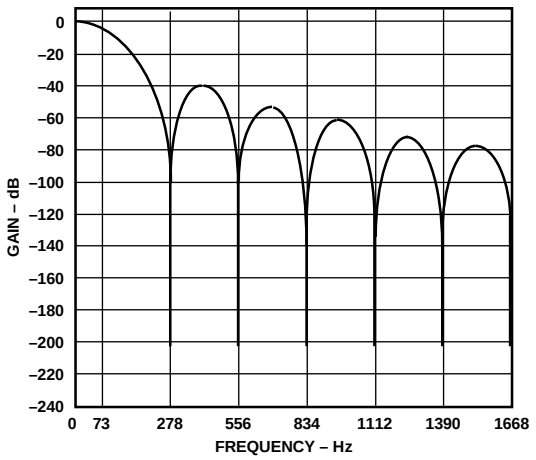


Figure 6. Frequency Response of AD7716 Filter

Figure 6 shows the filter frequency response for a cutoff frequency of 73 Hz. This is a $(\sin x/x)^3$ response (also called sinc^3) that provides greater than 100 dB rejection at the notch frequencies. The relationship between the programmed cutoff frequency and the first notch is constant ($f_{NOTCH} = 3.81 \times f_{CUTOFF}$). The first notch frequency is also the output data rate. The settling time to a full-scale step input is four times the output data period. Programming a different cutoff frequency via FC0–FC2 does not alter the profile of the filter response, it simply changes the frequency of the notches.

In Figure 6, the first notch is at 278 Hz. This is also the output data rate. Settling time to a full-scale step input is 10.8 ms.

The digital filter can be defined by the following equations.

$$H(z) = \left[\frac{1}{N} \times \frac{1 - Z^{-N}}{1 - Z^{-1}}\right]^3$$

$$\left|H(f)\right| = \left|\frac{\sin \pi f/f_S)}{\pi f/f_S)}\right|^3$$

where N = Ratio of Modulator Sampling Frequency to Output Rate

and f_S = Output Rate.

Post Filtering

In the AD7716, the on-chip modulator provides the digital filter with samples at a rate of 570 kHz. The filter decimates these samples to provide data at an output rate which corresponds to the programmed first notch frequency of the filter.

If the user wants to reduce the output noise from the device for bandwidths less than 36.5 Hz, then it is possible to employ extra filtering after the AD7716. This extra digital filtering is called post filtering. If a straight averaging filter is used, for example, a reduction in bandwidth by a factor of 2 results in $\sqrt{2}$ reduction in the rms noise. This additional filtering will also result in a longer settling time.

Antialias Considerations

The digital filter does not provide any rejection at integer multiples of the modulator sampling frequency (n × 570 kHz, where n = 1, 2, 3, . . .). This means that there are frequency bands, $\pm f_{3dB}$ wide (f_{3dB} is the cutoff frequency selected by FC0 to FC2) where noise passes unattenuated to the output. However, due to the AD7716's high oversampling ratio, these bands occupy only a small fraction of the spectrum and most broadband noise is filtered.

In spectral analysis applications, it is important to note that attenuation at half the output update rate is 16 dB. Extra front-end filtering or post filtering may be required to keep aliases in this frequency band at an acceptable level.

USING THE AD7716

SYSTEM DESIGN CONSIDERATIONS

The AD7716 operates differently from successive approximation ADCs or other integrating ADCs. Since it samples the signal continuously, like a tracking ADC, there is no need for a start convert command. The output register is updated at a rate dependent on the programmed cutoff frequency, and the output can be read at any time.

Input Signal Conditioning

The input range for the AD7716 is $\pm V_{REF}$, where V_{REF} = 2.5 V ± 10%. Other input ranges can be accommodated by input signal conditioning. This may take the form of gain to increase a smaller signal range, or passive attenuation to reduce a larger input voltage range.

Source Resistance
If passive attenuators are used in front of the AD7716, care must be taken to ensure that the source impedance is sufficiently low. The dc input resistance for the AD7716 is greater than 1 GΩ. In parallel with this there is a small sampling capacitor. The dynamic load presented by this varies with the clock frequency. The modulator sampling rate determines the amount of time available for the sampling capacitor to be charged. Any extra external impedances result in a longer overall charge time resulting in extra gain errors on the analog input. The AD7716 has a quite large gain error (1% FSR) due to the fact that there is no on-chip calibration. Thus, even an extra 10 kΩ source resistance and 50 pF source capacitance will have no significant effect on this.

Active signal conditioning circuits such as op amps generally do not suffer from problems of high source impedance. Their open-loop output resistance is normally only tens of ohms and, in any case, most modern general purpose op amps have sufficiently fast closed-loop settling time for this not to be a problem.

Accuracy
Sigma-delta ADCs, like VFCs and other integrating ADCs, do not contain any source of nonmonotonicity and inherently offer no missing codes performance.

The AD7716 achieves excellent linearity by the use of high quality, on-chip silicon dioxide capacitors, which have a very low capacitance/voltage coefficient.

Drift Considerations
The AD7716 uses autozeroing techniques to minimize input offset drift. Charge injection in the analog switches and leakage currents at the sampling node are the primary sources of offset voltage drift in the converter. Figure 7 indicates the typical offset due to temperature changes. Drift is relatively flat up to 85°C. Above this temperature, leakage current becomes the main source of offset drift. Since leakage current doubles approximately every 10°C, the offset drifts accordingly. The value of the voltage on the sample capacitor is updated at a rate determined by the master clock, therefore the amount of offset drift which occurs will be proportional to the elapsed time between samples.

Gain drift within the converter depends mainly upon the temperature tracking of the internal capacitors. It is not affected by leakage currents.

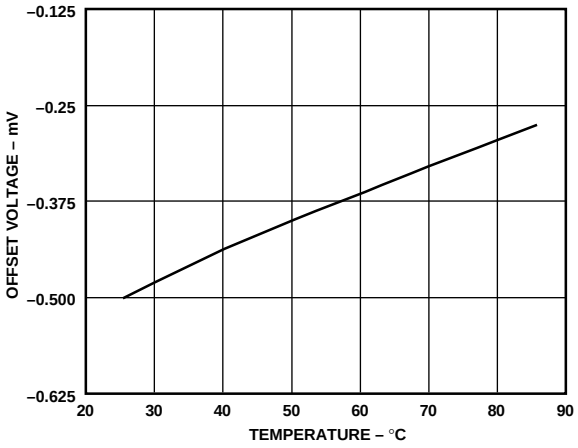


Figure 7. Typical Offset Drift

Voltage Reference
The voltage applied to the V_{REF} pin defines the analog input range. The specified reference voltage is 2.5 V ± 10%.

The reference input presents exactly the same dynamic load as the analog input, but in the case of the reference input, source resistance and long settling time introduce gain errors rather than offset errors. Most precision references however have sufficiently low output impedance and wide enough bandwidth to settle to the required accuracy in the time allowed by the AD7716.

The reference should be chosen to have minimal noise in the programmed passband. Recommended references are the AD780 or the REF43 from Analog Devices. These low noise references have typical noise spectral densities of 100 nV/$\sqrt{\text{Hz}}$ at 600 Hz. This corresponds to an rms noise of 2.5 μV in this band and is more than adequate for the AD7716.

Clock Generation
The device operates from a master clock which must be provided either from a crystal source or an external clock source. If a crystal is used, it must be connected across the CLKIN and CLKOUT pins. Typical loading capacitors of 15 pF are required on CLKIN, CLKOUT. The crystal manufacturers data should be consulted for more information. An external clock can also be used to drive the CLKIN input directly with a CMOS compatible clock. In this case, CLKOUT is left unconnected. The nominal clock frequency for the device is 8 MHz.

CONTROL REGISTER DESCRIPTION

The 16-bit control register is programmed in two 8-bit bytes; the low byte is programmed first and the high byte second. The loading format is LSB first (DB0 for the Least Significant Byte; DB8 for the Most Significant Byte). Three control lines are used: $\overline{TFS}$, SCLK and SDATA. On initial application of power to the AD7716, the control register will come up in an undetermined state. Programming the control register requires an SCLK input, a $\overline{TFS}$ input and an SDATA input. The MODE pin on the device determines whether it is in the master interface mode or the slave interface mode. In either mode, a falling edge on $\overline{TFS}$ causes the part to relinquish control of the SDATA and SCLK lines. When $\overline{TFS}$ goes low, data on the SDATA line is clocked into the control register on each succeeding falling edge of SCLK. When 8 bits have been clocked in, the transfer automatically stops. Only when another negative going edge is detected on $\overline{TFS}$ will new information be written into the control register. The control register programming model is shown in Table II. Bits DB8 and DB0 allow the control register to identify whether the MS Byte or the LS Byte has been programmed. Only when DB8 is a 1 and DB0 is a 0 will the register recognize that a complete valid word has been programmed.

Control register bit, DB15 (A3), acts as an extra address bit which must always be set to 1 to enable programming of the AD7716. If it is set to 0, then the programmed word is ignored. This allows the user to bypass the AD7716 control register and use the serial stream from the DSP or microcomputer to program other serial peripheral devices.

When a valid word has been received, the device interrogates the M0 bit. If this is 0, then the digital filter cutoff frequencies are programmed to the appropriate value if the device address pins correspond to the A2, A1, A0 bits in the control register. If the device address pins do not correspond to the A2, A1, A0 bits then the FC2, FC1, FC0 bits are ignored. If M0 is 1, then the digital filter cutoff frequencies are programmed to the FC2, FC1, FC0 value irrespective of the address bits. In a multichannel system this allows the user to either program all AD7716s to have the same cutoff frequency or else to give each device a separate cutoff frequency.

Control register bits FC2, FC1, FC0 program the digital filter cutoff frequency, see Table VI.

Control register bits D2, D1 control the digital output pins D2 and D1. These are programmed in the same way as FC2, FC1, FC0.

Table II. Control Register Programming Model

Most Significant Byte								Least Significant Byte							
DB15	**DB14**	**DB13**	**DB12**	**DB11**	**DB10**	**DB9**	**DB8**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
A3	A2	A1	A0	M0	FC2	FC1	1	FC0	DOUT2	DOUT1	X	X	X	X	0

Table III. M0 Truth Table

M0	Programming Mode
0	A2, A1, A0 determine which device is addressed and programmed with cutoff frequency and digital output.
1	A2, A1, A0 ignored. All devices are addressed and programmed with common cutoff frequency and digital output.

Table IV. Cutoff Frequency Truth Table

FC2	FC1	FC0	Cutoff Frequency (Hz)
0	0	0	584
0	0	1	292
0	1	0	146
0	1	1	73
1	0	0	36.6

RESET

The AD7716 has a hardware reset which can be used to synchronize many devices. When the RESET pin goes low after being high for at least four CLKIN cycles, the modulator sampling points and digital filter starting points are all synchronized. This synchronizes all devices which receive the RESET pulse and gives simultaneous sampling of all channels. It does not affect the control register but restarts the interface. Also, it is necessary to wait the requisite settling time after applying Reset to get valid data from the device.

CASCADING DEVICES

The AD7716 provides a facility for connecting multiple devices in series. The CASCIN and CASCOUT pins allow this. Connecting CASCOUT to CASCIN of the succeeding device means that the SDATA output of the second device will be disabled until the output register of the first device is empty.

In the case of the first device in the system, it is possible to drive CASCIN from CASCOUT of the last device or, alternatively, invert $\overline{DRDY}$ to drive it. If CASCIN is driven by CASCOUT, then a reset must be applied after every write to the control register. This also applies in single device systems that use CASCOUT to drive CASCIN

DATA OUTPUT INTERFACE MODES

When the control register has been programmed, the device begins conversion. There is an initial delay to allow the digital filters to settle. As already stated, these filters are $Sinc^3$, and so the filter output update rate is directly related to the programmed cutoff frequency. The ratio between these is 3.81. So, for a filter cutoff frequency of 584 Hz, the output update is 2.22 kHz. The falling edge of the $\overline{DRDY}$ output indicates that the output shift register has been updated. There are two interface modes. One is the master mode, where the AD7716 is the master in the system and the processor to which it is communicating is the slave. The other mode is the slave mode, where the AD7716 is the slave and the processor is the system master. In both of these modes the data output stream contains 4×32 bits, corresponding to the four input channels. The output data format is given in Table V. The conversion result DB21–DB0 occupies location DB31–DB10 of the output register. DB21 is the MSB and is transmitted first as shown in the timing diagrams. The channel address is given by CA0 and CA1 which occupy DB9 and DB8 of the output register. The channel address format is given in Table VI.

Master Mode Interface

The device may be placed in the Master Mode by tying the MODE pin low. In this mode, data is clocked out of the AD7716 by an internally generated serial clock and frame synchronization pulse. Two signals initiate the transfer. These are the input CASCIN and the internally generated $\overline{DRDY}$ signal. When a high level is detected on CASCIN, the device checks the state of $\overline{DRDY}$. Note, that on initial power-up or after a reset has been applied, the CASCIN input is not necessary on device 000 for the first data transfer but is required thereafter. If $\overline{DRDY}$ is low, then the 3-state output, $\overline{RFS}$ goes high on the next rising edge of CLKIN and stays high for one CLKIN cycle before going low again. The 3-state SCLK output is also activated on the same rising edge. As $\overline{RFS}$ goes low, DB31 is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK. Data is transmitted in 8-bit bytes. For each A_{IN}, there are 4, 8-bit bytes and 4 $\overline{RFS}$ pulses. When DB0 of A_{IN} 4 has been clocked out, SCLK goes back into 3-state and the CASCOUT output goes high for one master clock cycle. $\overline{DRDY}$ also goes high at this point. Successive devices can be networked together by tying the CASCOUT of one device to the CASCIN on the next one.

Note that on device 0 (A2, A1, A0 tied low), the CASCIN input should be driven by the inverse of the $\overline{DRDY}$ output. This is shown in the interface diagram of Figure 8.

The Master Mode interface is very suitable for loading data into a serial-to-parallel shift register or for DSPs which can accept a continuous stream of 8-bit bytes.

Slave Mode Interface

The device may be placed in the slave interface mode by tying the MODE pin high. In this mode, the master processor controls the transfer of data from the signal processing block. It starts the transfer by sending a frame synchronizations pulse and serial clock to the AD7716. This could be in response to an interrupt generated by the $\overline{DRDY}$ output on the AD7716. If the device has detected a high level on CASCIN or is device 000 on its first transfer, it starts to send out data on the next rising edge of SCLK. This data is then valid on the falling edge of SCLK. When all the data bits have been clocked out, the CASCOUT pin goes high for one CLKIN cycle and $\overline{DRDY}$ also goes high. The slave mode interface is suited to both microcomputers like the 8051 and 68HC11 and also DSPs like the TMS320C25, ADSP-2101 family and the DSP56000 family.

Table V. Output Data Word Format

DB31 . . . DB10	DB9 DB8	DB7 DB6 DB5	DB4	DB3	DB2 DB1 DB0
DB21 . . . DB0 Conversion Result	CA0 CA1 Channel Address	A0 A1 A2 Device Address	$D_{IN}1$ Pace Detect	OVFL Overflow	X X X Indeterminate

Table VI. Channel Address Format

Channel	CA1 (DB8)	CA0 (DB9)
A_{IN} 1	0	0
A_{IN} 2	0	1
A_{IN} 3	1	0
A_{IN} 4	1	1

MICROPROCESSOR INTERFACING

Interfacing the AD7716 to the ADSP-2100 Family

The ADSP-2100 family of microcomputers from Analog Devices are high speed, high performance digital signal processors. Many members of the family have serial ports (known as SPORTs) which are compatible with the AD7716. These include the ADSP-2101, ADSP-2105, ADSP-2111 and ADSP-2115. Full details of these are available in the *ADSP-2100 Family User's Manual* available from Analog Devices.

Figure 8 shows the hardware interface between two AD7716s and SPORT 0 of the ADSP-2101 DSP. This yields a very efficient 8-channel data acquisition system. The AD7716 is set up for slave interface mode by tying the MODE pin high. This means that the ADSP-2101 is the master in the system and supplies the necessary frame synchronization and SCLK Signals to the AD7716s when writing to and reading from the device.

On power up, the user should write to the AD7716 control register in order to set the filter cutoff frequencies. The appropriate SPORT 0 Control Register (0 × 3FF6) setting is "7EC7." This sets the transmit section for alternate inverted framing with a word length of 8 bits. Two 8-bit words should then be written to each AD7716 to program the filter cutoff frequencies. The control register programming model is given in Table II. Note that the LSB (DB0) must be loaded first as in the timing diagram of Figure 2.

When the write operation is complete, a reset pulse should be applied to both devices. This ensures that the sampling and interface timing of the device are synchronized. The reset can be under DSP control, in which case a flag output could be used.

After reset, the processor should jump to the read routine. For this read routine, there are several registers that need to be set.

The SPORT0 Control Register setting is "7FCF." This sets the receive section for internal SCLK, continuous receive with alternate inverted framing.

The SPORT0 SCLKDIV Register (0 × 3FF5) determines the SCLK frequency from the ADSP-2101. With "0000" loaded, the SCLK output is at its maximum (1/2 the master clock of 12.5 MHz).

In normal operation, a SPORT generates an interrupt when it has received a data word. Autobuffering provides a mechanism for receiving or transmitting an entire block of serial data before an interrupt is generated. Service routines can operate on the entire block of data, rather than on a single word, reducing overhead significantly. This is ideal for use with a device like the AD7716 where there is a requirement to read many bits of data (256 in this case) for each sampling instant. The SPORT0 Autobuffer Control Register (0 × 3FF3) is loaded with "0001" to enable the Receive Autobuffering.

The SPORT0 RFSDIV Register (0 × 3FF4) should be set to the minimum value of "000F." Finally the IRQ2 interrupt should be enabled.

The DSP will now wait for an interrupt from the AD7716. This interrupt is generated by the AD7716 $\overline{\text{DRDY}}$ line going low. If the interrupt service routine is set for autobuffered mode with a length of 16 (16-bit) words, then the DSP will read in the 256 bits from the two AD7716s in one continuous stream and then stop. The data from the two devices will be contained in the designated data memory area and the DSP can now go and operate on this as is necessary. Note that, because of the ADSP-2101 framing, a one-bit shift left will be necessary on the data in memory. For 16 data words, this will require 22 instruction cycles.

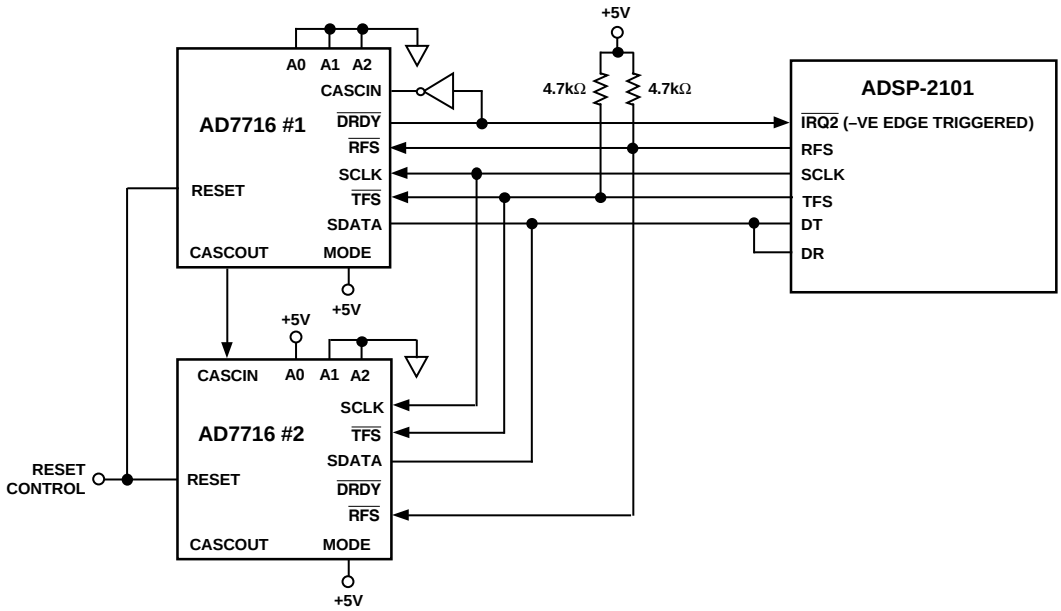


Figure 8. 8-Channel Data Acquisition System Using the ADSP-2101 Digital Signal Processor

When the AD7716 is programmed for the maximum cutoff frequency of 584 Hz, the output data rate is 2.25 kHz. This means that there is 440 µs available to read the data and do the necessary number crunching before the next sample must be read. Assuming that the ADSP-2101 is running from a master clock of 12.5 MHz means that the maximum SCLK available is 6.25 MHz (1/2 the master clock frequency). It will then take 40 µs to transfer the 256 bits of data from the ADC to the DSP. This leaves 400 µs for number crunching in the DSP. If the programmed cutoff frequency is lower then this allows even more time to the DSP.

MC68HC11 Interface

The MC68HC11 microcomputer can be interfaced to the AD7716 using the slave mode interface. Figure 9 shows a typical setup. The MODE pin on the AD7716 is tied high for slave mode operation. The SPI port of the MC68HC11 is used. The microcomputer is in its single chip mode. $\overline{DRDY}$ from the AD7716 is connected to the $\overline{IRQ}$ input of the MC68HC11. MISO and MOSI on the MC68HC11 should be configured for wired-or operation. Depending on the interface configuration, it may be necessary to provide bidirectional buffers between these lines.

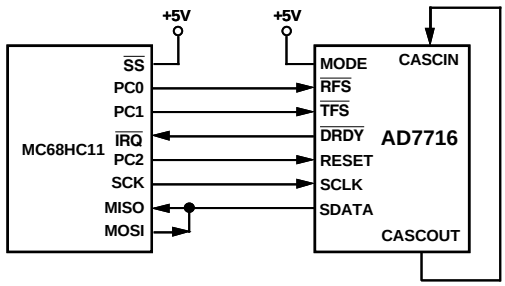


Figure 9. MC68HC11 to AD7716 Interface

The MC68HC11 is configured in the master mode with its CPOL bit set to a logic zero and its CPHA bit set to a logic one. With an 8 MHz CLKIN input on the AD7716, the device will operate with all four serial clock rates of the MC68HC11.

Sixteen, 8-bit read operations are necessary to read the 128 bits from the AD7716 output register. An extra read is necessary to reset the output register. This means a total of 17 read operations are needed from the MC68HC11.

DSP56001 Interface

Figure 10 shows an interface to the DSP56001 digital signal processor. The AD7716 is set up for the slave interface mode. The DSP56001 is set up for asynchronous operation with gated clock and normal framing. Data must be written to the AD7716 control register in two 8-bit bytes. The first byte is written to the DSP56001 SSI transmit data register (TX) and this is automatically transferred to the transmit shift register when the frame sync occurs. Data is shifted out to the STD pin by the internal bit clock (SCK) when the associated frame sync output is asserted.

The optimum setup for reading all four channels of the AD7716 into the DSP56001 is six 24-bit reads. This will provide 144 clock edges to shift out the 128 bits of data in the AD7716 output shift register. The first clock applied to the AD7716 will clock out DB21 of $A_{IN}1$. $\overline{DRDY}$ from the AD7716 can be used as an interrupt input to the DSP56001 to control the data transfer. Either $\overline{IRQA}$ or $\overline{IRQB}$ of the DSP56001 can be used to detect the interrupt.

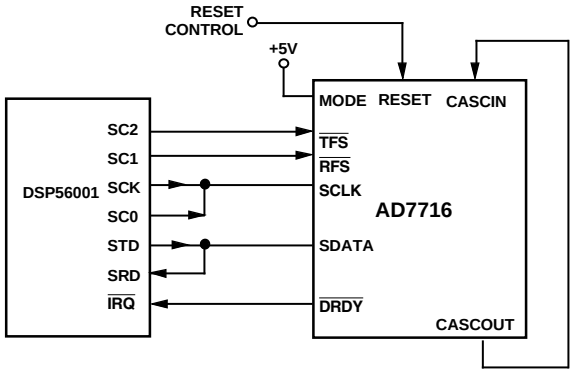


Figure 10. DSP56001 Interface

TMS320C25 Interface

Figure 11 shows the AD7716 interfaced to the TMS320C25 DSP using the master mode interface. For initial programming of the AD7716 control register, the external gated clock is required. FSX going low enables this. When the two 8-bit bytes have been sent to the AD7716, the FSX should go permanently high. The external gated clock will now be disabled and the AD7716 will take control of the SDATA line. It will begin transmitting data as soon as it becomes available. It also provides the clock and frame synchronization signals required by the DSP.

Reset for the AD7716 is provided by one of the DSP flag outputs.

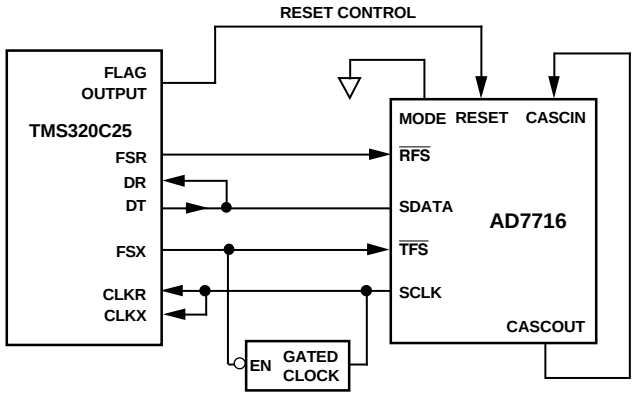


Figure 11. TMS320C25 to AD7716 Interface

Multibandwidth System

Some applications may require multiple AD7716's with different bandwidths programmed to each device. The best way to accomplish this is shown in Figure 12. The master mode interface is used for this example but the slave mode may also be used. The example shows an 8-channel system with Device #0 in the system programmed for a 292 Hz cutoff frequency and Device #1 programmed for a 146 Hz cutoff frequency.

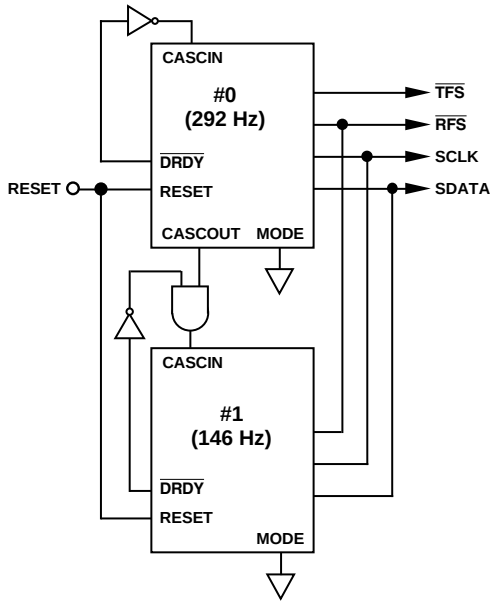


Figure 12. Multibandwidth System

The resultant output signals are also shown. Since Device #0 has a higher bandwidth it will also have a higher update rate. The receiving processor will be getting samples from this device at twice the rate of Device #1.

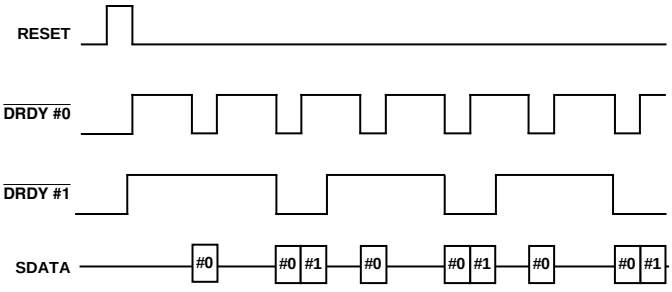
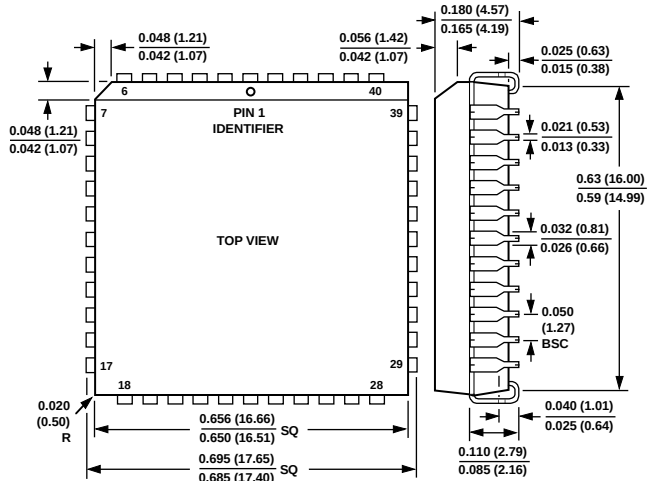


Figure 13. Output Signals for Figure 12

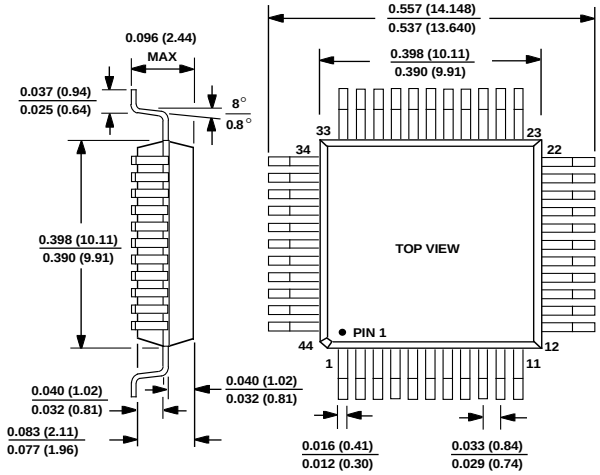
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

44-Lead PLCC
(P-44A)



44-Lead Plastic Quad Flatpack
(S-44)



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