# 16-Bit, 100 kSPS PulSAR, Differential ADC in MSOP

# AD7684

## FEATURES

- 16-bit resolution with no missing codes
- Throughput: 100 kSPS
- INL: ±1 LSB typical, ±3 LSB maximum
- True differential analog input range: $\pm V_{REF}$
  - 0 V to $V_{REF}$ with $V_{REF}$ up to VDD on both inputs
- Single-supply operation: 2.7 V to 5.5 V
- Serial interface SPI®-/QSPI-™/MICROWIRE-™/DSP-compatible
- Power dissipation
  - 4 mW @ 5 V
  - 1.5 mW @ 2.7 V
  - 150 µW @ 2.7 V/10 kSPS
- Standby current: 1 nA
- 8-lead MSOP package

## APPLICATIONS

- Battery-powered equipment
- Data acquisition
- Instrumentation
- Medical instruments
- Process control

## APPLICATION DIAGRAM

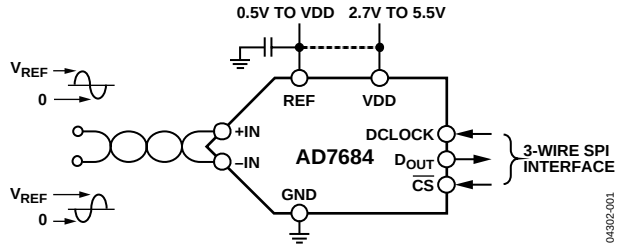



*Figure 1.*

**Table 1. MSOP, QFN (LFCSP)/SOT-23 14-/16-/18-Bit PulSAR ADC**

| Type | 100 kSPS | 250 kSPS | 400 kSPS to 500 kSPS | ≥ 1000 kSPS | ADC Driver |
|---|---|---|---|---|---|
| 18-Bit True Differential | | AD7691 | AD7690 | AD7982 | ADA4941 |
| | | | | AD7984 | ADA4841 |
| 16-Bit True Differential | AD7684 | AD7687 | AD7688 | | ADA4941 |
| | | | AD7693 | | ADA4841 |
| 16-Bit Pseudo Differential | AD7680 | AD7685 | AD7686 | AD7980 | ADA4841 |
| | AD7683 | AD7694 | | | |
| 14-Bit Pseudo Differential | AD7940 | AD7942 | AD7946 | | ADA4841 |

## GENERAL DESCRIPTION

The AD7684 is a 16-bit, charge redistribution, successive approximation, PulSAR® analog-to-digital converter (ADC) that operates from a single power supply, VDD, between 2.7 V to 5.5 V. It contains a low power, high speed, 16-bit sampling ADC with no missing codes, an internal conversion clock, and a serial, SPI-compatible interface port. The part also contains a low noise, wide bandwidth, short aperture delay, track-and-hold circuit.

On the $\overline{CS}$ falling edge, it samples the voltage difference between +IN and –IN pins. The reference voltage, REF, is applied externally and can be set up to the supply voltage. Its power scales linearly with throughput.

The AD7684 is housed in an 8-lead MSOP, with an operating temperature specified from −40°C to +85°C.

**Rev. A**
Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113 ©2004–2007 Analog Devices, Inc. All rights reserved.

# TABLE OF CONTENTS

Features ... 1
Applications ... 1
Application Diagram ... 1
General Description ... 1
Revision History ... 2
Specifications ... 3
Timing Specifications ... 5
Absolute Maximum Ratings ... 6
ESD Caution ... 6
Pin Configuration and Function Descriptions ... 7
Terminology ... 8
Typical Performance Characteristics ... 9
Application Information ... 12
Circuit Information ... 12
Converter Operation ... 12
Transfer Functions ... 12
Typical Connection Diagram ... 13
Analog Inputs ... 13
Driver Amplifier Choice ... 13
Voltage Reference Input ... 14
Power Supply ... 14
Digital Interface ... 14
Layout ... 14
Evaluating the Performance of the AD7684 ... 14
Outline Dimensions ... 15
Ordering Guide ... 15

## REVISION HISTORY

**10/07—Rev. 0 to Rev. A**

Changes to Table 1 ... 1
Changes to Table 2 ... 3
Changes to Layout ... 5
Changes to Table 6 and Layout ... 6
Changes to Table 7 ... 7
Changes to Figure 15 Caption ... 10
Changes to Figure 21 ... 12
Changes to Figure 22 and Analog Inputs Section ... 13
Changes to Table 9, Digital Interface Section, and Evaluating the Performance of the AD7684 Section ... 14
Updated Outline Dimensions ... 15
Changes to Ordering Guide ... 15

**10/04— Revision 0: Initial Version**

# SPECIFICATIONS

VDD = 2.7 V to 5.5 V; $V_{REF}$ = VDD; $T_A$ = −40°C to +85°C, unless otherwise noted.

**Table 2.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RESOLUTION | | 16 | | | Bits |
| ANALOG INPUT | | | | | |
| Voltage Range[1] | +IN − (−IN) | $-V_{REF}$ | | $+V_{REF}$ | V |
| Absolute Input Voltage | +IN, −IN | −0.1 | | VDD + 0.1 | V |
| Common-Mode Input Range | +IN, −IN | 0 | $V_{REF}/2$ | $V_{REF}/2$ + 0.1 | V |
| Analog Input CMRR | $f_{IN}$ = 100 kHz | | 65 | | dB |
| Leakage Current at 25°C | Acquisition phase | | 1 | | nA |
| Input Impedance | | See the Analog Inputs section | | | |
| THROUGHPUT SPEED | | | | | |
| Complete Cycle | | | | 10 | µs |
| Throughput Rate | | 0 | | 100 | kSPS |
| DCLOCK Frequency | | 0 | | 2.9 | MHz |
| REFERENCE | | | | | |
| Voltage Range | | 0.5 | | VDD + 0.3 | V |
| Load Current | 100 kSPS, $V_{+IN} = V_{-IN} = V_{REF}/2$ = 2.5 V | | 50 | | µA |
| DIGITAL INPUTS | | | | | |
| Logic Levels | | | | | |
| $V_{IL}$ | | −0.3 | | 0.3 × VDD | V |
| $V_{IH}$ | | 0.7 × VDD | | VDD + 0.3 | V |
| $I_{IL}$ | | −1 | | +1 | µA |
| $I_{IH}$ | | −1 | | +1 | µA |
| Input Capacitance | | | 5 | | pF |
| DIGITAL OUTPUTS | | | | | |
| Data Format | | Serial 16 bits twos complement | | | |
| $V_{OH}$ | $I_{SOURCE}$ = −500 µA | VDD − 0.3 | | | V |
| $V_{OL}$ | $I_{SINK}$ = +500 µA | | | 0.4 | V |
| POWER SUPPLIES | | | | | |
| VDD | Specified performance | 2.7 | | 5.5 | V |
| VDD Range[2] | | 2.0 | | 5.5 | V |
| Operating Current | 100 kSPS throughput | | | | |
| | VDD = 5 V | | 800 | | µA |
| | VDD = 2.7 V | | 560 | | µA |
| Standby Current[3, 4] | VDD = 5 V, 25°C | | 1 | 50 | nA |
| Power Dissipation | VDD = 5 V | | 4 | 6 | mW |
| | VDD = 2.7 V | | 1.5 | | mW |
| | VDD = 2.7 V, 10 kSPS throughput[3] | | 150 | | µW |
| TEMPERATURE RANGE | | | | | |
| Specified Performance | $T_{MIN}$ to $T_{MAX}$ | −40 | | +85 | °C |

[1] The inputs must be driven differentially 180° from each other. See Pin Configuration and Function Descriptions and Analog Inputs sections.
[2] See the Typical Performance Characteristics section for more information.
[3] With all digital inputs forced to VDD or GND, as required.
[4] During acquisition phase.

VDD = 5 V; $V_{REF}$ = VDD; $T_A$ = −40°C to +85°C, unless otherwise noted.

**Table 3.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ACCURACY | | | | | |
| No Missing Codes | | 16 | | | Bits |
| Integral Linearity Error | | −3 | ±1 | +3 | LSB |
| Transition Noise | | | 0.5 | | LSB |
| Gain Error,[1] $T_{MIN}$ to $T_{MAX}$ | | | ±2 | ±15 | LSB |
| Gain Error Temperature Drift | | | ±0.3 | | ppm/°C |
| Zero Error,[1] $T_{MIN}$ to $T_{MAX}$ | | | ±0.4 | ±1.6 | mV |
| Zero Temperature Drift | | | ±0.3 | | ppm/°C |
| Power Supply Sensitivity | VDD = 5 V ± 5% | | ±0.05 | | LSB |
| AC ACCURACY | | | | | |
| Signal-to-Noise Ratio | $f_{IN}$ = 1 kHz | 88 | 91 | | dB[2] |
| Spurious-Free Dynamic Range | $f_{IN}$ = 1 kHz | | −108 | | dB |
| Total Harmonic Distortion | $f_{IN}$ = 1 kHz | | −106 | | dB |
| Signal-to-(Noise + Distortion) | $f_{IN}$ = 1 kHz | 88 | 91 | | dB |
| Effective Number of Bits | $f_{IN}$ = 1 kHz | | 14.8 | | Bits |

[1] See the Terminology section. These specifications include full temperature range variation but do not include the error contribution from the external reference.
[2] All specifications in dB are referred to a full-scale input, FS. Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

VDD = 2.7 V; $V_{REF}$ = 2.5 V; $T_A$ = −40°C to +85°C, unless otherwise noted.

**Table 4.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ACCURACY | | | | | |
| No Missing Codes | | 16 | | | Bits |
| Integral Linearity Error | | −3 | ±1 | +3 | LSB |
| Transition Noise | | | 0.85 | | LSB |
| Gain Error,[1] $T_{MIN}$ to $T_{MAX}$ | | | ±2 | ±15 | LSB |
| Gain Error Temperature Drift | | | ±0.3 | | ppm/°C |
| Zero Error,[1] $T_{MIN}$ to $T_{MAX}$ | | | ±0.7 | ±3.5 | mV |
| Zero Temperature Drift | | | ±0.3 | | ppm/°C |
| Power Supply Sensitivity | VDD = 2.7 V ± 5% | | ±0.05 | | LSB |
| AC ACCURACY | | | | | |
| Signal-to-Noise Ratio | $f_{IN}$ = 1 kHz | | 86 | | dB[2] |
| Spurious-Free Dynamic Range | $f_{IN}$ = 1 kHz | | −100 | | dB |
| Total Harmonic Distortion | $f_{IN}$ = 1 kHz | | −98 | | dB |
| Signal-to-(Noise + Distortion) | $f_{IN}$ = 1 kHz | | 86 | | dB |
| Effective Number of Bits | $f_{IN}$ = 1 kHz | | 14 | | Bits |

[1] See the Terminology section. These specifications do include full temperature range variation but do not include the error contribution from the external reference.
[2] All specifications in dB are referred to a full-scale input, FS. Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

## TIMING SPECIFICATIONS

VDD = 2.7 V to 5.5 V, $T_A$ = −40°C to +85°C, unless otherwise noted.

**Table 5.**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Throughput Rate | $t_{CYC}$ | | | 100 | kHz |
| $\overline{CS}$ Falling to DCLOCK Low | $t_{CSD}$ | | | 0 | µs |
| $\overline{CS}$ Falling to DCLOCK Rising | $t_{SUCS}$ | 20 | | | ns |
| DCLOCK Falling to Data Remains Valid | $t_{HDO}$ | 5 | 16 | | ns |
| $\overline{CS}$ Rising Edge to $D_{OUT}$ High Impedance | $t_{DIS}$ | | 14 | 100 | ns |
| DCLOCK Falling to Data Valid | $t_{EN}$ | | 16 | 50 | ns |
| Acquisition Time | $t_{ACQ}$ | 400 | | | ns |
| $D_{OUT}$ Fall Time | $t_F$ | | 11 | 25 | ns |
| $D_{OUT}$ Rise Time | $t_R$ | | 11 | 25 | ns |

### *Timing Diagrams*

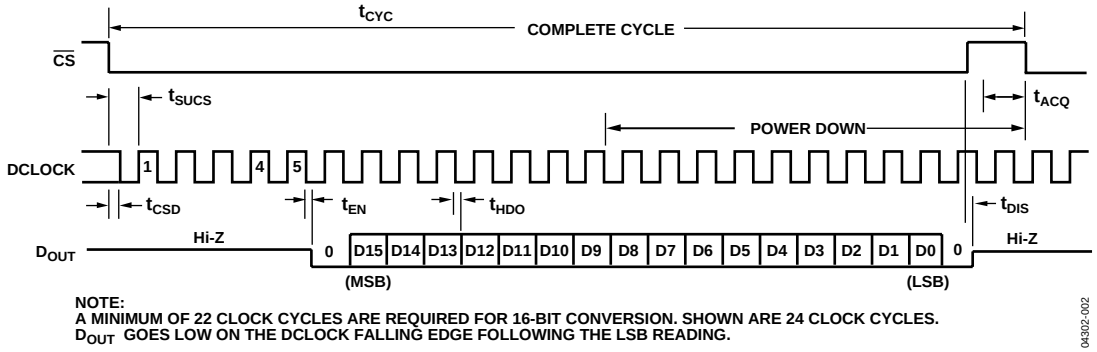



*Figure 2. Serial Interface Timing*

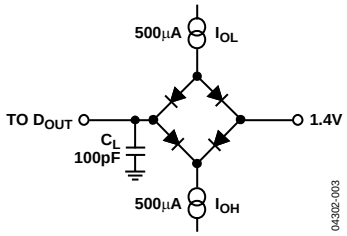



*Figure 3. Load Circuit for Digital Interface Timing*

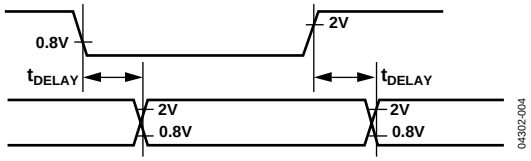



*Figure 4. Voltage Reference Levels for Timing*




*Figure 5. $D_{OUT}$ Rise and Fall Timing*

# ABSOLUTE MAXIMUM RATINGS

**Table 6.**

| Parameter | Rating |
|---|---|
| Analog Inputs | |
| +IN[1], –IN[1] | GND – 0.3 V to VDD + 0.3 V or ±130 mA |
| REF | GND – 0.3 V to VDD + 0.3 V |
| Supply Voltages | |
| VDD to GND | –0.3 V to +6 V |
| Digital Inputs to GND | –0.3 V to VDD + 0.3 V |
| Digital Outputs to GND | –0.3 V to VDD + 0.3 V |
| Storage Temperature Range | –65°C to +150°C |
| Junction Temperature | 150°C |
| $\theta_{JA}$ Thermal Impedance | 200°C/W |
| $\theta_{JC}$ Thermal Impedance | 44°C/W |
| Lead Temperature | JEDEC J-STD-20 |

[1] See the Analog Inputs section.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

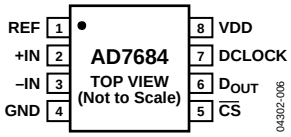



*Figure 6. 8-Lead MSOP Pin Configuration*

**Table 7. Pin Function Descriptions**

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 1 | REF | AI | Reference Input Voltage. The REF range is from 0.5 V to VDD. This pin is referred to the GND pin and should be decoupled closely to the GND pin with a ceramic capacitor of a few µF. |
| 2 | +IN | AI | Differential Positive Analog Input. Referenced to –IN. The input range for +IN is between 0 V and $V_{REF}$, centered about $V_{REF}/2$ and must be driven 180° out of phase with –IN. |
| 3 | –IN | AI | Differential Negative Analog Input. Referenced to +IN. The input range for –IN is between $V_{REF}$ and 0 V, centered about $V_{REF}/2$ and must be driven 180° out of phase with +IN. |
| 4 | GND | P | Power Supply Ground. |
| 5 | $\overline{CS}$ | DI | Chip Select Input. On its falling edge, it initiates the conversions. The part returns to shutdown mode as soon as the conversion is complete. It also enables $D_{OUT}$. When high, $D_{OUT}$ is high impedance. |
| 6 | $D_{OUT}$ | DO | Serial Data Output. The conversion result is output on this pin. It is synchronized to DCLOCK. |
| 7 | DCLOCK | DI | Serial Data Clock Input. |
| 8 | VDD | P | Power Supply. |

[1] AI = analog input, DI = digital input, DO = digital output, and P = power.

# TERMINOLOGY

**Integral Nonlinearity Error (INL)**
Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 21).

**Differential Nonlinearity Error (DNL)**
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

**Zero Error**
Zero error is the difference between the ideal midscale voltage, that is, 0 V, and the actual voltage producing the midscale output code, that is, 0 LSB.

**Gain Error**
The first transition (from 100 . . . 00 to 100 . . . 01) should occur at a level ½ LSB above the nominal negative full scale (−4.999924 V for the ±5 V range). The last transition (from 011…10 to 011…11) should occur for an analog voltage 1½ LSB below the nominal full scale (4.999771 V for the ±5 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

**Spurious-Free Dynamic Range (SFDR)**
SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

**Effective Number of Bits (ENOB)**
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD by the following formula

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

and is expressed in bits.

**Total Harmonic Distortion (THD)**
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in dB.

**Signal-to-Noise Ratio (SNR)**
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in dB.

**Signal-to-(Noise + Distortion) Ratio (SINAD)**
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in dB.

**Aperture Delay**
Aperture delay is a measure of the acquisition performance and is the time between the falling edge of the $\overline{CS}$ input and when the input signal is held for a conversion.

**Transient Response**
Transient response is the time required for the ADC to accurately acquire its input after a full-scale step function is applied.

# TYPICAL PERFORMANCE CHARACTERISTICS

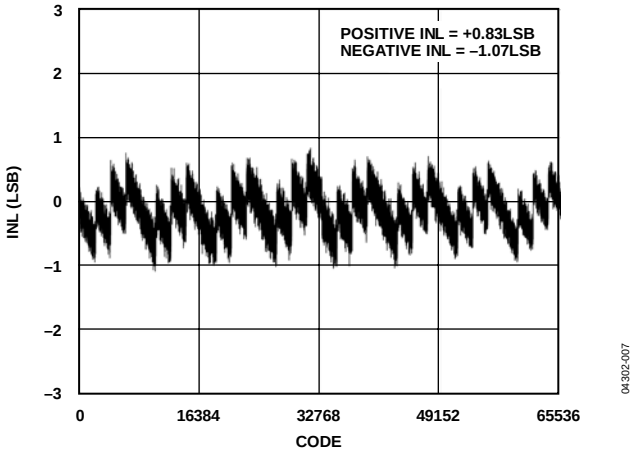



*Figure 7. Integral Nonlinearity vs. Code*

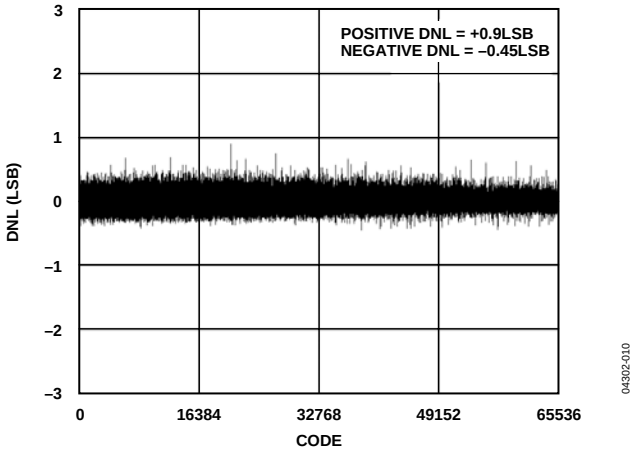



*Figure 10. Differential Nonlinearity vs. Code*

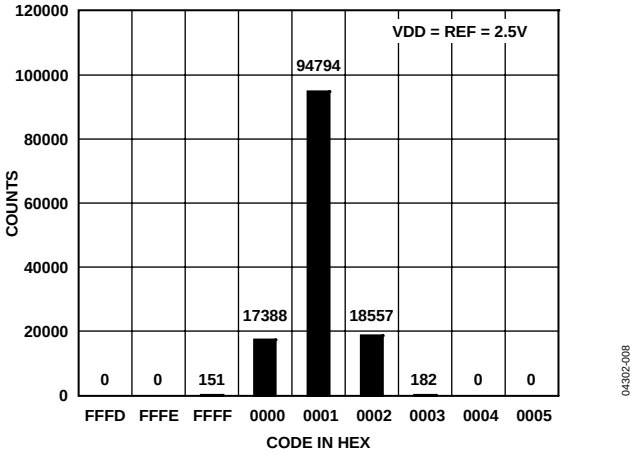



*Figure 8. Histogram of a DC Input at the Code Center*

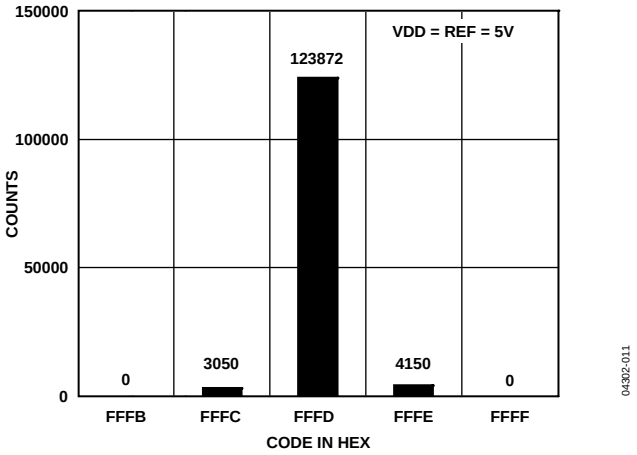



*Figure 11. Histogram of a DC Input at the Code Center*

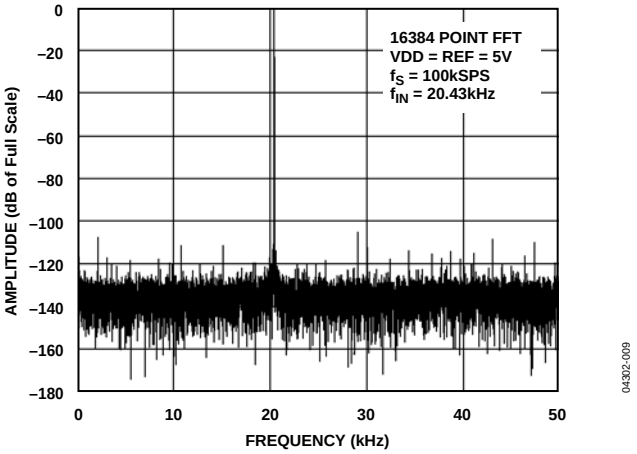



*Figure 9. FFT Plot*

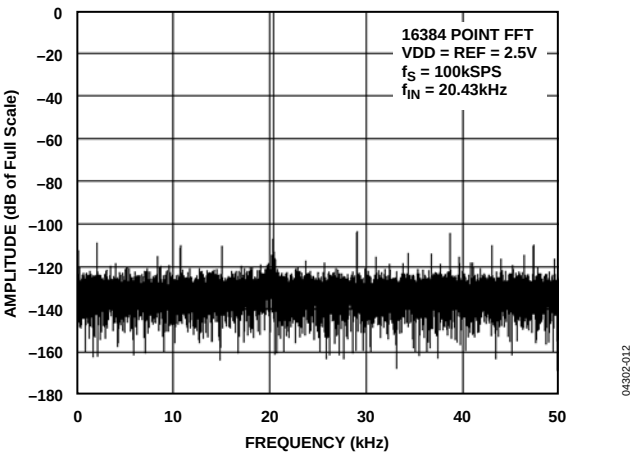



*Figure 12. FFT Plot*

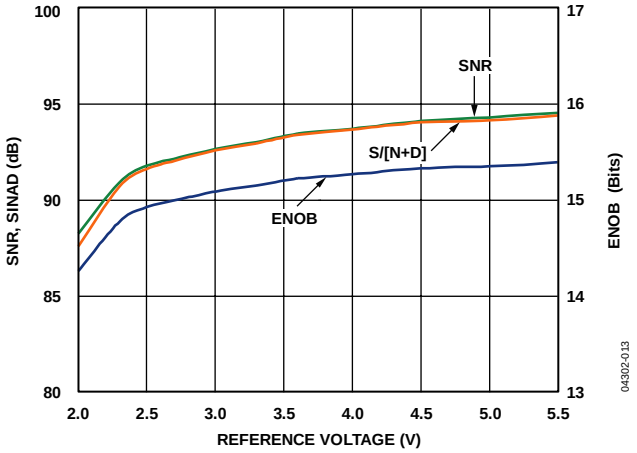



Figure 13. SNR, SINAD, and ENOB vs. Reference Voltage

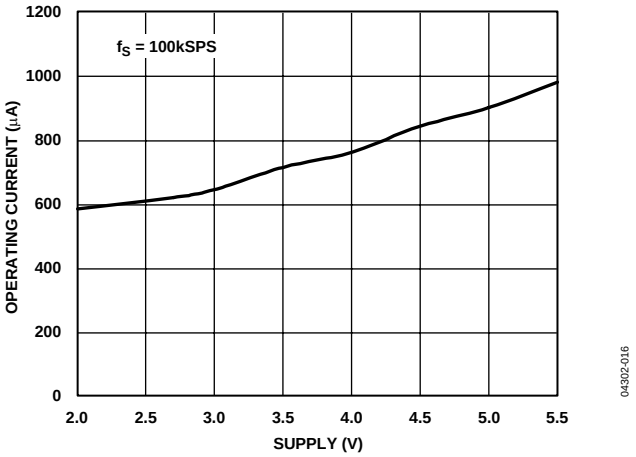



Figure 16. Operating Current vs. Supply

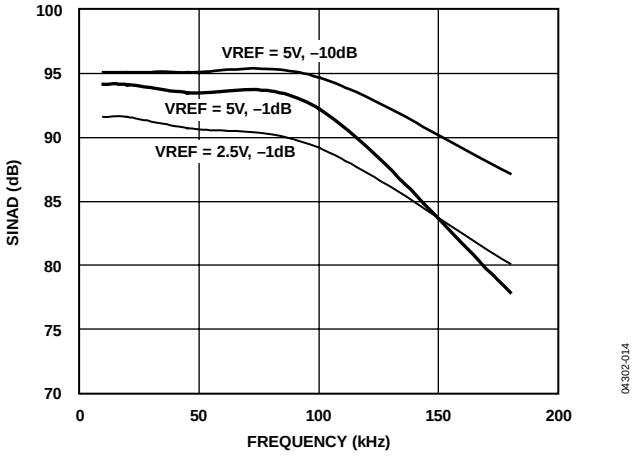



Figure 14. SINAD vs. Frequency

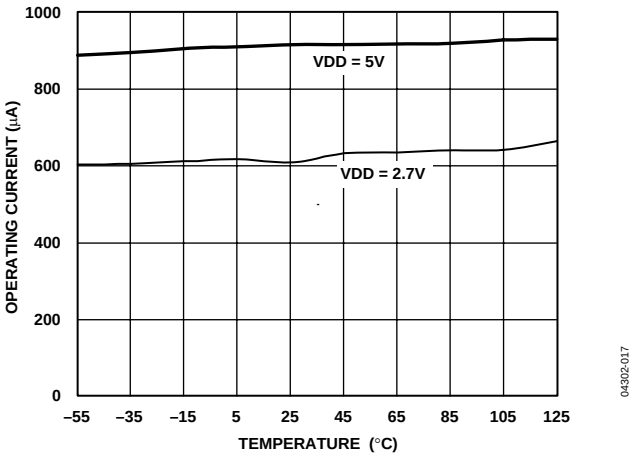



Figure 17. Operating Current vs. Temperature

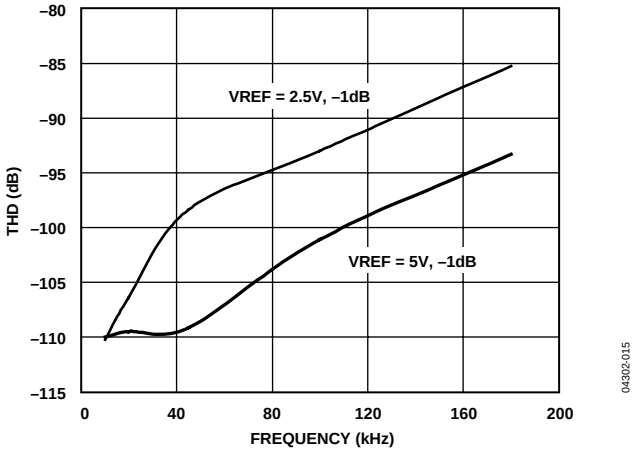



Figure 15. THD vs. Frequency

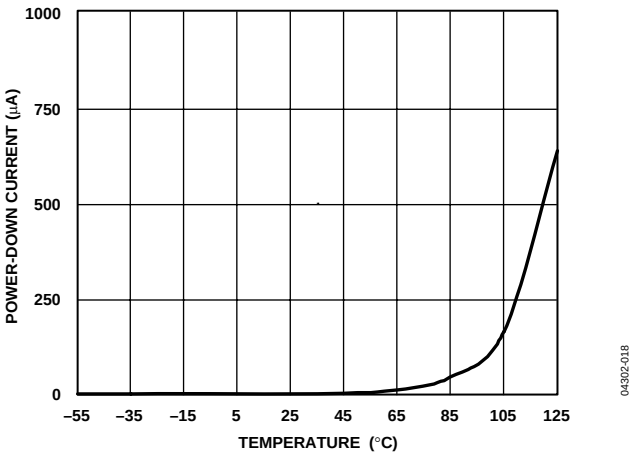



Figure 18. Power-Down Current vs. Temperature

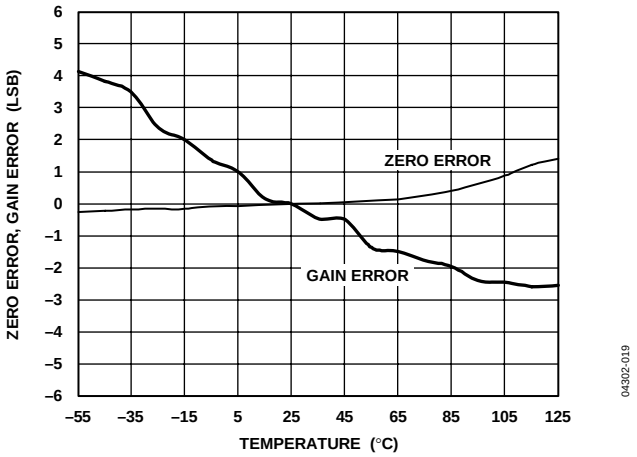



*Figure 19. Zero Error and Gain Error vs. Temperature*

# APPLICATION INFORMATION

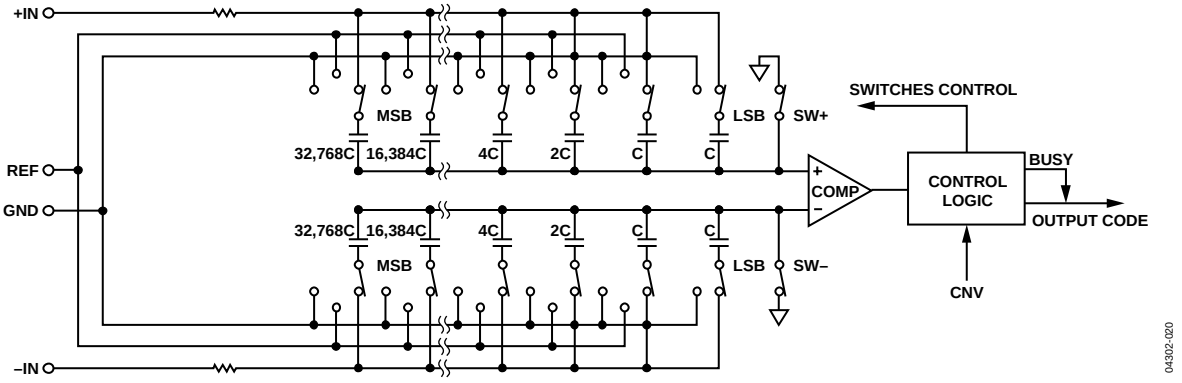



*Figure 20. ADC Simplified Schematic*

## CIRCUIT INFORMATION

The AD7684 is a low power, single-supply, 16-bit ADC using a successive approximation architecture. It is capable of converting 100,000 samples per second (100 kSPS) and powers down between conversions. When operating at 10 kSPS, for example, it consumes typically 150 μW with a 2.7 V supply, ideal for battery-powered applications.

The AD7684 provides the user with an on-chip, track-and-hold and does not exhibit any pipeline delay or latency, making it ideal for multiple, multiplexed channel applications.

The AD7684 is specified from 2.7 V to 5.5 V. It is housed in an 8-lead MSOP.

## CONVERTER OPERATION

The AD7684 is a successive approximation ADC based on a charge redistribution DAC. Figure 20 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary-weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the input of the comparator are connected to GND via SW+ and SW−. All independent switches are connected to the analog inputs. Therefore, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the +IN and −IN inputs. When the acquisition phase is complete and the $\overline{CS}$ input goes low, a conversion phase is initiated. When the conversion phase begins, SW+ and SW− are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the inputs, +IN and −IN, captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REF, the comparator input varies by binary-weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$...$V_{REF}/65{,}536$). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition. After the completion of this process, the part returns to the acquisition phase and the control logic generates the ADC output code.

## TRANSFER FUNCTIONS

The ideal transfer function for the AD7684 is shown in Figure 21 and Table 8.

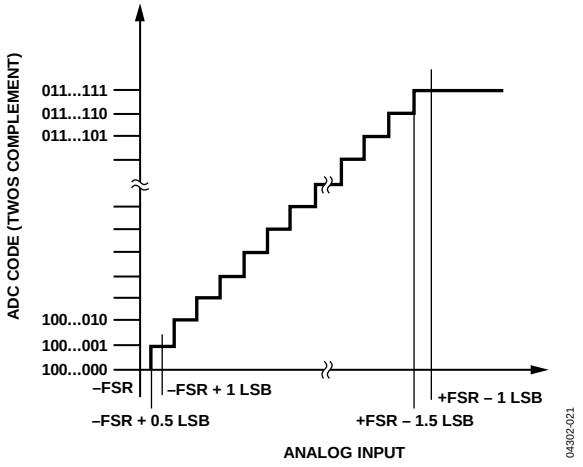



*Figure 21. ADC Ideal Transfer Function*

**Table 8. Output Codes and Ideal Input Voltages**

| Description | Analog Input $V_{REF}$ = 5 V | Digital Output Code Hex |
|---|---|---|
| FSR – 1 LSB | +4.999847 V | 7FFF[1] |
| Midscale + 1 LSB | +152.6 μV | 0001 |
| Midscale | 0 V | 0000 |
| Midscale – 1 LSB | −152.6 μV | FFFF |
| −FSR + 1 LSB | −4.999847 V | 8001 |
| −FSR | −5 V | 8000[2] |

[1] This is also the code for an overranged analog input ($V_{+IN} – V_{–IN}$ above $V_{REF} – V_{GND}$).
[2] This is also the code for an underranged analog input ($V_{+IN} – V_{–IN}$ below $–V_{REF} + V_{GND}$).

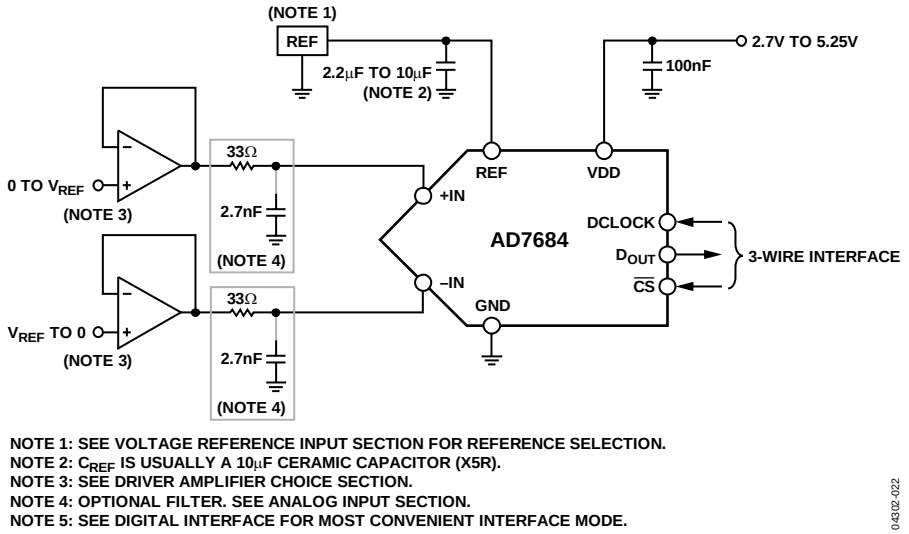



*Figure 22. Typical Application Diagram*

## TYPICAL CONNECTION DIAGRAM

Figure 22 shows an example of the recommended application diagram for the AD7684.

## ANALOG INPUTS

The analog inputs (+IN, −IN) need to be driven differentially 180° from each other, as shown in Figure 22. Holding either input at GND or a fixed dc gives erroneous conversion results because the AD7684 is intended for differential operation only. For applications requiring −IN to be at GND (±100 mV), the AD7683 should be used.

Figure 23 shows an equivalent circuit of the input structure of the AD7684. The two diodes, D1 and D2, provide ESD protection for the analog inputs, +IN and −IN. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 0.3 V because this causes these diodes to become forward-biased and start conducting current. However, these diodes can handle a forward-biased current of 130 mA maximum. For instance, these conditions could eventually occur when the supplies of the input buffer (U1) are different from VDD. In such a case, an input buffer with a short-circuit current limitation can be used to protect the part.

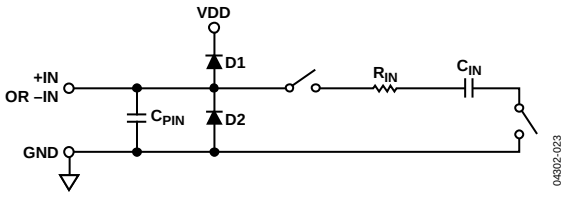



*Figure 23. Equivalent Analog Input Circuit*

This analog input structure allows the sampling of the differential signal between +IN and −IN. By using this differential input, small signals common to both inputs are rejected. During the acquisition phase, the impedance of the analog inputs can be modeled as a parallel combination of the Capacitor $C_{PIN}$ and the network formed by the series connection of $R_{IN}$ and $C_{IN}$. $C_{PIN}$ is primarily the pin capacitance. $R_{IN}$ is typically 600 Ω and is a lumped component made up of some serial resistors and the on-resistance of the switches. $C_{IN}$ is typically 30 pF and is mainly the ADC sampling capacitor. During the conversion phase, when the switches are opened, the input impedance is limited to $C_{PIN}$. $R_{IN}$ and $C_{IN}$ make a 1-pole, low-pass filter that reduces undesirable aliasing effects and limits the noise.

When the source impedance of the driving circuit is low, the AD7684 can be driven directly. Large source impedances significantly affect the ac performance, especially THD. The dc performances are less sensitive to the input impedance.

## DRIVER AMPLIFIER CHOICE

Although the AD7684 is easy to drive, the driver amplifier needs to meet the following requirements:

- The noise generated by the driver amplifier needs to be kept as low as possible to preserve the SNR and transition noise performance of the AD7684. Note that the AD7684 has a noise level much lower than most other 16-bit ADCs and, therefore, can be driven by a noisier op amp while preserving the same or better system performance. The noise coming from the driver is filtered by the AD7684 analog input circuit 1-pole, low-pass filter made by $R_{IN}$ and $C_{IN}$ or by the external filter, if one is used.
- For ac applications, the driver needs to have a THD performance commensurate with the AD7684. Figure 15 shows the THD vs. frequency that the driver should exceed.
- For multichannel multiplexed applications, the driver amplifier and the AD7684 analog input circuit must be able to settle for a full-scale step of the capacitor array at a 16-bit level (0.0015%). In the data sheet of the amplifier, settling at 0.1% to 0.01% is more commonly specified. This could differ significantly from the settling time at a 16-bit level and should be verified prior to driver selection.

**Table 9. Recommended Driver Amplifiers**

| Amplifier | Typical Application |
|---|---|
| ADA4841-x | Very low noise |
| ADA4941-1 | Very low noise, single to differential |
| AD8021 | Very low noise and high frequency |
| AD8022 | Low noise and high frequency |
| OP184 | Low power, low noise, and low frequency |
| AD8605, AD8615 | 5 V single-supply, low power |
| AD8519 | Small, low power, and low frequency |
| AD8031 | High frequency and low power |

## VOLTAGE REFERENCE INPUT

The AD7684 voltage reference input, REF, has a dynamic input impedance. It should therefore be driven by a low impedance source with efficient decoupling between the REF and GND pins, as explained in more detail in the Layout section.

When REF is driven by a very low impedance source (for example, an unbuffered reference voltage such as the low temperature drift ADR43x reference or a reference buffer using the AD8031 or the AD8605), a 10 µF (X5R, 0805 size) ceramic chip capacitor is appropriate for optimum performance.

If desired, smaller reference decoupling capacitor values down to 2.2 µF can be used with minimal impact on performance, especially DNL.

## POWER SUPPLY

The AD7684 powers down automatically at the end of each conversion phase and therefore the power scales linearly with the sampling rate, as shown in Figure 24. This makes the part ideal for low sampling rates (even of a few Hz) and low battery powered applications.

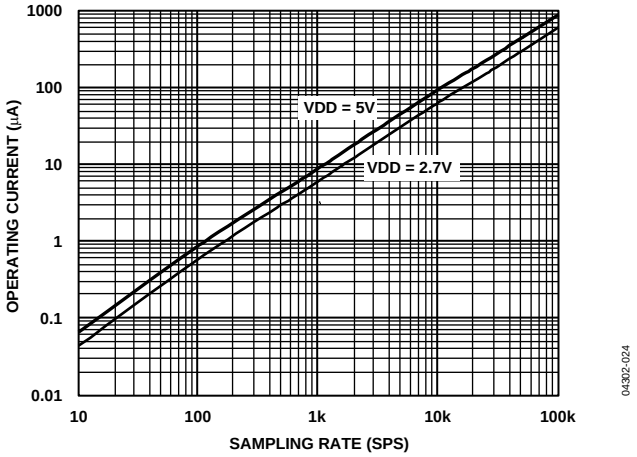



*Figure 24. Operating Current vs. Sampling Rate*

## DIGITAL INTERFACE

The AD7684 is compatible with SPI, QSPI, digital hosts, and DSPs (for example, Blackfin® ADSP-BF53x or ADSP-219x). The connection diagram is shown in Figure 25, and the corresponding timing is given in Figure 2.

A falling edge on $\overline{CS}$ initiates a conversion and the data transfer. After the fifth DCLOCK falling edge, $D_{OUT}$ is enabled and forced low. The data bits are then clocked MSB first by subsequent DCLOCK falling edges. The data is valid on both DCLOCK edges. Although the rising edge can be used to capture the data, a digital host also using the DCLOCK falling edge allows a faster reading rate, provided it has an acceptable hold time.

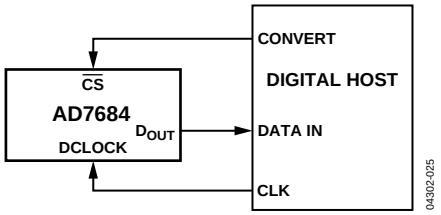



*Figure 25. Connection Diagram*

## LAYOUT

The printed circuit board housing the AD7684 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. The pinout of the AD7684 with all its analog signals on the left side and all its digital signals on the right side eases this task.

Avoid running digital lines under the device because these couple noise onto the die, unless a ground plane under the AD7684 is used as a shield. Fast switching signals, such as $\overline{CS}$ or clocks, should never run near analog signal paths. Crossover of digital and analog signals should be avoided.

At least one ground plane should be used. It could be common or split between the digital and analog sections. In such a case, it should be joined underneath the AD7684.

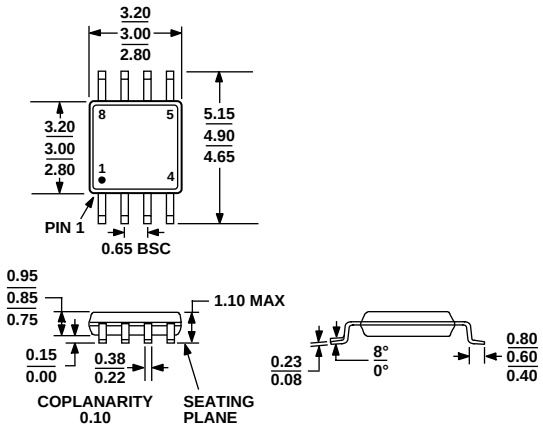
The AD7684 voltage reference input REF has a dynamic input impedance and should be decoupled with minimal parasitic inductances. This is done by placing the reference decoupling ceramic capacitor close to, and ideally right up against, the REF and GND pins and by connecting these pins with wide, low impedance traces.

Finally, the power supply, VDD, of the AD7684 should be decoupled with a ceramic capacitor, typically 100 nF, and placed close to the AD7684. It should be connected using short and large traces to provide low impedance paths and reduce the effect of glitches on the power supply lines.

## EVALUATING THE PERFORMANCE OF THE AD7684

Other recommended layouts for the AD7684 are outlined in the evaluation board for the AD7684 (EVAL-AD7684CBZ). The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the EVAL-CONTROL BRD3Z.

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MO-187-AA

*Figure 26. 8-Lead Mini Small Outline Package [MSOP]*
*(RM-8)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Integral Nonlinearity | Temperature Range | Package Description | Package Option | Ordering Quantity | Branding |
|---|---|---|---|---|---|---|
| AD7684BRM | ±3 LSB maximum | −40°C to +85°C | 8-Lead MSOP | RM-8 | 50 | C1D |
| AD7684BRMRL7 | ±3 LSB maximum | −40°C to +85°C | 8-Lead MSOP | RM-8 | 1,000 | C1D |
| AD7684BRMZ[1] | ±3 LSB maximum | −40°C to +85°C | 8-Lead MSOP | RM-8 | 50 | C39 |
| AD7684BRMZRL7[1] | ±3 LSB maximum | −40°C to +85°C | 8-Lead MSOP | RM-8 | 1,000 | C39 |
| EVAL-AD7684CBZ[1, 2] | | | Evaluation Board | | | |
| EVAL-CONTROL BRD3Z[1, 3] | | | Controller Board | | | |

[1] Z = RoHS Compliant Part.
[2] This board can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BRDx for evaluation/demonstration purposes.
[3] This board allows a PC to control and communicate with all the Analog Devices, Inc. evaluation boards ending in the CB designators.

# NOTES

©2004–2007 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D04302-0-10/07(A)