

FEATURES

Throughput

1 MSPS (Warp Mode)

800 kSPS (Normal Mode)

INL: ± 2.5 LSB Max ($\pm 0.0038\%$ of Full Scale)

16-Bit Resolution with No Missing Codes

S/(N+D): 90 dB Typ @ 250 kHz

THD: -100 dB Typ @ 250 kHz

Analog Input Voltage Ranges

Bipolar: ± 10 V, ± 5 V, ± 2.5 V

Unipolar: 0 V to 10 V, 0 V to 5 V, 0 V to 2.5 V

Both AC and DC Specifications

No Pipeline Delay

Parallel (8/16 Bits) and Serial 5 V/3 V Interface

SPI®/QSPI™/MICROWIRE™/DSP Compatible

Single 5 V Supply Operation

Power Dissipation

112 mW Typical

15 μ W @ 100 SPS

Power-Down Mode: 7 μ W Max

Package: 48-Lead Quad Flatpack (LQFP)

Package: 48-Lead Chip Scale (LFCSP)

Pin-to-Pin Compatible Upgrade of the AD7665/AD7664

APPLICATIONS

Data Acquisition

Communication

Instrumentation

Spectrum Analysis

Medical Instruments

Process Control

GENERAL DESCRIPTION

The AD7671 is a 16-bit, 1 MSPS, charge redistribution SAR, analog-to-digital converter that operates from a single 5 V power supply. It contains a high speed 16-bit sampling ADC, a resistor input scaler that allows various input ranges, an internal conversion clock, error correction circuits, and both serial and parallel system interface ports.

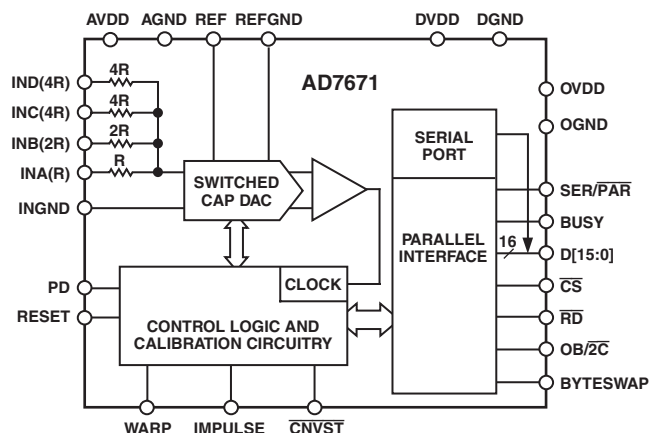
The AD7671 is hardware factory-calibrated and is comprehensively tested to ensure such ac parameters as signal-to-noise ratio (SNR) and total harmonic distortion (THD), in addition to the more traditional dc parameters of gain, offset, and linearity.

It features a very high sampling rate mode (Warp), a fast mode (Normal) for asynchronous conversion rate applications, and, for low power applications, a reduced power mode (Impulse) where the power is scaled with the throughput.

REV. C

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FUNCTIONAL BLOCK DIAGRAM



PulSAR Selection

Type/kSPS	100–250	500–570	800–1000
Pseudo Differential	AD7660	AD7650 AD7664	
True Bipolar	AD7663	AD7665	AD7671
True Differential	AD7675	AD7676	AD7677
18-Bit	AD7678	AD7679	AD7674
Simultaneous/ Multichannel		AD7654	AD7655

It is fabricated using Analog Devices' high performance, 0.6 micron CMOS process and is available in a 48-lead LQFP and a tiny 48-lead LFCSP, with operation specified from -40°C to $+85^{\circ}\text{C}$.

PRODUCT HIGHLIGHTS

- Fast Throughput**
The AD7671 is a very high speed (1 MSPS in Warp Mode and 800 kSPS in Normal Mode), charge redistribution, 16-bit SAR ADC.
- Single-Supply Operation**
The AD7671 operates from a single 5 V supply, dissipates only 112 mW typical, even lower when a reduced throughput is used with the reduced power mode (Impulse) and a power-down mode.
- Superior INL**
The AD7671 has a maximum integral nonlinearity of 2.5 LSB with no missing 16-bit code.
- Serial or Parallel Interface**
Versatile parallel (8 bits or 16 bits) or 2-wire serial interface arrangement compatible with both 3 V or 5 V logic.

AD7671—SPECIFICATIONS (–40°C to +85°C, AVDD = DVDD = 5 V, OVDD = 2.7 V to 5.25 V, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	$V_{IND} - V_{INGND}$	$\pm 4 \text{ REF}$, 0 V to 4 REF, $\pm 2 \text{ REF}$ (See Table I)			V
Common-Mode Input Voltage	V_{INGND}	–0.1		+0.5	V
Analog Input CMRR	$f_{IN} = 100 \text{ kHz}$		74		dB
Input Impedance			See Table I		
THROUGHPUT SPEED					
Complete Cycle	In Warp Mode			1	μs
Throughput Rate	In Warp Mode	1		1000	kSPS
Time between Conversions	In Warp Mode			1	ms
Complete Cycle	In Normal Mode			1.25	μs
Throughput Rate	In Normal Mode	0		800	kSPS
Complete Cycle	In Impulse Mode			1.5	μs
Throughput Rate	In Impulse Mode	0		666	kSPS
DC ACCURACY					
Integral Linearity Error		–2.5		+2.5	LSB ¹
No Missing Codes		16			Bits
Transition Noise			0.7		LSB
Bipolar Zero Error ² , T_{MIN} to T_{MAX}	$\pm 5 \text{ V}$ Range, Normal or Impulse Modes	–45		+45	LSB
	Other Range or Mode	–0.1		+0.1	% of FSR
Bipolar Full-Scale Error ² , T_{MIN} to T_{MAX}		–0.38		+0.38	% of FSR
Unipolar Zero Error ² , T_{MIN} to T_{MAX}		–0.18		+0.18	% of FSR
Unipolar Full-Scale Error ² , T_{MIN} to T_{MAX}		–0.76		+0.76	% of FSR
Power Supply Sensitivity	$AVDD = 5 \text{ V} \pm 5\%$		± 9.5		LSB
AC ACCURACY					
Signal-to-Noise	$f_{IN} = 20 \text{ kHz}$	89	90		dB ³
	$f_{IN} = 250 \text{ kHz}$		90		dB
Spurious-Free Dynamic Range	$f_{IN} = 250 \text{ kHz}$		100		dB
Total Harmonic Distortion	$f_{IN} = 20 \text{ kHz}$		–100	–96	dB
	$f_{IN} = 250 \text{ kHz}$		–100		dB
Signal-to-(Noise+Distortion)	$f_{IN} = 20 \text{ kHz}$	88.5	90		dB
	$f_{IN} = 250 \text{ kHz}$		30		dB
–3 dB Input Bandwidth	$f_{IN} = 250 \text{ kHz}$, –60 dB Input		9.6		MHz
SAMPLING DYNAMICS					
Aperture Delay			2		ns
Aperture Jitter			5		ps rms
Transient Response	Full-Scale Step			250	ns
REFERENCE					
External Reference Voltage Range		2.3	2.5	$AVDD - 1.85$	V
External Reference Current Drain	1 MSPS Throughput		200		μA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		–0.3		+0.8	V
V_{IH}		+2.0		$DVDD + 0.3$	V
I_{IL}		–1		+1	μA
I_{IH}		–1		+1	μA
DIGITAL OUTPUTS					
Data Format					
Pipeline Delay					
V_{OL}	$I_{SINK} = 1.6 \text{ mA}$				V
V_{OH}	$I_{SOURCE} = -570 \mu\text{A}$				V
		$OVDD - 0.6$		0.4	

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLIES					
Specified Performance					
AVDD		4.75	5	5.25	V
DVDD		4.75	5	5.25	V
OVDD		2.7		5.25 ⁴	V
Operating Current ⁵	1 MSPS Throughput				
AVDD			15		mA
DVDD ⁶			7.2		mA
OVDD ⁶			37		μA
Power Dissipation ^{6, 7}	666 kSPS Throughput ⁸		84	95	mW
	100 SPS Throughput ⁸		15		μW
	1 MSPS Throughput ⁵		112	125	mW
In Power-Down Mode ⁹				7	μW
TEMPERATURE RANGE¹⁰					
Specified Performance	T _{MIN} to T _{MAX}	−40		+85	°C

NOTES

¹LSB means least significant bit. With the ±5 V input range, one LSB is 152.588 μV.

²See Definition of Specifications section. These specifications do not include the error contribution from the external reference.

³All specifications in dB are referred to a full-scale input FS. Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

⁴The max should be the minimum of 5.25 V and DVDD + 0.3 V.

⁵In Warp Mode.

⁶Tested in Parallel Reading Mode.

⁷Tested with the 0 V to 5 V range and V_{IN} − V_{INGND} = 0 V. See Power Dissipation section.

⁸In Impulse Mode.

⁹With OVDD below DVDD + 0.3 V and all digital inputs forced to DVDD or DGND, respectively.

¹⁰Contact factory for extended temperature range.

Specifications subject to change without notice.

Table I. Analog Input Configuration

Input Voltage Range	IND(4R)	INC(4R)	INB(2R)	INA(R)	Input Impedance ¹
±4 REF ²	V _{IN}	INGND	INGND	REF	1.63 kΩ
±2 REF	V _{IN}	V _{IN}	INGND	REF	948 Ω
±REF	V _{IN}	V _{IN}	V _{IN}	REF	711 Ω
0 V to 4 REF	V _{IN}	V _{IN}	INGND	INGND	948 Ω
0 V to 2 REF	V _{IN}	V _{IN}	V _{IN}	INGND	711 Ω
0 V to REF	V _{IN}	V _{IN}	V _{IN}	V _{IN}	Note 3

NOTES

¹Typical analog input impedance.

²With REF = 3 V, in this range, the input should be limited to −11 V to +12 V.

³For this range the input is high impedance.

TIMING SPECIFICATIONS (−40°C to +85°C, AVDD = DVDD = 5 V, OVDD = 2.7 V to 5.25 V, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Refer to Figures 11 and 12					
Convert Pulsewidth	t ₁	5			ns
Time between Conversions (Warp Mode/Normal Mode/Impulse Mode)	t ₂	1/1.25/1.5		Note 1	μs
CNVST LOW to BUSY HIGH Delay	t ₃			30	ns
BUSY HIGH All Modes Except in Master Serial Read after Convert Mode (Warp Mode/Normal Mode/Impulse Mode)	t ₄			0.75/1/1.25	μs
Aperture Delay	t ₅		2		ns
End of Conversion to BUSY LOW Delay	t ₆	10			ns
Conversion Time (Warp Mode/Normal Mode/Impulse Mode)	t ₇			0.75/1/1.25	μs
Acquisition Time	t ₈	250			ns
RESET Pulsewidth	t ₉	10			ns

TIMING SPECIFICATIONS (continued)

Parameter	Symbol	Min	Typ	Max	Unit
Refer to Figures 13, 14, 15, and 16 (Parallel Interface Modes)					
$\overline{\text{CNVST}}$ LOW to DATA Valid Delay (Warp Mode/Normal Mode/Impulse Mode)	t_{10}			0.75/1/1.25	μs
DATA Valid to BUSY LOW Delay	t_{11}	20			ns
Bus Access Request to DATA Valid	t_{12}			40	ns
Bus Relinquish Time	t_{13}	5		15	ns
Refer to Figures 17 and 18 (Master Serial Interface Modes) ²					
$\overline{\text{CS}}$ LOW to SYNC Valid Delay	t_{14}			10	ns
$\overline{\text{CS}}$ LOW to Internal SCLK Valid Delay	t_{15}			10	ns
$\overline{\text{CS}}$ LOW to SDOUT Delay	t_{16}			10	ns
$\overline{\text{CNVST}}$ LOW to SYNC Delay (Read during Convert) (Warp Mode/Normal Mode/Impulse Mode)	t_{17}		25/275/525		ns
SYNC Asserted to SCLK First Edge Delay ³	t_{18}	4			ns
Internal SCLK Period ³	t_{19}	25		40	ns
Internal SCLK HIGH ³	t_{20}	15			ns
Internal SCLK LOW ³	t_{21}	9.5			ns
SDOUT Valid Setup Time ³	t_{22}	4.5			ns
SDOUT Valid Hold Time ³	t_{23}	2			ns
SCLK Last Edge to SYNC Delay ³	t_{24}	3			ns
$\overline{\text{CS}}$ HIGH to SYNC HI-Z	t_{25}			10	ns
$\overline{\text{CS}}$ HIGH to Internal SCLK HI-Z	t_{26}			10	ns
$\overline{\text{CS}}$ HIGH to SDOUT HI-Z	t_{27}			10	ns
BUSY HIGH in Master Serial Read after Convert ³	t_{28}		See Table II		μs
$\overline{\text{CNVST}}$ LOW to SYNC Asserted Delay (Warp Mode/Normal Mode/Impulse Mode)	t_{29}		0.75/1/1.25		μs
Master Serial Read after Convert					
SYNC Deasserted to BUSY LOW Delay	t_{30}		25		ns
Refer to Figures 19 and 21 (Slave Serial Interface Modes)					
External SCLK Setup Time	t_{31}	5			ns
External SCLK Active Edge to SDOUT Delay	t_{32}	3		16	ns
SDIN Setup Time	t_{33}	5			ns
SDIN Hold Time	t_{34}	5			ns
External SCLK Period	t_{35}	25			ns
External SCLK HIGH	t_{36}	10			ns
External SCLK LOW	t_{37}	10			ns

NOTES

¹In Warp Mode only, the maximum time between conversions is 1 ms; otherwise, there is no required maximum time.

²In serial interface modes, the SYNC, SCLK, and SDOUT timings are defined with a maximum load C_L of 10 pF; otherwise, the load is 60 pF maximum.

³In Serial Master Read during Convert Mode. See Table II for Master Read after Convert Mode.

Specifications subject to change without notice.

Table II. Serial Clock Timings in Master Read after Convert

DIVSCLK[1] DIVSCLK[0]		0 0	0 1	1 0	1 1	Unit
SYNC to SCLK First Edge Delay Minimum	t_{18}	4	20	20	20	ns
Internal SCLK Period Minimum	t_{19}	25	50	100	200	ns
Internal SCLK Period Maximum	t_{19}	40	70	140	280	ns
Internal SCLK HIGH Minimum	t_{20}	15	25	50	100	ns
Internal SCLK LOW Minimum	t_{21}	9	24	49	99	ns
SDOUT Valid Setup Time Minimum	t_{22}	4.5	22	22	22	ns
SDOUT Valid Hold Time Minimum	t_{23}	2	4	30	89	ns
SCLK Last Edge to SYNC Delay Minimum	t_{24}	3	60	140	300	ns
BUSY HIGH Width Maximum (Warp)	t_{28}	1.5	2	3	5.25	μs
BUSY HIGH Width Maximum (Normal)	t_{28}	1.75	2.25	3.25	5.5	μs
BUSY HIGH Width Maximum (Impulse)	t_{28}	2	2.5	3.5	5.75	μs

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹**Analog Inputs**

IND², INC², INB² -11 V to +30 V
 INA, REF, INGND, REFGND, AGND
 -0.3 V to AVDD + 0.3 V

Ground Voltage Differences

AGND, DGND, OGND ± 0.3 V

Supply Voltages

AVDD, DVDD, OVDD -0.3 V to +7 V
 AVDD to DVDD, AVDD to OVDD ± 7 V
 DVDD to OVDD -0.3 V to +7 V
 Digital Inputs -0.3 V to DVDD + 0.3 V

Internal Power Dissipation³ 700 mW

Internal Power Dissipation⁴ 2.5 W

Junction Temperature 150°C

Storage Temperature Range -65°C to +150°C

Lead Temperature Range

(Soldering 10 sec) 300°C

NOTES

¹ Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

² See Analog Inputs section.

³ Specification is for device in free air: 48-Lead LQFP: $\theta_{JA} = 91^\circ\text{C/W}$, $\theta_{JC} = 30^\circ\text{C/W}$.

⁴ Specification is for device in free air: 48-Lead LFCSP: $\theta_{JA} = 26^\circ\text{C/W}$.

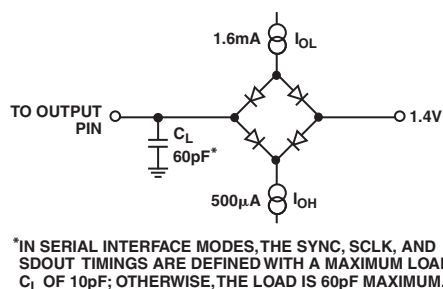
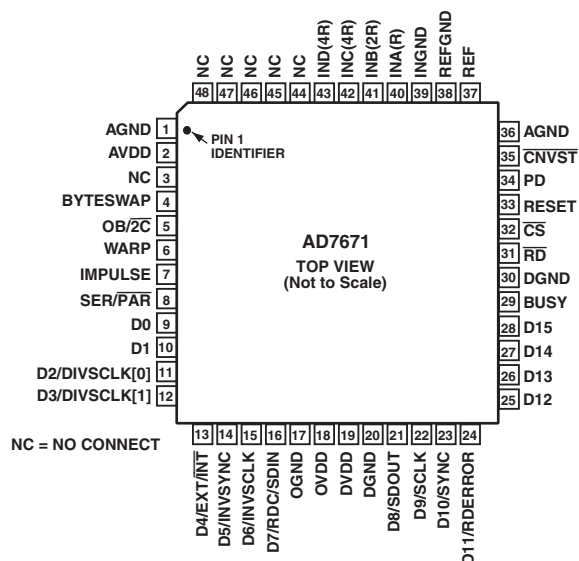


Figure 1. Load Circuit for Digital Interface Timing, SDOUT, SYNC, SCLK Outputs, $C_L = 10$ pF

PIN CONFIGURATION
ST-48 and CP-48-1**NOTES:**

1. PADDLE CONNECTED TO AGND FOR THE LFCSP (CP-48-1). THIS CONNECTION IS NOT REQUIRED TO MEET THE ELECTRICAL PERFORMANCES.

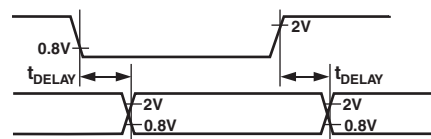


Figure 2. Voltage Reference Levels for Timing

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7671 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Type	Description
1	AGND	P	Analog Power Ground Pin.
2	AVDD	P	Input Analog Power Pin. Nominally 5 V.
3, 44–48	NC		No Connect.
4	BYTESWAP		Parallel Mode Selection (8-/16-Bit). When LOW, the LSB is output on D[7:0] and the MSB is output on D[15:8]. When HIGH, the LSB is output on D[15:8] and the MSB is output on D[7:0].
5	OB/ $\overline{2C}$	DI	Straight Binary/Binary Twos Complement. When OB/ $\overline{2C}$ is HIGH, the digital output is straight binary; when LOW, the MSB is inverted, resulting in a twos complement output from its internal shift register.
6	WARP	DI	Mode Selection. When HIGH and IMPULSE LOW, this input selects the fastest mode, the maximum throughput is achievable and a minimum conversion rate must be applied in order to guarantee full specified accuracy. When LOW, full accuracy is maintained independent of the minimum conversion rate.
7	IMPULSE	DI	Mode Selection. When HIGH and WARP LOW, this input selects a reduced Power Mode. In this mode, the power dissipation is approximately proportional to the sampling rate.
8	SER/ $\overline{PAR}$	DI	Serial/Parallel Selection Input. When LOW, the Parallel Port is selected; when HIGH, the Serial Interface Mode is selected and some bits of the data bus are used as a Serial Port.
9, 10	D[0:1]	DO	Bit 0 and Bit 1 of the Parallel Port Data Output Bus. When SER/ $\overline{PAR}$ is HIGH, these outputs are in high impedance.
11, 12	D[2:3] or DIVSCLK[0:1]	DI/O	When SER/ $\overline{PAR}$ is LOW, these outputs are used as Bit 2 and Bit 3 of the Parallel Port Data Output Bus. When SER/ $\overline{PAR}$ is HIGH, EXT/ $\overline{INT}$ is LOW and RDC/SDIN is LOW, which is the Serial Master Read after Convert Mode. These inputs, part of the Serial Port, are used to slow down, if desired, the internal serial clock that clocks the data output. In the other serial modes, these pins are high impedance outputs.
13	D[4] or EXT/ $\overline{INT}$	DI/O	When SER/ $\overline{PAR}$ is LOW, this output is used as Bit 4 of the Parallel Port Data Output Bus. When SER/ $\overline{PAR}$ is HIGH, this input, part of the Serial Port, is used as a digital select input for choosing the internal or an external data clock, called Master and Slave Modes, respectively. With EXT/ $\overline{INT}$ tied LOW, the internal clock is selected on SCLK output. With EXT/ $\overline{INT}$ set to a logic HIGH, output data is synchronized to an external clock signal connected to the SCLK input and the external clock is gated by $\overline{CS}$.
14	D[5] or INVSYN	DI/O	When SER/ $\overline{PAR}$ is LOW, this output is used as Bit 5 of the Parallel Port Data Output Bus. When SER/ $\overline{PAR}$ is HIGH, this input, part of the Serial Port, is used to select the active state of the SYNC signal. When LOW, SYNC is active HIGH. When HIGH, SYNC is active LOW.
15	D[6] or INVCLK	DI/O	When SER/ $\overline{PAR}$ is LOW, this output is used as Bit 6 of the Parallel Port Data Output Bus. When SER/ $\overline{PAR}$ is HIGH, this input, part of the Serial Port, is used to invert the SCLK signal. It is active in both Master and Slave Mode.
16	D[7] or RDC/SDIN	DI/O	When SER/ $\overline{PAR}$ is LOW, this output is used as Bit 7 of the Parallel Port Data Output Bus. When SER/ $\overline{PAR}$ is HIGH, this input, part of the Serial Port, is used as either an external data input or a read mode selection input, depending on the state of EXT/ $\overline{INT}$. When EXT/ $\overline{INT}$ is HIGH, RDC/SDIN could be used as a data input to daisy-chain the conversion results from two or more ADCs onto a single SDOUT line. The digital data level on SDIN is output on DATA with a delay of 16 SCLK periods after the initiation of the read sequence. When EXT/ $\overline{INT}$ is LOW, RDC/SDIN is used to select the Read Mode. When RDC/SDIN is HIGH, the previous data is output on SDOUT during conversion. When RDC/SDIN is LOW, the data can be output on SDOUT only when the conversion is complete.
17	OGND	P	Input/Output Interface Digital Power Ground.
18	OVDD	P	Input/Output Interface Digital Power. Nominally at the same supply as the supply of the host interface (5 V or 3 V).
19	DVDD	P	Digital Power. Nominally at 5 V.
20	DGND	P	Digital Power Ground.

PIN FUNCTION DESCRIPTION (continued)

Pin No.	Mnemonic	Type	Description
21	D[8] or SDOUT	DO	When $\text{SER}/\overline{\text{PAR}}$ is LOW, this output is used as Bit 8 of the Parallel Port Data Output Bus. When $\text{SER}/\overline{\text{PAR}}$ is HIGH, this output, part of the Serial Port, is used as a serial data output synchronized to SCLK. Conversion results are stored in an on-chip register. The AD7671 provides the conversion result, MSB first, from its internal shift register. The data format is determined by the logic level of $\text{OB}/\overline{2\text{C}}$. In Serial Mode, when $\text{EXT}/\overline{\text{INT}}$ is LOW, SDOUT is valid on both edges of SCLK. In Serial Mode, when $\text{EXT}/\overline{\text{INT}}$ is HIGH: If INVSCLK is LOW, SDOUT is updated on SCLK rising edge and valid on the next falling edge. If INVSCLK is HIGH, SDOUT is updated on SCLK falling edge and valid on the next rising edge.
22	D[9] or SCLK	DI/O	When $\text{SER}/\overline{\text{PAR}}$ is LOW, this output is used as Bit 9 of the Parallel Port Data Output Bus. When $\text{SER}/\overline{\text{PAR}}$ is HIGH, this pin, part of the Serial Port, is used as a serial data clock input or output, dependent upon the logic state of the $\text{EXT}/\overline{\text{INT}}$ pin. The active edge where the data SDOUT is updated depends upon the logic state of the INVSCLK pin.
23	D[10] or SYNC	DO	When $\text{SER}/\overline{\text{PAR}}$ is LOW, this output is used as Bit 10 of the Parallel Port Data Output Bus. When $\text{SER}/\overline{\text{PAR}}$ is HIGH, this output, part of the Serial Port, is used as a digital output frame synchronization for use with the internal data clock ($\text{EXT}/\overline{\text{INT}}$ = Logic LOW). When a read sequence is initiated and INVSCLK is LOW, SYNC is driven HIGH and remains HIGH while SDOUT output is valid. When a read sequence is initiated and INVSCLK is HIGH, SYNC is driven LOW and remains LOW while SDOUT output is valid.
24	D[11] or RDERROR	DO	When $\text{SER}/\overline{\text{PAR}}$ is LOW, this output is used as Bit 11 of the Parallel Port Data Output Bus. When $\text{SER}/\overline{\text{PAR}}$ is HIGH and $\text{EXT}/\overline{\text{INT}}$ is HIGH, this output, part of the Serial Port, is used as an incomplete read error flag. In Slave Mode, when a data read is started and not complete when the following conversion is complete, the current data is lost and RDERROR is pulsed HIGH.
25–28	D[12:15]	DO	Bit 12 to Bit 15 of the Parallel Port Data Output Bus. When $\text{SER}/\overline{\text{PAR}}$ is HIGH, these outputs are in high impedance.
29	BUSY	DO	Busy Output. Transitions HIGH when a conversion is started and remains HIGH until the conversion is complete and the data is latched into the on-chip shift register. The falling edge of BUSY could be used as a data-ready clock signal.
30	DGND	P	Must Be Tied to Digital Ground.
31	$\overline{\text{RD}}$	DI	Read Data. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both LOW, the Interface Parallel or Serial Output Bus is enabled.
32	$\overline{\text{CS}}$	DI	Chip Select. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both LOW, the Interface Parallel or Serial Output Bus is enabled. $\overline{\text{CS}}$ is also used to gate the external serial clock.
33	RESET	DI	Reset Input. When set to a logic HIGH, reset the AD7671. Current conversion, if any, is aborted. If not used, this pin could be tied to DGND.
34	PD	DI	Power-Down Input. When set to a logic HIGH, power consumption is reduced and conversions are inhibited after the current one is completed.
35	$\overline{\text{CNVST}}$	DI	Start Conversion. A falling edge on $\overline{\text{CNVST}}$ puts the internal sample-and-hold into the hold state and initiates a conversion. In Impulse Mode (IMPULSE HIGH and WARP LOW), if $\overline{\text{CNVST}}$ is held LOW when the acquisition phase (t_{a}) is complete, the internal sample-and-hold is put into the hold state and a conversion is immediately started.
36	AGND	P	Must Be Tied to Analog Ground.
37	REF	AI	Reference Input Voltage.
38	REFGND	AI	Reference Input Analog Ground.
39	INGND	P	Analog Input Ground.
40, 41, 42, 43	INA, INB, INC, IND	AI	Analog Inputs. Refer to Table I for input range configuration.

NOTES

AI = Analog Input

DI = Digital Input

DI/O = Bidirectional Digital

DO = Digital Output

P = Power

Paddle connected to AGND for the LFCSP (CP-48-1). This connection is not required to meet the electrical performances.

DEFINITION OF SPECIFICATIONS

Integral Nonlinearity Error (INL)

Linearity error refers to the deviation of each individual code from a line drawn from “negative full scale” through “positive full scale.” The point used as negative full scale occurs 1/2 LSB before the first code transition. Positive full scale is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity Error (DNL)

In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Full-Scale Error

The last transition (from 011 . . . 10 to 011 . . . 11 in twos complement coding) should occur for an analog voltage 1 1/2 LSB below the nominal full scale (2.499886 V for the ± 2.5 V range). The full-scale error is the deviation of the actual level of the last transition from the ideal level.

Bipolar Zero Error

The difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

Unipolar Zero Error

In Unipolar Mode, the first transition should occur at a level 1/2 LSB above analog ground. The unipolar zero error is the deviation of the actual transition from that point.

Spurious-Free Dynamic Range (SFDR)

The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)

A measurement of the resolution with a sine wave input. It is related to $S/(N+D)$ by the following formula:

$$ENOB = (S/[N + D]_{dB} - 1.76)/6.02$$

and is expressed in bits.

Total Harmonic Distortion (THD)

The rms sum of the first five harmonic components to the rms value of a full-scale input signal, expressed in decibels.

Signal-to-Noise Ratio (SNR)

The ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (S/[N+D])

The ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for $S/(N+D)$ is expressed in decibels.

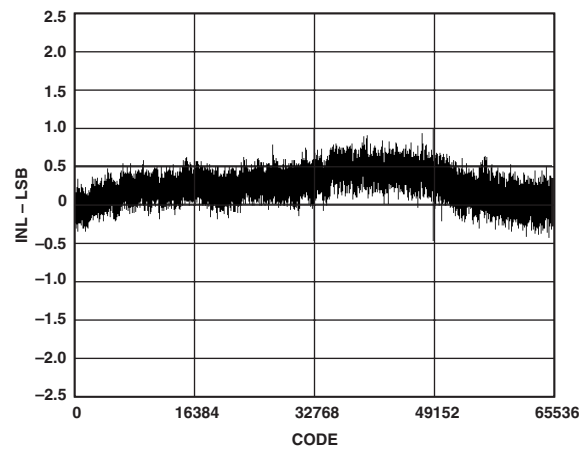
Aperture Delay

A measure of the acquisition performance measured from the falling edge of the $\overline{CNVST}$ input to when the input signal is held for a conversion.

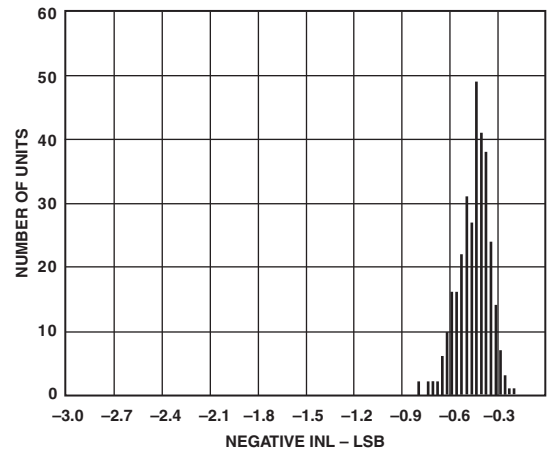
Transient Response

The time required for the AD7671 to achieve its rated accuracy after a full-scale step function is applied to its input.

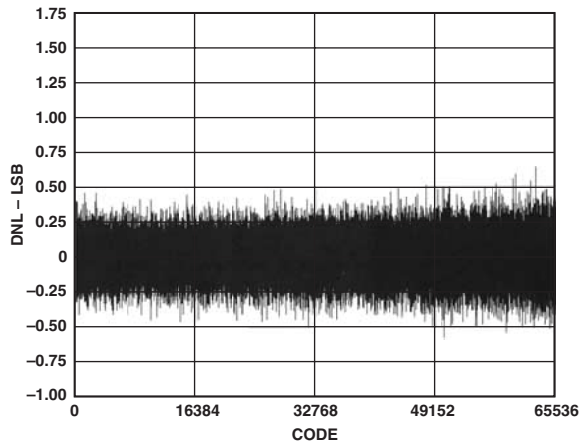
Typical Performance Characteristics—AD7671



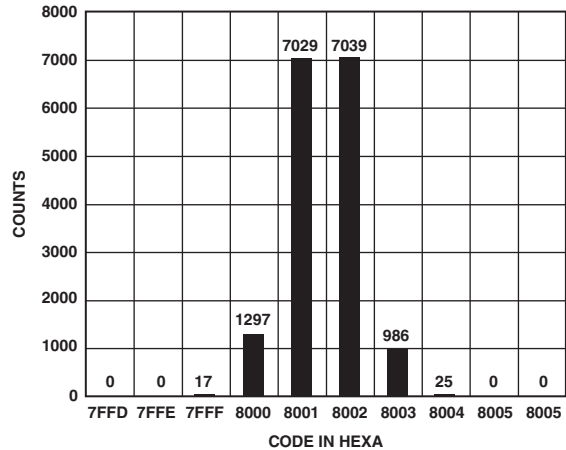
TPC 1. Integral Nonlinearity vs. Code



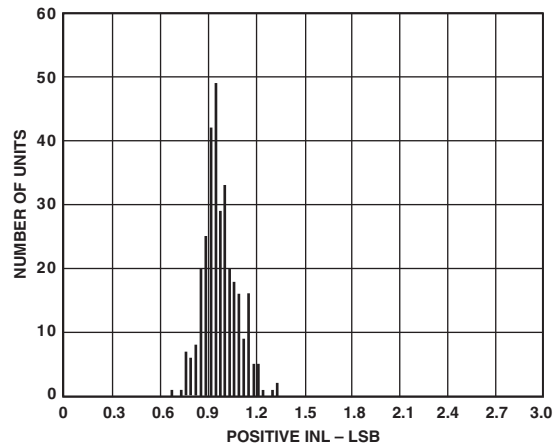
TPC 4. Typical Negative INL Distribution (314 Units)



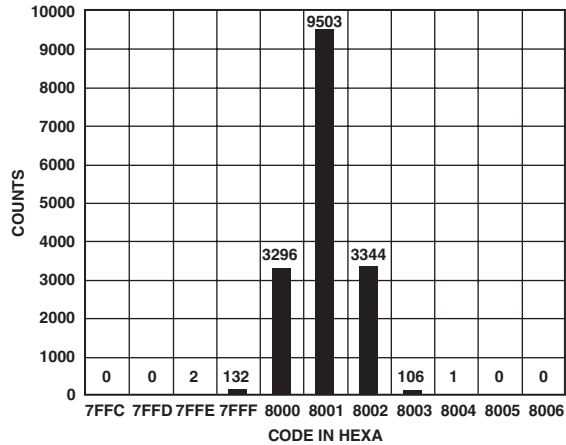
TPC 2. Differential Nonlinearity vs. Code



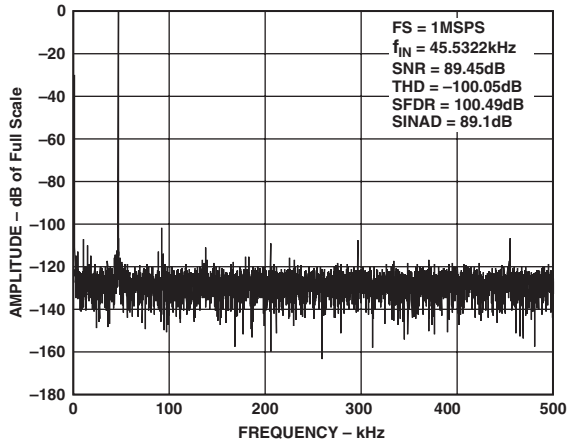
TPC 5. Histogram of 16,384 Conversions of a DC Input at the Code Transition



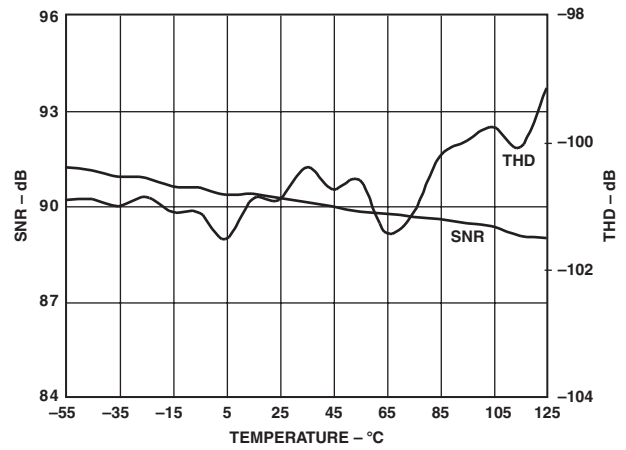
TPC 3. Typical Positive INL Distribution (314 Units)



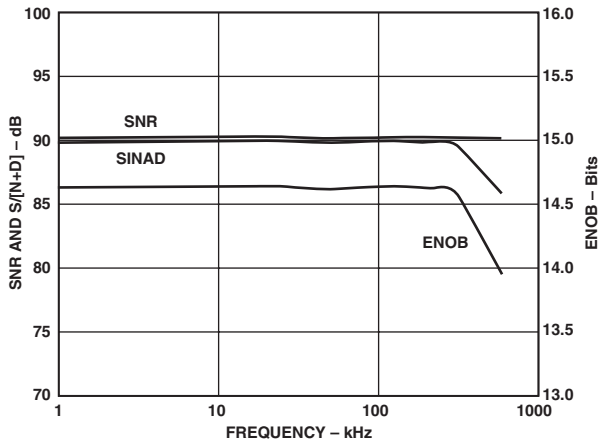
TPC 6. Histogram of 16,384 Conversions of a DC Input at the Code Center



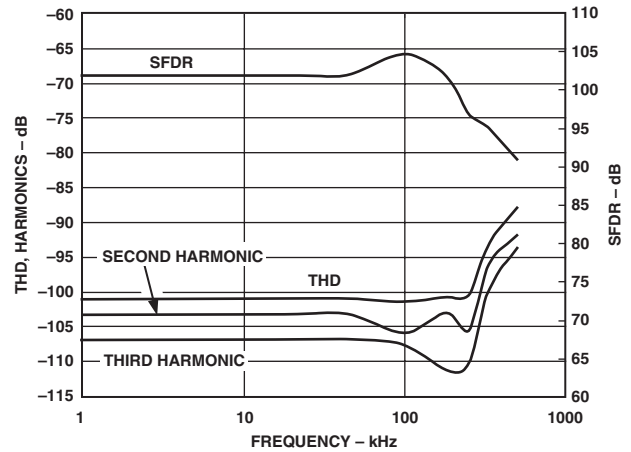
TPC 7. FFT Plot



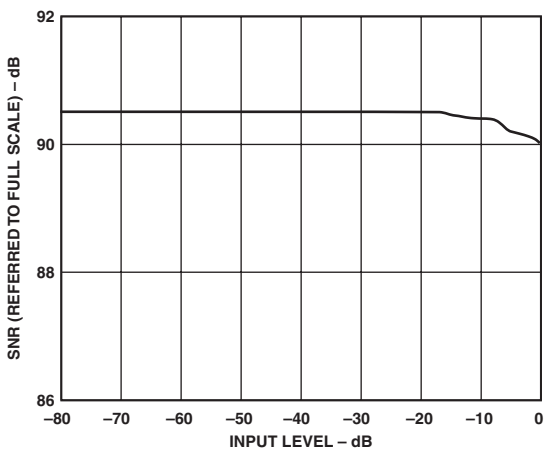
TPC 10. SNR, THD vs. Temperature



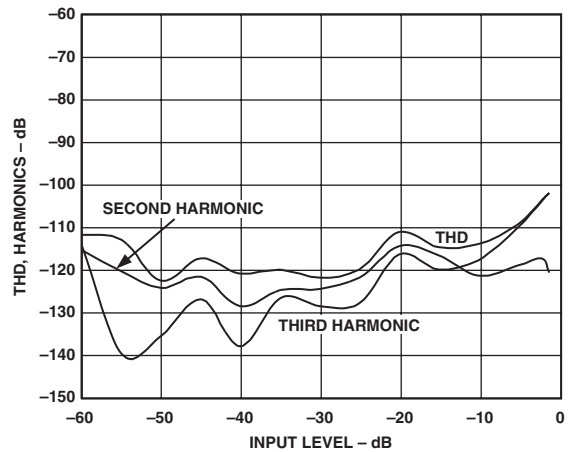
TPC 8. SNR, $S/(N + D)$, and ENOB vs. Frequency



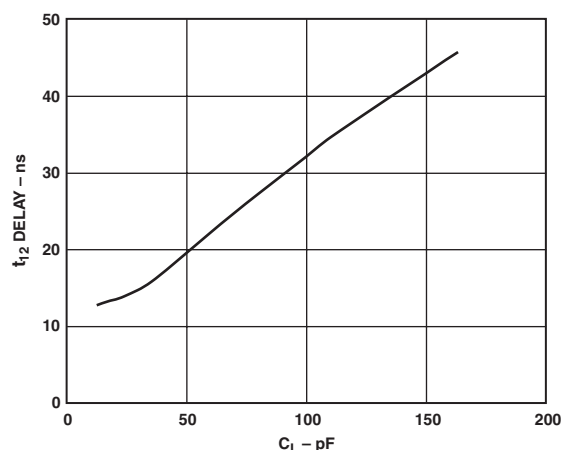
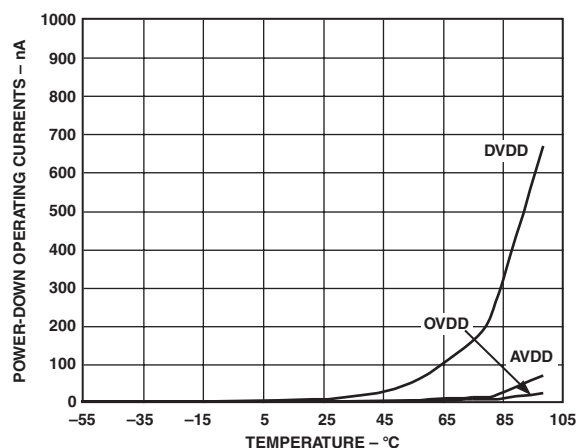
TPC 11. THD, Harmonics, and SFDR vs. Frequency



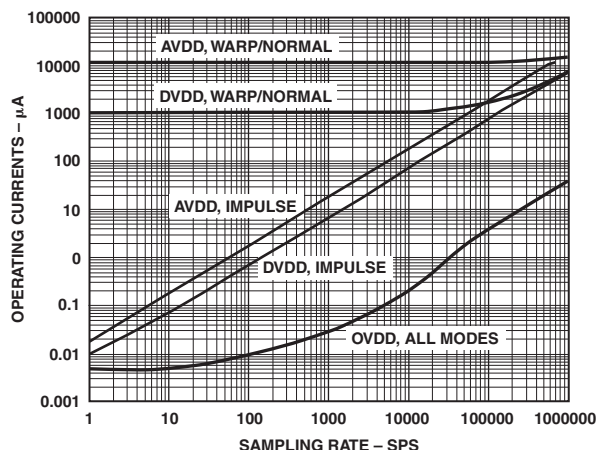
TPC 9. SNR vs. Input Level



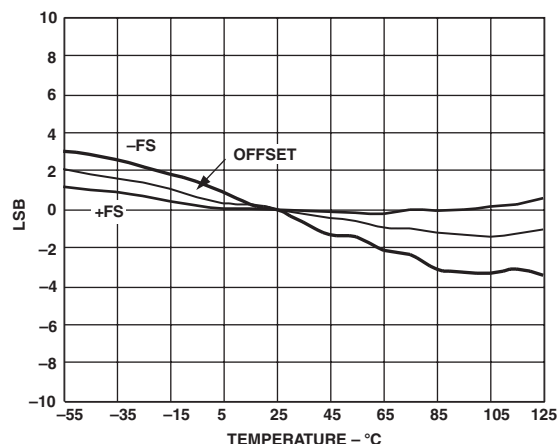
TPC 12. THD, Harmonics vs. Input Level

TPC 13. Typical Delay vs. Load Capacitance C_L 

TPC 15. Power-Down Operating Currents vs. Temperature



TPC 14. Operating Currents vs. Sample Rate



TPC 16. +FS, Offset, and -FS vs. Temperature

CIRCUIT INFORMATION

The AD7671 is a fast, low power, single-supply, precise 16-bit analog-to-digital converter (ADC). The AD7671 features different modes to optimize performances according to the applications.

In Warp Mode, the AD7671 is capable of converting 1,000,000 samples per second (1 MSPS).

The AD7671 provides the user with an on-chip track-and-hold, successive approximation ADC that does not exhibit any pipeline or latency, making it ideal for multiple multiplexed channel applications.

It is specified to operate with both bipolar and unipolar input ranges by changing the connection of its input resistive scaler.

The AD7671 can be operated from a single 5 V supply and be interfaced to either 5 V or 3 V digital logic. It is housed in a 48-lead LQFP package or a 48-lead LFCSP package that combines space savings and flexible configurations as either serial or parallel interface. The AD7671 is a pin-to-pin compatible upgrade of the AD7665 and AD7664.

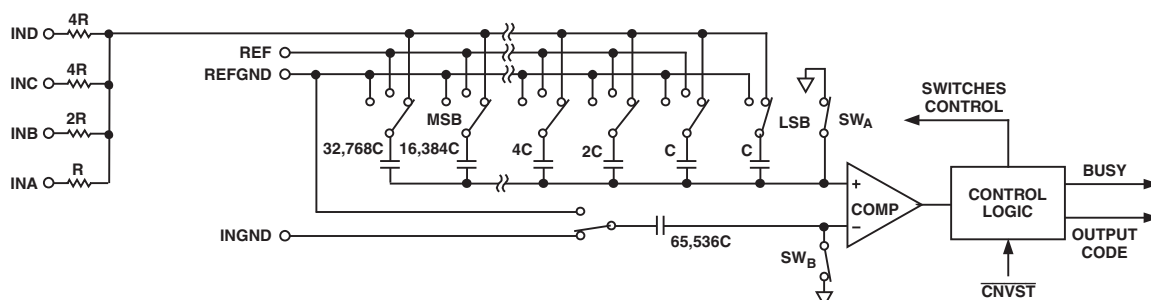


Figure 3. ADC Simplified Schematic

CONVERTER OPERATION

The AD7671 is a successive approximation analog-to-digital converter based on a charge redistribution DAC. Figure 3 shows the simplified schematic of the ADC. The input analog signal is first scaled down and level shifted by the internal input resistive scaler, which allows both unipolar ranges (0 V to 2.5 V, 0 V to 5 V, and 0 V to 10 V) and bipolar ranges (± 2.5 V, ± 5 V, and ± 10 V). The output voltage range of the resistive scaler is always 0 V to 2.5 V. The capacitive DAC consists of an array of 16 binary weighted capacitors and an additional “LSB” capacitor. The comparator’s negative input is connected to a “dummy” capacitor of the same value as the capacitive DAC array.

During the acquisition phase, the common terminal of the array tied to the comparator’s positive input is connected to AGND via SW_A . All independent switches are connected to the output of the resistive scaler. Thus, the capacitor array is used as a sampling capacitor and acquires the analog signal. Similarly, the dummy capacitor acquires the analog signal on INGND input.

When the acquisition phase is complete and the $\overline{CNVST}$ input goes or is LOW, a conversion phase is initiated. When the conversion phase begins, SW_A and SW_B are opened first. The capacitor array and the dummy capacitor are then disconnected from the inputs and connected to the REFGND input. Therefore, the differential voltage between the output of the resistive scaler and INGND captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced.

By switching each element of the capacitor array between REFGND or REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$. . . $V_{REF}/65,536$). The control logic toggles these switches, starting with the MSB first, in order to bring the comparator back into a balanced condition. After the completion of this process, the control logic generates the ADC output code and brings BUSY output LOW.

Modes of Operation

The AD7671 features three modes of operation, Warp, Normal, and Impulse. Each of these modes is more suitable for specific applications.

The Warp Mode allows the fastest conversion rate up to 1 MSPS. However, in this mode, and this mode only, the full specified accuracy is guaranteed only when the time between conversion does not exceed 1 ms. If the time between two consecutive conversions is longer than 1 ms, for instance, after power-up, the first conversion result should be ignored. This mode makes the AD7671 ideal for applications where both high accuracy and fast sample rate are required.

The Normal Mode is the fastest mode (800 kSPS) without any limitation about the time between conversions. This mode makes the AD7671 ideal for asynchronous applications such as data acquisition systems, where both high accuracy and fast sample rate are required.

The Impulse Mode, the lowest power dissipation mode, allows power saving between conversions. The maximum throughput in this mode is 666 kSPS. When operating at 100 SPS, for example, it typically consumes only 15 μ W. This feature makes the AD7671 ideal for battery-powered applications.

Transfer Functions

Using the $OB/2\overline{C}$ digital input, the AD7671 offers two output codings: straight binary and twos complement. The ideal transfer characteristic for the AD7671 is shown in Figure 4 and Table III.

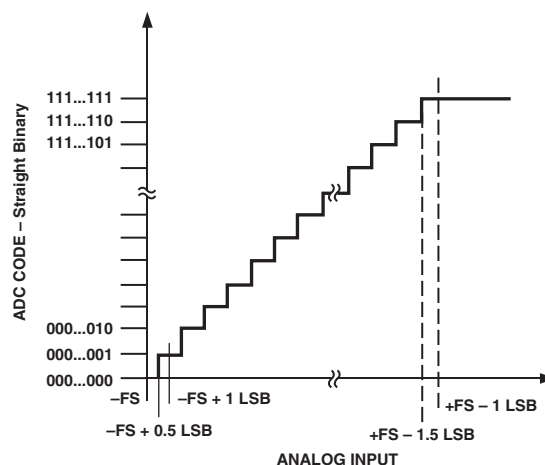


Figure 4. ADC Ideal Transfer Function

Table III. Output Codes and Ideal Input Voltages

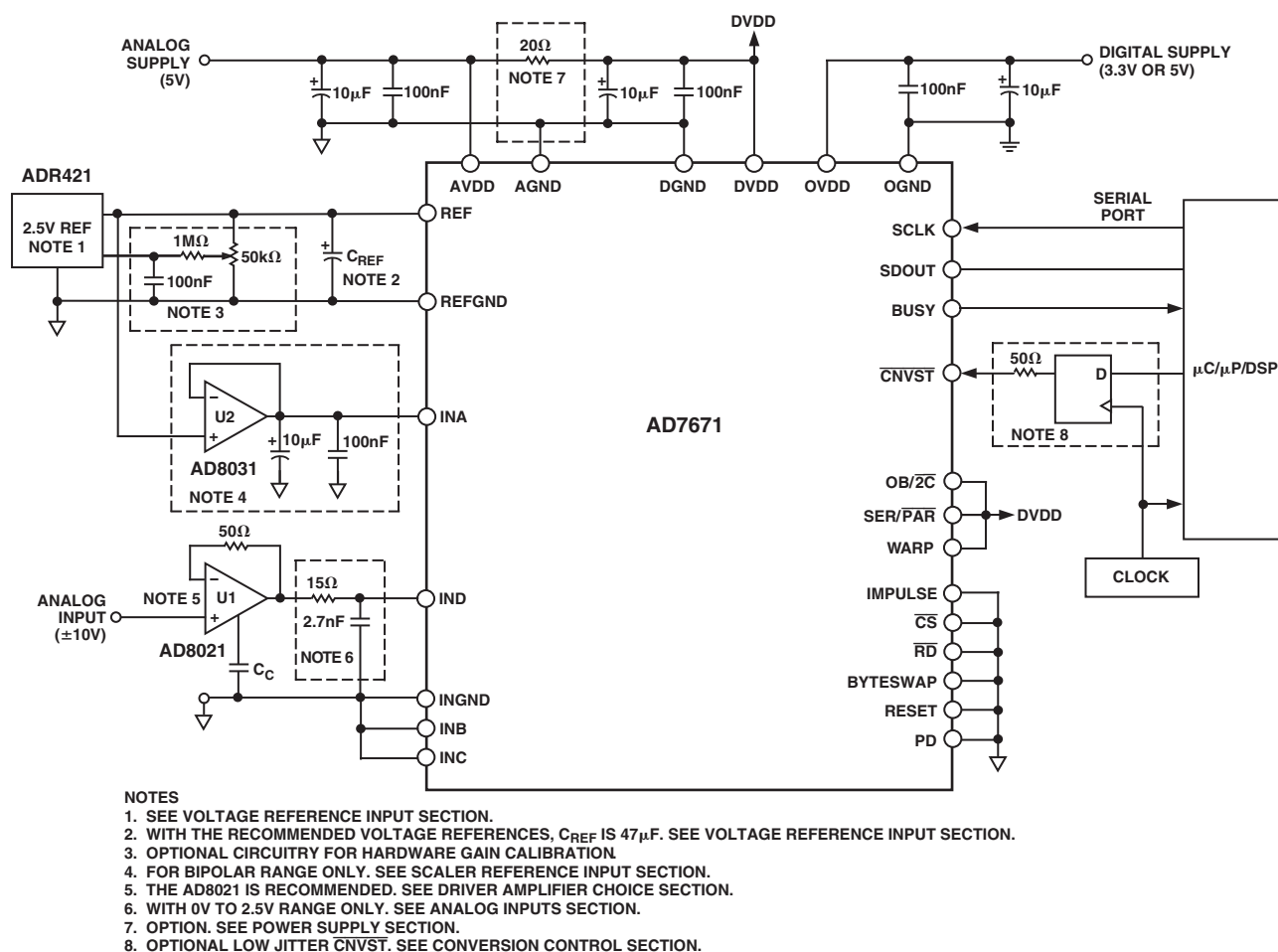
Description	Analog Input						Digital Output Code (Hexa)	
							Straight Binary	Twos Complement
Full-Scale Range ¹	±10 V	±5 V	±2.5 V	0 V to 10 V	0 V to 5 V	0 V to 2.5 V		
Least Significant Bit	305.2 μ V	152.6 μ V	76.3 μ V	152.6 μ V	76.3 μ V	38.15 μ V		
FSR – 1 LSB	9.999695 V	4.999847 V	2.499924 V	9.999847 V	4.999924 V	2.499962 V	FFFF ²	7FFF ²
Midscale + 1 LSB	305.2 μ V	152.6 μ V	76.3 μ V	5.000153 V	2.570076 V	1.257038 V	8001	0001
Midscale	0 V	0 V	0 V	5 V	2.5 V	1.25 V	8000	0000
Midscale – 1 LSB	–305.2 μ V	–152.6 μ V	–76.3 μ V	4.999847 V	2.499924 V	1.249962 V	7FFF	FFFF
–FSR + 1 LSB	–9.999695 V	–4.999847 V	–2.499924 V	152.6 μ V	76.3 μ V	38.15 μ V	0001	8001
–FSR	–10 V	–5 V	–2.5 V	0 V	0 V	0 V	0000 ³	8000 ³

NOTES

¹Values with REF = 2.5 V. With REF = 3 V, all values will scale linearly.²This is also the code for an overrange analog input.³This is also the code for an underrange analog input.

TYPICAL CONNECTION DIAGRAM

Figure 5 shows a typical connection diagram for the AD7671. Different circuitry shown on this diagram is optional and is discussed below.

Figure 5. Typical Connection Diagram (± 10 V Range Shown)

AD7671

Analog Inputs

The AD7671 is specified to operate with six full-scale analog input ranges. Connections required for each of the four analog inputs, IND, INC, INB, and INA, and the resulting full-scale ranges are shown in Table I. The typical input impedance for each analog input range is also shown.

Figure 6 shows a simplified analog input section of the AD7671.

The four resistors connected to the four analog inputs form a resistive scaler that scales down and shifts the analog input range to a common input range of 0 V to 2.5 V at the input of the switched capacitive ADC.

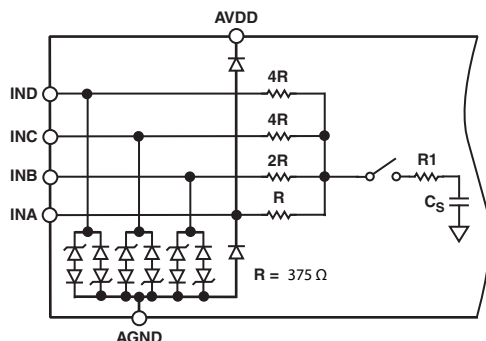


Figure 6. Simplified Analog Input

By connecting the four inputs INA, INB, INC, and IND to the input signal itself, the ground, or a 2.5 V reference, other analog input ranges can be obtained.

The diodes shown in Figure 6 provide ESD protection for the four analog inputs. The inputs INB, INC, and IND have a high voltage protection (–11 V to +30 V) to allow a wide input voltage range. Care must be taken to ensure that the analog input signal never exceeds the absolute ratings on these inputs, including INA (0 V to 5 V). This will cause these diodes to become forward-biased and start conducting current. These diodes can handle a forward-biased current of 120 mA maximum. For instance, when using the 0 V to 2.5 V input range, these conditions could eventually occur on the input INA when the input buffer's (U1) supplies are different from AVDD. In such cases, an input buffer with a short-circuit current limitation can be used to protect the part.

This analog input structure allows the sampling of the differential signal between the output of the resistive scaler and INGND. Unlike other converters, the INGND input is sampled at the same time as the inputs. By using this differential input, small signals common to both inputs are rejected as shown in Figure 7, which represents the typical CMRR over frequency. For instance, by using INGND to sense a remote signal ground, the difference of ground potentials between the sensor and the local ADC ground is eliminated. During the acquisition phase for ac signals, the AD7671 behaves like a one-pole RC filter consisting of the equivalent resistance of the resistive scaler $R/2$ in series with $R1$ and Cs . The resistor $R1$ is typically 100 Ω and is a lumped component made up of some serial resistors and the on resistance of the switches.

The capacitor Cs is typically 60 pF and is mainly the ADC sampling capacitor. This one-pole filter with a typical –3 dB cutoff frequency of 9.6 MHz reduces undesirable aliasing effects and limits the noise coming from the inputs.

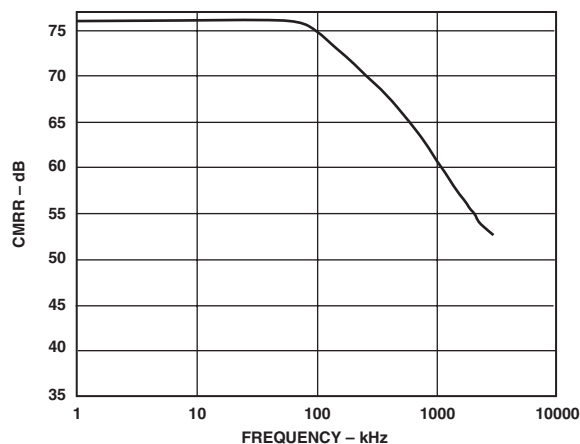


Figure 7. Analog Input CMRR vs. Frequency

Except when using the 0 V to 2.5 V analog input voltage range, the AD7671 has to be driven by a very low impedance source to avoid gain errors. That can be done by using a driver amplifier whose choice is eased by the primarily resistive analog input circuitry of the AD7671.

When using the 0 V to 2.5 V analog input voltage range, the input impedance of the AD7671 is very high so the AD7671 can be driven directly by a low impedance source without gain error. That allows, as shown in Figure 5, putting an external one-pole RC filter between the output of the amplifier output and the ADC analog inputs to even further improve the noise filtering done by the AD7671 analog input circuit. However, the source impedance has to be kept low because it affects the ac performances, especially the total harmonic distortion (THD). The maximum source impedance depends on the amount of total THD that can be tolerated. The THD degradation is a function of the source impedance and the maximum input frequency as shown in Figure 8.

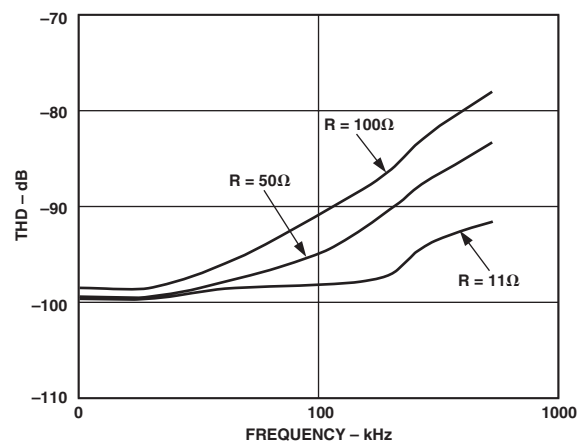


Figure 8. THD vs. Analog Input Frequency and Input Resistance (0 V to 2.5 V Only)

Driver Amplifier Choice

Although the AD7671 is easy to drive, the driver amplifier needs to meet at least the following requirements:

- The driver amplifier and the AD7671 analog input circuit must be able, together, to settle for a full-scale step the capacitor array at a 16-bit level (0.0015%). In the amplifier's data sheet, the settling at 0.1% to 0.01% is more commonly specified. It could significantly differ from the settling time at 16-bit level and it should therefore be verified prior to the driver selection. The tiny op amp AD8021, which combines ultralow noise and a high gain bandwidth, meets this settling time requirement even when used with a high gain up to 13.
- The noise generated by the driver amplifier needs to be kept as low as possible in order to preserve the SNR and transition noise performance of the AD7671. The noise coming from the driver is first scaled down by the resistive scaler according to the analog input voltage range used and is then filtered by the AD7671 analog input circuit one-pole, low-pass filter made by $(R/2 + R1)$ and C_S . The SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20 \text{ LOG} \left(\frac{28}{\sqrt{784 + \frac{\pi}{2} f_{-3dB} \left(\frac{2.5 N e_N}{FSR} \right)^2}} \right)$$

where:

f_{-3dB} is the -3 dB input bandwidth in MHz of the AD7671 (9.6 MHz) or the cutoff frequency of the input filter if any used (0 V to 2.5 V range).

N is the noise factor of the amplifier (1 if in buffer configuration).

e_N is the equivalent input noise voltage of the op amp in $nV/\sqrt{Hz}$.

FSR is the full-scale span (i.e., 5 V for ± 2.5 V range).

For instance, when using the 0 V to 5 V range, a driver like the AD8021, with an equivalent input noise of $2 nV/\sqrt{Hz}$ and configured as a buffer, thus with a noise gain of 1, the SNR degrades by only 0.08 dB.

- The driver needs to have a THD performance suitable to that of the AD7671. TPC 11 gives the THD versus frequency that the driver should preferably exceed.

The AD8021 meets these requirements and is usually appropriate for almost all applications. The AD8021 needs an external compensation capacitor of 10 pF. This capacitor should have good linearity as an NPO ceramic or mica type.

The AD8022 could also be used where a dual version is needed and a gain of 1 is used.

The AD829 is another alternative where high frequency (above 100 kHz) performance is not required. In a gain of 1, it requires an 82 pF compensation capacitor.

The AD8610 is another option where low bias current is needed in low frequency applications.

Voltage Reference Input

The AD7671 uses an external 2.5 V voltage reference.

The voltage reference input REF of the AD7671 has a dynamic input impedance; it should therefore be driven by a low impedance source with an efficient decoupling between REF and REFGND inputs. This decoupling depends on the choice of the voltage reference but usually consists of a 1 μF ceramic capacitor and a low ESR tantalum capacitor connected to the REF and REFGND inputs with minimum parasitic inductance. 47 μF is an appropriate value for the tantalum capacitor when used with one of the recommended reference voltages:

- The low noise, low temperature drift ADR421 and AD780 voltage references
- The low power ADR291 voltage reference
- The low cost AD1582 voltage reference

For applications using multiple AD7671s, it is more effective to buffer the reference voltage with a low noise, very stable op amp like the AD8031.

Care should also be taken with the reference temperature coefficient of the voltage reference that directly affects the full-scale accuracy if this parameter matters. For instance, a ± 15 ppm/ $^{\circ}C$ temperature coefficient of the reference changes the full scale by ± 1 LSB/ $^{\circ}C$.

Note that V_{REF} , as mentioned in the Specifications table, could be increased to $AVDD - 1.85$ V. The benefit here is the increased SNR obtained as a result of this increase. Since the input range is defined in terms of V_{REF} , this would essentially increase the $\pm REF$ range from ± 2.5 V to ± 3 V and so on with an $AVDD$ above 4.85 V. The theoretical improvement as a result of this increase in reference is 1.58 dB ($20 \log [3/2.5]$). Due to the theoretical quantization noise, however, the observed improvement is approximately 1 dB. The AD780 can be selected with a 3 V reference voltage.

Scaler Reference Input (Bipolar Input Ranges)

When using the AD7671 with bipolar input ranges, the connection diagram in Figure 5 shows a reference buffer amplifier. This buffer amplifier is required to isolate the REF pin from the signal dependent current in the IN_x pin. A high speed op amp, such as the AD8031, can be used with a single 5 V power supply without degrading the performance of the AD7671. The buffer must have good settling characteristics and provide low total noise within the input bandwidth of the AD7671.

Power Supply

The AD7671 uses three sets of power supply pins: an analog 5 V supply $AVDD$, a digital 5 V core supply $DVDD$, and a digital input/output interface supply $OVDD$. The $OVDD$ supply allows direct interface with any logic working between 2.7 V and $DVDD + 0.3$ V. To reduce the number of supplies needed, the digital core ($DVDD$) can be supplied through a simple RC filter from the analog supply as shown in Figure 5. The AD7671 is independent of power supply sequencing, once $OVDD$ does not exceed $DVDD$ by more than 0.3 V, and thus free from supply voltage induced latch-up. Additionally, it is very insensitive to power supply variations over a wide frequency range as shown in Figure 9.

AD7671

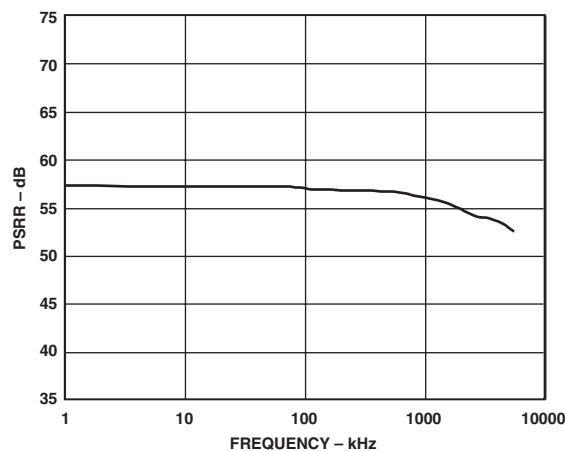


Figure 9. PSRR vs. Frequency

POWER DISSIPATION

In Impulse Mode, the AD7671 automatically reduces its power consumption at the end of each conversion phase. During the acquisition phase, the operating currents are very low, which allows a significant power savings when the conversion rate is reduced, as shown in Figure 10. This feature makes the AD7671 ideal for very low power battery applications.

This does not take into account the power, if any, dissipated by the input resistive scaler, which depends on the input voltage range used and the analog input voltage even in Power-Down Mode. There is no power dissipated when the 0 V to 2.5 V is used or when both the analog input voltage is 0 V and a unipolar range, 0 V to 5 V or 0 V to 10 V, is used.

It should be noted that the digital interface remains active even during the acquisition phase. To reduce the operating digital supply currents even further, the digital inputs need to be driven close to the power rails (i.e., DVDD and DGND) and OVDD should not exceed DVDD by more than 0.3 V.

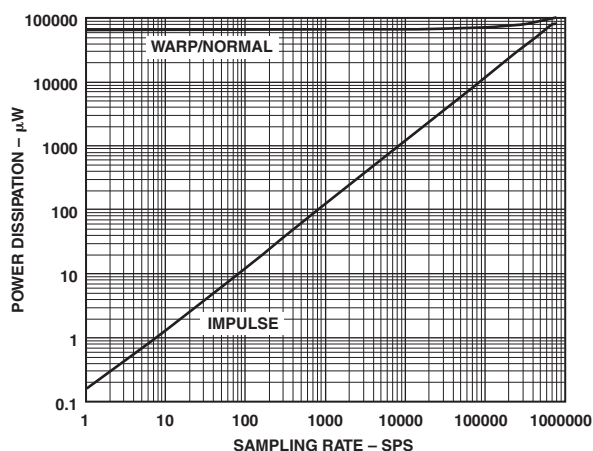


Figure 10. Power Dissipation vs. Sample Rate

CONVERSION CONTROL

Figure 11 shows the detailed timing diagrams of the conversion process. The AD7671 is controlled by the signal $\overline{\text{CNVST}}$, which initiates conversion. Once initiated, it cannot be restarted or aborted, even by the power-down input PD, until the conversion is complete. The $\overline{\text{CNVST}}$ signal operates independently of CS and RD signals.

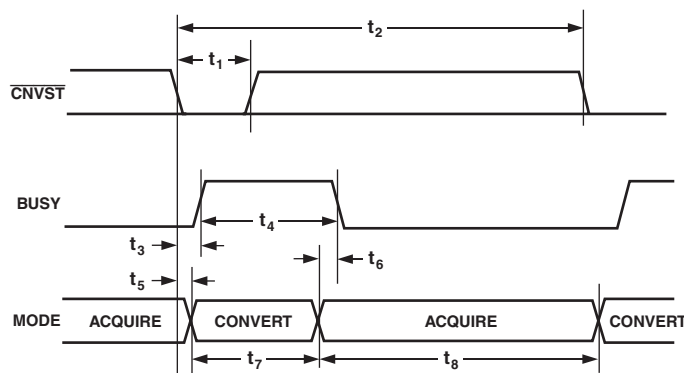


Figure 11. Basic Conversion Timing

In Impulse Mode, conversions can be automatically initiated. If $\overline{\text{CNVST}}$ is held LOW when BUSY is LOW, the AD7671 controls the acquisition phase and then automatically initiates a new conversion. By keeping $\overline{\text{CNVST}}$ LOW, the AD7671 keeps the conversion process running by itself. It should be noted that the analog input has to be settled when BUSY goes LOW. Also, at power-up, $\overline{\text{CNVST}}$ should be brought LOW once to initiate the conversion process. In this mode, the AD7671 could sometimes run slightly faster than the guaranteed limits in the Impulse Mode of 666 kSPS. This feature does not exist in Warp or Normal Modes.

Although $\overline{\text{CNVST}}$ is a digital signal, it should be designed with special care with fast, clean edges, and levels with minimum overshoot and undershoot or ringing. It is a good thing to shield the $\overline{\text{CNVST}}$ trace with ground and also to add a low value serial resistor (i.e., 50 Ω) termination close to the output of the component that drives this line.

For applications where the SNR is critical, the $\overline{\text{CNVST}}$ signal should have a very low jitter. To achieve this, some use a dedicated oscillator for $\overline{\text{CNVST}}$ generation, or at least to clock it with a high frequency low jitter clock as shown in Figure 5.

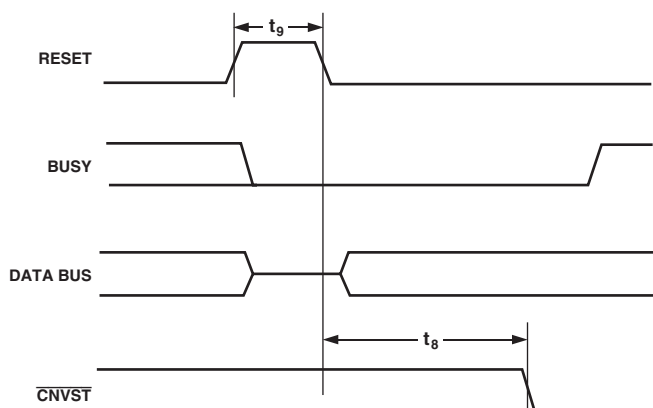


Figure 12. RESET Timing

DIGITAL INTERFACE

The AD7671 has a versatile digital interface; it can be interfaced with the host system by using either a serial or parallel interface. The serial interface is multiplexed on the parallel data bus. The AD7671 digital interface also accommodates both 3 V or 5 V logic by simply connecting the OVDD supply pin of the AD7671 to the host system interface digital supply. Finally, by using the OB/2C input pin, straight binary and twos complement coding can be used.

The two signals $\overline{CS}$ and $\overline{RD}$ control the interface. When at least one of these signals is HIGH, the interface outputs are in high impedance. Usually, $\overline{CS}$ allows the selection of each AD7671 in multicircuit applications and is held LOW in a single AD7671 design. $\overline{RD}$ is generally used to enable the conversion result on the data bus.

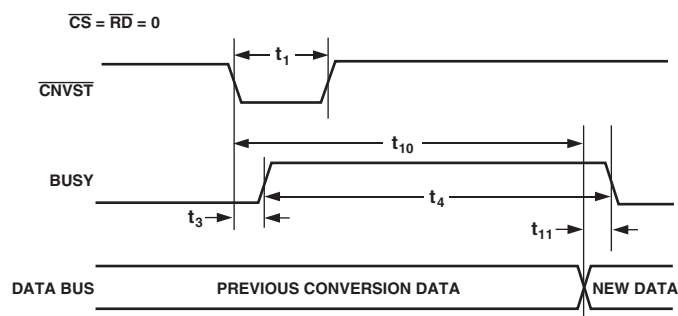


Figure 13. Master Parallel Data Timing for Reading (Continuous Read)

PARALLEL INTERFACE

The AD7671 is configured to use the parallel interface when the $\overline{SER}/\overline{PAR}$ is held LOW. The data can be read either after each conversion, which is during the next acquisition phase, or during the following conversion as shown, respectively, in Figures 14 and 15. When the data is read during the conversion, however, it is recommended that it be read-only during the first half of the conversion phase. That avoids any potential feedthrough between voltage transients on the digital interface and the most critical analog conversion circuitry.

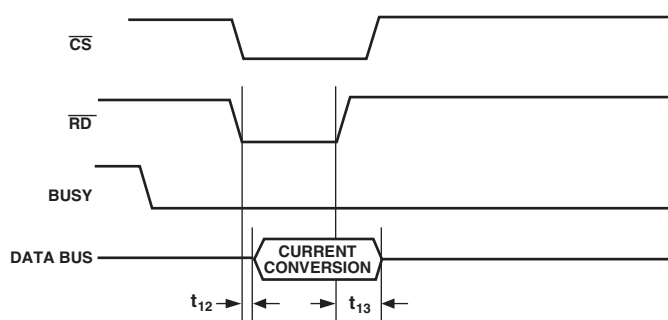


Figure 14. Slave Parallel Data Timing for Reading (Read after Convert)

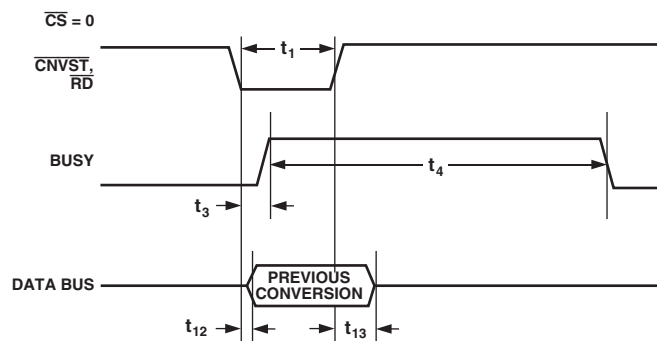


Figure 15. Slave Parallel Data Timing for Reading (Read during Convert)

The BYTESWAP pin allows a glueless interface to an 8-bit bus. As shown in Figure 16, the LSB is output on D[7:0] and the MSB is output on D[15:8] when BYTESWAP is LOW. When BYTESWAP is HIGH, the LSB and MSB bytes are swapped and the LSB is output on D[15:8] and the MSB is output on D[7:0]. By connecting BYTESWAP to an address line, the 16 data bits can be read in two bytes on either D[15:8] or D[7:0].

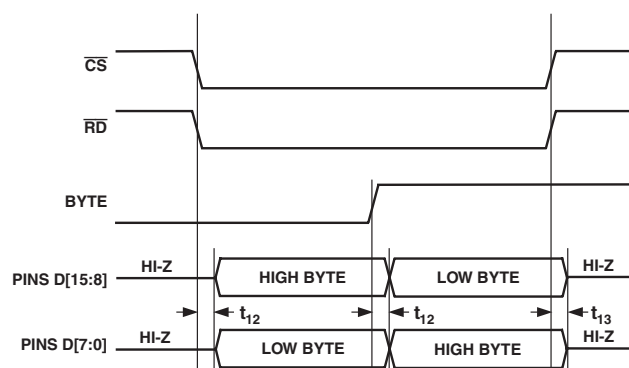


Figure 16. 8-Bit Parallel Interface

SERIAL INTERFACE

The AD7671 is configured to use the serial interface when the $\overline{SER}/\overline{PAR}$ is held HIGH. The AD7671 outputs 16 bits of data, MSB first, on the SDOUT pin. This data is synchronized with the 16 clock pulses provided on the SCLK pin. The output data is valid on both the rising and falling edge of the data clock.

SLAVE SERIAL INTERFACE

External Clock

The AD7671 is configured to accept an externally supplied serial data clock on the SCLK pin when the $\overline{EXT}/\overline{INT}$ pin is held HIGH. In this mode, several methods can be used to read the data. The external serial clock is gated by $\overline{CS}$ and the data are output when both $\overline{CS}$ and $\overline{RD}$ are LOW. Thus, depending on $\overline{CS}$, the data can be read after each conversion or during the following conversion. The external clock can be either a continuous or discontinuous clock. A discontinuous clock can be either normally HIGH or normally LOW when inactive. Figures 19 and 21 show the detailed timing diagrams of these methods.

AD7671

MASTER SERIAL INTERFACE

Internal Clock

The AD7671 is configured to generate and provide the serial data clock SCLK when the EXT/INT pin is held LOW. It also generates a SYNC signal to indicate to the host when the serial data is valid. The serial clock SCLK and the SYNC signal can be inverted if desired. Depending on RDC/SDIN input, the data can be read after each conversion or during conversion. Figures 17 and 18 show the detailed timing diagrams of these two modes.

Usually, because the AD7671 is used with a fast throughput, the mode master, read during conversion, is the most recommended Serial Mode when it can be used.

In Read-during-Conversion Mode, the serial clock and data toggle at appropriate instants, which minimizes potential feedthrough between digital activity and the critical conversion decisions.

In Read-after-Conversion Mode, it should be noted that unlike in other modes, the signal BUSY returns LOW after the 16 data bits are pulsed out and not at the end of the conversion phase, which results in a longer BUSY width.

While the AD7671 is performing a bit decision, it is important that voltage transients not occur on digital input/output pins or degradation of the conversion result could occur. This is particularly important during the second half of the conversion phase because

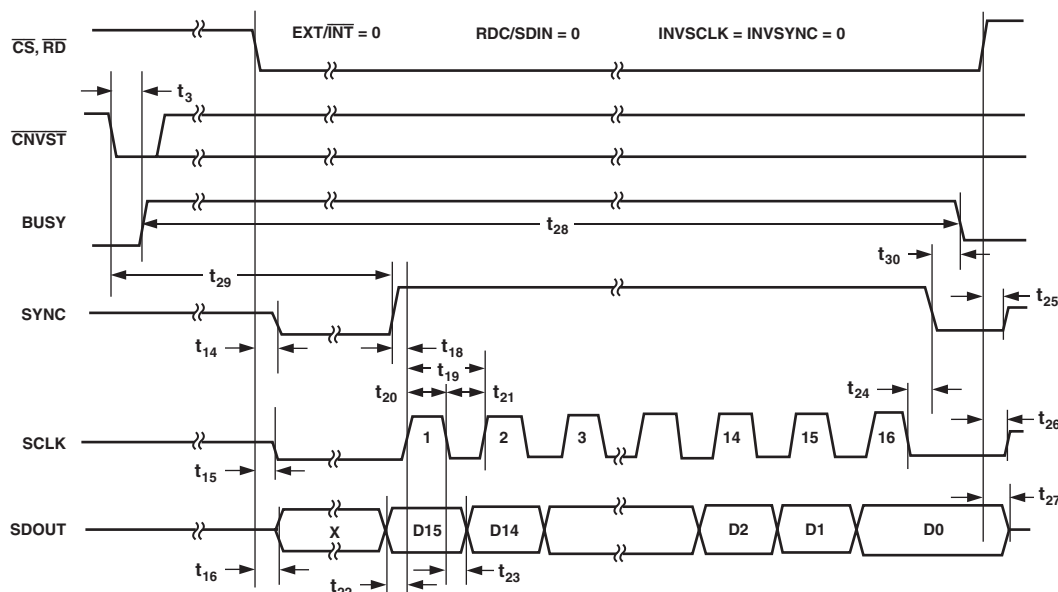


Figure 17. Master Serial Data Timing for Reading (Read after Convert)

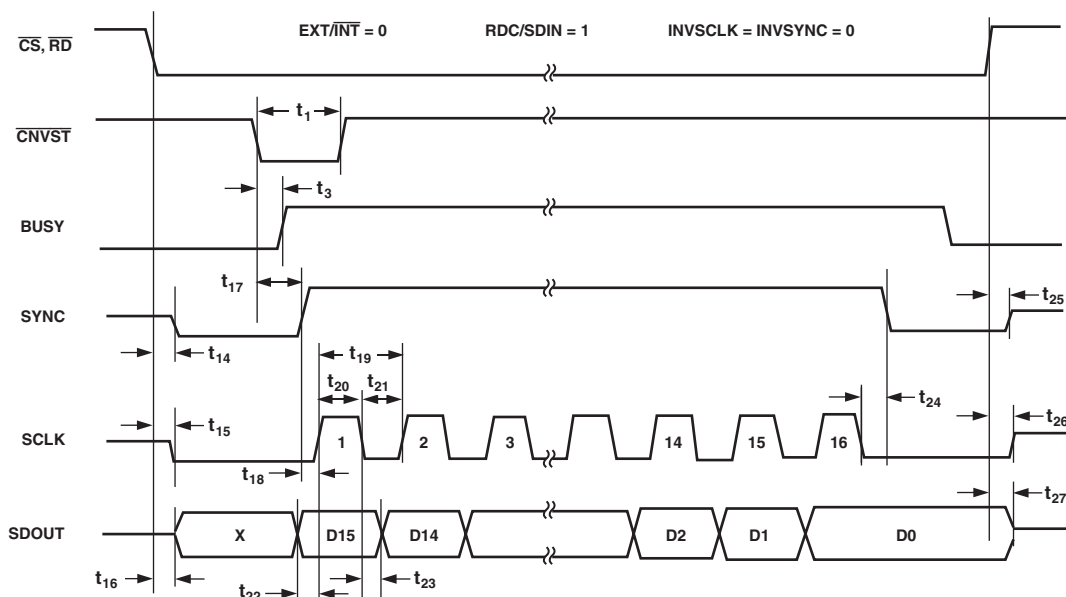


Figure 18. Master Serial Data Timing for Reading (Read Previous Conversion during Convert)

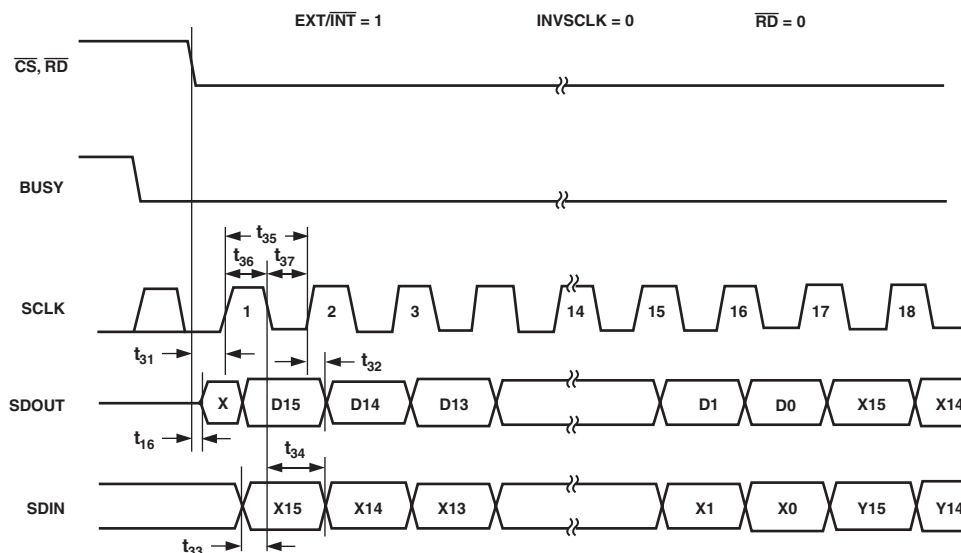


Figure 19. Slave Serial Data Timing for Reading (Read after Convert)

the AD7671 provides error correction circuitry that can correct for an improper bit decision made during the first half of the conversion phase. For this reason, it is recommended that when an external clock is being provided, it is a discontinuous clock that is toggling only when BUSY is LOW or, more importantly, that does not transition during the latter half of BUSY HIGH.

External Discontinuous Clock Data Read after Conversion

Though the maximum throughput cannot be achieved using this mode, it is the most recommended of the serial slave modes. Figure 19 shows the detailed timing diagrams of this method. After a conversion is complete, indicated by BUSY returning LOW, the result of this conversion can be read while both $\overline{CS}$ and $\overline{RD}$ are LOW. The data is shifted out, MSB first, with 16 clock pulses and is valid on both the rising and falling edge of the clock.

Among the advantages of this method, the conversion performance is not degraded because there are no voltage transients on the digital interface during the conversion process.

Another advantage is to be able to read the data at any speed up to 40 MHz, which accommodates both slow digital host interface and the fastest serial reading.

Finally, in this mode only, the AD7671 provides a “daisy-chain” feature using the RDC/SDIN input pin for cascading multiple converters together. This feature is useful for reducing component count and wiring connections when desired as, for instance, in isolated multiconverter applications.

An example of the concatenation of two devices is shown in Figure 20. Simultaneous sampling is possible by using a common $\overline{CNVST}$ signal. It should be noted that the RDC/SDIN input is latched on the opposite edge of SCLK of the one used to shift out the data on SDOUT. Therefore, the MSB of the “upstream” converter just follows the LSB of the “downstream” converter on the next SCLK cycle.

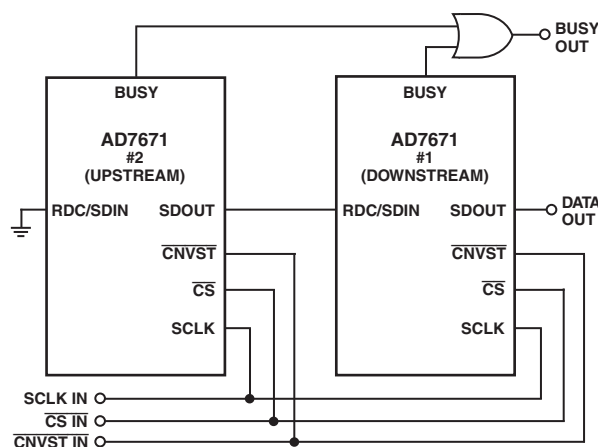


Figure 20. Two AD7671s in a Daisy-Chain Configuration

External Clock Data Read during Conversion

Figure 21 shows the detailed timing diagrams of this method. During a conversion, while both $\overline{CS}$ and $\overline{RD}$ are LOW, the result of the previous conversion can be read. The data is shifted out, MSB first, with 16 clock pulses and is valid on both the rising and the falling edge of the clock. The 16 bits have to be read before the current conversion is complete. If that is not done, RDERROR is pulsed HIGH and can be used to interrupt the host interface to prevent incomplete data reading. There is no daisy-chain feature in this mode, and RDC/SDIN input should always be tied either HIGH or LOW.

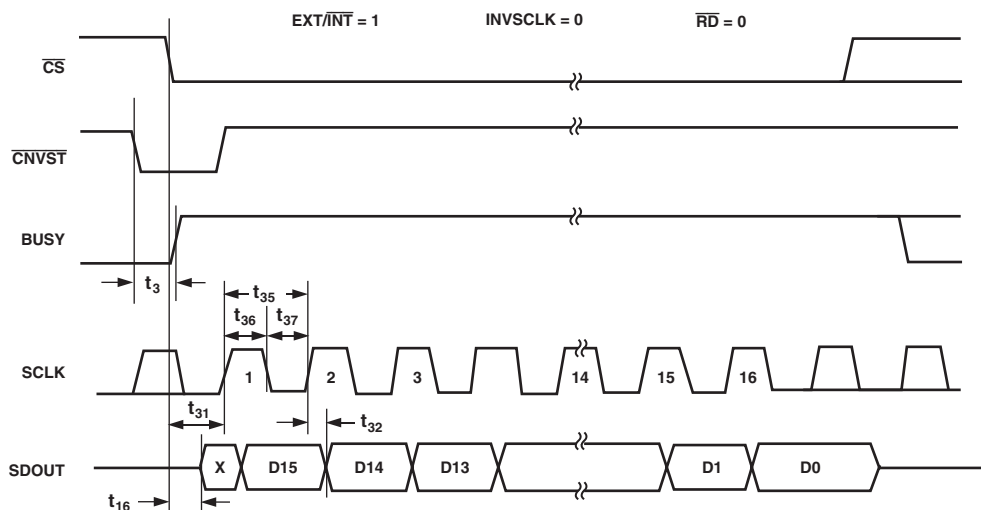


Figure 21. Slave Serial Data Timing for Reading (Read Previous Conversion during Convert)

To reduce performance degradation due to digital activity, a fast discontinuous clock of at least 25 MHz when Impulse Mode is used, 32 MHz when Normal or 40 MHz when Warp Mode is used, is recommended to ensure that all the bits are read during the first half of the conversion phase. It is also possible to begin to read the data after conversion and continue to read the last bits even after a new conversion has been initiated. That allows the use of a slower clock speed like 18 MHz in Impulse Mode, 21 MHz in Normal Mode, and 26 MHz in Warp Mode.

MICROPROCESSOR INTERFACING

The AD7671 is ideally suited for traditional dc measurement applications supporting a microprocessor and ac signal processing applications interfacing to a digital signal processor. The AD7671 is designed to interface either with a parallel 8-bit or 16-bit wide interface or with a general-purpose Serial Port or I/O Ports on a microcontroller. A variety of external buffers can be used with the AD7671 to prevent digital noise from coupling into the ADC. The following sections illustrate the use of the AD7671 with an SPI equipped microcontroller, the ADSP-21065L and ADSP-218x signal processors.

SPI Interface (MC68HC11)

Figure 22 shows an interface diagram between the AD7671 and an SPI-equipped microcontroller, such as the MC68HC11. To accommodate the slower speed of the microcontroller, the AD7671 acts as a slave device and data must be read after conversion. This mode also allows the daisy-chain feature. The convert command could be initiated in response to an internal timer interrupt. The reading of output data, one byte at a time if necessary, could be initiated in response to the end-of-conversion signal (BUSY going low) using an interrupt line of the microcontroller. The serial peripheral interface (SPI) on the MC68HC11 is configured for Master Mode (MSTR) = 1, Clock Polarity Bit (CPOL) = 0, Clock Phase Bit (CPHA) = 1, and SPI interrupt enable (SPIE) = 1 by writing to the SPI Control Register (SPCR). The IRQ is configured for edge-sensitive-only operation (IRQE = 1 in the OPTION register).

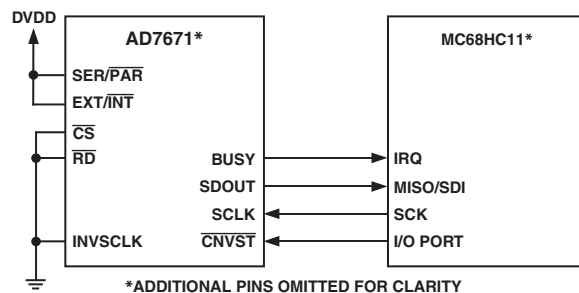


Figure 22. Interfacing the AD7671 to SPI Interface

ADSP-21065L in Master Serial Interface

As shown in Figure 23, the AD7671 can be interfaced to the ADSP-21065L using the serial interface in Master Mode without any glue logic required. This mode combines the advantages of reducing the wire connections and the ability to read the data during or after conversion at maximum speed transfer (DIVSCLK[0:1] both low).

The AD7671 is configured for the Internal Clock Mode (EXT/INT LOW) and acts therefore as the master device. The convert command can be generated by either an external low jitter oscillator or, as shown, by a FLAG output of the ADSP-21065L or by a frame output TFS of one Serial Port of the ADSP-21065L, which can be used like a timer. The Serial Port on the ADSP-21065L is configured for external clock (IRFS = 0), rising edge active (CKRE = 1), external late framed sync signals (IRFS = 0, LAFS = 1, RFSR = 1), and active HIGH (LRFS = 0). The Serial Port of the ADSP-21065L is configured by writing to its receive control register (SRCTL)—see ADSP-2106x SHARC User's Manual. Because the Serial Port within the ADSP-21065L will be seeing a discontinuous clock, an initial word reading has to be done after the ADSP-21065L has been reset to ensure that the Serial Port is properly synchronized to this clock during each following data read operation.

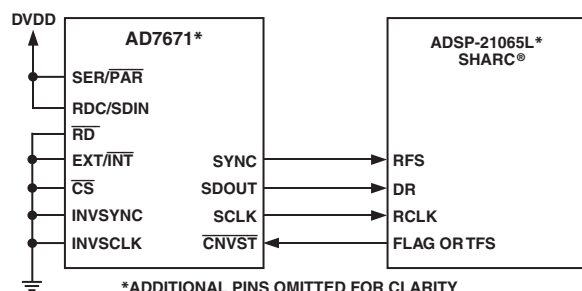


Figure 23. Interfacing to the ADSP-21065L Using the Serial Master Mode

APPLICATION HINTS

Layout

The AD7671 has very good immunity to noise on the power supplies as can be seen in Figure 9. However, care should still be taken with regard to grounding layout.

The printed circuit board that houses the AD7671 should be designed so the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. Digital and analog ground planes should be joined in only one place, preferably underneath the AD7671, or, at least, as close as possible to the AD7671. If the AD7671 is in a system where multiple devices require analog-to-digital ground connections, the connection should still be made at one point only, a star ground point, which should be established as close as possible to the AD7671.

It is recommended to avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7671 to avoid noise coupling. Fast switching signals like CNVST or clocks should be shielded with digital ground to avoid radiating noise to other sections of the board and should never run near analog signal paths. Crossover of digital and analog signals should be avoided. Traces on different but close layers of the board should run at right angles to each other. This will reduce the effect of feedthrough through the board.

The power supply lines to the AD7671 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Good decoupling is also important to lower the supplies impedance presented to the AD7671 and to reduce the magnitude of the supply spikes. Decoupling ceramic capacitors, typically 100 nF, should be placed on all of the power supply pins power supplies pins AVDD, DVDD, and OVDD close to, and ideally right up against, these pins and their corresponding ground pins. Additionally, low ESR 10 μ F capacitors should be located in the vicinity of the ADC to further reduce low frequency ripple.

The DVDD supply of the AD7671 can be either a separate supply or come from the analog supply, AVDD, or from the digital interface supply, OVDD. When the system digital supply is noisy, or fast switching digital signals are present, it is recommended, if no separate supply is available, to connect the DVDD digital supply to the analog supply AVDD through an RC filter as shown in Figure 5 and to connect the system supply to the interface digital supply OVDD and the remaining digital circuitry. When DVDD is powered from the system supply, it is useful to insert a bead to further reduce high frequency spikes.

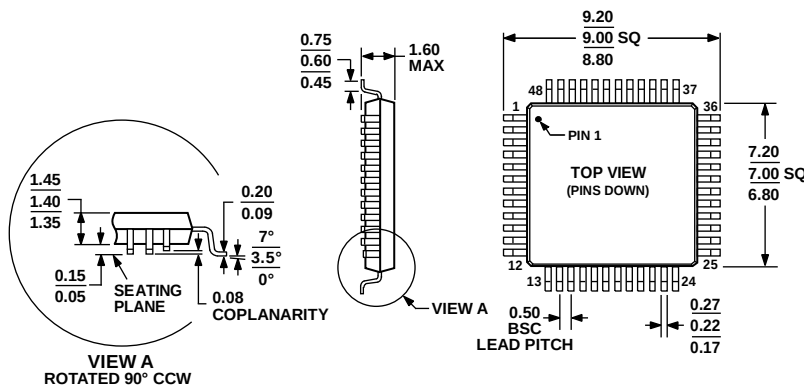
The AD7671 has five different ground pins: INGND, REFGND, AGND, DGND, and OGND. INGND is used to sense the analog input signal. REFGND senses the reference voltage and should be a low impedance return to the reference because it carries pulsed currents. AGND is the ground to which most internal ADC analog signals are referenced. This ground must be connected with the least resistance to the analog ground plane. DGND must be tied to the analog or digital ground plane depending on the configuration. OGND is connected to the digital system ground.

The layout of the decoupling of the reference voltage is important. The decoupling capacitor should be close to the ADC and connected with short and large traces to minimize parasitic inductances.

Evaluating the AD7671 Performance

A recommended layout for the AD7671 is outlined in the evaluation board for the AD7671. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the Eval-Control Board.

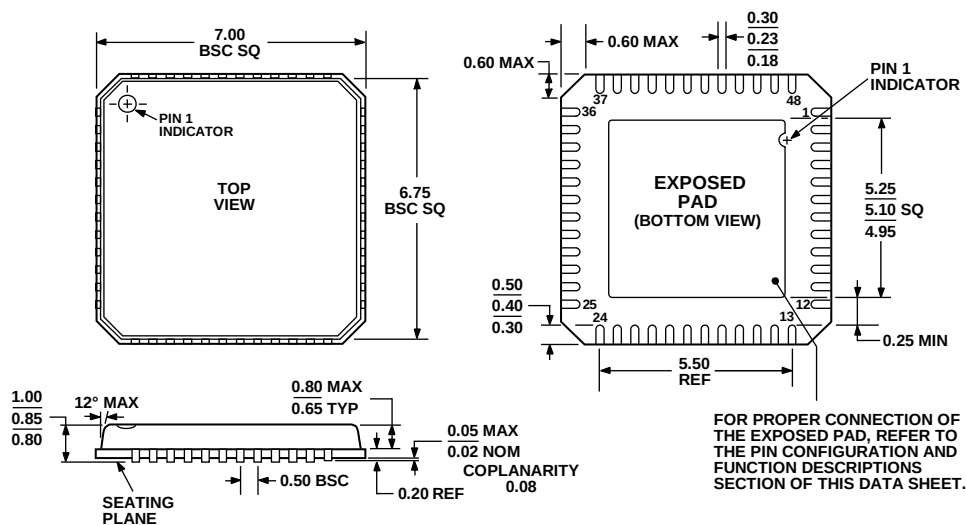
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BBC

Figure 1. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VKGD-2

Figure 2. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm × 7 mm Body, Very Thin Quad
(CP-48-1)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
AD7671ASTZ	−40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD7671ASTZRL	−40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD7671ACPZ	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-1
AD7671ACPZRL	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-1
EVAL-AD7671EDZ		Evaluation Board	
EVAL-CED1Z		Converter Evaluation and Development Board	

¹ Z = RoHS Compliant Part.

REVISION HISTORY**4/12—Rev. B to Rev. C**

Added Exposed Pad Notation to Pin Configuration	5
Added Exposed Pad Notation to Pin Function Description Table	7
Change to Figure 6	14
Updated Outline Dimensions	22
Changes to Ordering Guide	22

4/03—Rev. A to Rev. B.

Changes to PulSAR Selection Table	1
Changes to Ordering Guide	5
Changes to Figure 5	13
Updated Outline Dimensions	22

5/02—Rev. 0 to Rev. A.

Edits to Features	1
Edits to General Description	1
Chart Added to Product Highlights	1
Edits to Specifications	2–3
Edits to Table I	3
Edits to Absolute Maximum Ratings	5
Edits to Ordering Guide	5
Edits to TPC 4	9
New TPC 9	10
Addition of TPC 16	11
Edits to Table III	13
Edits to Driver Amplifier Choice Section	15
New Voltage Reference Input Section	15
New ST-48 Package Outline	22

NOTES