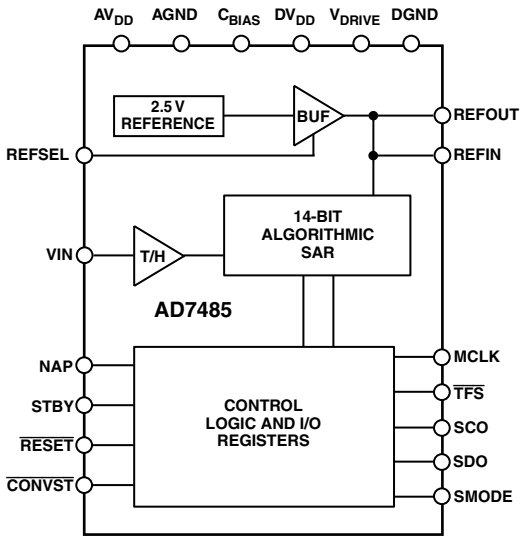
1 MSPS, Serial 14-Bit SAR ADC

AD7485

FEATURES

Fast Throughput Rate: 1 MSPS
Wide Input Bandwidth: 40 MHz
Excellent DC Accuracy Performance
Flexible Serial Interface
Low Power:
80 mW (Full Power) and 3 mW (NAP Mode)
STANDBY Mode: 2 μA Max
Single 5 V Supply Operation
Internal 2.5 V Reference
Full-Scale Overrange Indication

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7485 is a 14-bit, high speed, low power, successive-approximation ADC. The part features a serial interface with throughput rates up to 1 MSPS. The part contains a low noise, wide bandwidth track-and-hold that can handle input frequencies in excess of 40 MHz.

The conversion process is a proprietary algorithmic successive-approximation technique. The input signal is sampled and a conversion is initiated on the falling edge of the $\overline{\text{CONVST}}$ signal. The conversion process is controlled by an external master clock. Interfacing is via standard serial signal lines, making the part directly compatible with microcontrollers and DSPs.

The AD7485 provides excellent ac and dc performance specifications. Factory trimming ensures high dc accuracy resulting in very low INL, DNL, offset, and gain errors.

The part uses advanced design techniques to achieve very low power dissipation at high throughput rates. Power consumption in the normal mode of operation is 80 mW. There are two power-saving modes: a NAP mode keeps reference circuitry alive for quick power-up and consumes 3 mW, while a STANDBY mode reduces power consumption to a mere 10 μW.

The AD7485 features an on-board 2.5 V reference, but the part can also accommodate an externally provided 2.5 V reference source. The nominal analog input range is 0 V to 2.5 V.

The AD7485 also provides the user with overrange indication via a fifteenth bit. If the analog input range strays outside the 0 V to 2.5 V input range, the fifteenth data bit is set to a logic high.

The AD7485 is powered from a 4.75 V to 5.25 V supply. The part also provides a V_{DRIVE} pin that allows the user to set the voltage levels for the digital interface lines. The range for this V_{DRIVE} pin is from 2.7 V to 5.25 V. The part is housed in a 48-lead LQFP package and is specified over a –40°C to +85°C temperature range.

REV. A

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AD7485–SPECIFICATIONS[1] (V_{DD} = 5 V ± 5%, AGND = DGND = 0 V, V_{REF} = External, f_{SAMPLE} = 1 MSPS; all specifications T_{MIN} to T_{MAX} and valid for V_{DRIVE} = 2.7 V to 5.25 V, unless otherwise noted.)

Parameter	Specification	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE[2, 3]			f_{IN} = 500 kHz Sine Wave
Signal to Noise + Distortion (SINAD)[4]	76.5	dB min	
	78	dB typ	
	77	dB typ	Internal Reference
Total Harmonic Distortion (THD)[4]	–90	dB max	
	–95	dB typ	
	–92	dB typ	Internal Reference
Peak Harmonic or Spurious Noise (SFDR)[4]	–88	dB max	
Intermodulation Distortion (IMD)[4]			
Second-Order Terms	–96	dB typ	f_{IN1} = 95.053 kHz, f_{IN2} = 105.329 kHz
Third-Order Terms	–94	dB typ	
Aperture Delay	10	ns typ	
Full Power Bandwidth	40	MHz typ	@ 3 dB
	3.5	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	14	Bits	
Integral Nonlinearity[4]	±1	LSB max	
	±0.5	LSB typ	
Differential Nonlinearity[4]	±0.75	LSB max	Guaranteed No Missed Codes to 14 Bits
	±0.25	LSB typ	
Offset Error[4]	±6	LSB max	
	0.036	%FSR max	
Gain Error[4]	±6	LSB max	
	0.036	%FSR max	
ANALOG INPUT			
Input Voltage	0	V min	
	2.5	V max	
DC Leakage Current	±1	μA max	
Input Capacitance[5]	35	pF typ	
REFERENCE INPUT/OUTPUT			
V_{REFIN} Input Voltage	2.5	V	±1% for Specified Performance
V_{REFIN} Input DC Leakage Current	±1	μA max	
V_{REFIN} Input Capacitance[5]	25	pF typ	
V_{REFIN} Input Current[6]	220	μA typ	External Reference
V_{REFOUT} Output Voltage	2.5	V typ	
V_{REFOUT} Error @ 25°C	±50	mV typ	
V_{REFOUT} Error T_{MIN} to T_{MAX}	±100	mV max	
V_{REFOUT} Output Impedance	1	Ω typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	V_{DRIVE} –1	V min	
Input Low Voltage, V_{INL}	0.4	V max	
Input Current, I_{IN}	±1	μA max	
Input Capacitance, C_{IN}[5]	10	pF typ	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}[7]	$0.7 \times V_{DRIVE}$	V min	
Output Low Voltage, V_{OL}[7]	$0.3 \times V_{DRIVE}$	V max	
Floating-State Leakage Current	±10	μA max	
Floating-State Output Capacitance[5]	10	pF max	
Output Coding	Straight (Natural) Binary		
CONVERSION RATE			
Conversion Time	24	MCLKs	
Track/Hold Acquisition Time	100	ns max	Sine Wave Input
	70	ns max	Full-Scale Step Input
Throughput Rate	1	MSPS max	

Parameter	Specification	Unit	Test Conditions/Comments
POWER REQUIREMENTS			
V_{DD}	5	V	±5%
V_{DRIVE}	2.7	V min	
	5.25	V max	
I_{DD}			
Normal Mode (Static)	13	mA max	
Normal Mode (Operational)	17	mA max	
NAP Mode	0.6	mA max	
STANDBY Mode[8]	2	μA max	
	0.5	μA typ	
Power Dissipation			
Normal Mode (Operational)	85	mW max	
NAP Mode	3	mW max	
STANDBY Mode[8]	10	μW max	

NOTES
[1]Temperature ranges as follows: –40°C to +85°C.
[2]SINAD figures quoted include external analog input circuit noise contribution of approximately 1 dB.
[3]See Typical Performance Characteristics section for analog input circuits used.
[4]See Terminology.
[5]Sample tested @ 25°C to ensure compliance.
[6]Current drawn from external reference during conversion.
[7]I_{LOAD} = 200 μA.
[8]Digital input levels at GND or V_{DRIVE}.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1]

(V_{DD} = 5 V ± 5%, AGND = DGND = 0 V, V_{REF} = External; all specifications T_{MIN} to T_{MAX} and valid for V_{DRIVE} = 2.7 V to 5.25 V, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Master Clock Frequency	f_{MCLK}	0.01		25	MHz
MCLK Period	t_1	40		100000	ns
Conversion Time	t_2	$t_1 \times 24$			ns
$\overline{CONVST}$ Low Period (Mode 1)[2]	t_3	$t_1 \times 22$			ns
$\overline{CONVST}$ High Period (Mode 1)[2]	t_4	10			ns
MCLK High Period	t_5	$0.4 \times t_1$		$0.6 \times t_1$	ns
MCLK Low Period	t_6	$0.4 \times t_1$		$0.6 \times t_1$	ns
$\overline{CONVST}$ Falling Edge to MCLK Rising Edge	t_7	7			ns
MCLK Rising Edge to MSB Valid	t_8			15	ns
Data Valid before SCO Falling Edge	t_9	10			ns
Data Valid after SCO Falling Edge	t_{10}	20			ns
$\overline{CONVST}$ Rising Edge to SDO Three-State	t_{11}			6	ns
$\overline{CONVST}$ Low Period (Mode 2)[2]	t_{12}	10		$t_1 \times 2$	ns
$\overline{CONVST}$ High Period (Mode 2)[3]	t_{13}	10			ns
$\overline{CONVST}$ Falling Edge to $\overline{TFS}$ Falling Edge	t_{14}	10			ns
$\overline{TFS}$ Falling Edge to MSB Valid	t_{15}			30	ns
$\overline{TFS}$ Rising Edge to SDO Three-State	t_{16}			8	ns
$\overline{TFS}$ Low Period[4]	t_{17}	$t_1 \times 22$			ns
$\overline{TFS}$ High Period[4]	t_{18}	10			ns
MCLK Fall Time	t_{19}	5		25	ns
MCLK Rise Time	t_{20}	5		25	ns
MCLK – SCO Delay	t_{21}	6		25	ns

NOTES
[1]All timing specifications given above are with a 25 pF load capacitance. With a load capacitance greater than this value, a digital buffer or latch must be used.
[2]$\overline{CONVST}$ idling high. See Serial Interface section for further details.
[3]$\overline{CONVST}$ idling low. See Serial Interface section for further details.
[4]$\overline{TFS}$ can also be tied low in this mode.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C, unless otherwise noted.)

V_{DD} to GND . . . . . –0.3 V to +7 V
V_{DRIVE} to GND . . . . . –0.3 V to +7 V
Analog Input Voltage to GND . . . . . –0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to GND . . . . . –0.3 V to V_{DRIVE} + 0.3 V
REFIN to GND . . . . . –0.3 V to AV_{DD} + 0.3 V
Input Current to Any Pin except Supplies . . . . . ±10 mA
Operating Temperature Range
Commercial . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
θ_{JA} Thermal Impedance . . . . . 50°C/W
θ_{JC} Thermal Impedance . . . . . 10°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C
ESD . . . . . 1 kV

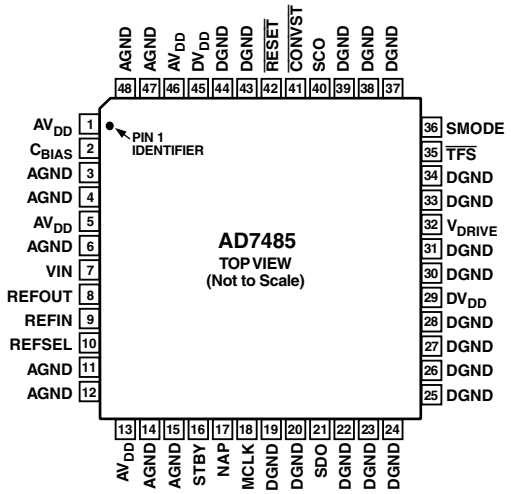
*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7485 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1, 5, 13, 46	AV_{DD}	Positive Power Supply for Analog Circuitry
2	C_{BIAS}	Decoupling Pin for Internal Bias Voltage. A 1 nF capacitor should be placed between this pin and AGND.
3, 4, 6, 11, 12, 14, 15, 47, 48	AGND	Power Supply Ground for Analog Circuitry
7	VIN	Analog Input. Single-ended analog input channel.
8	REFOUT	Reference Output. REFOUT connects to the output of the internal 2.5 V reference buffer. A 470 nF capacitor must be placed between this pin and AGND.
9	REFIN	Reference Input. A 470 nF capacitor must be placed between this pin and AGND. When using an external voltage reference source, the reference voltage should be applied to this pin.
10	REFSEL	Reference Decoupling Pin. When using the internal reference, a 1 nF capacitor must be connected from this pin to AGND. When using an external reference source, this pin should be connected directly to AGND.
16	STBY	Standby Logic Input. When this pin is logic high, the device will be placed in STANDBY mode. See the Power Saving section for further details.
17	NAP	Nap Logic Input. When this pin is logic high, the device will be placed in a very low power mode. See the Power Saving section for further details.
18	MCLK	Master Clock Input. This is the input for the master clock, which controls the conversion cycle. The frequency of this clock may be up to 25 MHz. Twenty-four clock cycles are required for each conversion.
19, 20, 22–28 30, 31, 33, 34 37–39, 43, 44	DGND	Ground Reference for Digital Circuitry
21	SDO	Serial Data Output. The conversion data is latched out on this pin on the rising edge of SCO. It should be latched into the receiving serial port of the DSP on the falling edge of SCO. The overrange bit is latched out first, then 14 bits of data (MSB first) followed by a trailing zero.
29, 45	DV_{DD}	Positive Power Supply for Digital Circuitry
32	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface logic of the AD7485 will operate.
35	$\overline{TFS}$	Transmit Frame Sync Input. In Serial Mode 2, this pin acts as a framing signal for the serial data being clocked out on SDO. A falling edge on $\overline{TFS}$ brings SDO out of three-state and the data starts to get clocked out on the next rising edge of SCO.
36	SMODE	Serial Mode Input. A logic low on this pin selects Serial Mode 1 and a logic high selects Serial Mode 2. See the Serial Interface section for further details.
40	SCO	Serial Clock Output. This clock is derived from MCLK and is used to latch conversion data from the device. See the Serial Interface section for further details.
41	$\overline{CONVST}$	Convert Start Logic Input. A conversion is initiated on the falling edge of the $\overline{CONVST}$ signal. The input track/hold amplifier goes from track mode to hold mode and the conversion process commences.
42	$\overline{RESET}$	Reset Logic Input. A falling edge on this pin resets the internal state machine and terminates a conversion that may be in progress. Holding this pin low keeps the part in a reset state.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e., AGND + 0.5 LSB.

Gain Error
This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e., V_{REF} – 1.5 LSB) after the offset error has been adjusted out.

Track/Hold Acquisition Time
Track/hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion (the point at which the track/hold returns to track mode).

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$Signal\ to\ (Noise + Distortion) = \left(6.02\ N + 1.76\right)\ dB$$

Thus, for a 14-bit converter this is 86.04 *dB*.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of the harmonics to the fundamental. For the AD7485, it is defined as:

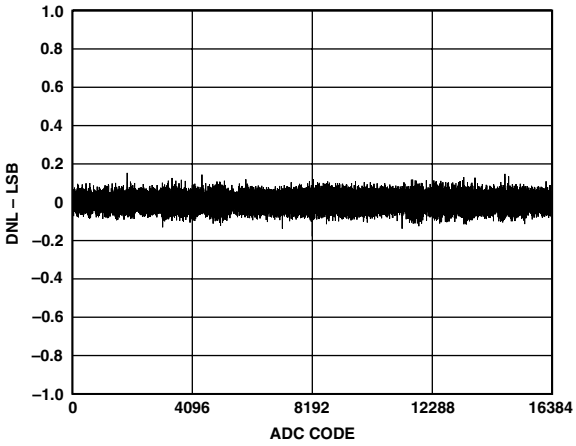
$$THD\ (dB) = 20\ log\ \frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through sixth harmonics.

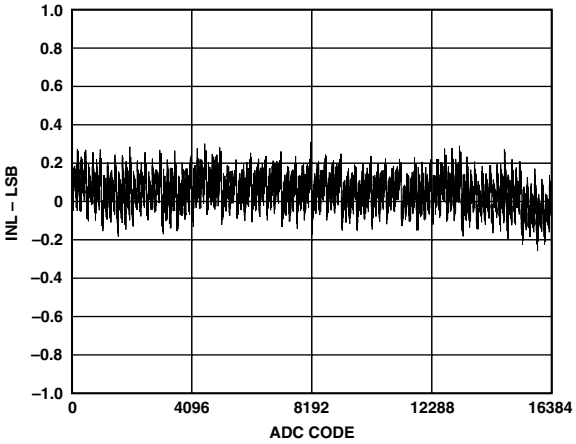
Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n is equal to zero. For example, the second-order terms include (fa + fb) and (fa – fb), while the third-order terms include (2fa + fb), (2fa – fb), (fa + 2fb), and (fa – 2fb).

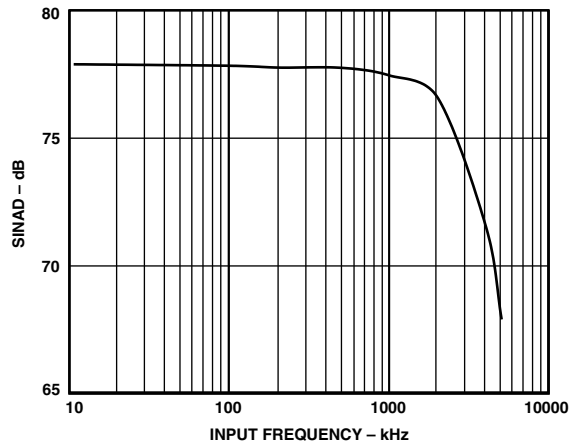
The AD7485 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.



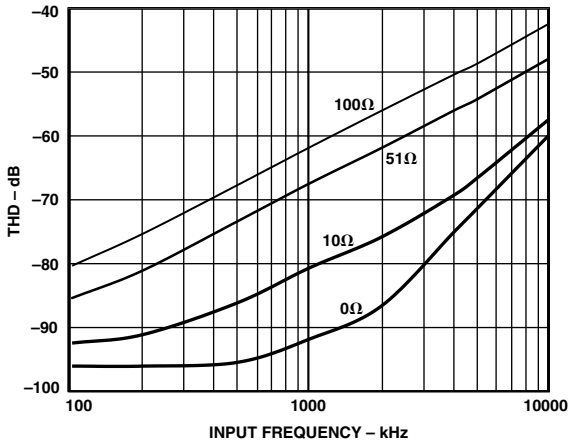
TPC 1. Typical DNL



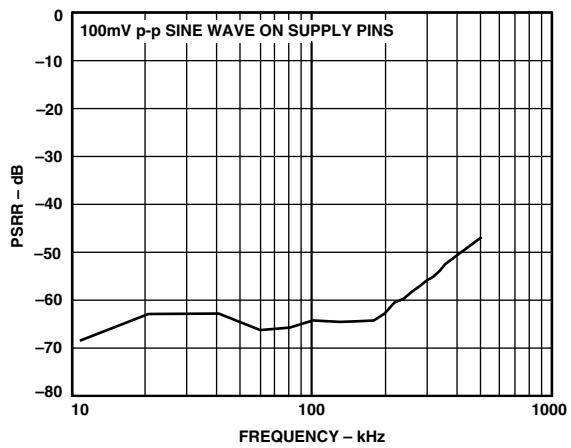
TPC 2. Typical INL



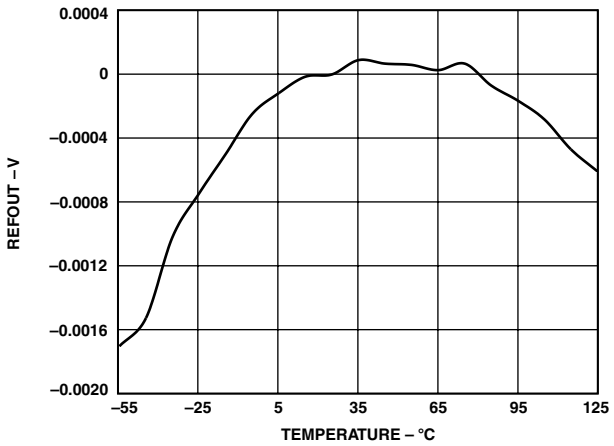
TPC 3. SINAD vs. Input Tone (AD8021 Input Circuit)



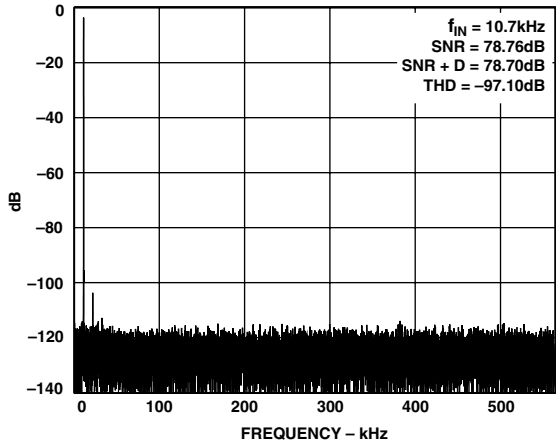
TPC 4. THD vs. Input Tone for Different Input Resistances



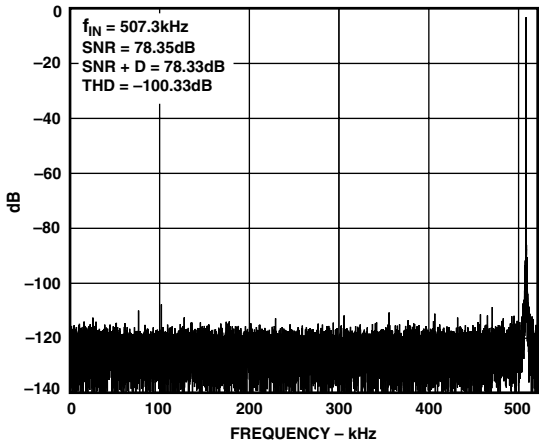
TPC 5. PSRR without Decoupling



TPC 6. Reference Error



TPC 7. 64k FFT Plot with 10 kHz Input Tone



TPC 8. 64k FFT Plot with 500 kHz Input Tone

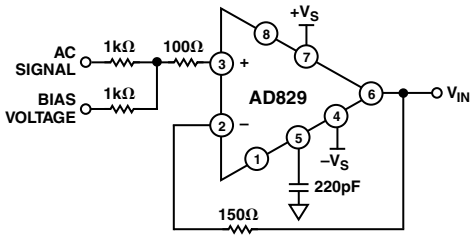


Figure 1. Analog Input Circuit Used for 10 kHz Input Tone

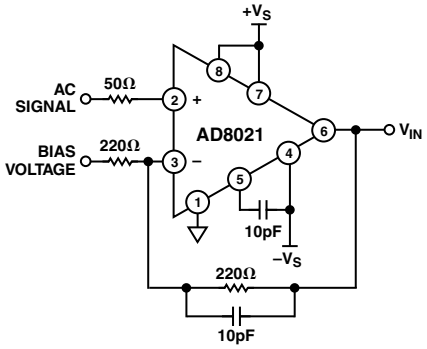


Figure 2. Analog Input Circuit Used for 500 kHz Input Tone

Figure 1 shows the analog input circuit used to obtain the data for the FFT plot shown in TPC 7. The circuit uses an Analog Devices AD829 op amp as the input buffer. A bipolar analog signal is applied as shown and biased up with a stable, low noise dc voltage connected to the labeled terminal shown. A 220 pF compensation capacitor is connected between Pin 5 of the AD829 and the analog ground plane. The AD829 is supplied with +12 V and –12 V supplies. The supply pins are decoupled as close to the device as possible, with both a 0.1 µF and 10 µF capacitor connected to each pin. In each case, the 0.1 µF capacitor should be the closer of the two capacitors to the device. More information on the AD829 is available on the Analog Devices website.

For higher input bandwidth applications, Analog Devices' AD8021 op amp (also available as a dual AD8022) is the recommended choice to drive the AD7485. Figure 2 shows the analog input circuit used to obtain the data for the FFT plot shown in TPC 8. A bipolar analog signal is applied to the terminal shown and biased with a stable, low noise dc voltage connected as shown. A 10 pF compensation capacitor is connected between Pin 5 of the AD8021 and the negative supply. As with the previous circuit, the AD8021 is supplied with +12 V and –12 V supplies. The supply pins are decoupled as close to the device as possible with both a 0.1 µF and 10 µF capacitor connected to each pin. In each case, the 0.1 µF capacitor should be the closer of the two capacitors to the device. The AD8021 Logic Reference pin is tied to analog ground and the $\overline{\text{DISABLE}}$ pin is tied to the positive supply as shown. Detailed information on the AD8021 is available on the Analog Devices website.

CIRCUIT DESCRIPTION

CONVERTER OPERATION

The AD7485 is a 14-bit algorithmic successive-approximation analog-to-digital converter based around a capacitive DAC. It provides the user with track-and-hold, reference, an A/D converter, and versatile interface logic functions on a single chip. The analog input signal range that the AD7485 can convert is 0 V to 2.5 V. The part requires a 2.5 V reference that can be provided from the part's own internal reference or an external reference source. Figure 3 shows a very simplified schematic of the ADC. The Control Logic, SAR, and Capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back to a balanced condition.

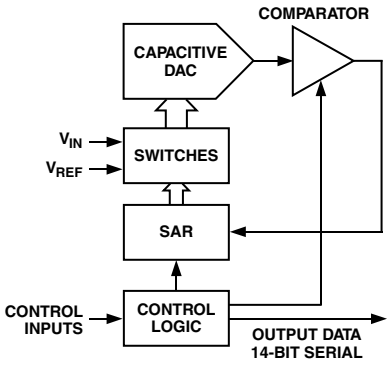


Figure 3. Simplified Block Diagram

Conversion is initiated on the AD7485 by pulsing the $\overline{\text{CONVST}}$ input. On the falling edge of $\overline{\text{CONVST}}$, the track/hold goes from track to hold mode and the conversion sequence is started. Conversion time for the part is 24 MCLK periods. Figure 4 shows the ADC during conversion. When conversion starts, SW2 will open and SW1 will move to position B causing the comparator to become unbalanced. The ADC then runs through its successive approximation routine and brings the comparator back into a balanced condition. When the comparator is rebalanced, the conversion result is available in the SAR register.

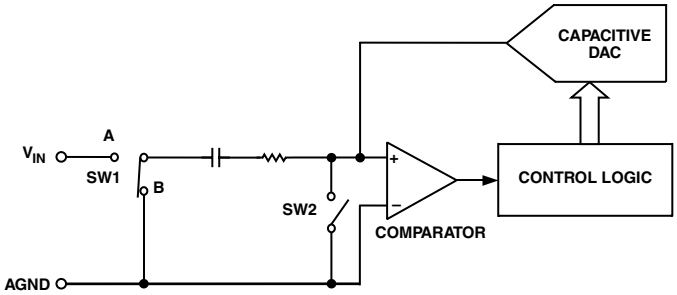


Figure 4. ADC Conversion Phase

At the end of conversion, track-and-hold returns to tracking mode and the acquisition time begins. The track/hold acquisition time is 70 ns. Figure 5 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on V_{IN}.

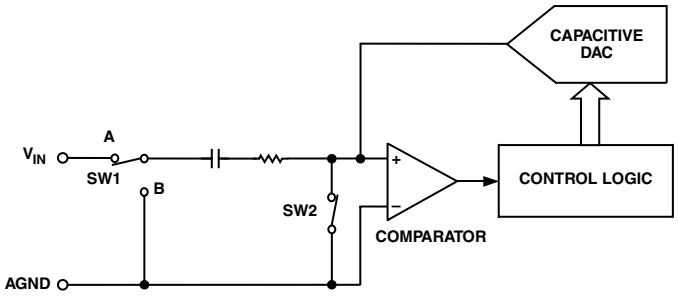


Figure 5. ADC Acquisition Phase

ADC TRANSFER FUNCTION

The output coding of the AD7485 is straight binary. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSB, and so on). The LSB size is $V_{REF}/16384$. The nominal transfer characteristic for the AD7485 is shown in Figure 6.

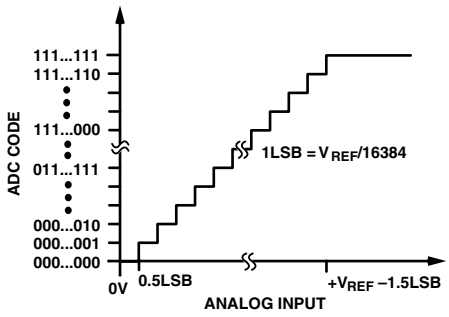


Figure 6. Transfer Characteristic

POWER SAVING

The AD7485 uses advanced design techniques to achieve very low power dissipation at high throughput rates. In addition to this, the AD7485 features two power saving modes, NAP mode and STANDBY mode. These modes are selected by bringing either the NAP or STBY pin to a logic high.

When operating the AD7485 with a 25 MHz MCLK in normal, fully powered mode, the current consumption is 16 mA during conversion and the quiescent current is 12 mA. Operating at a throughput rate of 500 kSPS, the conversion time of 960 ns contributes 38.4 mW to the overall power dissipation.

$$(960\ ns/2\ \mu s) \times (5V \times 16\ mA) = 38.4\ mW$$

For the remaining 1.04 µs of the cycle, the AD7485 dissipates 31.2 mW of power.

$$(1.04\ \mu s/2\ \mu s) \times (5V \times 12\ mA) = 31.2\ mW$$

Thus the power dissipated during each cycle is:

$$38.4\ mW + 31.2\ mW = 69.6\ mW$$

Figure 7 shows the AD7485 conversion sequence operating in normal mode.

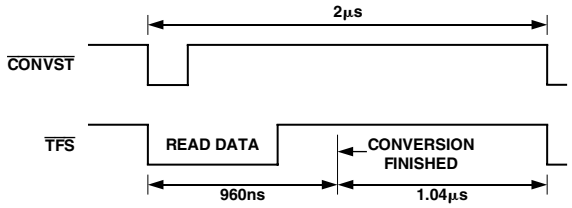


Figure 7. Normal Mode Power Dissipation

In NAP mode, all the internal circuitry except for the internal reference is powered down. In this mode, the power dissipation of the AD7485 is reduced to 3 mW. When exiting NAP mode, a minimum of 300 ns when using an external reference must be waited before initiating a conversion. This is necessary to allow the internal circuitry to settle after power-up and for the track/hold to properly acquire the analog input signal.

If the AD7485 is put into NAP mode after each conversion, the average power dissipation will be reduced but the throughput rate will be limited by the power-up time. Using the AD7485 with a throughput rate of 100 kSPS while placing the part in NAP mode after each conversion would result in average power dissipation as follows:

The power-up phase contributes:

$$(300\ ns/10\ \mu s) \times (5\ V \times 12\ mA) = 1.8\ mW$$

The conversion phase contributes:

$$(960\ ns/10\ \mu s) \times (5\ V \times 16\ mA) = 7.68\ mW$$

While in NAP mode for the rest of the cycle, the AD7485 dissipates only 2.185 mW of power.

$$(8.74\ \mu s/10\ \mu s) \times (5\ V \times 0.6\ mA) = 2.622\ mW$$

Thus the power dissipated during each cycle is:

$$1.8\ mW + 7.68\ mW + 2.622\ mW + 12.1\ mW$$

Figure 8 shows the AD7485 conversion sequence if putting the part into NAP mode after each conversion.

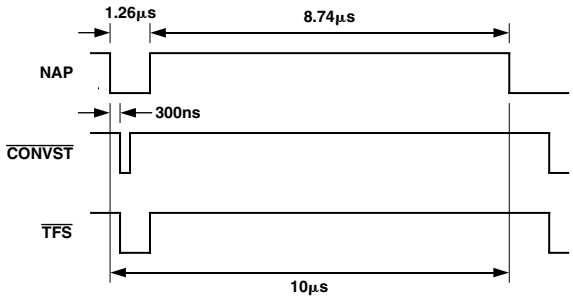


Figure 8. NAP Mode Power Dissipation

Figures 9 and 10 show a typical graphical representation of power versus throughput for the AD7485 when in normal and NAP modes, respectively.

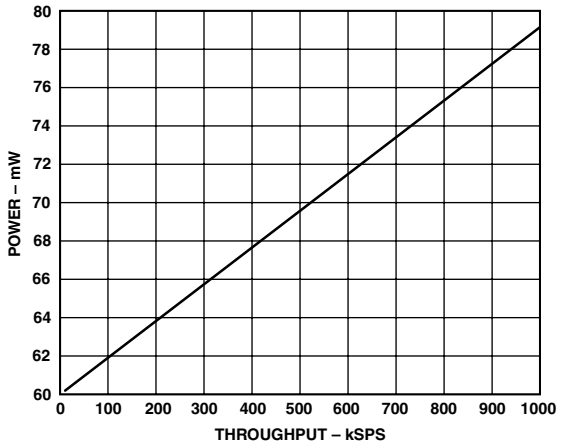


Figure 9. Normal Mode, Power vs. Throughput

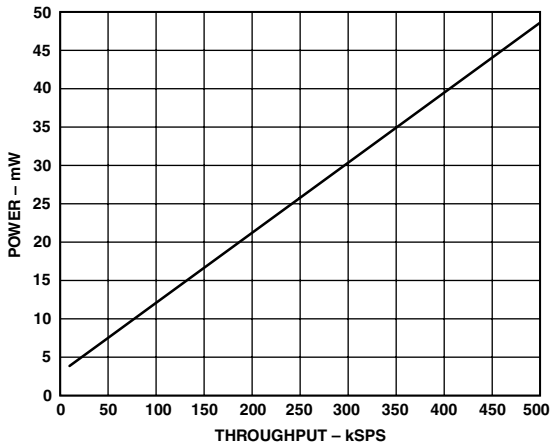


Figure 10. NAP Mode, Power vs. Throughput

In STANDBY mode, all the internal circuitry is powered down and the power consumption of the AD7485 is reduced to 10 µW. Because the internal reference has been powered down, the power-up time necessary before a conversion can be initiated is longer. If using the internal reference of the AD7485, the ADC must be brought out of STANDBY mode 500 ms before a conversion is initiated. Initiating a conversion before the required power-up time has elapsed will result in incorrect conversion data. If an external reference source is used and kept powered up while the AD7485 is in STANDBY mode, the power-up time required will be reduced to 80 µs.

SERIAL INTERFACE

The AD7485 has two serial interface modes, selected by the state of the SMODE pin. In both these modes, the MCLK pin must be supplied with a clock signal of between 10 kHz and 25 MHz. This MCLK signal controls the internal conversion process and is also used to derive the SCO signal. As the AD7485 uses an algorithmic successive-approximation technique, 24 MCLK cycles are required to complete a conversion. Due to the error-correcting operation of this ADC, all bit trials must be completed before the conversion result is calculated. This results in a single sample delay in the result that is clocked out.

In Serial Mode 1 (Figure 13), the $\overline{\text{CONVST}}$ pin is used to initiate the conversion and also frame the serial data. When $\overline{\text{CONVST}}$ is brought low, the SDO line is taken out of three-state, the overrange bit will be clocked out on the next rising edge of SCO followed by the 14 data bits (MSB first) and a trailing zero. $\overline{\text{CONVST}}$ must remain low for 22 SCO pulses to allow all the data to be clocked out and the conversion in progress to be completed. When $\overline{\text{CONVST}}$ returns to a logic high, the SDO line returns to three-state. $\overline{\text{TFS}}$ should be tied to ground in this mode.

In Serial Mode 2 (Figure 14), the $\overline{\text{CONVST}}$ pin is used to initiate the conversion, but the $\overline{\text{TFS}}$ signal is used to frame the serial data. The $\overline{\text{CONVST}}$ signal can idle high or low in this mode. Idling high, the $\overline{\text{CONVST}}$ pulsewidth must be between 10 ns and two MCLK periods. Idling low, the $\overline{\text{CONVST}}$ pulsewidth must be at least 10 ns. $\overline{\text{TFS}}$ must remain low for a minimum of 22 SCO cycles in this mode but can also be tied permanently low. If $\overline{\text{TFS}}$ is tied low, the SDO line will always be driven.

The relationship between the MCLK and SCO signals is shown in Figure 15.

Figure 11 shows a typical connection diagram for the AD7485. In this case, the MCLK signal is provided by a 25 MHz crystal oscillator module. It could also be provided by the second serial port of a DSP (e.g., ADSP-2189M) if one were available.

In Figure 11 the V_{DRIVE} pin is tied to DV_{DD}, which results in logic output levels being either 0 V or DV_{DD}. The voltage applied to V_{DRIVE} controls the voltage value of the output logic signals. For example, if DV_{DD} is supplied by a 5 V supply and V_{DRIVE} by a 3 V supply, the logic output levels would be either 0 V or 3 V. This feature allows the AD7485 to interface to 3 V devices while still enabling the A/D to process signals at 5 V supply.

The maximum slew rate at the input of the ADC should be limited to 500 V/µs while the conversion is taking place. This will prevent corruption of the current conversion. In any multiplexed application, the channel switching should occur as early as possible after the first MCLK period.

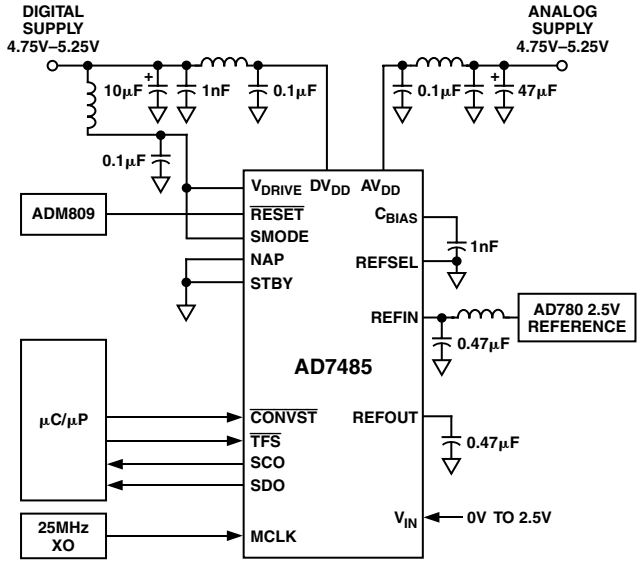


Figure 11. Typical Connection Diagram

Driving the $\overline{\text{CONVST}}$ Pin

To achieve the specified performance from the AD7485, the $\overline{\text{CONVST}}$ pin must be driven from a low jitter source. Since the falling edge on the $\overline{\text{CONVST}}$ pin determines the sampling instant, any jitter that may exist on this edge will appear as noise when the analog input signal contains high frequency components. The relationship between the analog input frequency (f_{IN}), timing jitter (t_j), and resulting SNR is given by the equation below.

$$SNR_{JITTER}(dB) = 10 \log \frac{1}{(2\pi \times f_{IN} \times t_j)^2}$$

As an example, if the desired SNR due to jitter was 100 dB with a maximum full-scale analog input frequency of 500 kHz, ignoring all other noise sources we get an allowable jitter of 3.18 ps on the $\overline{\text{CONVST}}$ falling edge. For a 14-bit converter (ideal SNR = 86.04 dB), the allowable jitter will be greater than the figure given above; but due consideration needs to be given to the design of the $\overline{\text{CONVST}}$ circuitry to achieve 14-bit performance with large analog input frequencies.

Board Layout and Grounding

To obtain optimum performance from the AD7485, it is recommended that a printed circuit board with a minimum of three layers is used. One of these layers, preferably the middle layer, should be as complete a ground plane as possible to give the best shielding. The board should be designed in such a way that the analog and digital circuitry are separated and confined to certain areas of the board. This practice, along with avoiding running digital and analog lines close together, should help to avoid coupling digital noise onto analog lines.

The power supply lines to the AD7485 should be approximately 3 mm wide to provide a low impedance path and reduce the effects of glitches on the power supply lines. It is vital that good decoupling is also present. A combination of ferrites and decoupling capacitors should be used as shown in Figure 11.

The decoupling capacitors should be as close to the supply pins as possible. This is made easier by the use of multilayer boards. The signal traces from the AD7485 pins can be run on the top layer while the decoupling capacitors and ferrites mounted on the bottom layer where the power traces exist. The ground plane between the top and bottom planes provides excellent shielding.

Figures 12a–12e show a sample layout of the board area immediately surrounding the AD7485. Pin 1 is the bottom left corner of the device. Figure 12a shows the top layer where the AD7485 is mounted with vias to the bottom routing layer highlighted. Figure 12b shows the bottom layer where the power routing is with the same vias highlighted. Figure 12c shows the bottom layer silkscreen where the decoupling components are soldered directly beneath the device. Figure 12d shows the silkscreen overlaid on the solder pads for the decoupling components, and Figure 12e shows the top and bottom routing layers overlaid. The black area in each figure indicates the ground plane present on the middle layer.

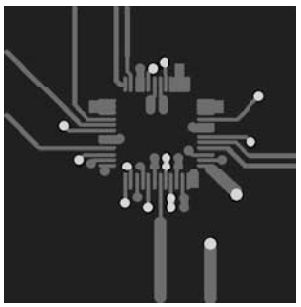


Figure 12a



Figure 12b



Figure 12c

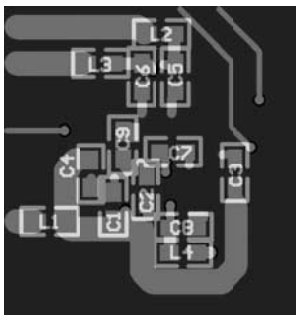


Figure 12d

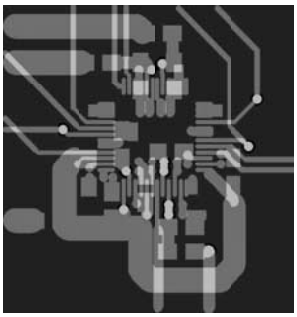


Figure 12e

C1-6 : 100 nF, C7–8: 470 nF, C9: 1 nF

L1-4: Meggit-Sigma Chip Ferrite Beads (BMB2A0600RS2)

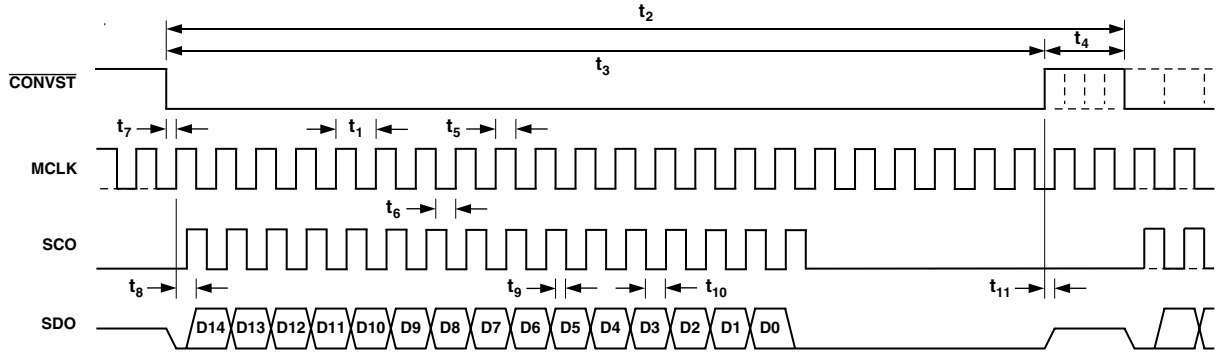


Figure 13. Serial Mode 1 (SMODE = 0) Read Cycle

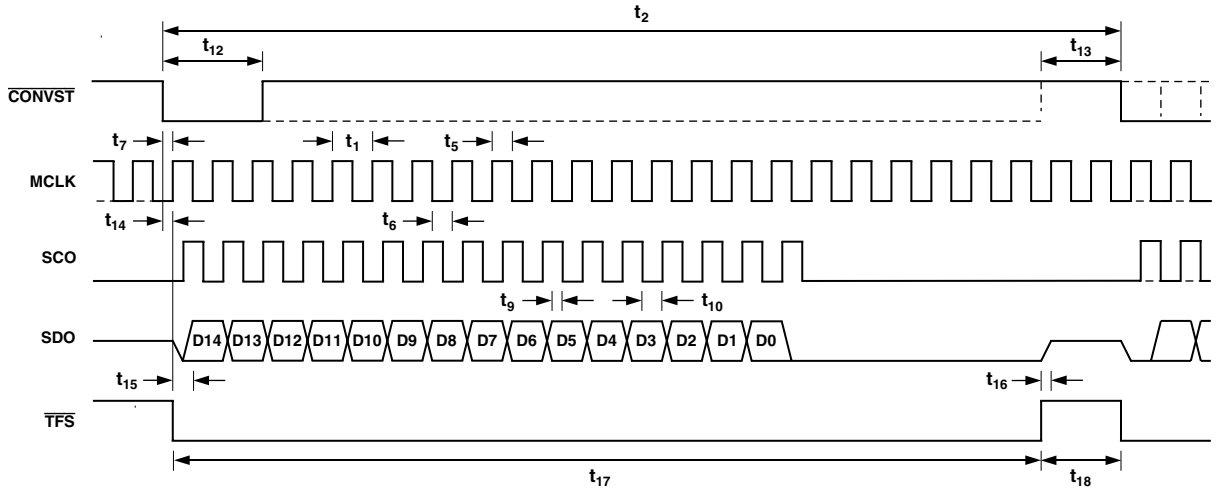


Figure 14. Serial Mode 2 (SMODE = 1) Read Cycle

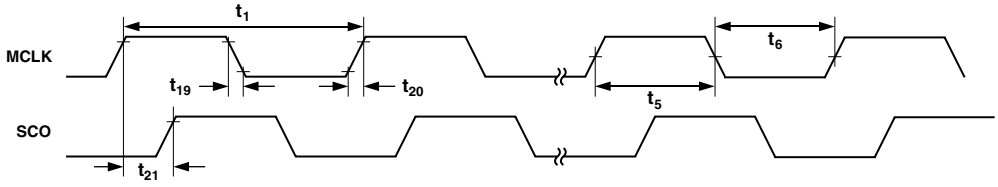


Figure 15. Serial Clock Timing

OUTLINE DIMENSIONS

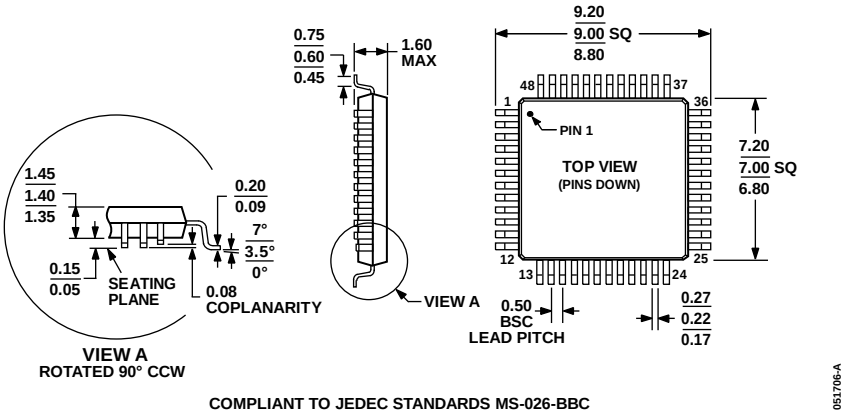


Figure 1. 48-Lead Low Profile Quad Flatpack [LQFP]
7 mm × 7 mm, Very Thin Quad
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7485BSTZ	−40°C to +85°C	48-Lead Low Profile Quad Flatpack [LQFP]	ST-48

[1] Z = RoHS Compliant Part.

REVISION HISTORY

4/10—Rev. 0 to Rev. A

Changes to Specifications Table 3

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D02758-0-4/10(A)