Quad-Channel, Software Configurable Input and Output

Data Sheet **AD74413R**

FEATURES

- Quad-channel software configurable input/output circuit
- Screw terminals tolerant to ±40 V dc
- Line protectors to block power from the screw terminals to supplies
- User configurable modes
  - Voltage input
  - Current input
  - Voltage output
  - Current output
  - Digital input
  - RTD measurement
- Internal 16-bit, Σ-Δ ADC with optional 50 Hz and 60 Hz rejection
- 13-bit monotonic DACs
- Charge pump for true zero voltage output
- HART-compatible
- Internal temperature sensor, ±5°C accuracy
- On-chip diagnostics including open circuit and short-circuit detection
- SPI-compatible
- Temperature range: −40°C to +105°C
- 64-lead LFCSP

APPLICATIONS

- Process control
- Factory automation
- Motor drives
- Building control systems

GENERAL DESCRIPTION

The AD74413R is a quad-channel software configurable input/output solution for building and process control applications. The AD74413R contains functionality for analog output, analog input, digital input, resistance temperature detector (RTD), and thermocouple measurements integrated into a single chip solution with a serial peripheral interface (SPI).

The device features a 16-bit, Σ-Δ analog-to-digital converter (ADC) and four configurable, 13-bit digital-to-analog converters (DACs) to provide four configurable input/output channels and a suite of diagnostic functions.

There are several modes related to the AD74413R. These modes are voltage output, current output, voltage input, externally powered current input, loop powered current input, external RTD measurement, digital input logic, and loop powered digital input.

The AD74413R contains a high accuracy 2.5 V internal reference to drive the DACs and the ADC.

COMPANION PRODUCTS

External Reference: ADR4525

PRODUCT HIGHLIGHTS

1. Quad-Channel, Software Configurable Channels.
2. Built In Diagnostics and Alert Features.
3. Robust Architecture.

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REVISION HISTORY

11/2019—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

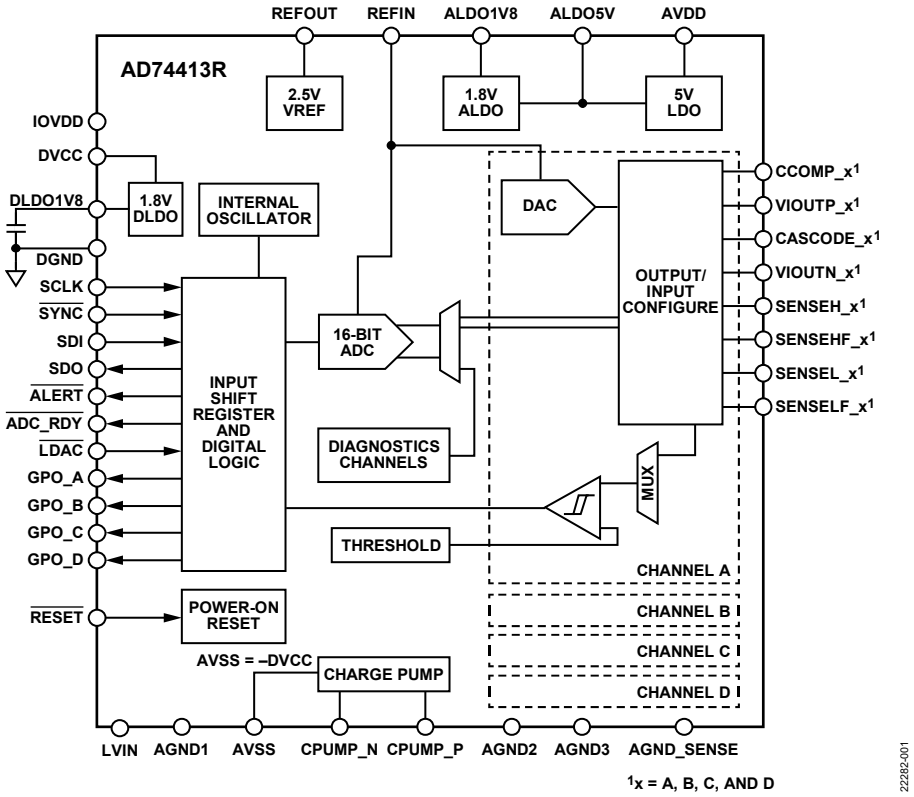


Figure 1.

SPECIFICATIONS

VOLTAGE OUTPUT

AVDD = 14 V to 28.8 V, AGND = DGND = 0 V, REFIN = 2.5 V (ideal), DVCC = 2.7 V to 5.5 V, IOVDD = 1.7 V to 5.5 V, and all specifications at T_A = −40°C to +105°C, unless otherwise noted. Resistor load (R_{LOAD}) = 100 kΩ and capacitor load (C_{LOAD}) = 10 nF per recommended configuration.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE OUTPUT					
Resolution	13			Bits	
Output Range	0		11	V	
ACCURACY					
Total Unadjusted Error (TUE)	−0.2		+0.2	%FSR	
TUE at 25°C	−0.15		+0.15	%FSR	
Integral Nonlinearity (INL)	−2		+2	LSB	
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Offset Error	−5.5		+5.5	mV	
Offset Error at 25°C	−3.0		+3.0	mV	
Gain Error	−0.2		+0.2	%FSR	
Gain Error 25°C	−0.18		+0.18	%FSR	
OUTPUT CHARACTERISTICS					
Load	500	100k		Ω	
Headroom (500 Ω Load)	4.1			V	Minimum voltage difference required between AVDD and the input/output positive (I/OP_x where x is the channel number) screw terminal to provide 11 V across a 500 Ω load
Short-Circuit Current (Sourcing)	24.5	29	32.5	mA	Per channel, lower limit bit = 0 (default)
	5.5	7	9	mA	Per channel, lower limit bit = 1
Short-Circuit Current (Sinking)	3.0	3.7	4.5	mA	
Maximum Capacitive Load			14	nF	System capacitance on the I/OP_x screw terminal including the recommended 10 nF; external compensation capacitor (C_{COMP}) not connected
			2	µF	External C_{COMP} = 200 pF connected
DC Output Impedance		0.12		Ω	
DC Power Supply Rejection Ratio (PSRR)		80		dB	
DYNAMIC PERFORMANCE					
Output Voltage Settling Time		50		µs	10 V step (0.5 V to 10.5 V or 10.5 V to 0.5 V) to ±0.05 %FSR; C_{LOAD} = 14 nF, no C_{COMP} connected
Noise (External Reference)					Measured at the I/OP_x screw terminal, 2.5 V output
Output Noise		0.07		LSB p-p	0.1 Hz to 10 Hz bandwidth
Output Noise Spectral Density		320		nV/√Hz	Measured at 1 kHz
AC PSRR		65		dB	200 mV at 1 kHz sine wave superimposed on the AVDD supply

CURRENT OUTPUT

AVDD = 14 V to 28.8 V, AGND = DGND = 0 V, REFIN = 2.5 V (ideal), DVCC = 2.7 V to 5.5 V, IOVDD= 1.7 V to 5.5 V, and all specifications at T_A = −40°C to +105°C, unless otherwise noted. R_{LOAD} = 250 Ω, C_{LOAD} = 10 nF per recommended configuration, and the sense resistor (R_{SENSE}) = 100 Ω (ideal).

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT OUTPUT					
Resolution	13			Bits	
Output Range	0		25	mA	
ACCURACY					
TUE[1]	−0.28		+0.28	%FSR	
TUE at 25°C	−0.2		+0.2	%FSR	
INL	−3		+3	LSB	From zero-scale to full-scale
DNL	−1		+1	LSB	Guaranteed monotonic
Offset Error	−15	2.0	+15	µA	
Offset Error at 25°C[1]	−11		+11	µA	
Gain Error[1]	−0.3		+0.3	%FSR	
Gain Error at 25°C[1]	−0.25		+0.25	%FSR	
OUTPUT CHARACTERISTICS					
Headroom	4.6			V	Minimum voltage difference required between AVDD and the I/OP_x screw terminal to source 25 mA
Open Circuit Voltage		AVDD		V	
Output Impedance	1.5	4		MΩ	
DC PSRR[2]		200		nA/V	PSRR measured with a change in AVDD
DYNAMIC PERFORMANCE[2]					
Output Current Settling Time		230		µs	25 mA step up or down, time to settle within a window of ±100 µA of final current
Output Current Settling Time (with HART® Slew Enabled)		55		ms	With HART slew enabled, 25 mA step up or step down, time to settle within a window of ±100 µA of final current
Noise					Measured at the I/OP_x screw terminal with 250 Ω load, 12.5 mA output
Output Noise		0.15		LSB p-p	0.1 Hz to 10 Hz bandwidth
Output Noise Spectral Density		2		nA/√Hz	Measured at 1 kHz, 12.5 mA output
AC PSRR		80		dB	Voltage on the supply at 1 kHz to the voltage across the 250 Ω.

[1] R_{SENSE} accuracy directly impacts the TUE and gain error.
[2] Guaranteed by design and characterization.

VOLTAGE INPUT

AVDD = 14 V to 28.8 V, AGND = DGND = 0 V, REFIN = 2.5 V (ideal), DVCC = 2.7 V to 5.5 V, IOVDD = 1.7 V to 5.5 V, and all specifications at T_A = −40°C to +105°C, unless otherwise noted. C_{LOAD} = 10 nF per recommended configuration.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE INPUT					
Input Resolution	16			Bits	
Input Range	0		10	V	
ACCURACY					
TUE	−0.1		+0.1	%FSR	
TUE at 25°C	−0.02		+0.02	%FSR	
INL	−4	±2	+4	LSB	
Offset Error	−4	±2	+4	LSB	
Offset Error at 25°C	−3		+3	LSB	
Gain Error	−700	±100	+700	ppm FSR	
Gain Error at 25°C	−330		+330	ppm FSR	
OTHER INPUT SPECIFICATIONS					
DC PSRR[1]		10		µV/V	
Normal Mode Rejection[1]		80		dB	50 Hz ± 1 Hz and 60 Hz ± 1 Hz
Input Bias Current	−100		+100	nA	As seen from the I/OP_x screw terminal, ADC is either idle or converting; 200 kΩ to GND is disabled (CH_200K_TO_GND bit = 0), does not include transient voltage suppressor (TVS) leakage
Input Bias Current at 25°C	−60	+15	+60	nA	
Input Resistance	175	195	215	kΩ	200 kΩ to GND enabled

[1] Guaranteed by design and characterization.

CURRENT INPUT EXTERNALLY POWERED AND CURRENT INPUT EXTERNALLY POWERED WITH HART

AVDD = 14 V to 28.8 V, AGND = DGND = 0 V, REFIN = 2.5 V (ideal), DVCC = 2.7 V to 5.5 V, IOVDD = 1.7 V to 5.5 V, and all specifications at T_A = −40°C to +105°C, unless otherwise noted. C_{LOAD} = 10 nF per recommended configuration. R_{SENSE} = 100 Ω (ideal). AGND − 0.5 V < I/OP_x screw terminal voltage < AVDD − 0.2 V.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT INPUT					
Input Resolution	16			Bits	
Input Range	0		25	mA	Sensed across the external 100 Ω resistor
Short-Circuit Current Limit	25		35	mA	Nonprogrammable
ACCURACY					
TUE[1]	−0.1		+0.1	%FSR	
TUE at 25°C[1]	−0.05		+0.05	%FSR	
INL	−10	±2	+10	LSB	Linearity specified from 0.1 mA to 25 mA
Offset Error	−5	±2	+5	LSB	
Offset Error at 25°C	−4		+4	LSB	
Gain Error[1]	−250	±200	+250	ppm FSR	
Gain Error at 25°C[1]	−250		+250	ppm FSR	
OTHER INPUT SPECIFICATIONS					
DC PSRR[2]		150		nA/V	
Input Impedance (Without HART Compatibility)		175		Ω	Current input, externally powered selected; including 100 Ω R_{SENSE}
Input Impedance (with HART Compatibility)	230		330	Ω	Current input, externally powered with HART selected; including 100 Ω R_{SENSE}
Compliance (Without HART Compatibility)	5.4			V	Current input, externally powered selected, minimum voltage required at the I/OP_x screw terminal to sink 25 mA
Compliance (with HART Compatibility)	7.0			V	Current input, externally powered with HART selected, minimum voltage required at the I/OP_x screw terminal to sink 20 mA

[1] R_{SENSE} accuracy directly impacts the TUE and gain error.
[2] Guaranteed by design and characterization.

CURRENT INPUT LOOP POWERED

AVDD = 14 V to 28.8 V, AGND = DGND = 0 V, REFIN = 2.5 V (ideal), DVCC = 2.7 V to 5.5 V, IOVDD = 1.7 V to 5.5 V, and all specifications at T_A = −40°C to +105°C, unless otherwise noted. C_{LOAD} = 10 nF per recommended configuration, R_{SENSE} = 100 Ω (ideal), AGND − 0.5 V < I/OP_x screw terminals voltage < AVDD − 0.2 V.

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT INPUTS					
Input Resolution	16			Bits	
Input Range	0		25	mA	Sensed across external 100 Ω resistor
Programmable Current Limit	0.5		24.5	mA	Typical programmable current limit, current input, loop powered enabled, 13-bit resolution
HART Mode Current Limit	23		30	mA	Current input, loop powered with HART enabled, nonprogrammable
ACCURACY					
TUE[1]	−0.1		+0.1	%FSR	
TUE at 25°C[1]	−0.05		+0.05	%FSR	
INL	−10	±2	+10	LSB	Linearity specified from 0.1 mA to 25 mA range
Offset Error	−5	±2	+5	LSB	
Offset Error at 25°C	−4		+4	LSB	
Gain Error[1]	−250	±200	+250	ppm FSR	
Gain Error at 25°C[1]	−250		+250	ppm FSR	
OTHER INPUT SPECIFICATIONS					
DC PSRR[2]		150		nA/V	
Input Impedance (Without HART Compatibility)		140		Ω	With current input, loop powered selected, includes 100 Ω R_{SENSE}
Input Impedance (with HART Compatibility)	230		315	Ω	With current input, loop powered with HART selected, includes 100 Ω R_{SENSE}
Headroom (Without HART Compatibility)	4.6			V	Minimum required difference between AVDD and the I/OP_x screw terminal voltage to source 25 mA; current input, loop powered selected
Headroom (with HART Compatibility)	6.7			V	Minimum required difference between AVDD and the I/OP_x screw terminal voltage to source 20 mA; current input, loop powered with HART selected

[1] R_{SENSE} accuracy directly impacts the TUE and gain error.
[2] Guaranteed by design and characterization.

RESISTANCE MEASUREMENT

AVDD = 14 V to 28.8 V, AGND = DGND = 0 V, REFIN = 2.5 V (ideal), DVCC = 2.7 V to 5.5 V, IOVDD = 1.7 V to 5.5 V, and all specifications at T_A = −40°C to +105°C, unless otherwise noted. R_{SENSE} = 100 Ω (ideal). External current limiting resistor of 2 kΩ (ideal) connected to the SENSEH_x pin.

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RESISTANCE MEASUREMENT					
Input Range	0		1	MΩ	2-wire RTD measurements supported
Bias Voltage		2.5		V	
Pull-Up Resistor ($R_{PULL-UP}$)		2.1		kΩ	$R_{PULL-UP}$ is comprised of the external 2 kΩ resistor and the external 100 Ω R_{SENSE}
ACCURACY					
Measurement Range					
0 Ω to 50 Ω			0.28	Ω	
50 Ω to 3 kΩ			±0.07%, ±0.23 Ω		±% of measured value plus ± fixed error
3 kΩ to 10 kΩ	−0.15	±0.1	+0.15	%	±% of measured value
10 kΩ to 200 kΩ	−3.0	±1.3	+3.0	%	±% of measured value
200 kΩ to 1 MΩ	−15	±6.0	+15	%	±% of measured value

DIGITAL INPUT LOGIC

AVDD = 14 V to 28.8 V, AGND = DGND = 0 V, REFIN = 2.5 V (ideal), DVCC = 2.7 V to 5.5 V, IOVDD = 1.7 V to 5.5 V, and all specifications at T_A = −40°C to +105°C, unless otherwise noted.

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL INPUTS					
Input Data Rate[1]		20		kHz	Unfiltered input, SENSEL_x pin driven by a low impedance source, 0 V to 10 V signal, duty cycle: 60:40
Maximum Input Voltage[1]			40	V	Limited by the TVS clamping voltage
Minimum Input Voltage[1]	−40				Limited by the TVS clamping voltage
CURRENT SINK					
Range 0					
Series Resistor Value		2.3		kΩ	
Current Sink Range	0		3.7	mA	Typical programmable current sink to AGND
Current Sink Resolution		120		µA	
Current Sink Accuracy		±2		%FSR	
Current Sink at Decimal Code 20	2.1	2.4		mA	Recommended for IEC61131-2 Type I and Type III for I/OP_x screw terminal > 6 V, DIN_SINK = decimal Code 20
Range 1					
Series Resistor Value		860		Ω	
Current Sink Range	0		7.4	mA	Typical programmable current sink to AGND
Current Sink Resolution		240		µA	
Current Sink Accuracy		±2		%FSR	
Current Sink at Decimal Code 29	6.1	7.0		mA	Recommended for IEC61131-2 Type I and Type III for I/OP_x screw terminal > 6 V, DIN_SINK = decimal Code 29
VOLTAGE THRESHOLDS MODES					
AVDD Threshold Mode					
Threshold Range	AVDD/60		AVDD × 59/60	V	Programmable trip level shared between all channels
Threshold Resolution		AVDD/30		V	
Hysteresis		AVDD/60		V	
Fixed Threshold Mode					
Threshold Range	0.5		16	V	Programmable trip level shared between all channels
Threshold Resolution		0.5		V	
Hysteresis		0.5		V	
Threshold Voltage at Decimal Code 16	8.2	8.5	8.8	V	Rising trip point, recommended for IEC61131-2 Type I, Type II, and Type III, COMP_THRESH bits = decimal Code 16
Threshold Accuracy		2		%FSR	

[1] Guaranteed by design and characterization.

DIGITAL INPUT LOOP POWERED

AVDD = 14 V to 28.8 V, AGND = DGND = 0 V, REFIN = 2.5 V (ideal), DVCC = 2.7 V to 5.5 V, IOVDD = 1.7 V to 5.5 V, and all specifications at T_A =−40°C to +105°C, unless otherwise noted.

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL INPUTS					
Input Data Rate[1]			5	kHz	Unfiltered input, typically dominated by wetting current, load capacitance, and threshold voltage
Dry Contact Wetting Current Range	0.5		24.5	mA	Loop powered, typical programmable current per channel
Headroom	4.6			V	Minimum required voltage difference between AVDD and the I/OP_x screw terminal to source 25 mA
THRESHOLD MODES					
AVDD Threshold Mode					
Threshold Range	AVDD/60		AVDD × 59/60	V	Programmable trip level shared by all channels
Threshold Resolution		AVDD/30		V	
Hysteresis		AVDD/60		V	
Fixed Threshold Mode					
Threshold Range	0.5		16	V	Programmable trip level shared by all channels
Threshold Resolution		0.5		V	
Hysteresis		0.5		V	
Threshold Accuracy		2		%FSR	

[1] Guaranteed by design and characterization.

ADC SPECIFICATIONS

AVDD = 14 V to 28.8 V, AGND = DGND = 0 V, REFIN = 2.5 V (ideal), DVCC = 2.7 V to 5.5 V, IOVDD = 1.7 V to 5.5 V, and all specifications at T_A =−40°C to +105°C, unless otherwise noted. AGND − 0.5 V < I/OP_x screw terminal voltage < AVDD − 0.2 V when measuring current by sensing voltage across R_{SENSE}.

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC SPECIFICATIONS					
Resolution	16			Bits	
No Missing Codes[1]	16			Bits	
Conversion Rates[1]					Sample rates vary depending on the number of channels selected and the use of single or continuous conversion modes.
		10		SPS	50 Hz and 60 Hz rejection enabled.
		20		SPS	50 Hz and 60 Hz rejection enabled.
		1.2		kSPS	50 Hz and 60 Hz rejection disabled.
		4.8		kSPS	50 Hz and 60 Hz rejection disabled.
Noise[1]					Refer to Table 19.
ADC INPUT RANGES					
0 V to 10 V					Typically used to measure voltage across I/OP_x to I/ON_x screw terminals (I/ON_x is the input/output negative, where x is the channel number).
Range	0		10	V	
TUE	−0.1	±0.02	+0.1	%FSR	
INL	−4	±2	+4	LSB	
Offset Error	−4	±2	+4	LSB	
Gain Error	−700	±100	+700	ppm FSR	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
0 V to 2.5 V					Typically used to measure the current flowing out of the AD74413R through the 100 Ω R_{SENSE} or RTD voltage measurements at the I/OP_x screw terminal.
Range	0		2.5	V	
TUE	−0.06	±0.02	+0.06	%FSR	
INL	−10	±2	+10	LSB	
Offset Error	−10	±4	+10	LSB	
Gain Error	−250	±200	+250	ppm FSR	
−2.5 V to 0 V					Typically used to measure the current flowing into the AD74413R across the 100 Ω R_{SENSE}.
Range	−2.5		0	V	
TUE	−0.06	±0.02	+0.06	%FSR	
INL	−10	±2	+10	LSB	
Offset Error	−10	±4	+10	LSB	
Gain Error	−250	±200	+250	ppm FSR	
−2.5 V to +2.5 V					Typically used to measure bidirectional current across 100 Ω sense resistor in voltage output mode.
Range	−2.5		+2.5	V	
TUE	−0.06	±0.02	+0.06	%FSR	
INL	−6	±1	+6	LSB	
Offset Error	−5	±2	+5	LSB	Measured at 0 V input voltage.
Gain Error	−250	±200	+250	ppm FSR	
±104.16 mV					Typically used for measuring thermocouple voltages in voltage input mode.
Range	−104.16		+104.16	mV	
TUE	−0.17	±0.05	+0.17	%FSR	
INL	−23	±5	+23	LSB	
Offset Error	−50	+10	+50	LSB	Measured at 0 V input voltage.
Gain Error	−1300	+200	+1300	ppm FSR	
DIAGNOSTICS SPECIFICATIONS					
LVIN Pin 2.5 V Range					
Range	0		2.5	V	
TUE	−0.025	±0.02	+0.025	%FSR	
INL	−8	±2	8	LSB	
Offset Error	−9	±2	+9	LSB	
Gain Error	−200	+50	+200	ppm FSR	
Noise[1]					Refer to 2.5 V range specifications in Table 19.
INTERNAL DIAGNOSTICS MEASUREMENTS					
Accuracy		±2		%	Percentage of measured value.
INTERNAL TEMPERATURE SENSOR[1]					
Junction Operating Temperature Range	−40		+125	°C	The 105°C maximum specified in the Ordering Guide refers to ambient temperature. However, the temperature sensor is specified to a die temperature of 125°C.
Accuracy		±5		°C	
Resolution		0.2		°C	

[1] Guaranteed by design and characterization; not production tested.

GENERAL SPECIFICATIONS

AVDD = 14 V to 28.8 V, AGND = DGND = 0 V, REFIN = 2.5 V (ideal), DVCC = 2.7 V to 5.5 V, IOVDD = 1.7 V to 5.5 V, and all specifications at T_A =−40°C to +105°C, unless otherwise noted.

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE SPECIFICATIONS					
Reference Input					
Reference Input Voltage	2.495	2.5	2.505	V	
DC Input Current	−1		+1	µA	
Reference Output					
Output Voltage	2.495	2.5	2.505	V	T_A = 25°C
Reference Temperature Coefficient[1]			15	ppm/°C	
Output Voltage Drift vs. Time[1]		-500		ppm FSR	Drift after 1000 hours, T_A = 85°C
Output Noise[1]		59		µV p-p	0.1 Hz to 10 Hz bandwidth.
Output Noise Spectral Density		2.3		µV/√Hz	Frequency = 1 kHz
Capacitive Load			100	nF	On REFOUT pin
Output Impedance		0.6		Ω	Sourcing or sinking up to 5 mA
Short Circuit		25		mA	
CHARGE PUMP					
Voltage		−DVCC		V	The charge pump generates a voltage that is equal to the negative of DVCC
Accuracy		±10		%	
Output Impedance		12.5		Ω	
CASCODE PINS					
Cascode Voltage	AVDD − 8	AVDD − 7	AVDD − 6	V	Channel output stage enabled, with decimal Code 0x000 loaded to the DAC
TEMPERATURE ALERT AND RESET[1]					Junction temperature
Temperature Alert		115		°C	Junction temperature, high temperature event flags the alert status and the $\overline{\text{ALERT}}$ pin (if unmasked)
Temperature Alert Accuracy		5		°C	
Temperature Reset		140		°C	Junction temperature, resets the device if over temperature event when EN_THERM_RST =1
Temperature Reset Accuracy		5		°C	
LOGIC INPUTS					SCLK, SDI, $\overline{\text{RESET}}$, $\overline{\text{SYNC}}$, $\overline{\text{LDAC}}$
Input Voltage					
High (V_{IH})	0.8 × IOVDD			V	IOVDD ≤ 2.7 V
	0.7 × IOVDD			V	IOVDD > 2.7 V
Low (V_{IL})			0.2 × IOVDD	V	IOVDD ≤ 2.7 V
			0.3 × IOVDD	V	IOVDD > 2.7 V
Input Current	−1		+1	µA	Per pin
Input Capacitance[1]		3		pF	Per pin
LOGIC OUTPUTS					
SDO Pin					
Output Voltage					
Low (V_{OL})			0.4	V	Sink current (I_{SINK}) = 200 µA
High (V_{OH})	IOVDD − 0.4			V	Source current (I_{SOURCE}) = 200 µA
High Impedance Leakage Current	−1		+1	µA	
GPO_x Pin					

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Output Voltage					
Low V_{OL}			0.4	V	I_{SINK} = 200 µA
		0.15	0.4	V	I_{SINK} = 3 mA for IOVDD > 2.7 V
High V_{OH}	IOVDD − 0.4			V	I_{SINK} = 200 µA
	IOVDD − 0.4			V	I_{SINK} = 3 mA for IOVDD > 2.7 V
Pull-Down Resistance		101		kΩ	
High Impedance Leakage Current	−1		+1	µA	
OPEN-DRAIN LOGIC OUTPUTS					$\overline{ADC_RDY}$, $\overline{ALERT}$
V_{OL}			0.4	V	10 kΩ pull-up resistor to IOVDD
			0.4	V	At 2.5 mA
High Impedance Leakage Current	−1		+1	V	
POWER SUPPLY MONITORS					
AVDD Threshold		9.5		V	
ALDO5V Threshold		4.1		V	
DVCC Threshold		2.0		V	
ALDO1V8 Threshold		1.4		V	
AVSS Threshold		−1.9		V	
POWER REQUIREMENTS					
Supply Voltages[1]					
AVDD	14	24	28.8	V	
DVCC	2.7	3.3	5.5	V	
IOVDD	1.7	DVCC	5.5	V	
Supply Quiescent Currents					
AVDD Current	10	13.5	18	mA	AD74413R powered up and in high-Z mode
	10	12.5	14	mA	Four channels configured in any output mode, no load current
	10	15	18	mA	Four channels configured in any input mode, no load current
DVCC Current	5.5	9.0	13.0	mA	AD74413R powered up and in high-Z mode
	8.5	10.5	12.5	mA	Four channels configured in any mode, no load current
IOVDD Current		15	100	µA	AD74413R powered up and in high-Z mode
CONFIGURATION TIMING					
Device Power-Up Time[1]		10		ms	After AVDD and DVCC power up
Device Reset Time[1]		1		ms	Time taken for device reset and calibration memory upload to complete hardware or software reset events after the device is powered up (see Table 11 for $\overline{RESET}$ pulse width specifications)
Use Case Switch Time[1]		130		µs	Time in use case before changing to another use case
Time in Use Case Before Loading DAC Codes[1]		150		µs	

[1] Guaranteed by design and characterization.

TIMING CHARACTERISTICS

SPI Timing Specifications

AVDD = 14 V to 28.8 V, AGND = DGND = 0 V, REFIN = 2.5 V internal or external, DVCC = 2.7 V to 5.5 V, IOVDD = 1.7 V to 5.5 V, and all specifications at T_A=−40°C to +105°C, unless otherwise noted.

Table 11.

Parameter[1, 2]	Description	IOVDD = 1.7 V to 2.7 V	IOVDD = 2.7 V to 5.5 V	Unit
t_1	SCLK pin cycle time	50	42	ns min
t_2	SCLK high time	20	17	ns min
t_3	SCLK low time	20	17	ns min
t_4	$\overline{\text{SYNC}}$ falling edge to SCLK falling edge setup time	25	21	ns min
t_5	Last SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	25	21	ns min
t_6	$\overline{\text{SYNC}}$ high time	650	650	ns min
t_7	Data setup time	5	5	ns min
t_8	Data hold time	5	5	ns min
t_9	$\overline{\text{RESET}}$ pulse width	50	50	µs min
		1	1	ms max
t_{10}	SCLK rising edge to SDO valid	39.5	23	ns max
t_{11}	$\overline{\text{SYNC}}$ falling edge to SDO valid (for readback MSB only)	34	15	ns max
t_{12}	$\overline{\text{SYNC}}$ rising edge to SDO tristate	15	14	ns min
t_{13}	$\overline{\text{LDAC}}$ pulse width ($\overline{\text{LDAC}}$ must not be pulsed low until after $\overline{\text{SYNC}}$ is returned high)	350	350	ns min
t_{14}	$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge	1	1	µs min
t_{15}	$\overline{\text{LDAC}}$ falling edge to DAC output response time	3	3	µs typ
t_{16}	$\overline{\text{SYNC}}$ rising edge to DAC output response time (when $\overline{\text{LDAC}}$ is 0)	3.5	3	µs typ
t_{17}[3]	$\overline{\text{ADC_RDY}}$ pulse	30	30	µs typ

[1] All input signals are specified with rise time (t_R) = fall time (t_F) = 5 ns (10% to 90% of the voltage on the IOVDD pin (V_{IOVDD})) and timed from a voltage level of V_{IOVDD}/2.
[2] Guaranteed by design and characterization; not production tested.
[3] t_{17} is not shown in Figure 2 because it is not an SPI timing specification. See Figure 52 for a diagram with the t_{17}.

Timing Diagrams

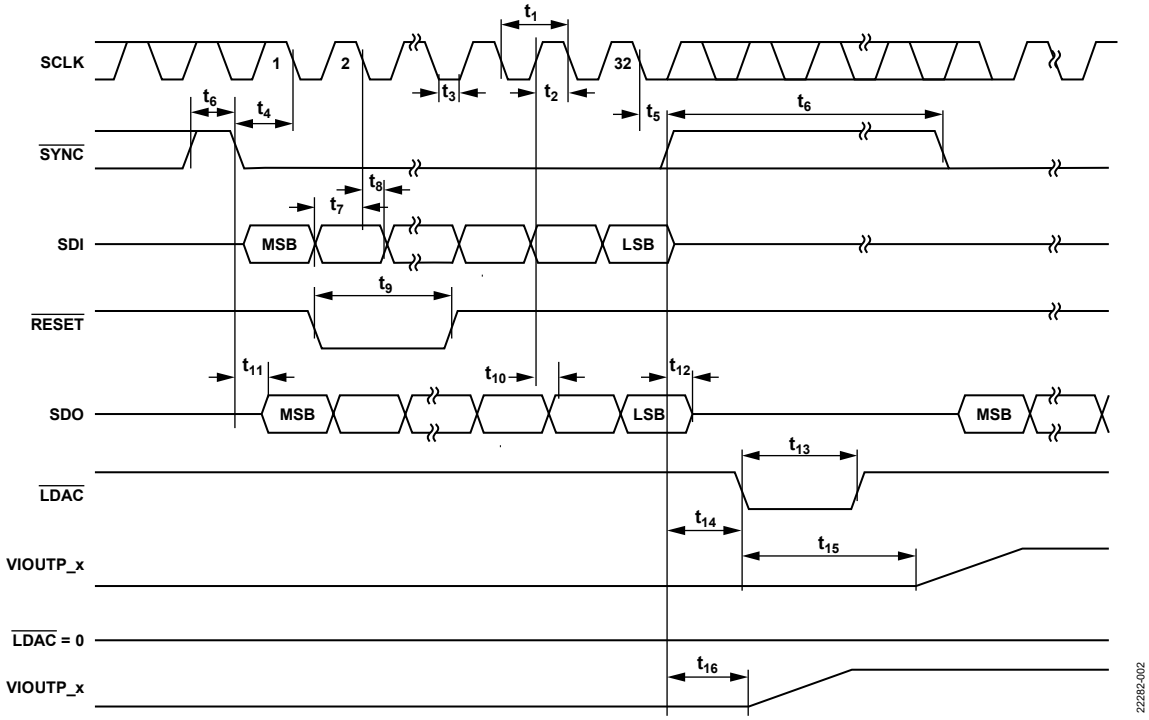


Figure 2. SPI Timing Diagram

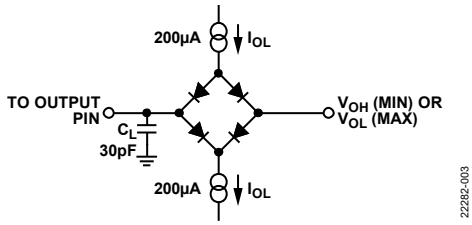


Figure 3. Load Circuit for Digital Output (SDO) Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.

With the recommended configuration, the I/OP_x screw terminal tolerates overvoltages to dc ± 40 V (limited by external TVS).

Table 12.

Parameter	Rating
AVDD to AGND	−0.3 V to +30 V
REFIN, REFOUT, LVIN to AGND	−0.3 V to +5 V
SENSEH_x[1], SENSEHF_x[1] SENSEL_x[1], SENSELF_x[1] to AGND	−50 V to +50 V
VIOUTP_x[1] to AGND	−50 V to AVDD + 0.3 V
VIOUTN_x[1] to AGND	AVSS − 0.3 V to +50 V
Digital Inputs to DGND ($\overline{\text{RESET}}$, $\overline{\text{SYNC}}$, SCLK, SDI, $\overline{\text{LDAC}}$)	−0.3 V to IOVDD + 0.3 V
Digital Outputs to DGND (GPO_x[1], SDO, $\overline{\text{ALERT}}$, $\overline{\text{ADC_RDY}}$)	−0.3 V to IOVDD + 0.3 V
DVCC, IOVDD to DGND	−0.3 V to +6.0 V
AGND_SENSE to AGND	−0.3 V to +0.3 V
DGND to AGND	−0.3 V to +0.3 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Reflow Profile	JEDEC industry standard J-STD-020
Junction Temperature (T_J Maximum)[2]	125°C
Power Dissipation	(T_J maximum − T_A)/θ_{JA}

[1] x = A, B, C, and D.

[2] It is important to manage the power dissipation of the AD74413R to ensure that the maximum junction temperature is not violated by using the recommended external field-effect transistor (FET). It is also recommended to enable the thermal shutdown function to avoid damage to the AD74413R.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the junction to ambient thermal resistance. θ_{JC} is the junction to case thermal resistance.

Table 13. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
CP-64-15	24.8	1.3	°C/W

[1] Based on simulated data using a JEDEC 2s2p thermal test board with a 7 × 7 array of thermal vias in a JEDEC natural convection environment. See JEDEC specification JESD-51 for details.

[2] Measured at exposed paddle surface with the cold plate in direct contact with the package top surface.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

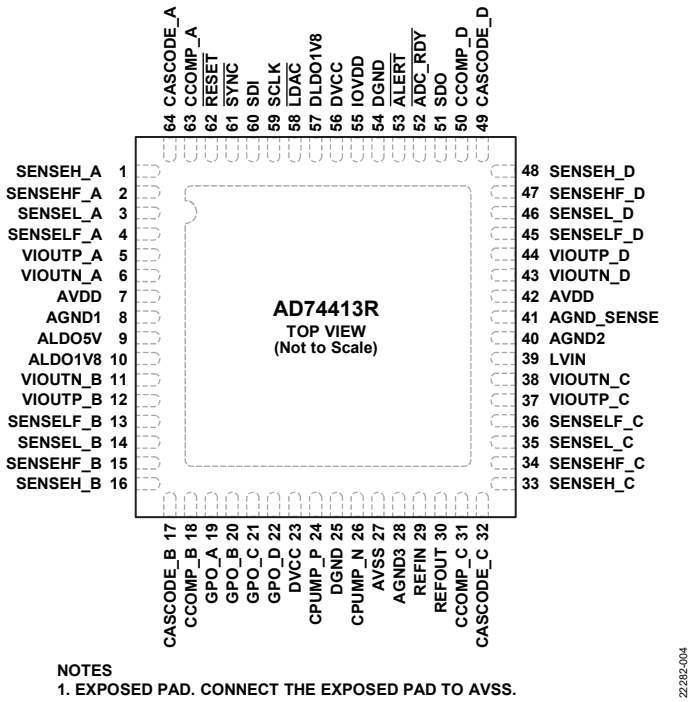


Figure 4. Pin Configuration

Table 14. Pin Function Description

Pin No.	Mnemonic	Description
1	SENSEH_A	High-Side Sense Pin on Channel A Closes Loop in Current Output Mode. This pin is routed to the AD74413R side of R_{SENSE}.
2	SENSEHF_A	Filtered High-Side Sense Pin on Channel A Can Be Switched to ADC Inputs. This pin is routed to the AD74413R side of R_{SENSE} through the off chip filter.
3	SENSEL_A	Low-Side Sense Pin on Channel A Closes Loop in Voltage and Current Output Modes. This pin is routed to the I/OP_x screw terminal side of R_{SENSE}.
4	SENSELF_A	Filtered Low-Side Sense Pin on Channel A Can Be Switched to ADC Inputs. This pin is routed to the I/OP_x screw terminal side of R_{SENSE} through the off chip filter.
5	VIOUTP_A	Voltage or Current High-Side Force Pin on Channel A. This pin operates in conjunction with the VIOUTN_A pin to provide a voltage or a current to the I/OP_x screw terminal.
6	VIOUTN_A	Voltage or Current Low-Side Force Pin on Channel A. This pin operates in conjunction with the VIOUTP_A pin to provide a voltage or a current to the I/OP_x screw terminal.
7	AVDD	Positive Analog Supply, 14 V to 28.8 V.
8	AGND1	Analog Ground.
9	ALDO5V	5 V Analog LDO Output. Decouple this pin with the recommended capacitor shown in Table 27. Do not use this pin externally.
10	ALDO1V8	1.8 V Analog LDO Output. Decouple this pin with the recommended capacitor shown in Table 27. Do not use this pin externally.
11	VIOUTN_B	Voltage or Current Low-Side Force Pin on Channel B. This pin operates in conjunction with the VIOUTP_B pin to provide a voltage or a current to the I/OP_x screw terminal.
12	VIOUTP_B	Voltage or Current High-Side Force Pin on Channel B. This pin operates in conjunction with the VIOUTN_B pin to provide a voltage or a current to the I/OP_x screw terminal.
13	SENSELF_B	Filtered Low-Side Sense Pin on Channel B Can Be Switched to ADC Inputs. This pin is routed to the I/OP_x screw terminal side of R_{SENSE} through the off chip filter.
14	SENSEL_B	Low-Side Sense Pin on Channel B Closes Loop in Voltage and Current Output Modes. This pin is routed to the I/OP_x screw terminal side of R_{SENSE}.
15	SENSEHF_B	Filtered High-Side Sense Pin on Channel B Can Be Switched to ADC Inputs. This pin is routed to the AD74413R side of R_{SENSE} through the off chip filter.
16	SENSEH_B	High-Side Sense Pin on Channel B Closes Loop in Current Output Mode. This pin is routed to the AD74413R side of R_{SENSE}.

Pin No.	Mnemonic	Description
17	CASCODE_B	Gate Drive Pin for Optional External Power Dissipating FET on Channel B. Leave this pin disconnected if not using this FET.
18	CCOMP_B	Compensation Capacitor Pin for Channel B. This pin allows the AD74413R to drive high capacitive loads in the voltage output use case. Connect the capacitor between the CCOMP_B pin and the I/OP_B screw terminal side of R_{SENSE}.
19	GPO_A	General-Purpose Digital Output Pin A. This pin can monitor the digital input comparator output.
20	GPO_B	General-Purpose Digital Output Pin B. This pin can monitor the digital input comparator output.
21	GPO_C	General-Purpose Digital Output Pin C. This pin can monitor the digital input comparator output.
22	GPO_D	General-Purpose Digital Output Pin D. This pin can monitor the digital input comparator output.
23	DVCC	Digital Supply, 2.7 V to 5.5 V. Decouple this pin with the recommended capacitor shown in Table 27.
24	CPUMP_P	Charge Pump Fly Capacitor Terminal. Connect the recommended fly capacitor between the CPUMP_P pin and the CPUMP_N pin.
25	DGND	Digital Ground.
26	CPUMP_N	Charge Pump Fly Capacitor Terminal. Connect the recommended fly capacitor between the CPUMP_P pin and the CPUMP_N pin.
27	AVSS	Charge Pump Output Voltage (Equal to Negative DVCC). Do not use this pin externally.
28	AGND3	Analog Ground.
29	REFIN	2.5 V Reference Input.
30	REFOUT	Internal 2.5 V Reference Output. This pin must be connected to the REFIN pin to use the internal reference.
31	CCOMP_C	Compensation Capacitor Pin for Channel C. This pin allows the AD74413R to drive high capacitive loads in the voltage output use case. Connect the capacitor between the CCOMP_C pin and the I/OP_C screw terminal side of R_{SENSE}.
32	CASCODE_C	Gate Drive Pin for Optional External Power Dissipating FET on Channel C. Leave this pin disconnected if not using this FET.
33	SENSEH_C	High-Side Sense Pin on Channel C Closes Loop in Current Output Mode. This pin is routed to the AD74413R side of R_{SENSE}.
34	SENSEHF_C	Filtered High-Side Sense Pin on Channel C Can Be Switched to ADC Inputs. This pin is routed to the AD74413R side of R_{SENSE} through the off chip filter.
35	SENSEL_C	Low-Side Sense Pin on Channel C Closes Loop in Voltage and Current Output Modes. This pin is routed to the I/OP_x screw terminal side of R_{SENSE}.
36	SENSELF_C	Filtered Low-Side Sense Pin on Channel C Can Be Switched to ADC Inputs. This pin is routed to the I/OP_x screw terminal side of R_{SENSE} through the off chip filter.
37	VIOUTP_C	Voltage or Current High-Side Force Pin on Channel C. This pin operates in conjunction with the VIOUTN_C pin to provide a voltage or a current to the I/OP_x screw terminal.
38	VIOUTN_C	Voltage or Current Low-Side Force Pin on Channel C. This pin operates in conjunction with the VIOUTP_C pin to provide a voltage or a current to the I/OP_x screw terminal.
39	LVIN	Low Voltage Input Pin. The voltage on this pin can be measured by selecting the LVIN option in the diagnostics block. The measurement voltage range is 0 V to 2.5 V. For best performance, use an antialiasing filter on this pin.
40	AGND2	Analog Ground.
41	AGND_SENSE	Analog Ground Sense. Tie this pin to the I/ON_x screw terminal.
42	AVDD	Positive Analog Supply, 14 V to 28.8 V.
43	VIOUTN_D	Voltage or Current Low-Side Force Pin on Channel D. This pin operates in conjunction with the VIOUTP_D pin to provide a voltage or a current to the I/OP_x screw terminal.
44	VIOUTP_D	Voltage or Current High-Side Force Pin on Channel D. This pin operates in conjunction with the VIOUTN_D pin to provide a voltage or a current to the I/OP_x screw terminal.
45	SENSELF_D	Filtered Low-Side Sense Pin on Channel D Can Be Switched to ADC Inputs. This pin is routed to the I/OP_x screw terminal side of R_{SENSE} through the off chip filter.
46	SENSEL_D	Low-Side Sense Pin on Channel D Closes Loop in Voltage and Current Output Modes. This pin is routed to the I/OP_x screw terminal side of R_{SENSE}.
47	SENSEHF_D	Filtered High-Side Sense Pin on Channel D Can Be Switched to ADC Inputs. This pin is routed to the AD74413R side of R_{SENSE} through the off chip filter.
48	SENSEH_D	High-Side Sense Pin on Channel D Closes Loop in Current Output Mode. This pin is routed from the AD74413R side of R_{SENSE}.
49	CASCODE_D	Gate Drive Pin for Optional External Power Dissipating FET on Channel D. Leave this pin disconnected if not using this FET.

Pin No.	Mnemonic	Description
50	CCOMP_D	Compensation Capacitor Pin for Channel D. This pin allows the AD74413R to drive high capacitive loads in the voltage output use case. Connect the capacitor between the CCOMP_D pin and the I/OP_D screw terminal side of R_{SENSE}.
51	SDO	Serial Interface Data Out.
52	$\overline{\text{ADC_RDY}}$	Active Low, Open-Drain Output. This pin asserts when a new sequence of ADC conversion results is ready to be read. Connect this pin to a pull-up resistor to the IOVDD pin.
53	$\overline{\text{ALERT}}$	Active Low, Open-Drain Output. This pin asserts low when an alert condition occurs. Read the ALERT_STATUS register when this pin is asserted. Connect this pin to the IOVDD pin via a pull-up resistor.
54	DGND	Digital Ground.
55	IOVDD	Digital Input/Output Supply, 1.7 V to 5.5 V
56	DVCC	Digital Supply, 2.7 V to 5.5 V.
57	DLDO1V8	1.8 V Digital LDO Output. Decouple with the recommended capacitor shown in Table 27. Do not use this pin externally.
58	$\overline{\text{LDAC}}$	Load DAC Pin. Active low input. Drive this pin low to update all four DACs in parallel. This pin can be tied permanently low if simultaneous updates are not required.
59	SCLK	Serial Interface Clock.
60	SDI	Serial Interface Data In.
61	$\overline{\text{SYNC}}$	Serial Interface Frame Synchronization Pin. Active low input.
62	$\overline{\text{RESET}}$	Hardware Reset Pin. Active low input. This pin resets the AD74413R to the power-on state.
63	CCOMP_A	Compensation Capacitor Pin for Channel A. This pin allows the AD74413R to drive high capacitive loads in the voltage output use case. Connect the capacitor between the CCOMP_A pin and the I/OP_A screw terminal side of R_{SENSE}.
64	CASCODE_A	Gate Drive Pin for Optional External Power Dissipating FET on Channel A. Leave this pin disconnected if not using this FET.
	Exposed Pad	Exposed Pad. Connect the exposed pad to the AVSS pin.

TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE OUTPUT

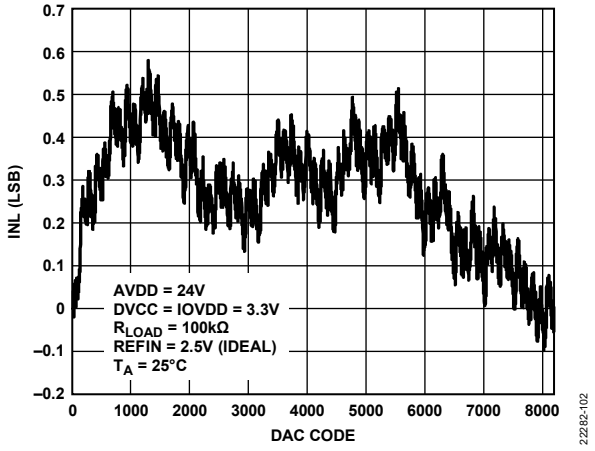


Figure 5. INL vs. DAC Code

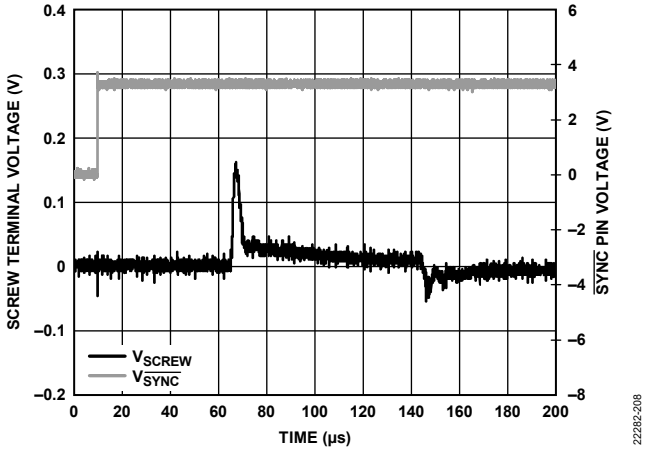


Figure 8. Screw Terminal Voltage (V_{SCREW}) and $\overline{SYNC}$ Pin Voltage ($V_{\overline{SYNC}}$) vs. Time on Voltage Output Enable

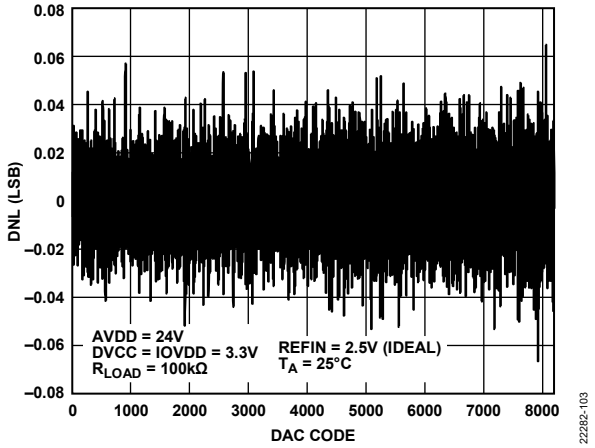


Figure 6. DNL vs. DAC Code

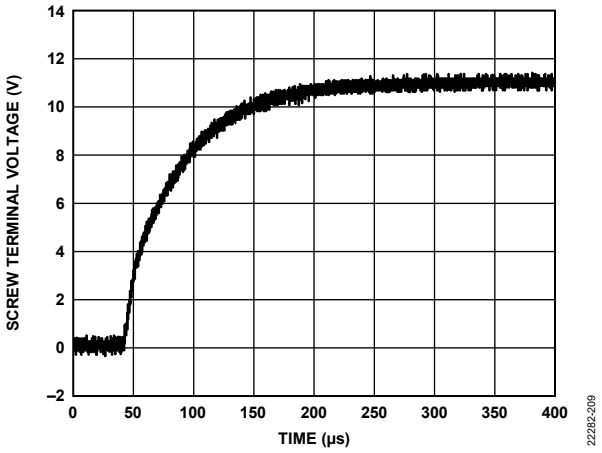


Figure 9. Full-Scale Positive Step

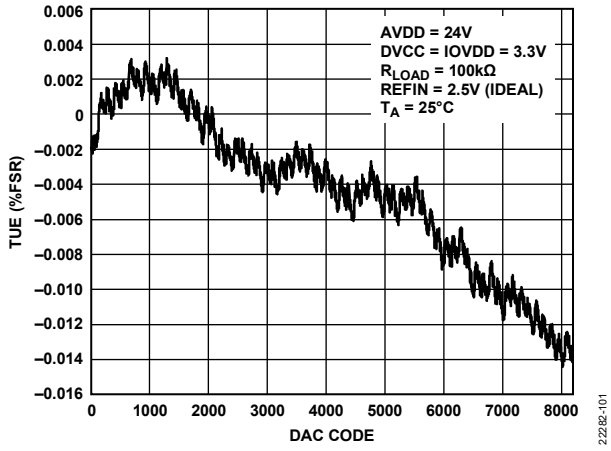


Figure 7. TUE vs. DAC Code

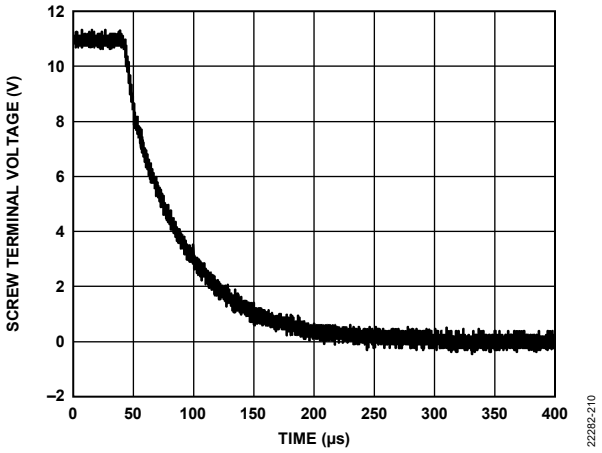


Figure 10. Full-Scale Negative Step

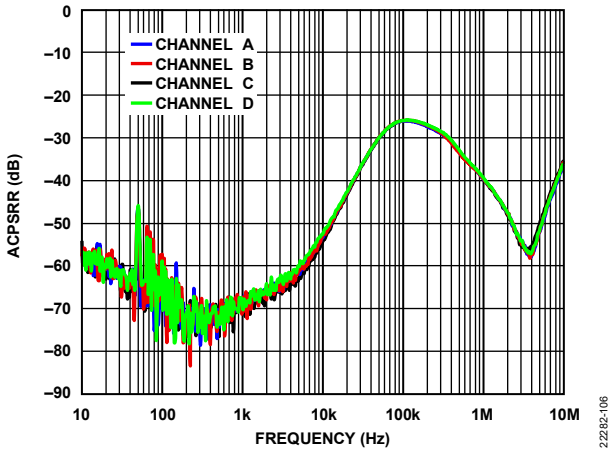


Figure 11. AC PSRR vs. Frequency

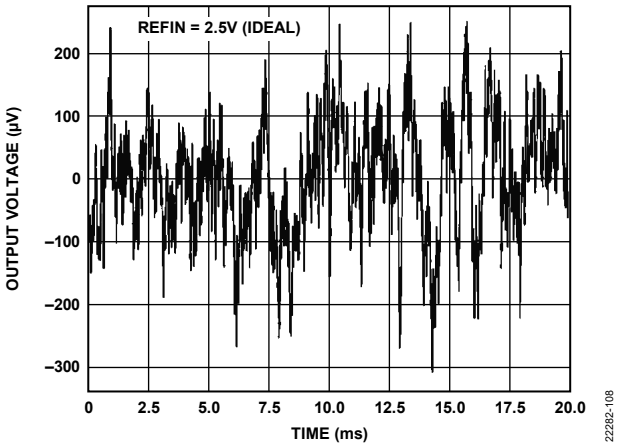


Figure 13. Peak-to-Peak Noise (100 kHz Bandwidth)

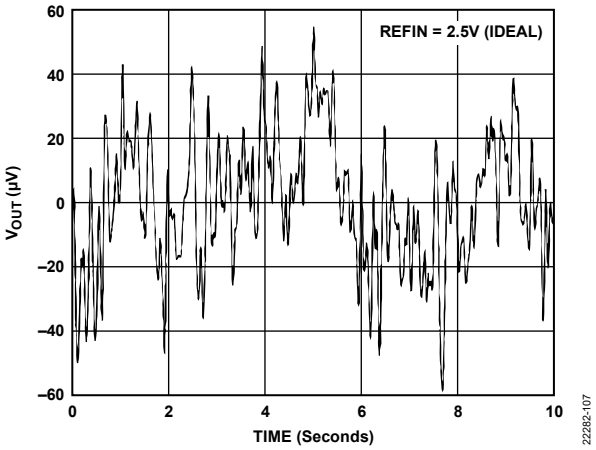


Figure 12. Peak-to-Peak Noise (0.1 Hz to 10 Hz Bandwidth)

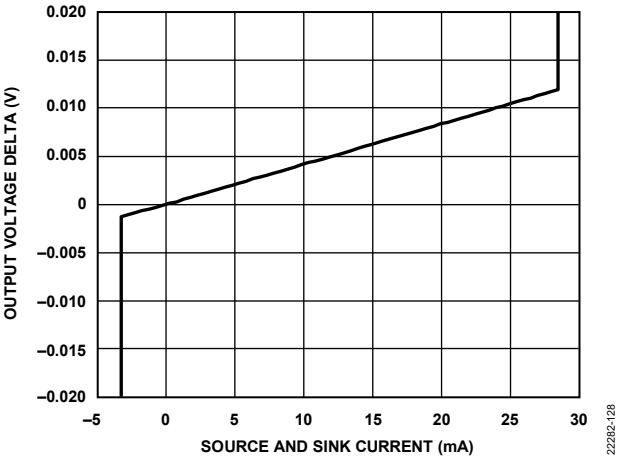


Figure 14. Output Voltage (V_{OUT}) Source and Sink Capability

CURRENT OUTPUT

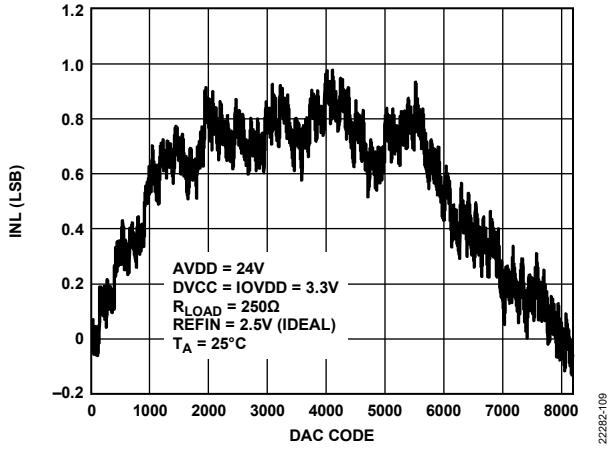


Figure 15. INL vs. DAC Code

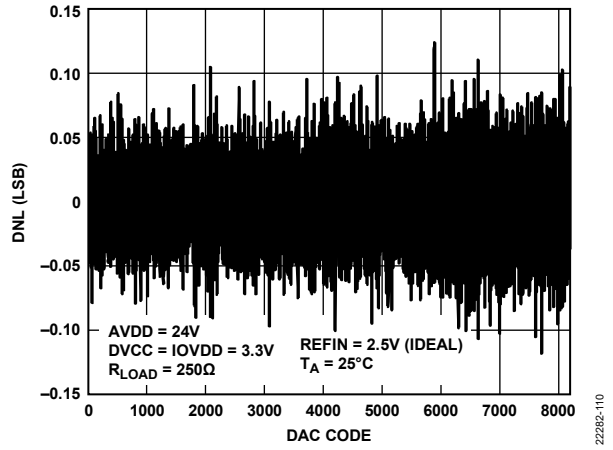


Figure 16. DNL vs. DAC Code

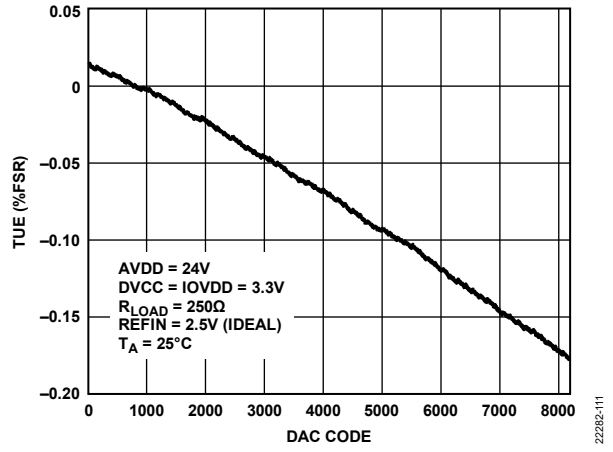


Figure 17. TUE vs. DAC Code

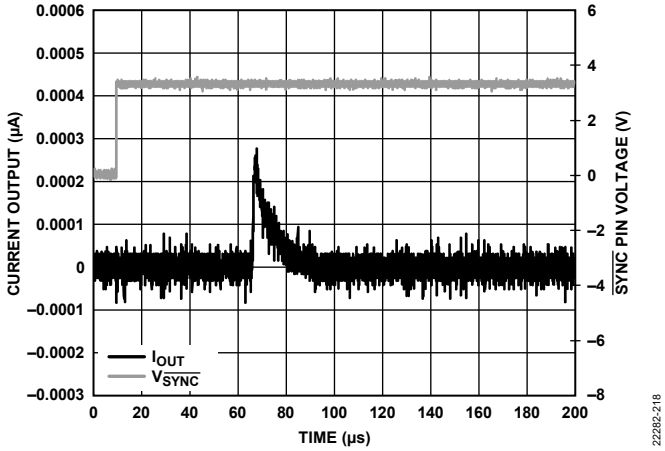


Figure 18. Current Output (I_{OUT}) and $\overline{SYNC}$ Pin Voltage ($V_{\overline{SYNC}}$) vs. Time on Output Enable

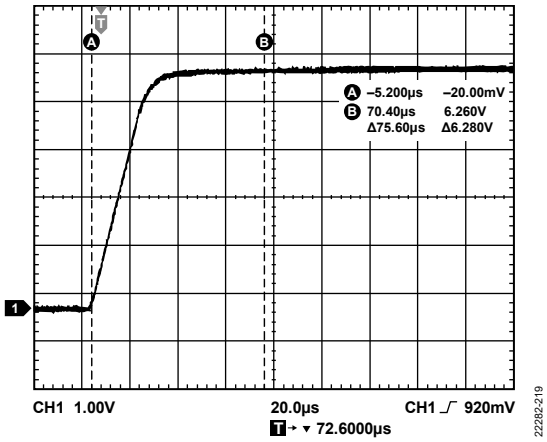


Figure 19. I_{OUT} Settling Time

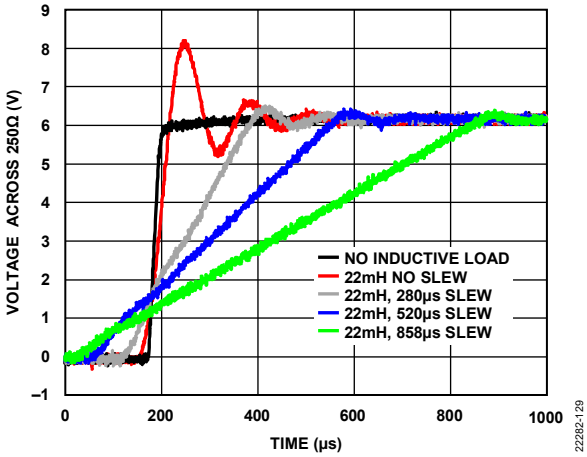


Figure 20. I_{OUT} Settling Time with Inductive Load With and Without Slew Rate Enabled

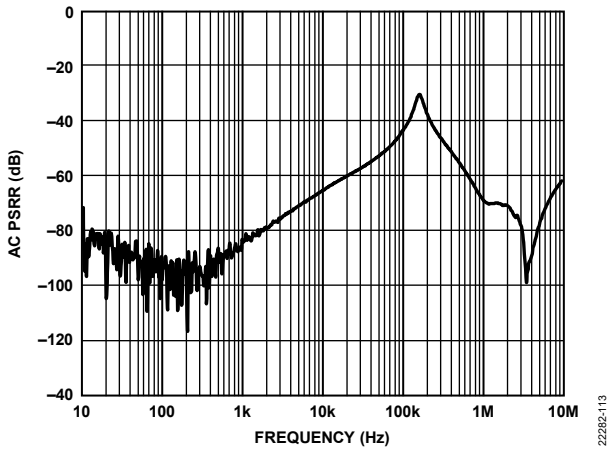


Figure 21. AC PSRR vs. Frequency

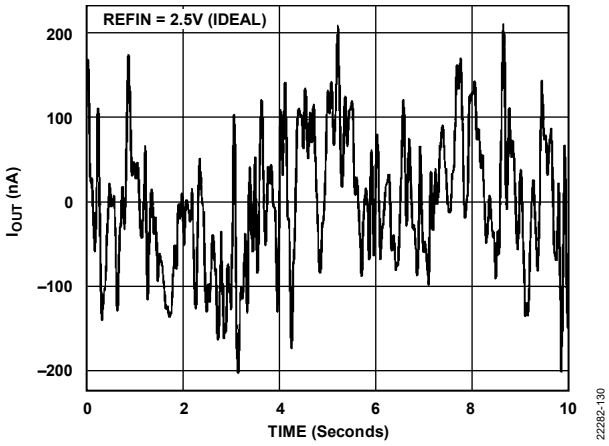


Figure 23. Peak-to-Peak Noise (0.1 Hz to 10 Hz Bandwidth)

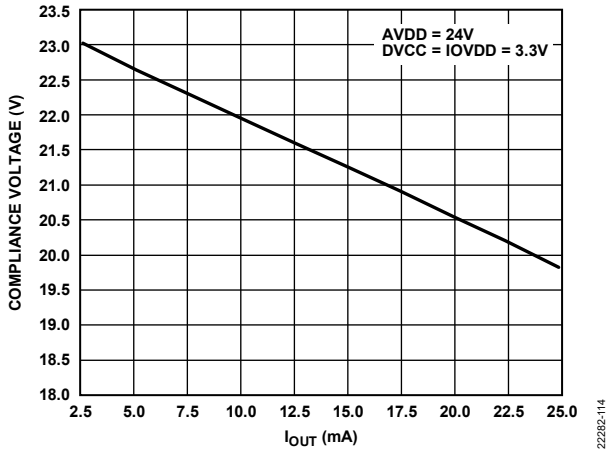


Figure 22. Compliance Voltage vs. I_{OUT}

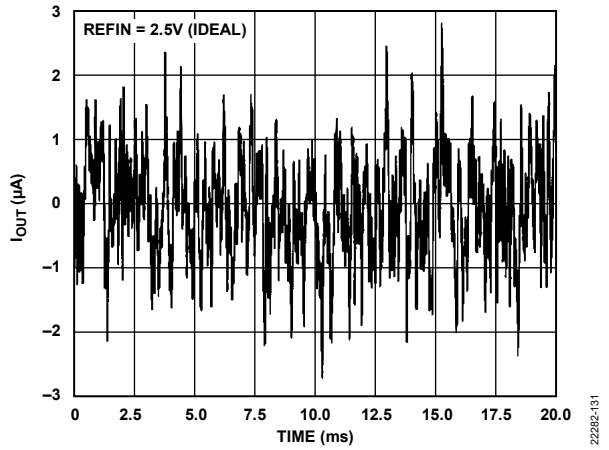


Figure 24. Peak-to-Peak Noise (100 kHz Bandwidth)

DIGITAL INPUT

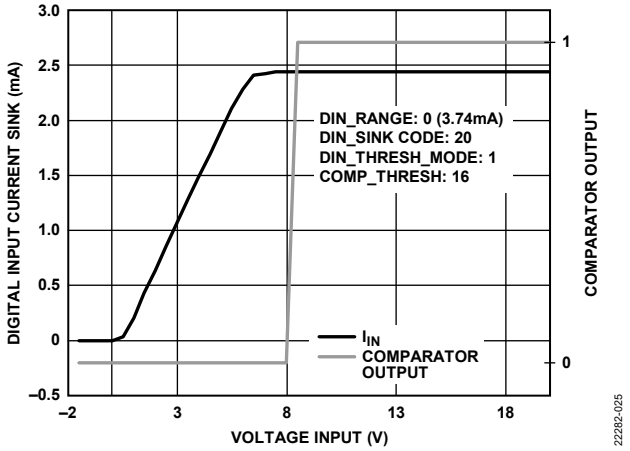


Figure 25. Digital Input Current Sink vs. Voltage Input for IEC 61131-2, Type I and Type III

RESISTANCE MEASUREMENT

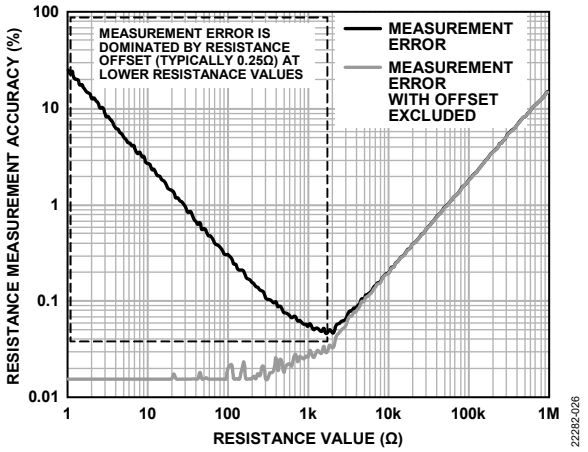


Figure 26. Resistance Measurement Accuracy vs Resistance Value

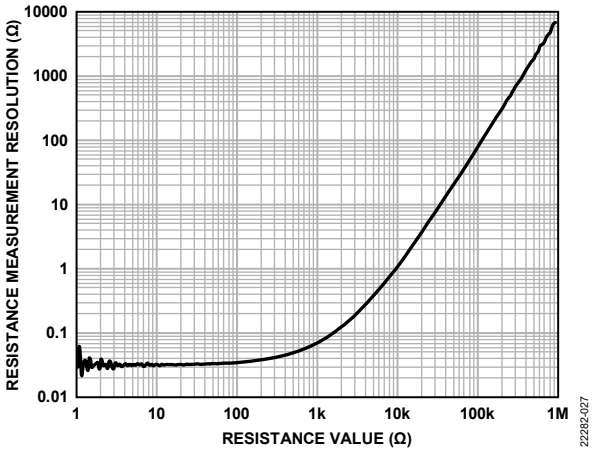


Figure 27. Resistance Measurement Resolution vs Resistance Value

REFERENCE

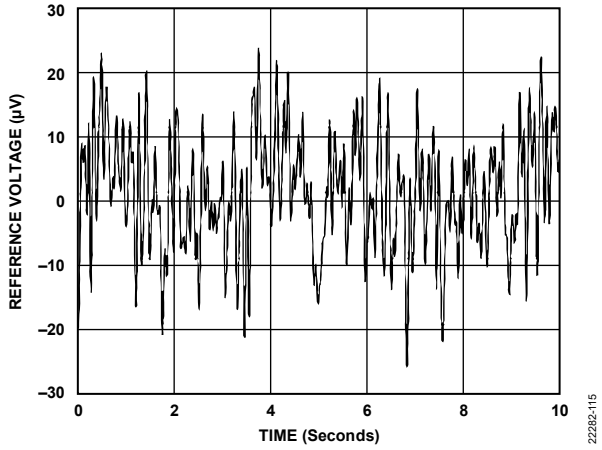


Figure 28. Peak-to-Peak Noise (0.1 Hz to 10 Hz Bandwidth)

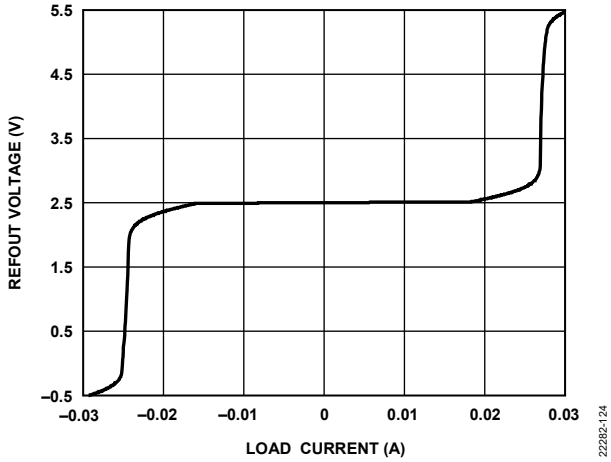


Figure 30. REFOUT Voltage vs. Load Current

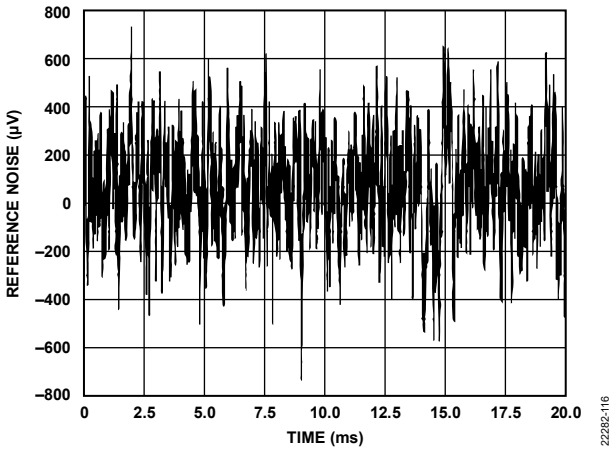


Figure 29. Peak-to-Peak Noise (100 kHz Bandwidth)

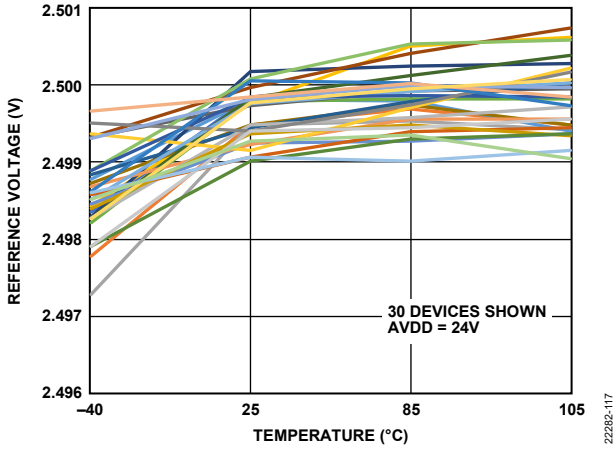


Figure 31. Reference Voltage vs. Temperature

ADC

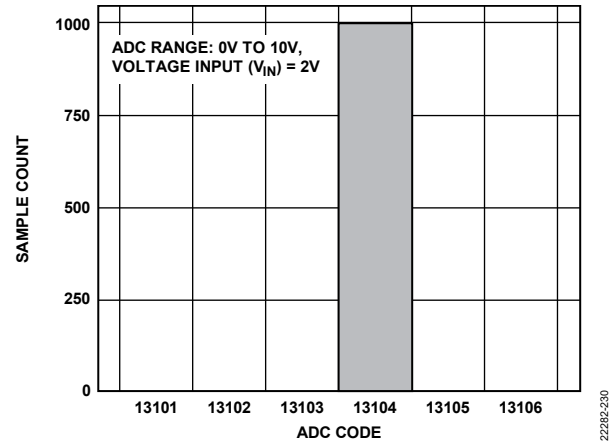


Figure 32. ADC Noise Histogram with Output Data Rate (ODR) = 10 SPS

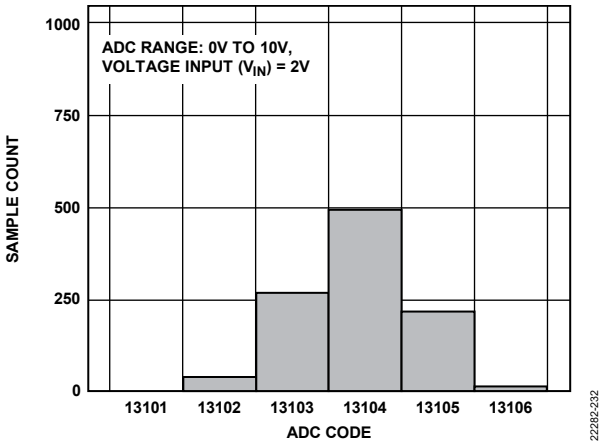


Figure 34. ADC Noise Histogram with ODR = 1.2 kSPS

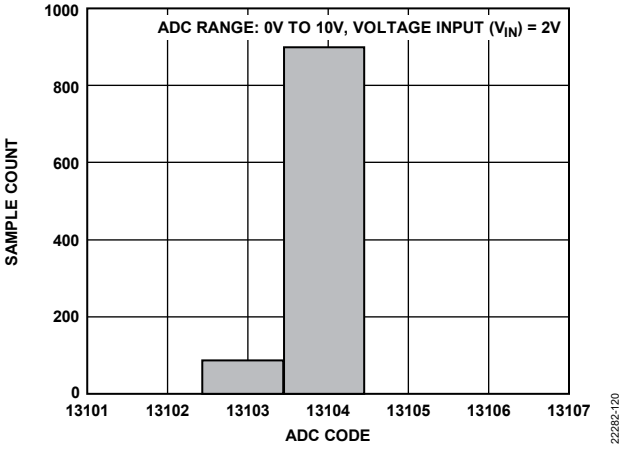


Figure 33. ADC Noise Histogram with ODR = 20 SPS

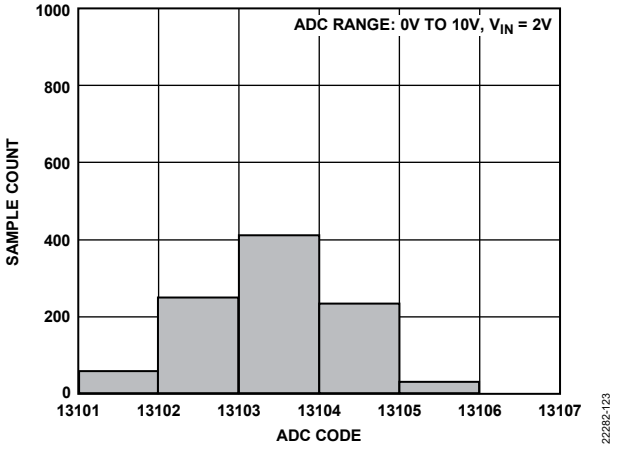


Figure 35. ADC Noise Histogram with ODR = 4.8 kSPS

SUPPLIES

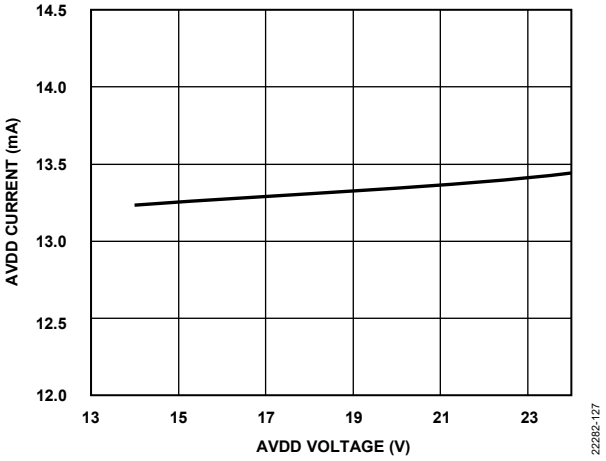


Figure 36. AVDD Current vs. AVDD Voltage

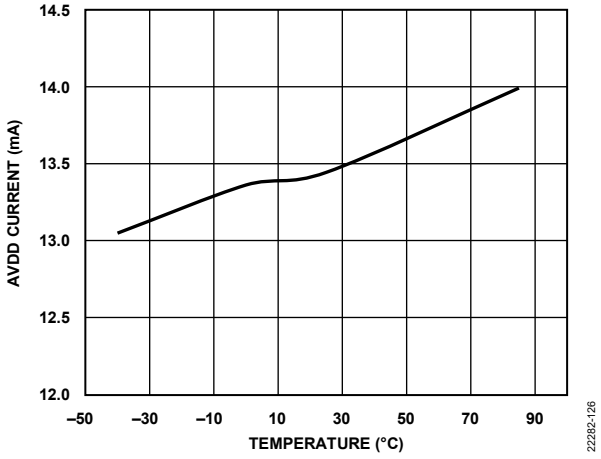


Figure 38. AVDD Current vs. Temperature

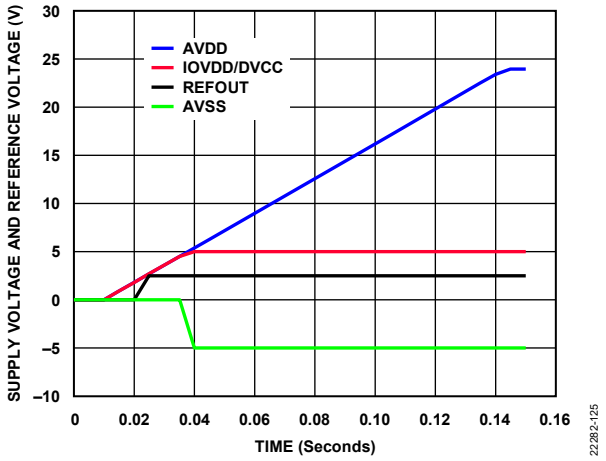


Figure 37. Supply Voltage and Reference Voltage vs. Time on Power-Up

THEORY OF OPERATION

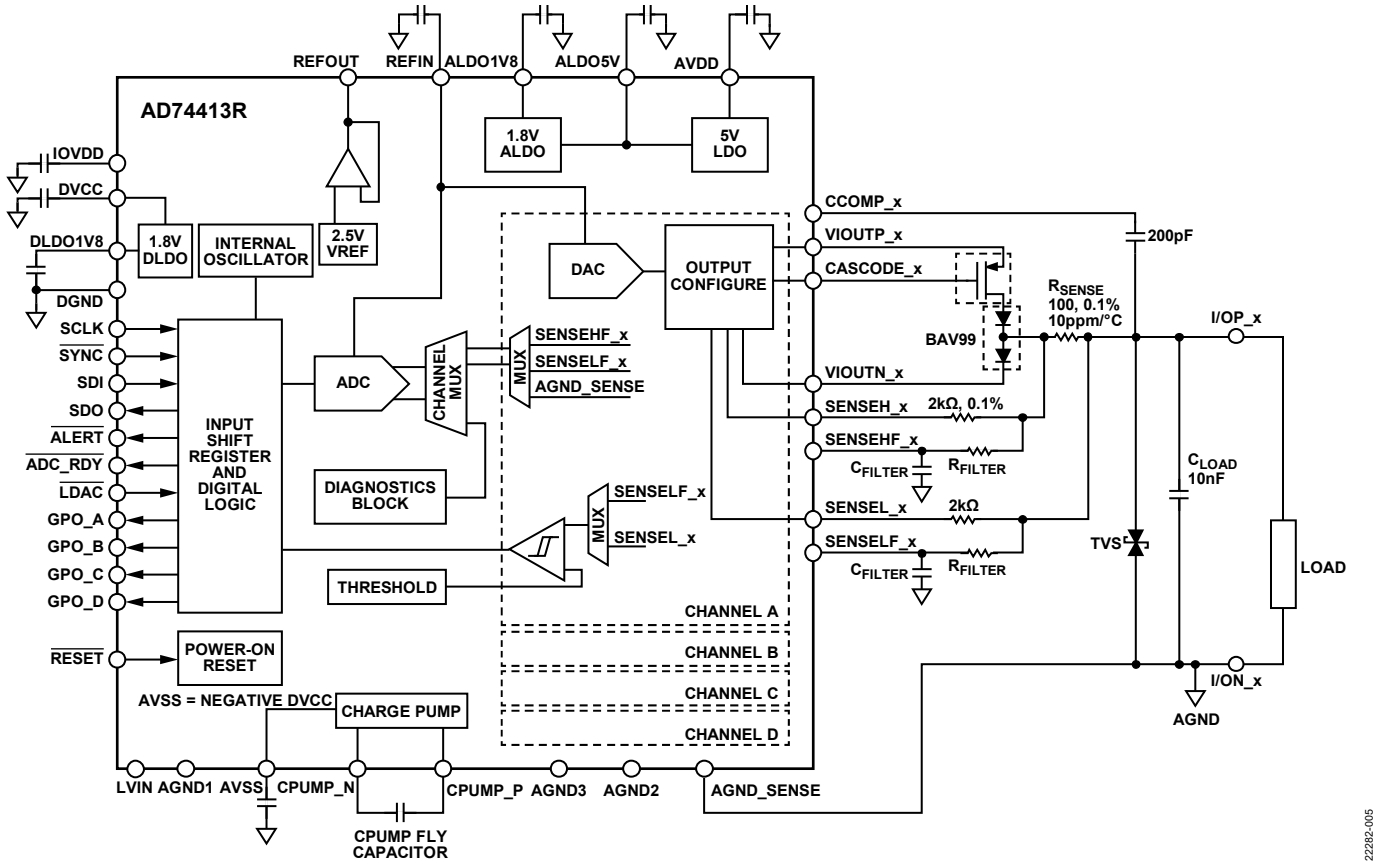


Figure 39. Detailed Functional Block Diagram

The AD74413R is a quad-channel software configurable input/output designed to meet the requirements of process control, factory automation, and building control applications. The device provides a fully integrated single chip solution for input and output operation. The AD74413R features a 16-bit, Σ-Δ ADC and multiple DACs, and the device is packaged in a 9 mm × 9 mm, 64-lead LFCSP. The four channels are configured by writing to the configuration registers. Users can refine the default configurations of each operation mode via the AD74413R register map (see Table 28). Refer to Figure 39 for a detailed functional block diagram of the AD74413R.

ROBUST ARCHITECTURE

The AD74413R system is robust in noisy environments and can withstand overvoltage scenarios such as miswire and surge events.

On-chip line protectors ensure that the I/OP_x screw terminals do not provide power to the IC when brought to a higher potential than the AVDD pin.

The recommended external components shown in Figure 39 and Table 27, including the TVS, are selected to withstand surge on the input/output terminals.

With the recommended components, the I/OP_x and I/ON_x screw terminals tolerate overvoltages up to dc ± 40 V (limited by the external TVS).

A cyclic redundancy check (CRC) function is built into the SPI interface to ensure error free communications in noisy environments.

SERIAL INTERFACE

The AD74413R is controlled over a versatile 4-wire serial interface that operates at clock speeds of up to 24 MHz (refer the t_1 parameter in Table 11) and is compatible with SPI, QSPI™, MICROWIRE™, and DSP standards. Data coding is always straight binary.

DAC ARCHITECTURE

The AD74413R contains four 13-bit DACs, one per channel. Each DAC core is a 13-bit string DAC. The architecture structure consists of a string of resistors, each with a value of R. The digital input code that is loaded to the DAC_CODEx registers determines which node on the string the voltage is tapped off from and fed into the output amplifier. This architecture is inherently monotonic and linear.

ADC OVERVIEW

The AD74413R provides the user with a single multichannel multiplexer and a single, 16-bit Σ-Δ ADC. The channel multiplexer selects which of the four channels the ADC measures. The ADC can measure either the voltage across the 100 Ω R_{SENSE} or the voltage at the I/OP_x screw terminal of each channel. The ADC also provides diagnostic information on user-selectable inputs such as supplies, internal die temperature, reference, and regulators. The ADC contains a 50 Hz and 60 Hz rejection filter that the user can enable.

REFERENCE

The AD74413R can operate with either an external or an internal reference. The reference input requires 2.5 V for the AD74413R to function correctly. The reference voltage is internally buffered before being applied to the DAC and the ADC. If using the internal reference, the REFIN pin must be tied to the REFOUT pin.

Reference Noise

It is recommended to decouple the reference voltage with a 100 nF capacitor. The reference specifications are generated assuming this 100 nF configuration.

Users can reduce the reference noise with the following additional external components:

- No resistor, 100 nF capacitor (default)
- 10 kΩ, 100 nF capacitor
- 10 kΩ, 1 µF capacitor

The reference power-on time is affected by the selection of additional external components.

Charge Pump

The AD74413R has an internal charge pump that provides a negative voltage that enables the AD74413R to force out 0 V while sinking current in voltage output mode. For correct operation, the charge pump requires an external capacitor (CPUMP fly capacitor in Figure 40) between the CPUMP_N pin and the CPUMP_P pin. Note that the AVSS pin cannot drive external circuitry.

POWER-ON STATE OF THE AD74413R

Upon initial power-up or a device reset of the AD74413R, the output channels are disabled and placed in a high impedance state by default.

DEVICE FUNCTIONS

The following sections describe the various programmable device functions of the AD74413R with block diagrams and guidelines on how to interpret the ADC results if converting with the default settings. These functions are programmed within the CH_FUNC_SETUPx registers.

Each device function is configured with default measurement settings. However, users can adjust these settings as required within the register map (see Table 28).

High Impedance

High impedance is the default function upon power-up or after a device reset. All channels are high impedance.

The CASCODE_x pins are pulled to ground via a 100 µA current sink to ground.

The CCOMP_x pins have a 40 kΩ resistor and a Zener diode in parallel to ground.

If a channel is held in high impedance for an extended time, such as when the channel is not in use, it is recommended to enable the 200 kΩ resistor to ground. Enable the 200 kΩ resistor by setting the CH_200K_TO_GND bit in the ADC_ CONFIGx registers.

Interpreting ADC Data

In high impedance mode, the ADC, by default, measures the voltage across the screw terminals (I/OP_x to I/ON_x) in a 0 V to 10 V range. Use the following equation to calculate the ADC measurement result:

$$V_{ADC} = (ADC_CODE/65{,}535) \times Voltage\ Range$$

where:
V_{ADC} is the measured voltage in volts.
ADC_CODE is the value of the ADC_RESULTx registers.
Voltage Range is the measurement range of the ADC and is 10 V.

Voltage Output Mode

The voltage output amplifier can generate unipolar voltages up to 11 V. An internal low voltage charge pump allows the amplifier to generate a true zero output voltage. The voltage on the low-side of the R_{SENSE} is sensed on the SENSEL_x pin via a 2 kΩ resistor, which closes the feedback loop and maintains stability.

The short-circuit limit in voltage output mode is programmable per channel. The circuit minimizes glitching on the I/OP_x screw terminal when the AVDD supply (V_{AVDD}) is ramping or when the use case configuration is changed.

Figure 40 shows the current, voltage, and measurement paths of the voltage output mode.

Voltage Output Short-Circuit Protection

The short-circuit limit for the voltage output mode of the AD74413R is typically 29 mA per channel when sourcing current. To provide flexibility for the user, a lower short-circuit limit of typically 7 mA can be selected per channel by setting the I_LIMIT bit in the OUTPUT_CONFIGx registers. The current limit for when the AD74413R is sinking current is typically 3.8 mA. If the selected short-circuit limit is reached on a channel, a voltage output short-circuit error is flagged for that channel and the $\overline{\text{ALERT}}$ pin asserts.

Interpreting ADC Data

In voltage output mode, the ADC, by default, measures the current through the R_{SENSE} in a −25 mA to +25 mA range. Use the ADC measurement result to calculate the current through the R_{SENSE} with the following equation:

$$I_{R_{SENSE}} = \frac{\left(V_{MIN} + \left(\left(\frac{ADC_CODE}{65{,}535}\right) \times Voltage\ Range\right)\right)}{R_{SENSE}}$$

where:

$I_{R_{SENSE}}$ is the measured current in amps. A negative current indicates the current is sourced from the AD74413R. A positive current indicates that the AD74413R is sinking the current.
V_{MIN} is the minimum voltage of the selected ADC range, which is −2.5 V by default.
ADC_CODE is the value of the ADC_RESULTx registers.
Voltage Range is the full span of the ADC range, which is 5 V.
R_{SENSE} is the R_{SENSE} resistor, which is 100 Ω.

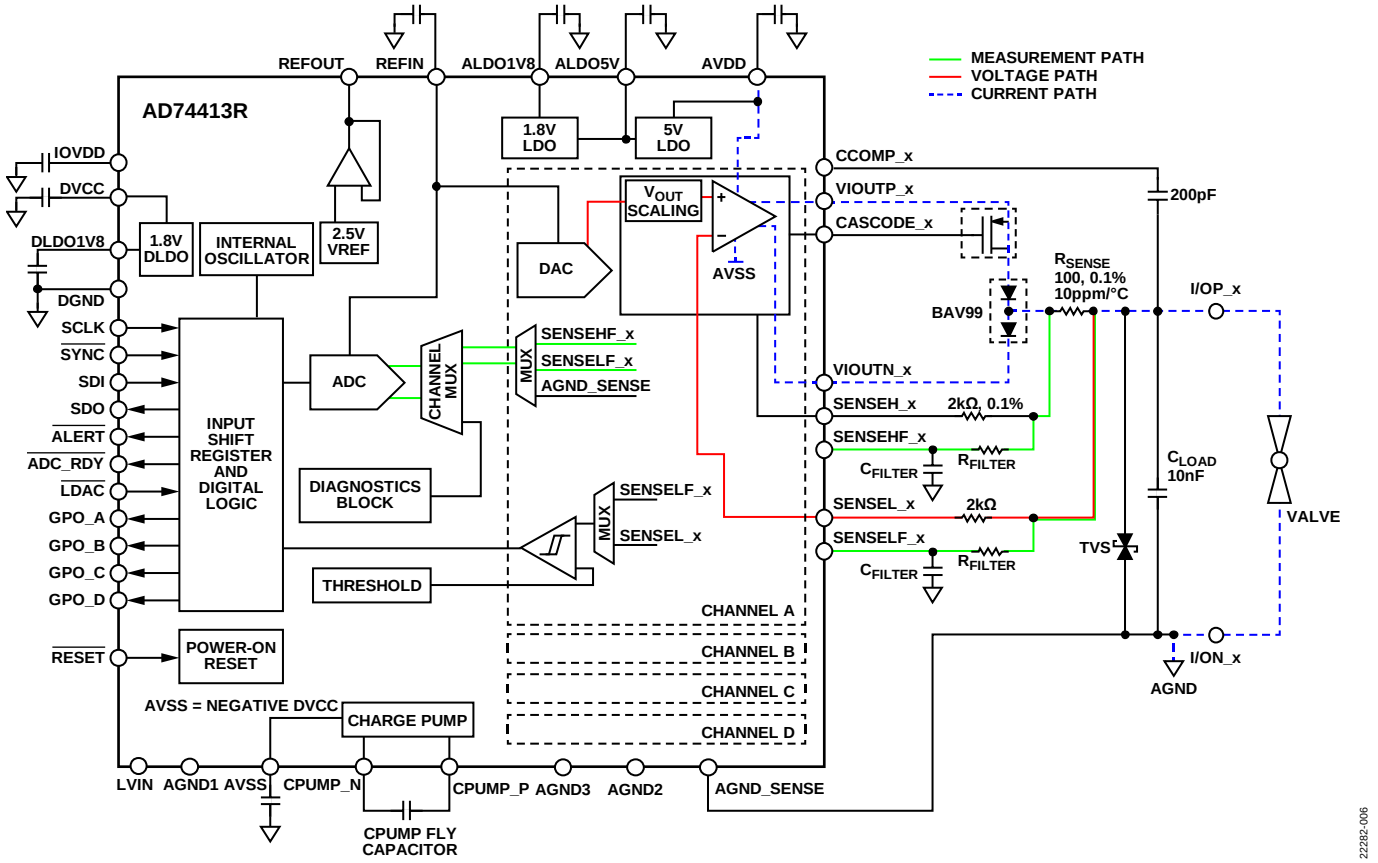


Figure 40. Voltage Output Mode Configuration

Current Output Mode

In current output mode, the DAC provides a current output on the VIOUTP_x pin that is regulated by sensing the differential voltage across R_{SENSE} by using the SENSEL_x and SENSEH_x pins. In addition, an optional, external P channel FET can pass the 0 mA to 25 mA current output to lower power dissipation on the die in cases where a low resistive load is present.

The circuit minimizes glitching on the I/OP_x screw terminal when the V_{AVDD} is ramping or when the use case configuration is changed.

Figure 41 shows the current, voltage, and measurement paths of the current output mode.

Current Output Open Circuit Detection

In current output mode, if the headroom voltage falls below the compliance voltage (specified in Table 2), due to an open-loop circuit on any channel, a current output open circuit error is flagged for that channel and the $\overline{\text{ALERT}}$ pin asserts. If the V_{AVDD} is insufficient to drive the programmed current output, the open circuit error is flagged.

Interpreting ADC Data

In current output mode, the ADC, by default, is configured to measures the voltage across the screw terminals (I/OP_x to I/ON_x) in a 0 V to 10 V range. Use the ADC measurement result to calculate the voltage across these screw terminals by using the following equation:

$$V_{ADC} = (ADC_CODE/65{,}535) \times Voltage\ Range$$

where:
V_{ADC} is the measured voltage in volts.
ADC_CODE is the value of the ADC_RESULTx registers.
Voltage Range is the measurement range of the ADC and is 10 V.

HART Compatibility

Current output mode is compatible with HART transmit functionality when users enable the HART compliant slew option via the SLEW_EN bit in the OUTPUT_CONFIGx register.

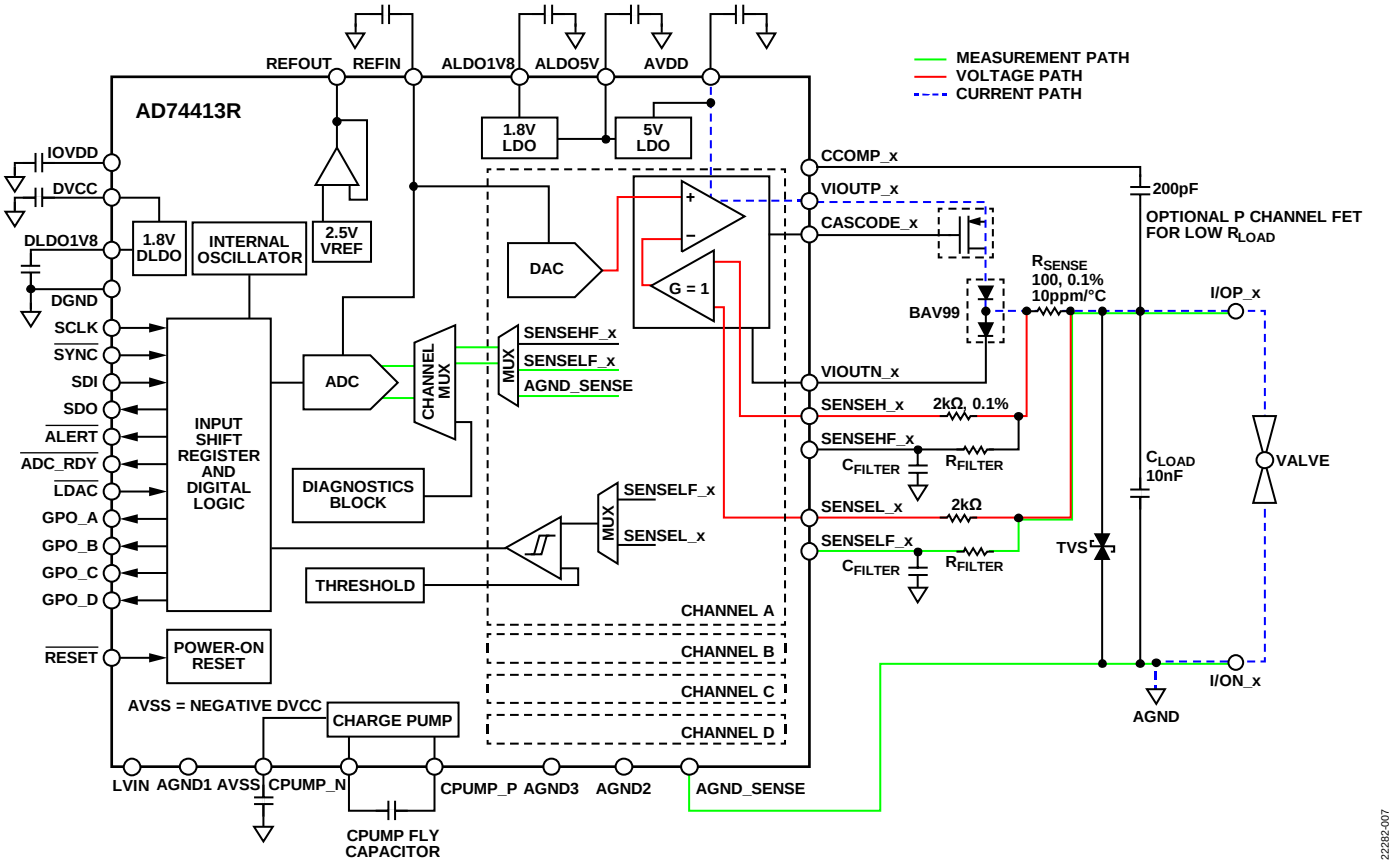


Figure 41. Current Output Mode Configuration

Voltage Input Mode

In voltage input mode, the voltage across the screw terminals (I/OP_x to I/ON_x) is measured by the ADC via the SENSELF_x and the AGND_SENSE pins. It is essential to connect the AGND_SENSE pin as close as possible to the I/ON_x screw terminal to ensure an accurate voltage measurement. Figure 42 shows the current and measurement paths of the voltage input mode.

Selectable 200 kΩ to GND

In voltage input mode, there is an option to connect the VIOUTN_x pins to ground via a 200 kΩ resistor, which is enabled via the ADC_CONFIGx registers (disabled by default). This option is useful if there is a discrepancy in the ADC measurement of the I/OP_x screw terminals, such as floating voltages. By enabling the 200 kΩ resistor, a small current is drawn through the 200 kΩ resistor, which pulls the voltage to ground.

Interpreting ADC Data

In voltage input mode, the ADC, by default, is configured to measure the voltage across the screw terminals (I/OP_x to I/ON_x) in a 0 V to 10 V range. Use the ADC measurement result to calculate the voltage across these screw terminals by using the following equation:

$$V_{ADC} = V_{MIN} + (ADC_CODE/65{,}535) \times Voltage\ Range$$

where:
V_{MIN} is the minimum input voltage of the selected ADC range and is 0 V by default.
V_{ADC} is the measured voltage in volts.
ADC_CODE is value of the ADC_RESULTx registers.
Voltage Range is the measurement range of the ADC and is 10 V.

Thermocouple Measurement

Voltage input mode can measure the voltage of a thermocouple when the thermocouple is connected across the screw terminals (I/OP_x to I/ON_x). To accurately measure the thermocouple voltage, select the ±104.16 mV input range via the ADC_CONFIGx register in voltage input mode.

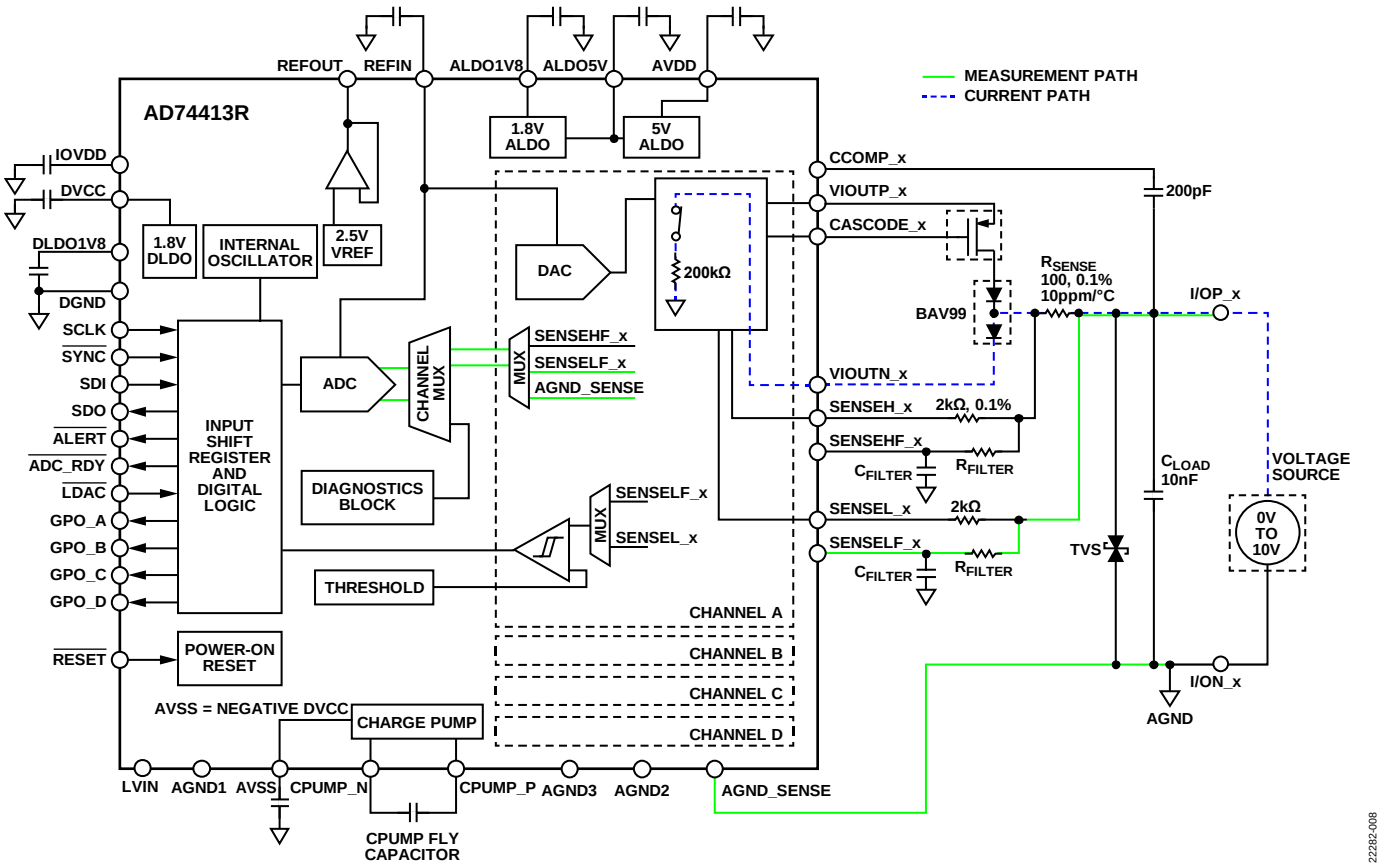


Figure 42. Voltage Input Mode Configuration

Current Input, Externally Powered Mode

In current input, externally powered mode, the AD74413R provides a current limited path to ground via the VIOUTN_x pin for an external current source. The 16-bit, Σ-Δ ADC automatically measures the current through R_{SENSE}. The current is measured by digitizing the voltage across R_{SENSE} via the SENSEHF_x and the SENSELF_x pins. Figure 43 shows the current and measurement paths of the current input, externally powered mode.

Short-Circuit Protection

The maximum short-circuit limit is 35 mA in the current input, externally powered mode to both protect the external circuitry and to limit the power dissipated on the AD74413R device.

If the digital input comparator is enabled, the ALERT_STATUS register can detect a short circuit.

Enable the digital input comparator with a threshold voltage of AVDD/2. In normal operation, the voltage on I/OP_x is typically within 5 V of ground. If the current source attempts to sink more than 35 mA into the AD74413R, the voltage on the SENSEL_x pin instantly ramps. When the voltage on the I/OP_x screw terminal is above the programmed threshold voltage, the comparator trips, setting the relevant VI_ERR_x bit in the ALERT_STATUS register.

Interpreting ADC Data

In current input mode, the ADC, by default, measures the current flowing from the I/OP_x screw terminal into the AD74413R through the R_{SENSE} in a 25 mA range. Use the ADC measurement current to calculate the current through the R_{SENSE} with the following equation:

$$I_{R_{SENSE}} = \frac{\left(\left(\frac{ADC_CODE}{65,535}\right) \times Voltage\ Range\right)}{RSENSE}$$

where:

$I_{R_{SENSE}}$ is the measured current in amps.

ADC_CODE is the value of the ADC_RESULTx registers.

Voltage Range is the full span of the ADC range and is 2.5 V.

R_{SENSE} is the sense resistor, which is set to 100 Ω.

Current Input, Externally Powered with HART Compatibility Mode

This mode is a HART compatible version of the current input, externally powered mode. The input impedance from the I/OP_x screw terminal is set to a minimum of 230 Ω to be compliant with the HART receive impedance.

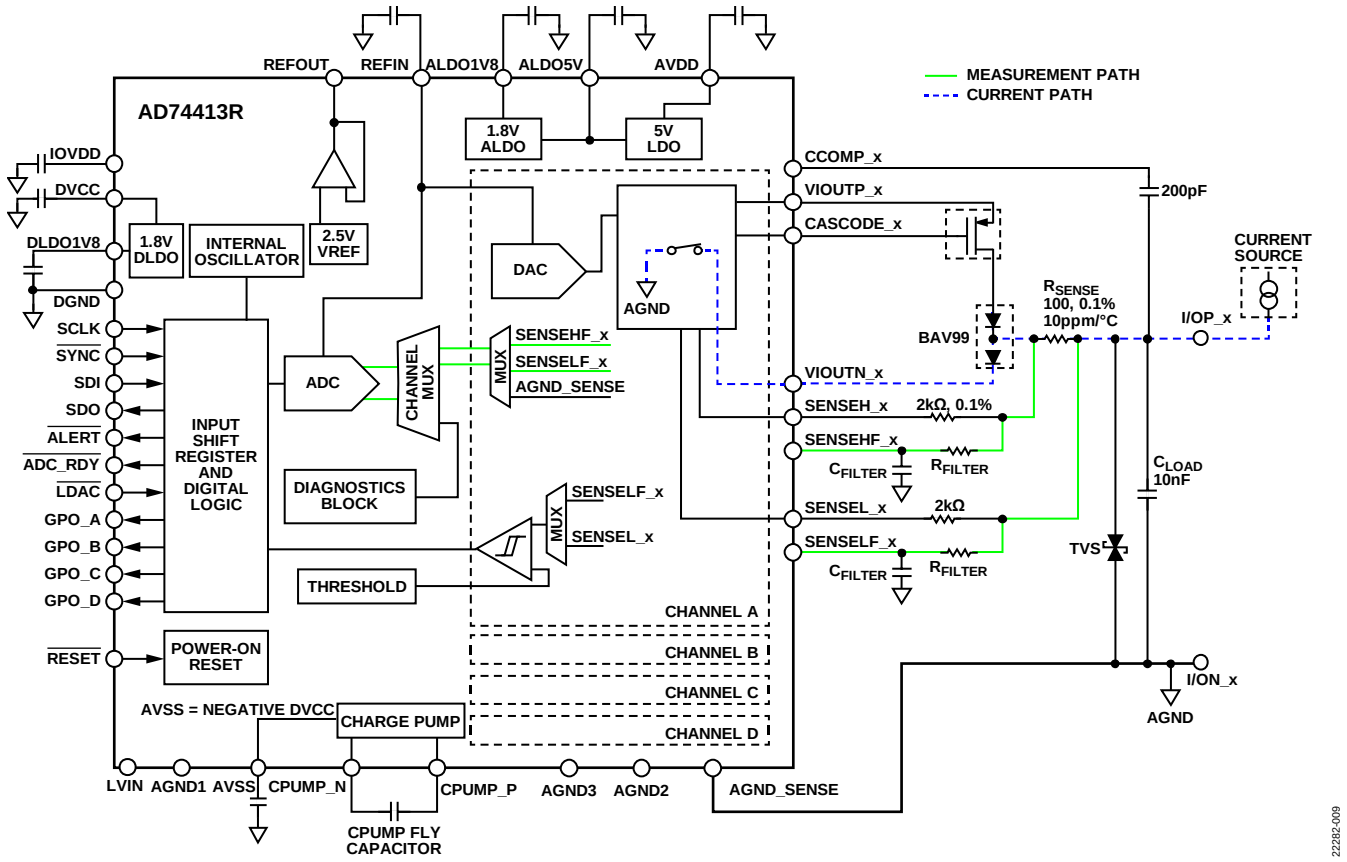


Figure 43. Current Input, Externally Powered Mode Configuration

Current Input, Loop Powered Mode

In current input loop powered mode, the AD74413R provides a current limited voltage to the I/OP_x screw terminal. The current is measured by digitizing the voltage across R_{SENSE} via the SENSEHF_x and the SENSELF_x pins. When selecting the current input loop powered function, tie the VIOUTN_x pin to ground via the on-chip 200 kΩ resistor by enabling the CH_200K_TO_GND bit in the ADC_CONFIGx registers. Figure 44 shows the current, voltage, and measurement paths of the current input, loop powered mode.

Short-Circuit Protection

The current from the AD74413R is limited by the programmable DAC code (maximum 24.5 mA).

If the digital input comparator is enabled, the ALERT_STATUS register detects short circuits.

Enable the digital input comparator with a threshold voltage of AVDD/2 and with the output inverted. During normal operation, the voltage on I/OP_x is typically within 5 V of the V_{AVDD}. If the load is short circuited to ground, the voltage on the I/OP_x is pulled to ground. When the voltage on the I/OP_x screw terminal falls below the programmed threshold level, the comparator trips low, setting the relevant VI_ERR_x bit in the ALERT_STATUS register.

Interpreting ADC Data

In current input loop, powered mode, the ADC, by default, measures the current flowing from the AD74413R into the I/OP_x screw terminal through the R_{SENSE} in a 25 mA range. Use the ADC measurement result to calculate the current with the following equation:

$$I_{R_{SENSE}} = \frac{\left(\left(\frac{ADC_CODE}{65,535}\right) \times Voltage\ Range\right)}{RSENSE}$$

where:

$I_{R_{SENSE}}$ is the measured current in amps.

ADC_CODE is the value of the ADC_RESULTx registers.

Voltage Range is the full ADC span of the ADC range and is 2.5 V.

R_{SENSE} is the sense resistor, which has a value of 100 Ω.

Current Input, Loop Powered with HART Compatibility Mode

This mode is a HART compatible version of the current input, loop powered mode. However, the current source is not programmable so the DACs do not need to be configured. A current limited source of typically 30 mA is enabled when the current input, loop powered with HART mode is selected. The input impedance from the I/OP_x screw terminal is set to a minimum of 230 Ω to be compliant with the HART receive impedance.

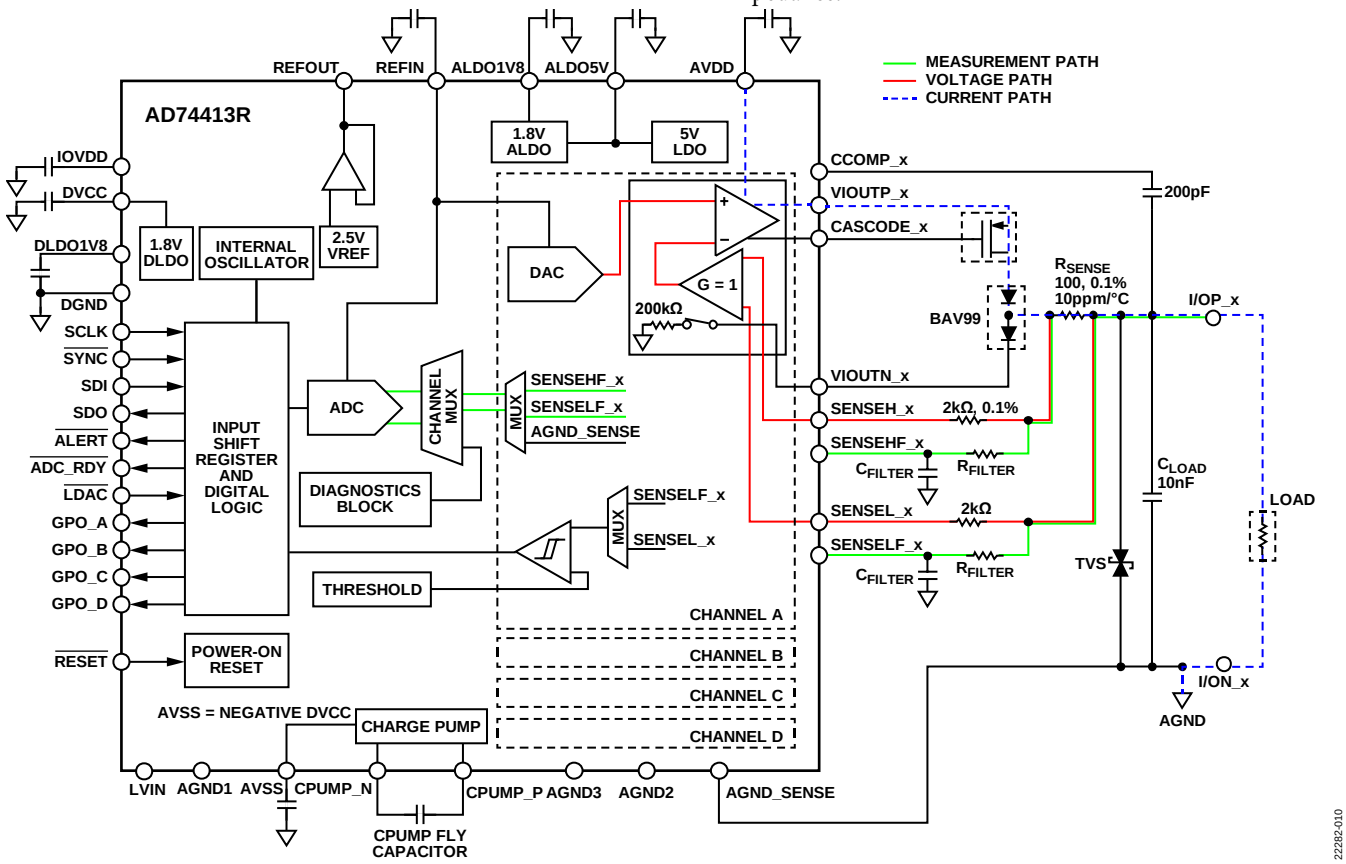


Figure 44. Current Input, Loop Powered Mode Configuration

Resistance Measurement (External 2-Wire RTD)

The resistance measurement configuration biases an external 2-wire RTD with a voltage derived from a 2.5 V bias. The resultant excitation current flows through the 2 kΩ and 100 Ω resistors (shown as $R_{PULL-UP}$ in Figure 45). This configuration ensures an accurate ratiometric measurement. The 16-bit, Σ-Δ ADC automatically digitizes the voltage across the RTD. The low excitation current ensures that the power dissipated by the RTD is minimized, reducing self heating. See Figure 45 for an example of the RTD bias circuit.

It is essential that the AGND_SENSE pin connects to the low-side of the measured RTD. Figure 46 shows the current, voltage, and measurement paths of the resistance measurement configuration.

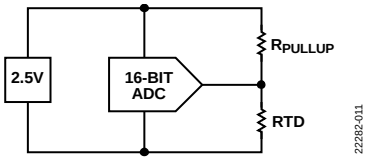


Figure 45. RTD Bias Circuit

Interpreting ADC Data

In resistance measurement mode, the 16-bit, Σ-Δ ADC automatically digitizes the voltage across the RTD in a 2.5 V range.

When a conversion is carried out, the ADC code reflects the ratio between the RTD and the $R_{PULL-UP}$. Use the ADC code to calculate the RTD resistance with the following equation:

$$Resistance_{RTD} = \frac{(ADC_CODE \times R_{PULL-UP})}{(65{,}535 - ADC_CODE)}$$

where:
$Resistance_{RTD}$ is the calculated RTD resistance in Ωs.
ADC_CODE is the code of the ADC_RESULTx registers.
$R_{PULL-UP}$ has a value of 2100 Ω.

Do not change the ADC_MUX bits in the settings of the ADC_CONFIGx registers if in RTD mode. Changing from the default ADC mux configuration results in a void ADC result.

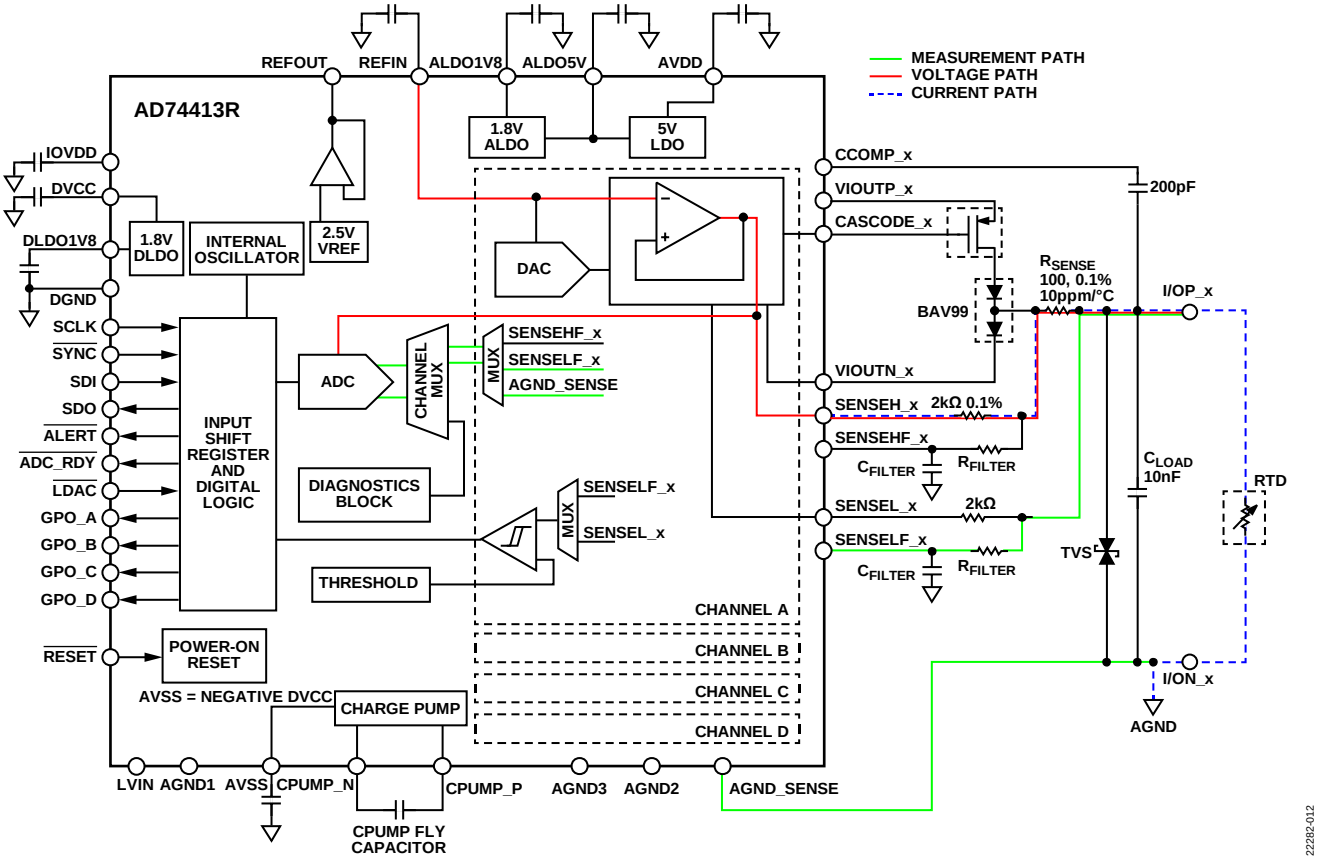


Figure 46. Resistance Measurement Configuration

Digital Input Logic

The digital input circuit can convert high voltage digital inputs from the I/OP_x screw terminal to low voltage logic signals on the GPO_x pins or on the SPI.

An externally powered sensor provides a high voltage digital input on the I/OP_x screw terminal. Either the unfiltered screw voltage on the SENSEL_x pin or a filtered version of the screw voltage on the SENSELF_x pin can be routed to the on-chip comparator. The comparator compares the voltage of the selected pin to a programmable threshold (see the Digital Input Threshold Setting section for additional information). To debounce the comparator output see the Debounce Function section.

Monitor the digital input comparator outputs by reading from the DIN_COMP_OUT register. Alternatively, each channel has a corresponding GPO_x pin associated with the channel. These GPO_x pins are configured via the GPO_CONFIGx registers to drive out the debounced digital input signal.

Figure 47 shows the current, voltage, and output paths of the digital input logic mode.

Interpreting ADC Data

The ADC is not required for digital input operation. However, the ADC is available for voltage and current measurements while the digital input logic mode is enabled. In digital input logic mode, the ADC, by default, measures the voltage across the I/OP_x to I/ON_x screw terminals in a 0 V to 10 V range when in digital input logic mode. Use the ADC result to calculate the voltage across the I/OP_x to I/ON_x screw terminals by using the following equation:

$$V_{ADC} = (ADC_CODE/65{,}535) \times Voltage\ Range$$

where:
V_{ADC} is the measured voltage in volts.
ADC_CODE is the value of the ADC_RESULTx registers.
Voltage Range is the ADC measurement range and is 10 V.

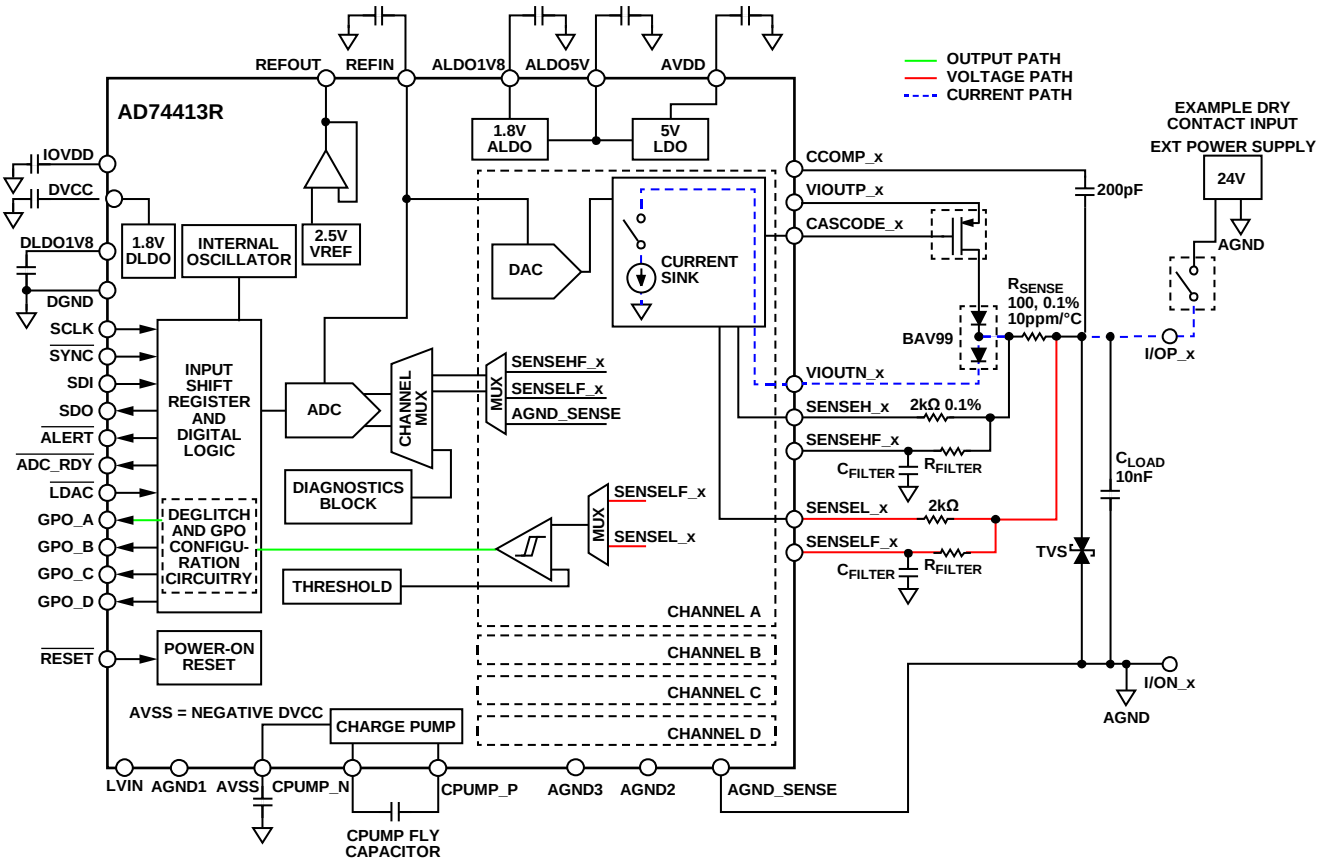


Figure 47. Digital Input Logic Mode Configuration

Digital Input Threshold Setting

The digital input thresholds are set by an internal DAC. The reference to this DAC is driven by either the V_{AVDD} or the reference voltage, V_{REFIN}. This reference is configured by writing to the DIN_THRESH_MODE bit within the DIN_THRESH register.

The specific threshold levels are programmed using the COMP_THRESH bits in the DIN_THRESH register. There are five bits available to configure the threshold.

The following equation shows the relationship between the programmed code in the COMP_THRESH bits and the corresponding threshold voltage when the DAC reference is set to AVDD.

$$V_{THRESH(AVDD)} = \frac{V_{AVDD}}{60} + Code \times \left(\frac{2 \times V_{AVDD}}{60} \right)$$

where:
$V_{THRESH(AVDD)}$ is the comparator threshold expressed in volts.
V_{AVDD} is the AVDD supply value in volts.
Code is the decimal code loaded to the COMP_THRESH bits.

The maximum programmable code in this mode is Decimal 29.

The following equation shows the relationship between the programmed code in the COMP_THRESH bits and the corresponding threshold voltage when the DAC reference is set to V_{REFIN}.

$$V_{THRESH(FIXED\ VOLTAGE)} = 0.5 + (Code \times 0.5)$$

where:
$V_{THRESH(FIXED\ VOLTAGE)}$ is the comparator threshold expressed in volts.
Code is the decimal code loaded to the COMP_THRESH bits.

The maximum programmable code in this mode is Decimal 31.

Digital Input Current Sink

The AD74413R includes a programmable current sink. The current sink is programmed via the DIN_RANGE bit and the DIN_SINK bits within the DIN_CONFIGx registers. This current sink programmability enables compatibility with Type I, Type II, and Type III of the IEC 61131-2.

Program the current sink and the threshold voltages to enable compatibility with Type I and Type III of the IEC 61131-2.

For Type I and Type III, it is recommended to program the bits in the DIN_CONFIGx and DIN_THRESH registers as follows:

- DIN_RANGE bit: 0x0
- DIN_SINK bits: 0x14
- DIN_THRESH_MODE bit: 0x1
- COMP_THRESH bits: 0x10

Programming these bits results in a typical current sink of 2.4 mA and a rising voltage trip point of typically 8.5 V.

For Type II, it is recommended to program the DIN_CONFIGx and DIN_THRESH registers as follows:

- DIN_RANGE bit: 0x1
- DIN_SINK bits: 0x1D
- DIN_THRESH_MODE bit: 0x1
- COMP_THRESH bits: 0x10

Programming these bits result in a typical current sink of 6.96 mA and a rising voltage trip point of 8 V.

Debounce Function

The digital input comparator outputs are sampled at regular intervals and passed to a user-programmable debounce operation.

The comparator outputs can be debounced for a user-programmable amount of time via the 5-bit DEBOUNCE_TIME bits within the DIN_CONFIGx registers. Set these bits to 0x00 to bypass the debouncer. Table 15 shows the available programmable debounce times.

Table 15. Digital Input Programmable Debounce Times

DEBOUNCE_TIME Code (Hex)	Debounce Time (ms)
00	Bypass
01	0.0130
02	0.0187
03	0.0244
04	0.0325
05	0.0423
06	0.0561
07	0.0756
08	0.1008
09	0.1301
0A	0.1805
0B	0.2406
0C	0.3203
0D	0.4203
0E	0.5602
0F	0.7504
10	1.0008
11	1.3008
12	1.8008
13	2.4008
14	3.2008
15	4.2008
16	5.6008
17	7.5007
18	10.0007
19	13.0007
1A	18.0006
1B	24.0006
1C	32.0005
1D	42.0004
1E	56.0003
1F	75.0000

The debounce circuit has the following two modes of operation: Debounce Mode 0 and Debounce Mode 1. Both modes are programmed via the DEBOUNCE_MODE bit in the DIN_CONFIGx registers.

Debounce Mode 0 (Default)

In this mode, the sampled comparator outputs are counted. A high sample occurrence is counted in one direction (either up or down), whereas a low sample occurrence is counted in the opposite direction. The DIN_COMP_OUT register changes state when the programmed counter target is reached.

Figure 48 shows an example of Debounce Mode 0 in operation. The debounce time is set to 100 µs in the DIN_CONFIGx registers. A clock with an approximate frequency of 800 ns samples counts the comparator signal. After the comparator signal changes state from the current debounced signal, the debounce function counter begins to count the duration of the signal at the new state. The count direction changes if the comparator signal reverts back to the original state. After the counter reaches the target count, the DIN_COMP_OUT is updated with the state of the comparator signal.

Debounce Mode 1

In this mode, a counter counts the sampled comparator outputs. After a change of state occurs on the sampled comparator output, the counter increments until the programmed debounce time is reached, at which point the DIN_COMP_OUT register changes state, and the counter resets. If the sampled comparator output returns to the current DIN_COMP_OUT register value, the counter resets.

Figure 49 shows an example of Debounce Mode 1 in operation. Like Debounce Mode 0, the debounce time is set to 100 µs. In Debounce Mode 1, the counter value is reset each time the comparator signal returns to the original state. The comparator output must be at the new state for the full duration of the debounce time to update the DIN_COMP_OUT signal.

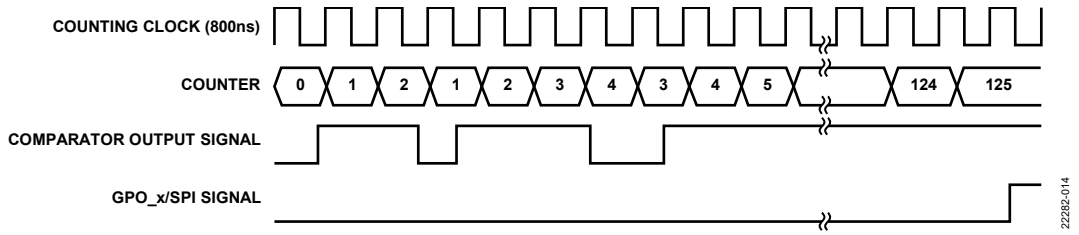


Figure 48. Digital Input Debounce Mode 0 Timing Example

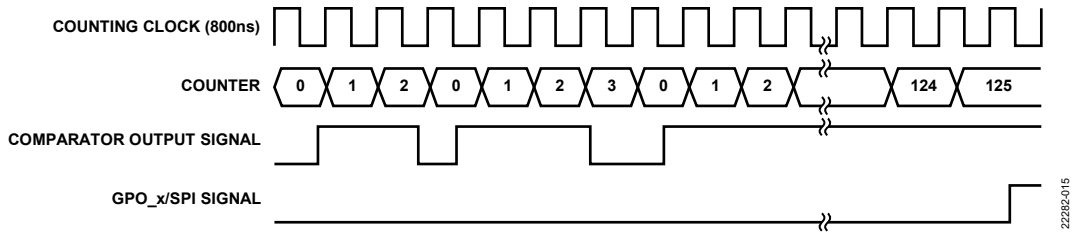


Figure 49. Digital Input Debounce Mode 1 Timing Example

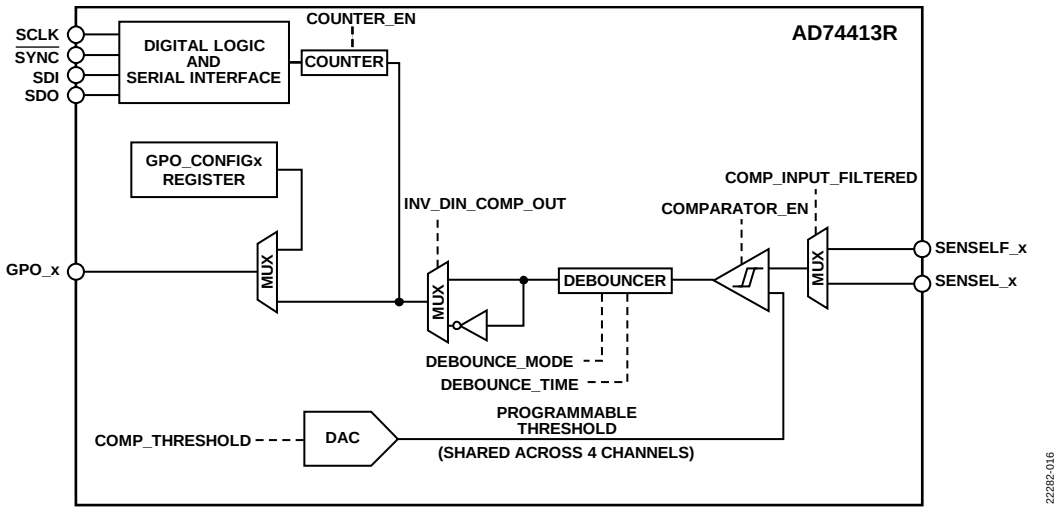


Figure 50. Digital Input Configuration

Digital Input Inverter

The debounced comparator signal can pass directly to the DIN_COMP_OUT register. Alternatively, the signal can be inverted before being sent to the DIN_COMP_OUT register. To enable this inverter, set the INV_DIN_COMP_OUT bit in the DIN_CONFIGx registers.

Digital Input Counter

A counter is available in the digital input modes and the counter allows the user to count the debounced digital input edges. The counter can be programmed to count the positive edges or the negative edges, which depends on whether the digital input inverter is being used. Enable the digital input counter and configure the inverter in the DIN_CONFIGx registers. The count value is accessed in the DIN_COUNTERx registers.

The counter is reset to 0 when the device is reset. When the counter reaches full scale, it rolls over to 0. The counter freezes if the COUNT_EN bit is set to 0.

Figure 50 shows a detailed view of the digital input configuration including the comparator, debouncer, inverter, counter, and GPO_x hook up.

DIGITAL INPUT, LOOP POWERED MODE

Like the current output mode function (see the Current Output Mode section), the digital input, loop powered function configures the output state to provide a high-side current output that can power an external sensor. Program the DAC_CODEx registers to provide the required current source limit.

Either the unfiltered voltage on the SENSEL_x pin or the filtered input on the SENSELF_x pin can be routed to the on-chip comparators. These comparators compare the voltage on the selected pin to a programmable threshold that can either be a fixed voltage or a voltage proportional to the V_{AVDD}. See the Digital Input Threshold Setting section for more information on the programmable threshold voltages.

The output of the comparators can be debounced (see the Debounce Function section) or passed directly or inverted to the serial interface and/or to the parallel output pins.

The digital input comparator outputs are monitored by reading from the DIN_COMP_OUT register. The comparator outputs can also be monitored with the GPO_x pins. Each channel has a corresponding GPO_x pin that is configured via the GPO_CONFIGx registers to drive out the debounced comparator output signal.

Figure 51 shows the current, voltage, and output paths of the digital input, loop powered mode configuration.

Interpreting ADC Data

The ADC is not required for digital input operation. However, the ADC is available for voltage and current measurements when the digital input loop powered mode is enabled. In digital input loop powered mode, the ADC, by default, measures the voltage across the I/OP_x to I/ON_x screw terminals in a 0 V to 10 V range. Use the ADC measurement result to calculate this voltage by using the following equation:

$$V_{ADC} = (ADC_CODE/65{,}535) \times Voltage\ Range$$

where:

V_{ADC} is the measured voltage in volts.
ADC_CODE is the value of the ADC_RESULTx registers.
Voltage Range is 10 V, the measurement range of the ADC.

If the default measurement configuration is changed to measure the current, tie the VIOUTN_x pin to ground via the on-chip 200 kΩ resistor by enabling the CH_200K_TO_GND bit in the ADC_CONFIGx registers.

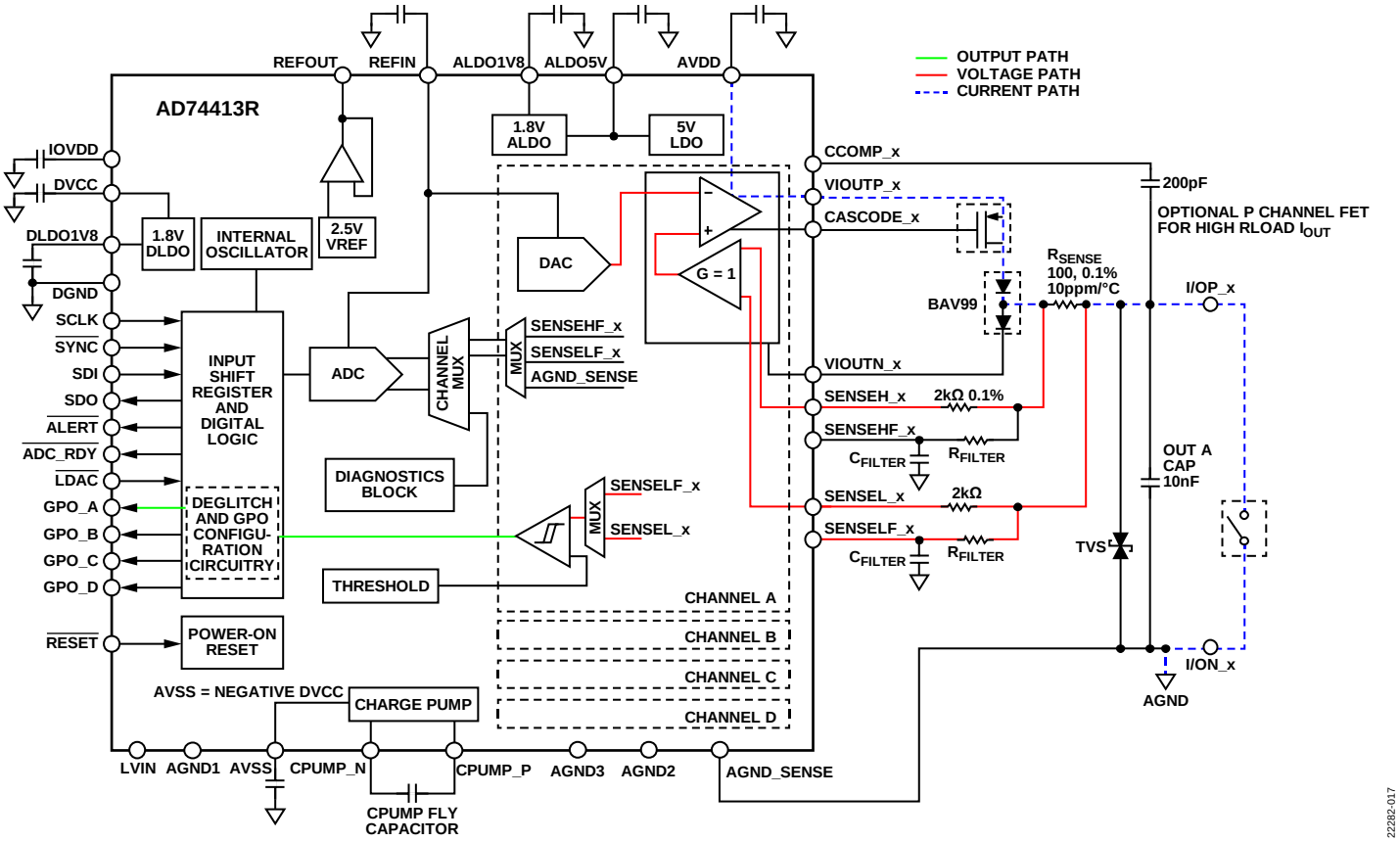


Figure 51. Digital Input, Loop Powered Configuration Mode

GETTING STARTED

The following three external supplies are required to power up the AD74413R: V_{AVDD}, which is the positive analog supply, the voltage on the DVCC pin (V_{DVCC}), which is the digital and charge pump supply, and the VIOVDD, which is the input/output pads supply. The IOVDD pin and the DVCC pin can be connected to the same external supply. V_{IOVDD} can also be driven as low as 1.8 V separately to allow SPI communications at 1.8 V. See Table 10 for the voltage range of the three external supplies and the associated conditions.

A charge pump generates a negative supply, V_{AVSS}, that is equal to negative V_{DVCC}. V_{AVSS} cannot be used to drive the external circuitry.

When powering up the AD74413R, apply ground connections first. After power-up, the user must wait approximately 10 ms (see Table 10) before any transaction to the device can take place.

After initial power-up, the $\overline{\text{ALERT}}$ pin is pulled low as a result of various bits, such as the RESET_OCCURRED bit and the CHARGE_PUMP_ERR bit, being set in the ALERT_STATUS register. It is recommended to clear the alert status before continuing to use the AD74413R. Write 1 to clear each bit in the ALERT_STATUS register.

Upon initial power-up or after device reset, the output channels are disabled and default to a high impedance state.

USING CHANNEL FUNCTIONS

The channel function is selected using the CH_FUNC_SETUPx registers. After a channel function is selected, the contents of the ADC_CONFIGx registers and the DIN_CONFIGx registers are updated with predefined values, which allows the user to configure the device with a minimal set of commands. Table 16 outlines the default settings of the bits for any given channel function.

After configuring the channel function, users can configure the DAC_CODEx registers, if required. If the $\overline{\text{LDAC}}$ pin is not tied low, a load DAC (LDAC) command is required to update the channel outputs after the DAC codes are updated. See the LDAC Function section more information.

Switching Channel Functions

Take care when switching from one channel function to another. All functions must be selected for a minimum of 130 µs before changing to another function.

The DAC_CODEx registers are not reset by changing channel functions. Prior to changing channel functions, it is recommended to set the DAC code to 0x0000 via the DAC_CODEx registers. Set the channel function to high impedance via the CH_FUNC_SETUPx registers before transitioning to the new channel function. After the new channel function is configured, it is recommended to wait 150 µs before updating the DAC code.

Table 16. Register Edits based on Channel Function Selection

Channel Function (Programmed via the CH_FUNC_SETUPx Registers)	Defaults of the ADC_CONFIGx Registers		Defaults of the DIN_CONFIGx Registers	
	ADC_MUX Bits	RANGE Bits	COMPARATOR_EN Bit	DIN_SINK Bits
High Impedance	00: voltage across the I/OP_x to I/ON_x screw terminals	000: 0 V to 10 V	0: comparator disabled	0: I_{SINK} off
Voltage Output	01: voltage across R_{SENSE}	011: −2.5 V to +2.5 V	0: comparator disabled	0: I_{SINK} off
Current Output	00: voltage across the I/OP_x to I/ON_x screw terminals	000: 0 V to 10 V	0: comparator disabled	0: I_{SINK} off
Voltage Input	00: voltage across the I/OP_x to I/ON_x screw terminals	000: 0 V to 10 V	0: comparator disabled	0: I_{SINK} off
Current Input, Externally Powered	01: voltage across R_{SENSE}	010: −2.5 V to 0 V	0: comparator disabled	0: I_{SINK} off
Current Input, Loop Powered	01: voltage across R_{SENSE}	001: 0 V to 2.5 V	0: comparator disabled	0: I_{SINK} off
Resistance Measurement	00: voltage across the I/OP_x to I/ON_x screw terminals	001: 0 V to 2.5 V	0: comparator disabled	0: I_{SINK} off
Digital Input Logic	00: voltage across the I/OP_x to I/ON_x screw terminals	000: 0 V to 10 V	1: comparator enabled	0: I_{SINK} off
Digital Input, Loop Powered	00: voltage across the I/OP_x to I/ON_x screw terminals	000: 0 V to 10 V	1: comparator enabled	0: I_{SINK} off
Current Input, Externally Powered, with HART	01: voltage across R_{SENSE}	010: −2.5 V to 0 V	0: comparator disabled	0: I_{SINK} off
Current Input, Loop Powered, with HART	01: voltage across R_{SENSE}	001: 0 V to 2.5 V	0: comparator disabled	0: I_{SINK} off

ADC FUNCTIONALITY

The default measurement configurations for each mode are described in the Using Channel Functions section. The ADC can measure either current or voltage on one or more of the four input/output channels and up to four diagnostic inputs with one conversion request.

The measurement settings of the channels and conversion rates are configured via the ADC_CONFIGx registers. The diagnostics settings are configured via the DIAG_ASSIGN register. The diagnostics conversion rate is programmed in the ADC_CONV_CTRL register.

After the measurements are configured, enable the relevant ADC inputs via the ADC_CONV_CTRL register.

Select either single conversion or continuous conversion mode by setting the appropriate value to the CONV_SEQ bits in the ADC_CONV_CTRL register.

In single conversion mode, the ADC sequencer starts conversions at the lowest enabled channel before cycling through successively higher enabled channel numbers, followed by the enabled diagnostics. After each enabled channel is converted once, the ADC enters idle mode, and conversions are stopped.

In continuous conversion mode, the ADC channel sequencer continuously converts each enabled channel and diagnostic until a command is written to stop the conversions. Set the stop command by setting the CONV_SEQ bits in the ADC_CONV_CTRL register bits to idle mode or power-down mode. The command stops conversions at the end of the current sequence.

If the enabled channels or the measurement configuration on any given channel require a function change, continuous conversions must be stopped before making the changes. Restart the continuous conversions after making the appropriate changes.

After a sequence is complete, either single conversion or continuous conversion, all data results are transferred to the relevant ADC_RESULTx and DIAG_RESULTx registers, asserting the $\overline{\text{ADC_RDY}}$ pin.

ADC Conversion Rates

The available ADC conversion rates on the AD74413R are 1.2 kSPS and 4.8 kSPS, with 50 Hz and 60 Hz rejection disabled, and 10 SPS and 20 SPS, with 50 Hz and 60 Hz rejection enabled.

Each of the four input/output channels can be individually configured to a conversion rate via the ADC_CONFIGx registers. The conversion rate of the diagnostics inputs is set via the ADC_CONV_CTRL register. One conversion rate selection applies to all diagnostic inputs.

The time it takes for a sequence of conversions to complete is dependent on several factors, such as the number of selected channels, the selected conversion rates, and whether single or continuous mode conversions are enabled. Conversions are clocked by an on-chip oscillator, which has a typical accuracy of ±1%. Table 17 outlines the various components required to estimate a complete conversion time for any given sequence.

For single channel conversions, consider the following time components when calculating the overall sequence time:

- The time taken for the SPI transaction to start the conversions.
- An initial pipeline delay prior to the first conversion.
- The conversion time for each ADC conversion.

Figure 52 shows the timing breakdown of a single channel conversion example. In this example, only Channel A is enabled, and continuous conversions are initiated with a 4.8 kSPS conversion rate.

The time to the first complete conversion (the $\overline{\text{SYNC}}$ pin falling edge to the $\overline{\text{ADC_RDY}}$ pin falling edge) is 284.32 µs and is calculated by adding the SPI transfer time, the pipeline delay time, and the conversion rate on Channel A at 4.8 kSPS (208.33 µs)

The time between conversions (the $\overline{\text{ADC_RDY}}$ pin falling edge to the $\overline{\text{ADC_RDY}}$ pin falling edge) is 208.33 µs.

Table 17. Conversion Times Components

Conversion Rate	SPI Transfer Time (µs), 42 ns SCLK	Start-Up Pipeline Delay (µs)	Single ADC Conversion Time	Channel Switch Time, Multiple Enabled Channels (µs)
4.8 kSPS	1.99	74	208.33 µs	24.4
1.2 kSPS	1.99	74	833.33 µs	24.4
20 SPS	1.99	74	50 ms	24.4
10 SPS	1.99	74	100ms	24.4

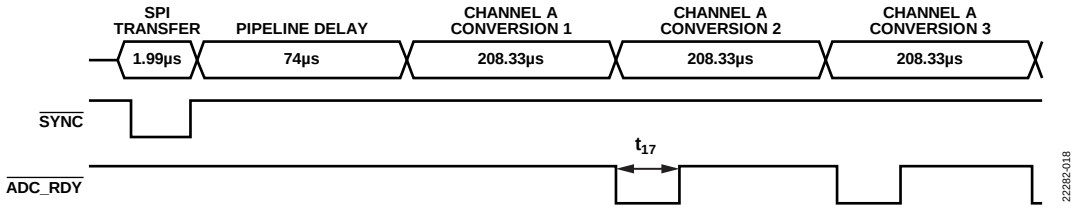


Figure 52. Single Channel, Continuous Conversions Timing Diagram

For multichannel conversions, consider the following components when calculating the overall sequence time:

- The time taken for the SPI transaction to start the conversions.
- An initial pipeline delay prior to the first conversion.
- The conversion time needed for each ADC conversion.
- A channel switch time for each time the selected ADC channel is switched.

Figure 53 shows an example of the timing breakdown for a multichannel conversion. In this example, Channel A and Channel B, with Diagnostic 0 and Diagnostic 1 enabled. Continuous conversions are initiated with a 20 SPS conversion rate.

The time it takes for the first complete conversion ($\overline{SYNC}$ falling edge to $\overline{ADC_RDY}$ falling edge), is 200.149 ms and is calculated by adding the SPI transfer time, the pipeline delay time, and the conversion time on Channel A at 20 SPS, followed by adding the channel switch time and conversion time for the remaining three conversions.

The time between all subsequent conversion sequences (the $\overline{ADC_RDY}$ pin falling edge to the $\overline{ADC_RDY}$ pin falling edge) is 200.0976 ms and is calculated by adding the channel switch time with the conversion time for the four selected ADC inputs.

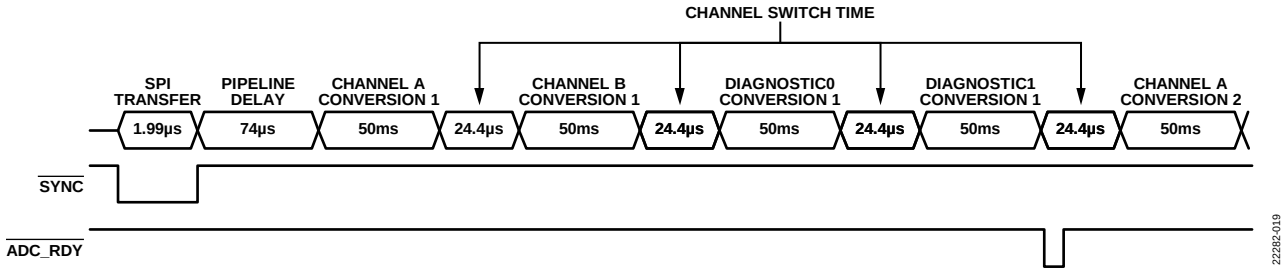


Figure 53. Multichannel, Continuous Conversions Timing Diagram

$\overline{\text{ADC_RDY}}$ Functionality

The $\overline{\text{ADC_RDY}}$ pin asserts low at the end of a sequence of conversions for either single conversion or continuous conversion mode.

The pin deasserts in any of the following scenarios:

- A 1 is written to the ADC_DATA_RDY status bit in the LIVE_STATUS register.
- After 24 µs in continuous mode.
- After writing to either the ADC_CONV_CTRL register.

See Figure 54 and Figure 55 for timing diagrams of the $\overline{\text{ADC_RDY}}$ pin in single and continuous conversion modes.

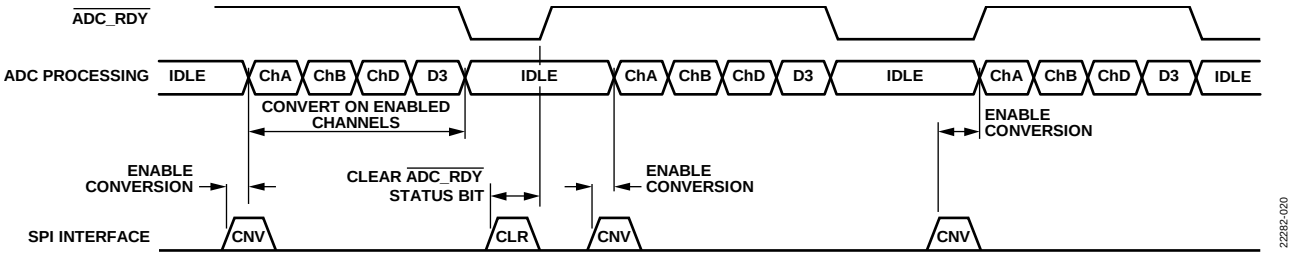


Figure 54. $\overline{\text{ADC_RDY}}$ Functionality in Single Conversion Mode

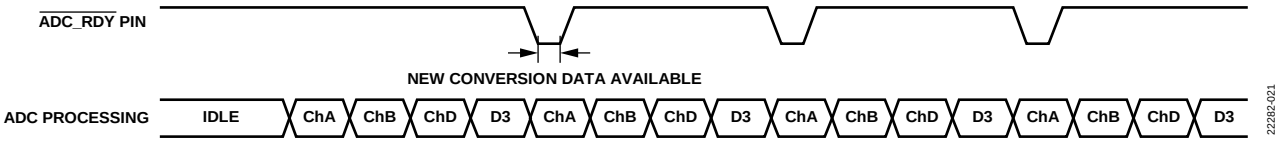


Figure 55. $\overline{\text{ADC_RDY}}$ Functionality in Continuous Conversion Mode

ADC Output Data Format

Table 18 outlines the expected ADC results for inputs specified in the table for each voltage range.

Table 18. ADC Output Data Format[1]

RANGE Bits	ADC_MUX Bits	ADC Data for Negative Full-Scale Input	ADC Data for Zero Input	ADC Data for Positive Full-Scale Input
000: 0 V to 10 V	0: voltage across the I/OP_x to I/ON_x screw terminals	Not applicable	Code 0x0000 for 0 V	Code 0xFFFF for 10 V
	1: voltage from SENSELF_x pin to SENSEHF_x pin across R_{SENSE}	Not applicable	Code 0x0000 for 0 mA flowing into the AD74413R through R_{SENSE}	Code 0x3FFF for 25 mA flowing into the AD74413R through R_{SENSE}
001: 0 V to 2.5 V[2]	0: voltage across the I/OP_x to I/ON_x screw terminals	Not applicable	Code 0x0000 for 0 V	Code 0xFFFF for 2.5 V
	1: voltage from SENSELF_x pin to SENSEHF_x pin across R_{SENSE} (SENSELF_x > SENSEHF_x)	Not applicable	Code 0x0000 for 0 mA flowing into the AD74413R through R_{SENSE}	Code 0xFFFF for 25 mA flowing into the AD74413R through R_{SENSE}
010: 0 V to 2.5 V[3]	0: voltage across the I/OP_x to I/ON_x screw terminals	Code 0xFFFF for −2.5 V[4]	Code 0x0000 for 0 V	Not applicable
	1: voltage from SENSELF_x pin to SENSEHF_x pin across R_{SENSE} (SENSELF_x < SENSEHF_x)	Code 0xFFFF for 25 mA flowing out of the AD74413R through R_{SENSE}	Code 0x0000 for 0 mA flowing out of the AD74413R through R_{SENSE}	Not applicable
011: −2.5 V to +2.5 V	0: voltage across the I/OP_x to I/ON_x screw terminals	Code 0x0000 for −2.5 V[4]	Code 0x8000 for 0 V	Code 0xFFFF for 2.5 V
	1: voltage from SENSELF_x pin to SENSEHF_x pin across R_{SENSE}	Code 0x0000 for 25 mA flowing out of the AD74413R through R_{SENSE}	Code 0x8000 for 0 mA flowing through R_{SENSE}	Code 0xFFFF for 25 mA flowing into the AD74413R through R_{SENSE}
100: −104.16 mV to +104.16 mV	0: voltage across the I/OP_x to I/ON_x screw terminals	Code 0x0000 for −104.16 mV	Code 0x8000 for 0 V	Code 0xFFFF for 104.16 mV
	1: voltage from SENSELF_x pin to SENSEHF_x pin across R_{SENSE}	Code 0x0000 for 1.0416 mA flowing out of the AD74413R through R_{SENSE}	Code 0x8000 for 0 mA flowing through R_{SENSE}	Code 0xFFFF for 1.0416 mA flowing into the AD74413R through R_{SENSE}

[1] When measuring across the R_{SENSE}, the I/OP_x screw terminal voltage must be between V_{AVDD} − 0.2 and the voltage on the AGND pin (V_{AGND}) − 500 mV for valid measurements. A supplemental screw terminal diagnostic measurement is recommended.
[2] Predominantly used to measure current sinking to AD74413R.
[3] Predominantly used to measure current sourced by the AD74413R.
[4] The lowest measurable negative voltage, with respect to ground, depends on the V_{AVSS}. The full ADC range of 2.5 V is not available.

If the voltage measured by the ADC is either above full scale or below zero scale, an ADC_CONV_ERR bit is set in the ALERT_STATUSx registers, asserting the $\overline{\text{ALERT}}$ pin. In this case, the ADC output reads 0xFFFF or 0x0000, respectively. The ADC_CONV_ERR bit can be masked via the ALERT_ MASK register (optional) if these alerts are not required.

ADC Noise

Table 19 shows the peak-to-peak noise of the AD74413R for each of the output data rates and voltage ranges. These numbers are typical and are generated with a differential input voltage of 0 V when the ADC is continuously converting on a single channel.

Table 19. Peak-to-Peak Noise in LSBs per Voltage Range and Output Data Rate (Inputs Shorted)

Output Data Rate (SPS)	+10 V Range (LSBs)	+2.5 V Range (LSBs)	±2.5 V Range (LSBs)	±104.16 mV Range (LSBs)
10	0.1	0.1	0.06	0.8
20	0.2	0.2	0.1	1.3
1.2k	1.3	1.4	0.7	10.5
4.8k	3.0	3.5	1.8	20.7

Table 20 shows the peak-to-peak resolution for each voltage range and output data rate.

Table 20. Peak-to-Peak Resolution in Bits per Voltage Range and Output Data Rate

Output Data Rate (SPS)	+10 V Range (Bits)	+2.5 V Range (Bits)	±2.5 V Range (Bits)	±104.16 mV Range (Bits)
10	16	16	16	16
20	16	16	16	15.9
1.2k	15.9	15.7	16	12.9
4.8k	14.7	14.4	15.4	11.9

DIAGNOSTICS

The AD74413R has a diagnostic function that allows the ADC to measure various on-chip voltages. These diagnostic voltages are scaled to be measurable within the ADC range.

The diagnostics inputs are independent of the four, configurable output channels of the AD74413R. The DIAG_ASSIGN register assigns the voltage measurements to each diagnostic input. Select a diagnostic input to be measured by the ADC by enabling that input in the ADC_CONV_CTRL register. Users can also select the conversion rate via the ADC_CONV_CTRL register. The following two conversion rates are available for selection within the ADC_CONFIGx registers: 4.8 kSPS (50 Hz and 60 Hz rejection disabled) or 20 SPS (50 Hz and 60 Hz reject enabled).

Table 21 shows a full list of available diagnostics, and the equations required to calculate the diagnostic value.

In the equations listed in Table 21, DIAG_CODE is the ADC result code read from the DIAG_RESULTx registers, and voltage range is the ADC measurement range and is 2.5 V.

Table 21. User Selectable Diagnostics

Diagnostic	Formula to Interpret ADC Result
V_{AGND}	$V_{AGND} = \frac{DIAG_CODE}{65,535} \times Voltage\ Range$
Temperature Sensor (Internal Die Temperature Measurement)/°C	$Temperature = \left(\frac{DIAG_CODE - 2034}{8.95}\right) - 40$
Voltage on AVDD Pin (V_{AVDD})	$V_{AVDD} = 16 \times \left(\frac{DIAG_CODE}{65,535}\right) \times Voltage\ Range$
Voltage on DLDO1V8 Pin ($V_{DLDO1V8}$)	$V_{DLDO1V8} = 3 \times \left(\frac{DIAG_CODE}{65,535}\right) \times Voltage\ Range$
V_{AVSS}	$V_{AVSS} = (0.0001776 \times DIAG_CODE) - 5.98$
Voltage on REFOUT Pin (V_{REFOUT})	$V_{REFOUT} = \frac{\left(\frac{DIAG_CODE}{65,535}\right) \times Voltage\ Range}{0.762}$
Voltage on ALDO5V Pin (V_{ALDO5V})	$V_{ALDO5V} = 7 \times \left(\frac{DIAG_CODE}{65,535}\right) \times Voltage\ Range$
Voltage on ALDO1V8 Pin ($V_{ALDO1V8}$)	$V_{ALDO1V8} = 2.33 \times \left(\frac{DIAG_CODE}{65,535}\right) \times Voltage\ Range$
V_{DVCC}	$V_{DVCC} = 3.3 \times \left(\frac{DIAG_CODE}{65,535}\right) \times Voltage\ Range$
V_{IOVDD}	$V_{IOVDD} = 3.3 \times \left(\frac{DIAG_CODE}{65,535}\right) \times Voltage\ Range$
Measure of SENSEL_x Pin Voltage (V_{SENSEL_x})	$V_{SENSEL_x} = 12 \times \left(\frac{DIAG_CODE}{65,535}\right) \times Voltage\ Range$

DACs

There are three sources for the code loaded to the DAC. The typical option is to load a code to the DAC from the DAC_CODEx registers. The DAC can also be loaded from the DAC_CLR_CODEx registers when the 0x73D1 code (DAC clear key) is written to the CMD_KEY register (see Table 51). See the Clear Code Function section for more information on the clear functionality. The third option is to enable the digital linear slew that controls the rate at which the DAC code is loaded to the DAC.

The code loaded to the DAC from any of the three sources is also loaded to the DAC_ACTIVEx registers. The DAC_ACTIVEx registers contain the current code loaded to the DAC, irrespective of the code source.

LDAC Function

The LDAC function controls when the DACs are updated. To control the timing of the DAC updates, tie the $\overline{\text{LDAC}}$ pin high while programming the DAC_CODEx registers. To update the DAC code, pulse the $\overline{\text{LDAC}}$ pin low, or alternatively, program the 0x953A code (LDAC key) to the CMD_KEY register (see Table 51).

To ensure that the DAC is properly updated, only pulse the $\overline{\text{LDAC}}$ pin low after the SPI write to the DAC_CODEx registers is complete.

If simultaneous updates are not required on all four DACs, tie the $\overline{\text{LDAC}}$ pin permanently low to allow the DACS to instantly update after the DAC_CODEx registers are programmed.

When a DAC update takes place, the DAC_ACTIVEx registers are updated at the same time as a new DAC code is passed to the DAC.

Clear Code Function

The clear code function allows the user to clear the DACs to a preprogrammed code at any given time.

To clear an output channel, take the following steps.

1. Enable the clear option for the channel by setting the CLR_EN bit in the OUTPUT_CONFIGx register. The channel can now be cleared at any time.
2. Program the desired 13-bit clear code to the DAC_CLR_CODEx registers.
3. Write the DAC clear key to the CMD_KEY register to clear the DAC to the preprogrammed 13-bit code. If the CLR_EN bit is not set, the output remains in the current state.

When a DAC clear takes place, the DAC_ACTIVEx registers are updated at the same time as a new DAC code is passed to the DAC.

If a channel is cleared by writing to the DAC clear key, and if the $\overline{\text{LDAC}}$ pin is held low to update the DACs, the clear function takes priority over the LDAC function.

If a DAC update is required after a clear has taken place, program each individual DAC_CODEx register with the desired code.

Digital Linear Slew Rate Control

The digital linear slew rate control feature of the AD74413R controls the rate at which the output transitions to the new value. This slew rate control feature is available for both the current and voltage outputs.

When the slew rate control feature is disabled, the output value transitions at a rate limited by the output drive circuitry and the attached load.

To reduce the slew rate, enable the digital slew rate control feature via the OUTPUT_CONFIGx registers.

After the digital slew rate control feature is enabled, the output steps digitally at a rate defined by the user in the OUTPUT_CONFIGx registers. The SLEW_LIN_STEP bits dictate the number of codes per increment, and the SLEW_LIN_RATE bits dictate the rate at which the codes are updated. Table 22 shows the typical programmable slew rates for a zero-scale to full-scale (or full-scale to zero-scale) DAC update that are available on the AD74413R.

The DAC_ACTIVEx registers can monitor the progress of slewing to a target DAC code. These registers contain the code that is currently loaded to the DAC.

Note that if the digital slew rate control feature is enabled and the DAC clear key is written to the CMD_KEY register, the output slews at the preprogrammed slew rate to the programmed CLR_CODE bits in the DAC_CLR_CODEx registers.

HART Compliant Slew

An enhanced slew option is available to allow compatibility with the HART analog rate of change requirements. Set the SLEW_EN bit in the OUTPUT_CONFIGx register to enable this slew option.

Table 22. Programmable Slew Times for a Zero-Scale to Full-Scale Code Update

	Step Size (Codes), Programmable via SLEW_LIN_STEP Bits[1]			
Update Slew Rate, Programmable via SLEW_LIN_RATE Bits (kHz)	64	120	500	1820
4	31.7 ms	17 ms	4 ms	1 ms
64	2.0 ms	1.1 ms	259 µs	75.8 µs
150	858 µs	459 µs	113 µs	40.1 µs
240	520 µs	280 µs	73.6 µs	38.6 µs

[1] These are theoretical values. The final slew rate is limited by C_{LOAD} capacitor value.

DRIVING INDUCTIVE LOADS

It is recommended to use the digital slew rate control when driving inductive loads greater than approximately 4 mH. Controlling the output slew rate minimizes ringing when stepping the output current by minimizing the current rate of change (dI/dt).

If an open circuit is detected via the ALERT_STATUS register, it is recommended to set the I_{OUT} current to 0 mA before reconnecting the load to avoid ringing on the I/OP_x screw terminal.

RESET FUNCTION

After the AD74413R is reset, all registers are reset to the default state, and the calibration memory is refreshed. The device is configured in high impedance mode. A reset can be initiated in several ways.

The hardware reset is initiated by pulsing the $\overline{\text{RESET}}$ pin low. The $\overline{\text{RESET}}$ pulse width must comply with the specifications in Table 11.

A software reset is initiated by writing the 0x15FA code (Software Reset Key1) followed by the 0xAF51 code (Software Reset Key2) to the CMD_KEY register (see Table 51).

A reset can also be initiated via the thermal reset function, which is described in the Thermal Alert and Thermal Reset section.

If the $V_{DLDO1V8}$ drops below 1.62 V or if the V_{DVCC} drops below approximately 1.93 V, the internal power-on reset function resets the AD74413R. The device does not come out of reset until the $V_{DLDO1V8}$ and the V_{DVCC} rise above these voltage levels.

After a reset cycle completes, the RESET_OCCURRED bit is set in the ALERT_STATUS register. If an SPI transfer is attempted before the reset cycle is complete (see Table 11 for typical reset time), the CAL_MEM_ERR bit in the ALERT_STATUS register is also set to indicate that the calibration memory is not fully refreshed. After the reset time elapses, clear these bits in the ALERT_STATUS register before continuing to use the device.

THERMAL ALERT AND THERMAL RESET

If the AD74413R die temperature reaches 110°C, a high temperature error bit (HI_TEMP_ERR) is set in the ALERT_STATUS register to alert the user of increasing die temperature.

The device can also be configured to reset at higher die temperatures. To reset the device at higher temperatures, enable the thermal reset function by setting the EN_THERM_RST bit in the THERM_RST register. After this bit is set, the device goes through a full reset after the die temperature reaches 140°C.

FAULTS AND ALERTS

The AD74413R is equipped with several fault monitors to detect an error condition.

If an alert or fault condition occurs, the $\overline{\text{ALERT}}$ pin asserts. To determine the source of the alert condition, read the ALERT_STATUS register. This register contains a latched bit for each alert condition. After the error condition is removed, clear the activated flag by writing 1 to the location of the corresponding bits. See Table 45 for a detailed description of each alert condition.

The LIVE_STATUS register is a live representation of the error conditions. The bits in this register are not latched and are only cleared after the error condition is no longer present. A full list of the LIVE_STATUS bits is shown in Table 46.

The ALERT_MASK register prevents certain error conditions from activating the $\overline{\text{ALERT}}$ pin.

Channel Faults

Each channel is equipped with a V_{OUT} short-circuit error, an I_{OUT} open circuit error, and current input (I_{IN}) short-circuit error as described in the Device Functions section.

Note that the AD74413R is not designed to withstand more than one fault condition at any point in time. Manage faults as the faults appear and reset the channel, if necessary, to avoid overheating the device.

POWER SUPPLY MONITORS

The AD74413R includes four power supply monitors (PSMs) to detect a supply failure. If any of the supplies falls below a defined threshold (shown in Table 23), the corresponding bit is set in the ALERT_STATUS register.

Table 23. PSM Trip Levels

Power Supply Monitor	Typical Trip Level (V)
ALDO1V8	+1.35
DVCC	+1.93
AVDD	+9.26
ALDO5V	+4.05
Charge Pump	−1.65

GPO_x PINS

The AD74413R has four GPO_x pins, one per channel. Each channel GPO_x pin can be configured in the following ways:

- With a 100 kΩ pull-down resistor, the default state of the GPO_x pins
- As the logic outputs of the digital input functions
- As a logic high or low output
- In a high impedance state

The GPO_x configuration can be set via the GPO_SELECT bits within the GPO_CONFIGx registers. When configuring the GPO_x pins as logic outputs, the data of the pins can be written to the GPO_DATA bit in the GPO_CONFIGx registers. If parallel updates are required on all channels, the appropriate data can be written to the GPO_PARALLEL register before being written to the GPO_SELECT bits in the GPO_CONFIGx registers to enable parallel updates.

SPI INTERFACE AND DIAGNOSTICS

The AD74413R is controlled over a 4-wire serial interface with an 8-bit CRC. The input shift register is 32 bits wide, and data is loaded into the device MSB first under the control of SCLK. Data is clocked in on the falling edge of SCLK. Table 24 shows the structure of an SPI write frame.

Table 24. Writing to a Register

MSB			LSB
D31	**[D30:D24]**	**[D23:D8]**	**[D7:D0]**
Reserved	Register address	Data	CRC

SPI CRC

To ensure that data is received correctly in noisy environments, the AD74413R has a CRC implemented in the SPI interface. This CRC is based on an 8-bit CRC. The device controlling the AD74413R generates an 8-bit frame check sequence using the following polynomial:

$$C(x) = x^8 + x^2 + x^1 + 1$$

This frame check sequence is added to the end of the data-word, and the 32-bit data-word is sent to the AD74413R before taking the $\overline{\text{SYNC}}$ high pin.

The user must supply a frame 32 bits wide containing the 24 data bits and 8 CRC bits. If the CRC check is valid, the data is written to the selected register. If the CRC check fails, the data is ignored, the SPI_CRC_ERR status bit in the ALERT_STATUS register is asserted, and the $\overline{\text{ALERT}}$ pin goes low.

Clear the SPI_CRC_ERR bit (ALERT_STATUS register) by writing a 1, which returns the $\overline{\text{ALERT}}$ pin (assuming that there are no other active alerts). The SPI CRC error can be masked by writing to the relevant bit in the ALERT_MASK register.

SPI Interface SCLK Count Feature

An SCLK count feature is built into the SPI diagnostics. Only SPI frames with exactly 32 SCLK falling edges are accepted by the interface as a valid write. SPI frames of lengths other than 32, or a multiple of 32 in streaming mode, are ignored, and the SPI_SCLK_CNT_ERR bit flag asserts in the ALERT_STATUS register. Mask the SPI_SCLK_CNT_ERR bit via the ALERT_MASK register.

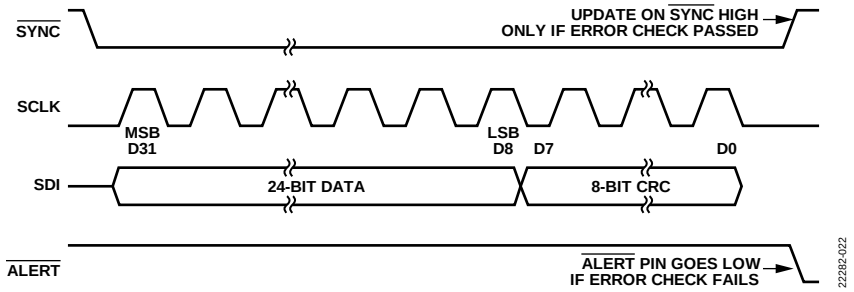


Figure 56. CRC Timing

Readback Mode

Two SPI frames are required to read a register location. In the first frame, the address of the register to be read is written to the READ_SELECT register. The second SPI frame consists of either a no operation (NOP) command, another write to the READ_SELECT register, or a write to any other register. The contents of the selected register are available on the SDO during the second frame. Figure 57 shows the timing diagram of the two-stage readback.

During the second read frame, Bits[D30:D24] provide status information on the SDO pin, as shown in Table 25 and Table 26. The content of these bits is determined by setting the SPI_RD_RET_INFO bit in the READ_SELECT register.

The data is shifted out MSB first. The MSB (Bit 31) is always set to 1 to allow the SPI master to detect if the SDO line is stuck low. If the SDO line is stuck low, a CRC of all 0s is calculated. In this case, the master cannot detect a stuck low condition. By tying the MSB high, the master can check this bit to detect a stuck low fault by checking the MSB is 1. Only this MSB is timed off the falling $\overline{\text{SYNC}}$ edge. All other bits are clocked out on the SCLK rising edge.

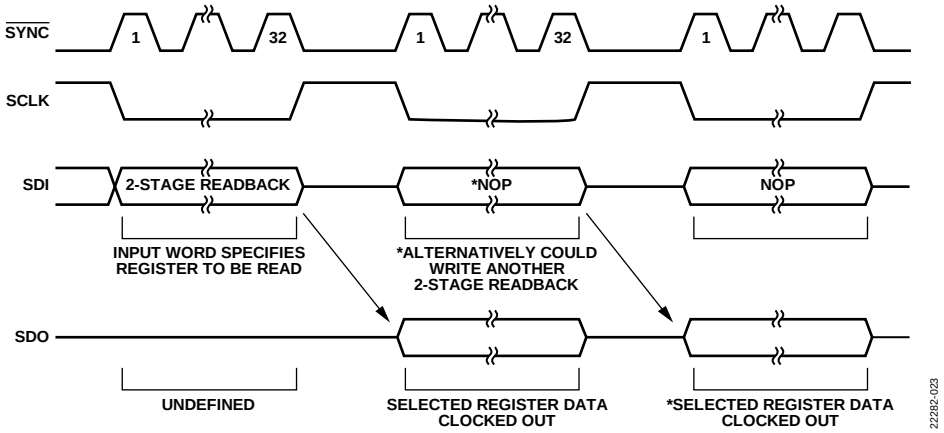


Figure 57. Two-Stage Readback Timing Diagram

Table 25. SDO Contents for a Read Operation when the SPI_RD_RET_INFO Bit = 0

MSB			LSB
D31	**[D30:D24]**	**[D23:D8]**	**[D7:D0]**
1	READBACK_ADDR[6:0]	Read data	CRC

Table 26. SDO Contents for a Read Operation when the SPI_RD_RET_INFO Bit = 1

MSB						LSB
D31	**D30**	**D29**	**D28**	**[D27:D24]**	**[D23:D8]**	**[D7:D0]**
1	0	ALERT	ADC_DATA_ RDY	DIN_COMP_OUT[3:0]	Read data	CRC

Streaming Mode

The AD74413R incorporates a streaming mode where the data is continuously clocked out on the SDO as long as there are sufficient SCLKs. The $\overline{\text{SYNC}}$ line must be kept low after the second frame of a two-stage readback (see the Readback Mode section). The AD74413R increments through addresses clocking out the 32-bit contents repeatedly. An SPI_SCLK_CNT_ERR error is reported if the transaction does not end with 32 + (n × 24) SCLK rising edges, where n is the number of transactions. Figure 58 shows the contents on the SDO line when streaming ADC data.

The data appearing on the SDO includes the register address (when the SPI_RD_RET_INFO is set to 0), the 16-bit data, and the 8-bit CRC.

If the $\overline{\text{SYNC}}$ pin is kept low and the clocks are applied, the data from the next sequential address is clocked out.

Writes to the register map are not supported in streaming mode.

Auto Readback

Auto readback allows the user to read from a selected register during every SPI transaction. To enable auto readback, set the AUTO_RD_EN bit in the READ_SELECT register.

If auto readback is disabled, perform a read as described in the Readback Mode section.

If auto readback is enabled, the contents of the address written to the READ_ADDR bits are output on the SDO lines during each SPI transfer.

At the end of readback sequence, if the $\overline{\text{SYNC}}$ pin is returned high, the device automatically reads the address previously written to the READ_SELECT register. If the $\overline{\text{SYNC}}$ pin is held low after the first read, the device streams through each consecutive address as described in the Streaming Mode section.

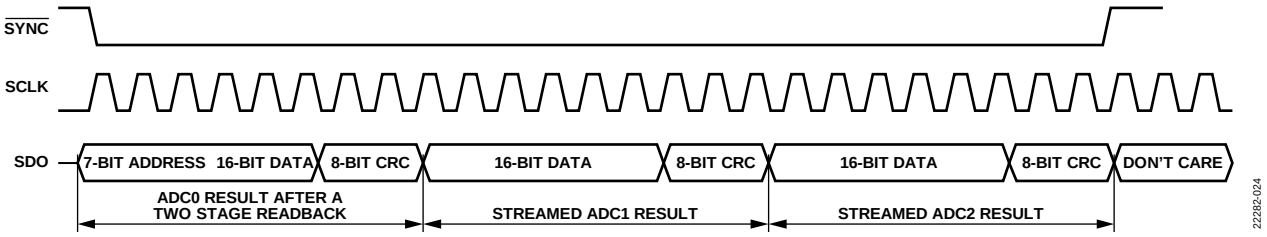


Figure 58. Streaming Mode SDO Contents

BOARD DESIGN AND LAYOUT CONSIDERATIONS

This section outlines the critical board design and layout considerations for the AD74413R.

To guarantee stability for the SENSEL_A pin, the SENSEL_B pin, the SENSEL_C pin, and the SENSEL_D pin, limit the capacitance to ground and the required 2 kΩ resistor to <10 pF.

To guarantee stability for the SENSEH_A pin, the SENSEH_B pin, the SENSEH_C pin, and the SENSEH_D pin, limit the capacitance to ground between the SENSEL_A pin, the SENSEL_B pin, SENSEL_C pin, or SENSEL_D pin and the required 2 kΩ resistor to <10 pF.

To guarantee stability for the CCOMP_A pin, the CCOMP_B pin, the CCOMP_C pin, and the CCOMP_D pin, limit the capacitance to ground between the pin and the C_{COMP} capacitor (if required) to <10 pF.

For optimal charge pump performance, connect the charge pump fly capacitor between the CPUMP_P pin and the CPUMP_N pin and place the capacitor as close as possible to the AD74413R

To optimize thermal performance, design the AD74413R boards with a minimum of four layers and with multiple thermal vias connecting the paddle to the bottom layer of the board. See the JEDEC JESD-51 specifications for more details. Users are recommended to thermally connect the exposed pad of the AD74413R to the thermal vias.

When grounding the AD74413R pins, it is recommended to connect all the AGNDx pins and DGND pins to a single ground plane. The I/ON_x screw terminals must also be tied to this ground plane.

The AGND_SENSE pin senses the voltage at the I/ON_x screw terminals and provides this voltage as an input to the ADC. It is not recommended to directly connect the AGND_SENSE pin to ground. Instead, users must route a single trace from the AGND_SENSE pin to the I/ON_x screw terminals. This connection can be done by connecting the AGND_SENSE pin and the four I/ON_x screw terminals to a common star point on the AD74413R board.

APPLICATIONS INFORMATION

Table 27 lists the external components that are recommended to operate the AD74413R.

Table 27. External Components

Component	Value			Voltage Rating (V)[1]	Recommended Component[1, 2]	Notes/Comments
	Min	Typical	Max			
Capacitors						
ALDO1V8 Decoupling	1 µF	2.2 µF		6.3	GRM21BR70J225MA01	
		0.1 µF		6.3	N/A	
DLDO1V8 Decoupling	1 µF	2.2 µF		6.3	GRM21BR70J225MA01	
		0.1 µF		6.3	N/A	
ALDO5V Decoupling		100 nF	470 nF	16	N/A	
DVCC Decoupling		10 µF		16	GRM21BR70J225MA01	Recommended on the DVCC pin (Pin 23) to ensure optimal performance of the charge pump.
		0.1 µF		16	N/A	One decoupling capacitor per DVCC pin.
IOVDD Decoupling		10 µF		16	N/A	If IOVDD is tied to DVCC, the additional 10 µF capacitor is not required.
		0.1 µF		16	N/A	
AVDD Decoupling		10 µF		50	N/A	
		0.1 µF		50	N/A	One decoupling capacitor per AVDD pin.
REFOUT Decoupling		0.1 µF	0.1 µF	6.3	N/A	
Charge Pump Fly		330 nF		10	GRM188R71A334KA61	Connect between the CPUMP_P pin and the CPUMP_N pin.
AVSS Charge Pump Reservoir		10 µF		16	N/A	
Screw Terminal		10 nF		100	N/A	
CCOMP_x Pin Compensation		220 pF		100	N/A	Recommended for total C_{LOAD} > 14 nF and tie between the CCOMP_x pin and the I/OP_x screw terminal.
SENSEHF_x Filter		10 nF		100	N/A	
SENSELF_x Filter		10 nF		100	N/A	
Resistors						
R_{SENSE}		100 Ω		N/A	N/A	R_{SENSE} accuracy directly affects current output, current input, and RTD accuracy. Resistors like VPG RWB100R0AL offer 0.05%, 2 ppm/°C.
SENSEH_x Precision		2 kΩ		N/A	N/A	The SENSEH_x resistor accuracy directly affects RTD specifications. Resistors like VPG RWB2k00AL offer 0.05%, 2 ppm/°C.
SENSEL_x		2 kΩ		N/A	N/A	1% accuracy.
SENSEHF_x Filter		10 kΩ		N/A	N/A	1% accuracy.
SENSELF_x Filter		10 kΩ		N/A	N/A	1% accuracy.
Other Components						
External FET				N/A	FDC5614P	Optional.
Screw Terminal TVS				N/A	SMCJ40CA	1500 W, 40 V TVS from STMicroelectronics.
Screw Terminal Isolation Diodes				N/A	BAV99WTIG	2 diodes per package.

[1] N/A means not applicable.
[2] Use recommended components or ones that are similar.

REGISTER MAP

Table 28 summarizes the register map for the AD74413R with information on how to read and write to and from the registers.

R indicates read only access, R/W indicates read and write access, R/W1C indicates read, write, or clear, and W indicates write only access.

Table 28. Register Summary

Address	Name[1]	Description	Reset	Access
0x00	NOP	NOP register	0x0000	R
0x01 to 0x04	CH_FUNC_SETUPx	Function setup registers per channel	0x0000	R/W
0x05 to 0x08	ADC_CONFIGx	ADC configuration registers per channel	0x0000	R/W
0x09 to 0x0C	DIN_CONFIGx	Digital input configuration registers per channel	0x000B	R/W
0x0D	GPO_PARALLEL	GPO parallel data register	0x0000	R/W
0x0E to 0x11	GPO_CONFIGx	GPO configuration registers per channel	0x0000	R/W
0x12 to 0x15	OUTPUT_CONFIGx	Output configuration registers per channel	0x0000	R/W
0x16 to 0x19	DAC_CODEx	DAC code registers per channel	0x0000	R/W
0x1A to 0x1D	DAC_CLR_CODEx	DAC clear code registers per channel	0x0000	R/W
0x1E to 0x21	DAC_ACTIVEx	DAC active code registers per channel	0x0000	R
0x22	DIN_THRESH	Digital input threshold register	0x0000	R/W
0x23	ADC_CONV_CTRL	ADC conversion control register	0x0000	R/W
0x24	DIAG_ASSIGN	Diagnostics select register	0x0000	R/W
0x25	DIN_COMP_OUT	Digital output level register	0x0000	R
0x26 to 0x29	ADC_RESULTx	ADC conversion results registers per channel	0x0000	R
0x2A to 0x2D	DIAG_RESULTx	Diagnostic results registers per diagnostic channel	0x0000	R
0x2E	ALERT_STATUS	Alert status register	0x8000	R/W1C
0x2F	LIVE_STATUS	Live status register	0x0000	R/W1C
0x3C	ALERT_MASK	Alert mask register	0x0000	R/W
0x3D to 0x40	DIN_COUNTERx	Debounced digital input count registers per channel.	0x0000	R
0x41	READ_SELECT	Readback select register	0x0000	R/W
0x43	THERM_RST	Thermal reset enable register	0x0000	R/W
0x44	CMD_KEY	Command register	0x0000	W
0x45	SCRATCH	Scratch or spare register	0x0000	R/W
0x46	SILICON_REV	Silicon revision register	0x0008	R

[1] x stands for Channel A, Channel B, Channel C, or Channel D in the register names.

NOP REGISTER

Address: 0x00, Reset: 0x0000, Name: NOP

Read only register. Writing to this register results in a no operation (NOP) command.

Table 29. Bit Descriptions for NOP

Bits	Bit Name	Description	Reset	Access
[15:0]	NOP	Write 0x0000 to perform a NOP command.	0x0	R

FUNCTION SETUP REGISTER PER CHANNEL

Address: 0x01 to 0x04 (Increments of 0x01), Reset: 0x0000, Name: CH_FUNC_SETUPx

Write to these four registers to select the functions for Channel A, Channel B, Channel C, and Channel D.

When the CH_FUNC_SETUPx registers are programmed, some fields in the corresponding ADC_CONFIGx registers and DIN_CONFIGx registers may change for that channel.

When changing the function for a channel, high-Z use case must be entered as an intermediate step before entering the new use case.

Table 30. Bit Descriptions for CH_FUNC_SETUPx

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
[3:0]	CH_FUNC	Sets the channel function. The default state on initial power-up or reset is high impedance. Values other than those listed in this table select the high impedance function. 0000: high impedance. ADC is functional in this mode. 0001: voltage output. Force voltage measure current (FVMI). 0010: current output, FVMI. 0011: voltage input, which measures the voltage across the I/OP_x to I/ON_x screw terminals. 0100: current input externally powered. 0101: current input loop powered. 0110: resistance measurement. 0111: digital input (logic). 1000: digital input (loop powered). 1001: current input externally powered with HART termination impedance. 1010: current input loop powered with HART termination impedance.	0x0	R/W

ADC CONFIGURATION REGISTER PER CHANNEL

Address: 0x05 to 0x08 (Increments of 0x01), Reset: 0x0000, Name: ADC_CONFIGx

These four registers select the ADC settings for each channel.

Table 31. Bit Descriptions for ADC_CONFIGx

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:5]	RANGE	Selects the ADC range. Values outside of those listed in this table select the 0 V to 10 V range. Note that these bits may change when the corresponding CH_FUNC_SETUPx register is written to. 000: 0 V to 10 V range. Typically used to measure the voltage across the I/OP_x to I/ON_x screw terminals. 001: 2.5 V range, RTD and input current (I_{IN}) externally powered. Typically used to measure the current flowing through R_{SENSE} and into the AD74413R when the SENSELF_x voltage is higher than the SENSEHF_x voltage (I_{IN} externally powered). This voltage range is also used for RTD voltage measurements across the I/OP_x to I/ON_x screw terminals. 010: 2.5 V range, I_{IN} loop powered. Typically used to measure the current flowing through R_{SENSE} and out of the AD74413R when the SENSELF_x voltage is less than the SENSEHF_x voltage (I_{IN} loop powered). 011:−2.5 V to +2.5 V range. Typically used to measure the bidirectional current across R_{SENSE} when in voltage output mode. 100: −104.16 mV to +104.16 mV range. Typically used to measure thermocouple voltages at the I/OP_x and I/ON_x screw terminals.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
[4:3]	EN_50_60_HZ	Enables the 50 Hz and 60 Hz rejection and sets the ADC conversion rate for channel conversions. There is a separate bit in the ADC_CONV_CTRL register that sets the conversion rates for the diagnostic conversions. 00: enables the 50 Hz and 60 Hz rejection, resulting in a sampling rate of 20 SPS. 01: disables the 50 Hz and 60 Hz rejection, resulting in a sampling rate of 4.8 kSPS. 10: enables the 50 Hz and 60 Hz rejection and HART noise rejection, resulting in a sampling rate of 10 SPS. 11: disables the 50 Hz and 60 Hz rejection, resulting in a sampling rate of 1.2 kSPS.	0x0	R/W
2	CH_200K_TO_GND	Enables the 200 kΩ resistor to ground. This bit is set to 0 when the corresponding CH_FUNC_SETUPx register is programmed, irrespective of the function.	0x0	R/W
[1:0]	ADC_MUX	Selects the ADC input node. Values outside of those listed in this table select the voltage across the I/OP_x to I/ON_x screw terminals. These bits may change when the corresponding CH_FUNC_SETUPx register is written to. 00: voltage between the I/OP_x screw terminals and the AGND_SENSE pin. 01: voltage across the 100 Ω resistor. Typically used to measure the current.	0x0	R/W

DIGITAL INPUT CONFIGURATION REGISTER PER CHANNEL

Address: 0x09 to 0x0C (Increments of 0x01), Reset: 0x000B, Name: DIN_CONFIGx

These four registers configure the digital input for each channel.

Table 32. Bit Descriptions for DIN_CONFIGx

Bits	Bit Name	Description	Reset	Access
15	COUNT_EN	Enables DIN count. If INV_DIN_COMP_OUT is 0, the positive edges of the debounced DIN are counted. If INV_DIN_COMP_OUT is 1, the negative edges of the debounced DIN are counted. The count is reflected in the DIN_COUNTERx register.	0x0	R/W
14	COMP_INPUT_FILTERED	Set to 0 to select the unfiltered input to the comparator on the SENSELF_x pin. Set to 1 to select the filtered input to the comparator on the SENSELF_x pin.	0x0	R/W
13	INV_DIN_COMP_OUT	Set to 1 to invert the output from the digital input comparator.	0x0	R/W
12	COMPARATOR_EN	Set to 1 to enable the comparator. This bit may change when the corresponding CH_FUNC_SETUPx register is programmed.	0x0	R/W
11	DIN_RANGE	Selects the DIN_SINK current range. 0: Range 0. See Table 7 for typical range, resolution, and series resistance values. 1: Range 1. See Table 7 for typical range, resolution, and series resistance values.	0x0	R/W
[10:6]	DIN_SINK	Sets the sink current in digital input logic mode. These bits allow the current to be programmed within the range selected by the DIN_RANGE bit. Set the DIN_SINK bits to 0x00 to turn off the current sink. Note that these bits are set to 0 when the corresponding CH_FUNC_SETUPx register is written to, irrespective of the function.	0x0	R/W
5	DEBOUNCE_MODE	This bit determines how the digital input debounce logic operates as described in the Digital Input Logic section. 0: Debounce Mode 0. Integrator method is used. A counter increments when the comparator input is asserted and decrements when the signal is deasserted. 1: Debounce Mode 1. A simple counter increments while a signal is asserted, and the counter value resets when the signal deasserts.	0x0	R/W
[4:0]	DEBOUNCE_TIME	These bits configure the debounce time in the digital input modes. Reset the value for these bits to 240 µs. Set DEBOUNCE_TIME to 0x0 to bypass the debounce circuit.	0xB	R/W

GPO PARALLEL DATA REGISTER

Address: 0x0D, Reset: 0x0000, Name: GPO_PARALLEL

This register sets the logic level on the GPO_x pins simultaneously when the GPO_SELECT bits within the GPO_CONFIGx registers are configured to enable the parallel writes.

Table 33. Bit Descriptions for GPO_PARALLEL

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	GPO_PAR_DATA_D	When a pad is configured for parallel GPO data, this bit sets the logic level of the GPO_D pin.	0x0	R/W
2	GPO_PAR_DATA_C	When a pad is configured for parallel GPO data, this bit sets the logic level of the GPO_C pin.	0x0	R/W
1	GPO_PAR_DATA_B	When a pad is configured for parallel GPO data, this bit sets the logic level of the GPO_B pin.	0x0	R/W
0	GPO_PAR_DATA_A	When a pad is configured for parallel GPO data, this bit sets the logic level of the GPO_A pin.	0x0	R/W

GPO CONFIGURATION REGISTER PER CHANNEL

Address: 0x0E to 0x11 (Increments of 0x01), Reset: 0x0000, Name: GPO_CONFIGx

These four registers configure the GPO_x pins for each channel.

Table 34. Bit Descriptions for GPO_CONFIGx

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	GPO_DATA	This bit sets the GPO logic state when the GPO_SELECT bit = 001 0: drives a logic low on the GPO_x pin. 1: drives a logic high on the GPO_x pin.	0x0	R/W
[2:0]	GPO_SELECT	Selects the GPO mode. Values outside of those listed in this table place the GPO_x pin in a high impedance state. 000: the GPO_x pin is configured with a 100 kΩ pull-down resistor. 001: the GPO_x pin logic state is set by the GPO_DATA bit. 010: the GPO_x pin is configured by the GPO_PAR_DATA_x bit in the GPO_PARALLEL register. Note this mode is for parallel updates to all GPO_x pins. 011: the GPO_x pin is configured to output the debounced comparator output of the digital input circuit. 100: The GPO_x pin is configured in a high impedance state.	0x0	R/W

OUTPUT CONFIGURATION REGISTER PER CHANNEL

Address: 0x12 to 0x15 (Increments of 0x01), Reset: 0x0000, Name: OUTPUT_CONFIGx

These four registers configure the output mode settings for each channel.

Table 35. Bit Descriptions for OUTPUT_CONFIGx

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:6]	SLEW_EN	Set to 1 to slew to the requested DAC code. 00: disables slewing. Slewing stops immediately when disabled. 01: enable linear slew on the DAC output. 10: enables HART compliant slewing on the DAC output.	0x0	R/W
[5:4]	SLEW_LIN_STEP	Step size for digital linear slew. 00: digital linear slew step size of 64 decimal codes. 01: digital linear slew step size of 120 decimal codes. 10: digital linear slew step size of 500 decimal codes. 11: digital linear slew step size of 1820 decimal codes.	0x0	R/W
[3:2]	SLEW_LIN_RATE	Update rate for digital linear slew. 00: the digital linear slew controller updates at a rate of 4 kHz. 01: the digital linear slew controller updates at a rate of 64 kHz. 10: the digital linear slew controller updates at a rate of 150 kHz. 11: the digital linear slew controller updates at a rate of 240 kHz.	0x0	R/W
1	CLR_EN	Enables clear function for the channel. Set this bit to enable the clear function. If this bit is set, the channel clears to the code programmed in the DAC_CLR_CODEx registers when the DAC clear key is written.	0x0	R/W
0	I_LIMIT	This bit sets the source current limit in V_{OUT} mode. Note that the V_{OUT} sink current limit is typically fixed at 4.5 mA 0: 30 mA current limit. 29 mA typical current limit. 1: 7.5 mA current limit. 7 mA typical current limit.	0x0	R/W

DAC CODE REGISTER PER CHANNEL

Address: 0x16 to 0x19 (Increments of 0x01), Reset: 0x0000, Name: DAC_CODEx

Table 36. Bit Descriptions for DAC_CODEx

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R
[12:0]	DAC_CODE	13-bit DAC code data for the channel.	0x0	R/W

DAC CLEAR CODE REGISTER PER CHANNEL

Address: 0x1A to 0x1D (Increments of 0x01), Reset: 0x0000, Name: DAC_CLR_CODEx

The DAC_CLR_CODEx value is loaded to the DACs when the CLR_EN bit in the OUTPUT_CONFIGx registers is asserted and the DAC clear key is written.

Table 37. Bit Descriptions for DAC_CLR_CODEx

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R
[12:0]	CLR_CODE	DAC clear code for the channel.	0x0	R/W

DAC ACTIVE CODE REGISTER PER CHANNEL

Address: 0x1E to 0x21 (Increments of 0x01), Reset: 0x0000, Name: DAC_ACTIVEx

The current value of the code loaded to the DAC. If slewing is enabled, this register reflects the current slew step.

Table 38. Bit Descriptions for DAC_ACTIVEx

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R
[12:0]	DAC_ACTIVE_CODE	The active DAC code on the channel. The contents of this register can determine if the $\overline{\text{LDAC}}$ pin is toggled low and the current slew step if the digital slew is enabled.	0x0	R

DIGITAL INPUT THRESHOLD REGISTER

Address: 0x22, Reset: 0x0000, Name: DIN_THRESH

This register selects the comparator threshold used by the channels configured to use the digital input function.

Table 39. Bit Descriptions for DIN_THRESH

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
[5:1]	COMP_THRESH	Comparator threshold.	0x0	R/W
0	DIN_THRESH_MODE	This bit sets the reference to the digital input threshold DAC. 0: threshold is set between GND and the AVDD pin. The threshold scales with V_{AVDD}. 1: threshold is set between GND and 16 V. The threshold does not scale with V_{AVDD}.	0x0	R/W

ADC CONVERSION CONTROL REGISTER

Address: 0x23, Reset: 0x0000, Name: ADC_CONV_CTRL

This register controls the ADC conversions that must be performed. If enabling a sequence, ensure that the previous sequence is complete. For example, wait until the ADC_BUSY bit within the LIVE_STATUS register is 0 before enabling the next sequence.

Table 40. Bit Descriptions for ADC_CONV_CTRL

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	EN_50_60_HZ_REJ_DIAG	Enable 50 Hz or 60 Hz rejection for diagnostics. Set this bit to 0 to disable 50 Hz or 60 Hz rejection, which results in a sampling rate of 4.8 kSPS for diagnostics. Set this bit to 1 to enable 50 Hz or 60 Hz rejection, which results in a sampling rate of 20 samples per second for diagnostics.	0x0	R/W
[9:8]	CONV_SEQ	Selects single or continuous mode. 00: stops continuous conversions and leaves the ADC powered up or powers up the ADC. If exiting ADC power-down, it takes approximately 100 µs to power up the ADC. The ADC_BUSY bit is set to 1 while the ADC is powering up. If using the CONV_SEQ bits to exit ADC power-down, wait for the ADC to power up before writing to these bits again to start a single or continuous sequence. 01: starts single sequence conversion and performs a single conversion on each enabled channel and diagnostic. These bits do not clear when a conversion completes. To enable a subsequent conversion, the user must repeat the write to enable the conversion. If the ADC is powered down, writing 01 to the CONV_SEQ bits automatically powers up the ADC. The user must wait 100 µs before starting conversions. 10: starts continuous conversions. Sequences continuously through the enabled channels and diagnostics. The enabled channels and diagnostics cannot be modified if a continuous sequence is in progress. To modify the enabled channels, stop the sequence, modify the enabled channels and diagnostics, and start the sequence again. If the ADC is powered down, writing a 01 to the CONV_SEQ bits automatically powers up the ADC. The user must wait 100 µs before starting conversions. If moving from continuous conversion mode to single conversion mode, enter idle mode first. 11: stops continuous conversions and powers down the ADC.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
7	DIAG_3_EN	Enables conversions on Diagnostic 3	0x0	R/W
6	DIAG_2_EN	Enables conversions on Diagnostic 2.	0x0	R/W
5	DIAG_1_EN	Enables conversions on Diagnostic 1.	0x0	R/W
4	DIAG_0_EN	Enables conversions on Diagnostic 0.	0x0	R/W
3	CH_D_EN	Enables conversions on Channel D.	0x0	R/W
2	CH_C_EN	Enables conversions on Channel C.	0x0	R/W
1	CH_B_EN	Enables conversions on Channel B.	0x0	R/W
0	CH_A_EN	Enables conversions on Channel A.	0x0	R/W

DIAGNOSTICS SELECT REGISTER

Address: 0x24, Reset: 0x0000, Name: DIAG_ASSIGN

This register assigns diagnostics to the four available diagnostics inputs.

Table 41. Bit Descriptions for DIAG_ASSIGN

Bits	Bit Name	Description	Reset	Access
[15:12]	DIAG3_ASSIGN	Selects the diagnostic assigned to the DIAG_RESULTx registers, Bit 3. Values other than those listed in this table select the V_{AGND} input. 0000: assigns the AGND pin to Diagnostic 3. 0001: assigns the temperature sensor to Diagnostic 3. 0010: assigns the AVDD pin to Diagnostic 3. 0011: assigns the charge pump voltage, V_{AVSS}, to Diagnostic 3. 0100: assigns the REFOUT pin to Diagnostic 3. 0101: assigns the ALDO5V pin to Diagnostic 3. 0110: assigns the ALDO1V8 pin to Diagnostic 3. 0111: assigns the DLDO1V8 pin to Diagnostic 3. 1000: assigns the DVCC pin to Diagnostic 3. 1001: assigns the IOVDD pin to Diagnostic 3. 1010: assigns the SENSEL_A pin to Diagnostic 3. Allows the user to check the terminal voltage. 1011: assigns the SENSEL_B pin to Diagnostic 3. Allows the user to check the terminal voltage. 1100: assigns the SENSEL_C pin to Diagnostic 3. Allows the user to check the terminal voltage. 1101: assigns the SENSEL_D pin to Diagnostic 3. Allows the user to check the terminal voltage. 1110: assigns the LVIN pin to Diagnostic 3.	0x0	R/W
[11:8]	DIAG2_ASSIGN	Selects the diagnostic assigned to the DIAG_RESULTx registers, Bit 2. Values other than those listed in this table select the AGND pin. 0000: assigns the AGND pin to Diagnostic 2. 0001: assigns the temperature sensor to Diagnostic 2. 0010: assigns the AVDD pin to Diagnostic 2. 0011: assigns V_{AVSS} to Diagnostic 2. 0100: assigns the REFOUT pin to Diagnostic 2. 0101: assigns the ALDO5V pin to Diagnostic 2. 0110: assigns the ALDO1V8 pin to Diagnostic 2. 0111: assigns the DLDO1V8 pin to Diagnostic 2. 1000: assigns the DVCC pin to Diagnostic 2. 1001: assigns the IOVDD pin to Diagnostic 2. 1010: assigns the SENSEL_A pin to Diagnostic 2. Allows the user to check the terminal voltage. 1011: assigns the SENSEL_B pin to Diagnostic 2. Allows the user to check the terminal voltage. 1100: assigns the SENSEL_C pin to Diagnostic 2. Allows the user to check the terminal voltage. 1101: assigns the SENSEL_D pin to Diagnostic 2. Allows the user to check the terminal voltage. 1110: assigns the LVIN pin to Diagnostic 2.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
[7:4]	DIAG1_ASSIGN	Selects the diagnostic assigned to the DIAG_RESULTx registers, Bit 1. Values other than those listed in this table select the AGND pin. 0000: assigns the AGND pin to Diagnostic 1. 0001: assigns the temperature sensor to Diagnostic 1. 0010: assigns the AVDD pin to Diagnostic 1. 0011: assigns the V_{AVSS} to Diagnostic 1. 0100: assigns the REFOUT pin to Diagnostic 1. 0101: assigns the ALDO5V pin to Diagnostic 1. 0110: assigns the ALDO1V8 pin to Diagnostic 1. 0111: assigns the DLDO1V8 pin to Diagnostic 1. 1000: assigns the DVCC pin to Diagnostic 1. 1001: assigns the IOVDD pin to Diagnostic 1. 1010: assigns the SENSEL_A pin to Diagnostic 1. Allows the user to check the terminal voltage. 1011: assigns the SENSEL_B to Diagnostic 1. Allows the user to check the terminal voltage. 1100: assigns the SENSEL_C pin to Diagnostic 1. Allows the user to check the terminal voltage. 1101: assigns the SENSEL_D pin to Diagnostic 1. Allows the user to check the terminal voltage. 1110: assigns the LVIN pin to Diagnostic 1.	0x0	R/W
[3:0]	DIAG0_ASSIGN	Selects the diagnostic assigned to the DIAG_RESULTx registers, Bit 0. Values other than those listed in this table select the AGND pin. 0000: assigns the AGND pin to Diagnostic 0. 0001: assigns the temperature sensor to Diagnostic 0. 0010: assigns the AVDD pin to Diagnostic 0. 0011: assigns V_{AVSS} to Diagnostic 0. 0100: assigns the REFOUT pin to Diagnostic 0. 0101: assigns the ALDO5V pin to Diagnostic 0. 0110: assigns the ALDO1V8 pin to Diagnostic 0. 0111: assigns the DLDO1V8 pin to Diagnostic 0. 1000: assigns the DVCC pin to Diagnostic 0. 1001: assigns the IOVDD pin to Diagnostic 0. 1010: assigns the SENSEL_A pin to Diagnostic 0. Allows the user to check the terminal voltage. 1011: assigns the SENSEL_B pin to Diagnostic 0. Allows the user to check the terminal voltage. 1100: assigns the SENSEL_C pin to Diagnostic 0. Allows the user to check the terminal voltage. 1101: assigns the SENSEL_D pin to Diagnostic 0. Allows the user to check the terminal voltage. 1110: assigns the LVIN pin to Diagnostic 0.	0x0	R/W

DIGITAL OUTPUT LEVEL REGISTER

Address: 0x25, Reset: 0x0000, Name: DIN_COMP_OUT

For digital input mode, select the SENSEL_x or SENSELF_x pins via the DIN_CONFIGx registers. The value of the selected pin is compared to a threshold voltage programmed in the DIN_THRESH register. The output of this comparison is fed into a programmable debounce circuit. The DIN_COMP_OUT register shows the output of the debounce circuit for each channel.

Table 42. Bit Descriptions for DIN_COMP_OUT

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	DIN_COMP_OUT_D	Debounced digital input state of Channel D.	0x0	R
2	DIN_COMP_OUT_C	Debounced digital Input state of Channel C.	0x0	R
1	DIN_COMP_OUT_B	Debounced digital Input state of Channel B.	0x0	R
0	DIN_COMP_OUT_A	Debounced digital Input state of Channel A.	0x0	R

ADC CONVERSION RESULTS REGISTER PER CHANNEL

Address: 0x26 to 0x29 (Increments of 0x01), Reset: 0x0000, Name: ADC_RESULTx

These four registers contain the 16-bit ADC conversion results for each channel.

Table 43. Bit Descriptions for ADC_RESULTx

Bits	Bit Name	Description	Reset	Access
[15:0]	CH_ADC_RESULT	Contains the 16-bit result of the ADC conversion on Channel x.	0x0	R

DIAGNOSTIC RESULTS REGISTERS PER DIAGNOSTIC CHANNEL

Address: 0x2A to 0x2D (Increments of 0x01), Reset: 0x0000, Name: DIAG_RESULTx

These four registers contain the four 16-bit diagnostic ADC conversion results.

Table 44. Bit Descriptions for DIAG_RESULTx

Bits	Bit Name	Description	Reset	Access
[15:0]	DIAG_RESULT	Contains the 16-bit diagnostic result on Diagnostic Channel x.	0x0	R

ALERT STATUS REGISTER

Address: 0x2E, Reset: 0x8000, Name: ALERT_STATUS

This register contains the alert status of some of the alert status bits. Write 1 to clear any of the bits in this register.

Table 45. Bit Descriptions for ALERT_STATUS

Bits	Bit Name	Description	Reset	Access
15	RESET_OCCURRED	Reset occurred. This bit is asserted after a reset event, which asserts the $\overline{\text{ALERT}}$ pin after the reset. Write a 1 to this bit to clear the flag. Note that a mask bit is not provided for this bit.	0x1	R/W1C
14	CAL_MEM_ERR	Calibration Memory Error. This flag asserts under the following two conditions: When a calibration memory CRC error or an uncorrectable error correcting code (ECC) error is detected on the calibration memory upload. It is not possible to clear this bit if there is a CRC error or uncorrectable ECC error. It is recommended to reset the device and check the supplies in this situation. When there is an attempted SPI access to a register before the calibration memory refresh is complete. Do not address the device until the calibration memory is refreshed. Writing 1 to this bit clears the flag, if the flag is asserted due to this condition.	0x0	R/W1C
13	SPI_CRC_ERR	SPI CRC error detected. This bit is asserted if an invalid CRC is received.	0x0	R/W1C
12	SPI_SCLK_CNT_ERR	SPI SCLK count error detected. This bit is asserted if an SPI command is applied but 32 SCLKs are not provided.	0x0	R/W1C
11	ADC_SAT_ERR	ADC Saturation Error. ADC may be outside the user selected measurement range.	0x0	R/W1C
10	ADC_CONV_ERR	ADC Conversion Error. ADC results may be outside the selected measurement range.	0x0	R/W1C
9	ALDO1V8_ERR	ALDO1V8 Power Supply Monitor Error. This bit is asserted when the ALDO1V8 pin falls below 1.35 V.	0x0	R/W1C
8	DVCC_ERR	DVCC Power Supply Monitor Error. This bit is asserted when the DVCC pin falls below 1.93 V.	0x0	R/W1C
7	AVDD_ERR	AVDD Power Supply Monitor Error. This bit is asserted when the AVDD pin falls below 9.26 V.	0x0	R/W1C
6	ALDO5V_ERR	ALDO5V Power Supply Monitor Error. This bit is asserted when the ALDO5V pin falls below 4.05 V.	0x0	R/W1C
5	CHARGE_PUMP_ERR	Charge pump error detected. This bit is asserted when the AVSS pin rises above −1.65 V.	0x0	R/W1C
4	HI_TEMP_ERR	High temperature detected. After the die temperature typically reaches 115°C, this bit is asserted.	0x0	R/W1C

Bits	Bit Name	Description	Reset	Access
3	VI_ERR_D	Voltage or current error detected on Channel D. This bit is interpreted differently depending on which of the following functions are selected in the CH_FUNC_SETUPD register: Voltage output: short-circuit error. The error condition is debounced for 2 ms before the status bit is set. Current output: open circuit error. The error condition is debounced for 2 ms before the status bit is set. Current input, loop powered: short-circuit error. A short to ground is detected if the digital input comparator is enabled as described in Current Input Loop Powered section with a trip point of AVDD/2 and the digital output is inverted via the INV_DIN_COMP_OUT bit in the DIN_CONFIGx registers. The debounce time of this error detect is user-programmable, via the DEBOUNCE_TIME bit in the DIN_CONFIGx registers. Current input, externally powered: short-circuit error. A current source >25 mA is detected if the digital input comparator is enabled as described in Current Input Loop Powered section with a trip point of AVDD/2. The debounce time of this error detect is user-programmable via the DEBOUNCE_TIME bits in the DIN_CONFIGx registers.	0x0	R/W1C
2	VI_ERR_C	Voltage or current error detected on Channel C. This bit is interpreted differently depending on which of the following functions is selected in the CH_FUNC_SETUPC register: Voltage output: short-circuit error. The error condition is debounced for 2 ms before the status bit is set. Current output: open circuit error. The error condition is debounced for 2 ms before the status bit is set. Current input, loop powered: short-circuit error. A short to ground is detected if the digital input comparator is enabled as described in Current Input Loop Powered section with a trip point of AVDD/2 and the digital output is inverted via the INV_DIN_COMP_OUT bit in the DIN_CONFIGx register. The debounce time of this error detect is user-programmable, via the DEBOUNCE_TIME bits in the DIN_CONFIGx register. Current input, externally powered: short-circuit error. A current source >25 mA is detected if the digital input comparator is enabled as described in Current Input Loop Powered section with a trip point of AVDD/2. The debounce time of this error detect is user-programmable via the DEBOUNCE_TIME bits in the DIN_CONFIGx register.	0x0	R/W1C
1	VI_ERR_B	Voltage or current error detected on Channel B. This bit is interpreted differently depending on which of the following functions is selected in the CH_FUNC_SETUPB register: Voltage output: short-circuit error. The error condition is debounced for 2 ms before the status bit is set. Current output: open circuit error. The error condition is debounced for 2 ms before the status bit is set. Current input, loop powered: short-circuit error. A short to ground is detected if the digital input comparator is enabled as described in Current Input Loop Powered section with a trip point of AVDD/2 and the digital output is inverted via the INV_DIN_COMP_OUT bit in the DIN_CONFIGx registers. The debounce time of this error detect is user-programmable via the DEBOUNCE_TIME bits in the DIN_CONFIGx registers. Current input, externally powered: short-circuit error. A current source >25 mA is detected if the digital input comparator is enabled as described in Current Input Loop Powered section with a trip point of AVDD/2. The debounce time of this error detect is user-programmable via the DEBOUNCE_TIME bits in the DIN_CONFIGx registers.	0x0	R/W1C
0	VI_ERR_A	Voltage or current error detected on Channel A. This bit is interpreted differently depending on which of the following function selected in the CH_FUNC_SETUPA register: Voltage output: short-circuit error. The error condition is debounced for 2 ms before the status bit is set. Current output: open circuit error. The error condition is debounced for 2 ms before the status bit is set. Current input, loop powered: short-circuit error. A short to ground is detected if the digital input comparator is enabled as described in Current Input Loop Powered section with a trip point of AVDD/2 and the digital output is inverted via the INV_DIN_COMP_OUT bit in the DIN_CONFIGx registers. The debounce time of this error detect is user-programmable via the DEBOUNCE_TIME bits in the DIN_CONFIGx registers. Current input, externally powered: short-circuit error. A current source >25 mA is detected if the digital input comparator is enabled as described in Current Input Loop Powered section with a trip point of AVDD/2. The debounce time of this error detect is user-programmable via the DEBOUNCE_TIME bits in the DIN_CONFIGx registers.	0x0	R/W1C

LIVE STATUS REGISTER

Address: 0x2F, Reset: 0x0000, Name: LIVE_STATUS

This register contains the live status of some of the status bits. The bits in this register are not latched and directly reflect the status bits.

Table 46. Bit Descriptions for LIVE_STATUS

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	ADC_DATA_RDY	ADC data ready. The ADC_DATA_RDY bit asserts when a conversion cycle has completed. The bit stays asserted until a user writes 1 to clear the bit. In single conversion mode, the ADC_RDY pin follows the ADC_DATA_RDY bit and only deasserts when the ADC_DATA_RDY bit is cleared. In continuous conversion mode, the ADC_RDY pin returns high after 24 µs.	0x0	R/W1C
13	ADC_BUSY	ADC busy status bit.	0x0	R
[12:10]	ADC_CH_CURR	The channel and diagnostics currently being converted by the ADC. 000: Channel A. 001: Channel B. 010: Channel C. 011: Channel D. 100: Diagnostics 0. 101: Diagnostics 1. 110: Diagnostics 2. 111: Diagnostics 3.	0x0	R
9	ALDO1V8_STATUS	Live status of the ALDO1V8_ERR bit.	0x0	R
8	DVCC_STATUS	Live status of the DVCC_ERR bit.	0x0	R
7	AVDD_STATUS	Live status of the AVDD_ERR bit.	0x0	R
6	ALDO5V_STATUS	Live status of the ALDO5V_ERR bit.	0x0	R
5	CHARGE_PUMP_STATUS	Live status of the CHARGE_PUMP_ERR bit.	0x0	R
4	HI_TEMP_STATUS	Live status of the HI_TEMP_ERR bit. If the die temperature is typically at or above 115°C, the HI_TEMP_STATUS bit is asserted.	0x0	R
3	VI_ERR_CURR_D	Live status of the VI_ERR_D bit.	0x0	R
2	VI_ERR_CURR_C	Live status of the VI_ERR_C bit.	0x0	R
1	VI_ERR_CURR_B	Live status of the VI_ERR_B bit.	0x0	R
0	VI_ERR_CURR_A	Live status of the VI_ERR_A bit.	0x0	R

ALERT MASK REGISTER

Address: 0x3C, Reset: 0x0000, Name: ALERT_MASK

This register masks the alert status bits, outlined in the ALERT_STATUS register, from activating the $\overline{\text{ALERT}}$ pin. The position of mask bits in this register line up with the corresponding status bits in the ALERT_STATUS register.

Table 47. Bit Descriptions for ALERT_MASK

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	CAL_MEM_ERR_MASK	Mask bit for the CAL_MEM_ERR bit.	0x0	R/W
13	SPI_CRC_ERR_MASK	Mask bit for the SPI_CRC_ERR bit.	0x0	R/W
12	SPI_SCLK_CNT_ERR_MASK	Mask bit for the SPI_SCLK_CNT_ERR bit.	0x0	R/W
11	ADC_SAT_ERR_MASK	Mask bit for the ADC_SAT_ERR bit.	0x0	R/W
10	ADC_CONV_ERR_MASK	Mask bit for the ADC_CONV_ERR bit.	0x0	R/W
9	ALDO1V8_ERR_MASK	Mask bit for the ALDO1V8_ERR bit.	0x0	R/W
8	DVCC_ERR_MASK	Mask bit for the DVCC_ERR bit.	0x0	R/W
7	AVDD_ERR_MASK	Mask bit for the AVDD_ERR bit.	0x0	R/W
6	ALDO5V_ERR_MASK	Mask bit for the ALDO5V_ERR bit.	0x0	R/W
5	CHARGE_PUMP_ERR_MASK	Mask bit for the CHARGE_PUMP_ERR bit.	0x0	R/W
4	HI_TEMP_ERR_MASK	Mask bit for the HI_TEMP_ERR bit.	0x0	R/W
3	VI_ERR_MASK_D	Mask bit for the VI_ERR_D bit.	0x0	R/W
2	VI_ERR_MASK_C	Mask bit for the VI_ERR_C bit.	0x0	R/W
1	VI_ERR_MASK_B	Mask bit for the VI_ERR_B bit.	0x0	R/W
0	VI_ERR_MASK_A	Mask bit for the VI_ERR_A bit.	0x0	R/W

DEBOUNCED DIN COUNT REGISTER PER CHANNEL

Address: 0x3D to 0x40 (Increments of 0x01), Reset: 0x0000, Name: DIN_COUNTERx

This counter is enabled when the COUNT_EN bit in DIN_CONFIGx register is set. The INV_DIN_COMP_OUT bit inverts the deglitched output, allowing the counter increment edge to be modified.

Table 48. Bit Descriptions for DIN_COUNTERx

Bits	Bit Name	Description	Reset	Access
[15:0]	DIN_CNT	This counter is enabled when the COUNT_EN bit in the DIN_CONFIGx register is set. The count is frozen when the enable signal is low. This counter value rolls over from full scale back to 0. Therefore, read this register often enough to avoid unexpected roll over. When INV_DIN_COMP_OUT is set to 0, the counter increments on the rising digital input edges. When INV_DIN_COMP_OUT is set to 1, the counter increments on the falling digital input edges.	0x0	R

READBACK SELECT REGISTER

Address: 0x41, Reset: 0x0000, Name: READ_SELECT

This register selects the address of the register required to be read back and determines the contents of the SPI readback frame.

Table 49. Bit Descriptions for READ_SELECT

Bits	Bit Name	Description	Reset	Access
[15:10]	RESERVED	Reserved.	0x0	R
9	AUTO_RD_EN	Automatic read enabled. When this bit is set to 0, a read is performed by first writing the readback address to the READ_SELECT register, followed by a frame where the read data is returned on the SDO only for the next SPI transaction, which is called a two-stage read. When this bit is set to 1, read data is returned on the SDO for every SPI access. The location read is determined by the current value of the READBACK_ADDR bits, Bits[7:0]. Repeated reads of a register location can execute without needing a write to the READ_SELECT register between each read. For streaming mode, the address starts at the value of the READBACK_ADDR bits, Bits[7:0] and increments until the read stops. At the start of the next burst read, the address reverts to the value of the READBACK_ADDR bits, Bits[7:0]. Repeated burst reads can execute without needing a write to the READ_SELECT register between each burst read.	0x0	R/W
8	SPI_RD_RET_INFO	Determines the content of the MSBs in the SPI read frame. When this bit is set to 0, the READBACK_ADDR is returned in bits, Bits[30:24] (the MSB is not shown) of any subsequent SPI read. When this bit is set to 1, the ADC_RDY bit, alert flags, and the four digital input outputs are returned in Bits[30:24] of any subsequent SPI read.	0x0	R/W
[7:0]	READBACK_ADDR	Bits[D7:D0] contains the register address to be read.	0x0	R/W

THERMAL RESET ENABLE REGISTER

Address: 0x43, Reset: 0x0000, Name: THERM_RST

Table 50. Bit Descriptions for THERM_RST

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	EN_THERM_RST	Set to 1 to enable thermal reset functionality. If the die temperature reaches typically 140°C, a thermal reset event triggers a digital reset. This reset event is detected via a change in the $\overline{\text{ALERT}}$ pin and the RESET_OCCURRED flag.	0x0	R/W

COMMAND REGISTER

Address: 0x44, Reset: 0x0000, Name: CMD_KEY

Specific key codes are written to this register to execute the functions shown in Table 51. Using specific keys to initiate actions such as reset, LDAC, or clear provides extra system robustness as using these keys reduce the probability of initiating these tasks in error.

Table 51. Bit Descriptions for CMD_KEY

Bits	Bit Name	Description	Reset	Access
[15:0]	CMD_KEY	Enter a key to execute a command. 0x0000: NOP. 0x15FA: Software Reset Key1. To trigger a software reset, write this key followed by Software Reset Key2. The SPI writes must be back to back. 0xAF51: Software Reset Key2. To trigger a software reset, write Software Reset Key1 followed by this key. The SPI writes must be back to back. 0x953A: LDAC key. A DAC update is triggered on all channels when this key is entered, which is equivalent to asserting the $\overline{\text{LDAC}}$ pin. 0x73D1: DAC clear key. When entering this key, the DAC_CLR_CODEx registers for a channel are sent to the DAC, provided that the clear function is enabled in the OUTPUT_CONFIGx registers. Note that if slewing is enabled when the channel is cleared, the output slews at the programmed rate to the clear code.	0x0	W

SCRATCH OR SPARE REGISTER

Address: 0x45, Reset: 0x0000, Name: SCRATCH

Table 52. Bit Descriptions for SCRATCH

Bits	Bit Name	Description	Reset	Access
[15:0]	SCRATCH_BITS	Scratch or spare register field.	0x0	R/W

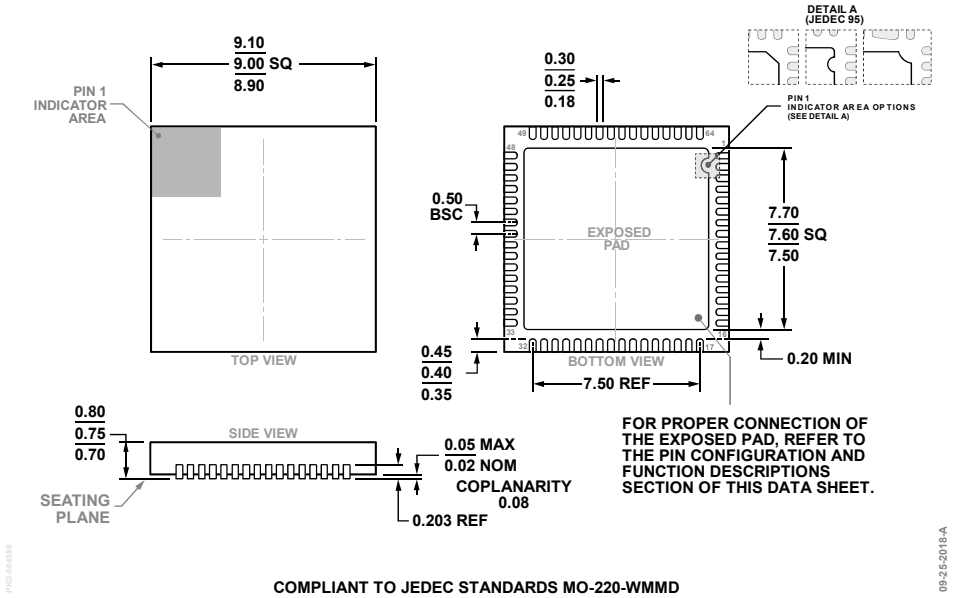
SILICON REVISION REGISTER

Address: 0x46, Reset: 0x0003, Name: SILICON_REV

Table 53. Bit Descriptions for SILICON_REV

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	SILICON_REV_ID	Silicon revision identification.	0x8	R

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WMMD

Figure 59. 64-Lead Lead Frame Chip Scale Package [LFCSP]
9 mm × 9 mm Body and 0.75 mm Package Height
(CP-64-15)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
AD74413RBCPZ	−40°C to +105°C	64-Lead Lead Frame Chip Scale Package [LFCSP]	CP-64-15
AD74413RBCPZ-RL7	−40°C to +105°C	64-Lead Lead Frame Chip Scale Package [LFCSP]	CP-64-15
EV-AD74413RSDZ		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] When ordering the EV-AD74413RSDZ, the USB interface board, EVAL-SDP-CS1Z, must be ordered separately.

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