Ultra-Low Power, 1-Channel, Capacitance Converter for Proximity Sensing

AD7151

FEATURES

- **Ultra-low power**
  - **2.7 V to 3.6 V, 70 µA**
- **Response time: 10 ms**
- **Adaptive environmental compensation**
- **1 capacitance input channel**
  - **Sensor capacitance (C_{SENS}) 0 pF up to 13 pF**
  - **Sensitivity to 1 fF**
- **EMC tested**
- **2 modes of operation**
  - **Standalone with fixed settings**
  - **Interfaced to a microcontroller for user-defined settings**
- **Proximity detection output flag**
- **2-wire serial interface (I^2C compatible)**
- **Operating temperature**
  - **−40°C to +85°C**
- **10-lead MSOP package**

APPLICATIONS

- **Proximity sensing**
- **Contactless switching**
- **Position detection**
- **Level detection**

GENERAL DESCRIPTION

The AD7151 delivers a complete signal processing solution for capacitive proximity sensors, featuring an ultra-low power converter with fast response time. The AD7150 is a 2-channel alternative to the AD7151.

The AD7151 uses Analog Devices, Inc., capacitance-to-digital converter (CDC) technology, which combines features important for interfacing to real sensors, such as high input sensitivity and high tolerance of both input parasitic ground capacitance and leakage current.

The integrated adaptive threshold algorithm compensates for any variations in the sensor capacitance due to environmental factors like humidity and temperature or due to changes in the dielectric material over time.

By default, the AD7151 operates in standalone mode using the fixed power-up settings and indicates detection on a digital output. Alternatively, the AD7151 can be interfaced to a microcontroller via the serial interface, the internal registers can be programmed with user-defined settings, and the data and status can be read from the part.

The AD7151 operates with a 2.7 V to 3.6 V power supply. It is specified over the temperature range of −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

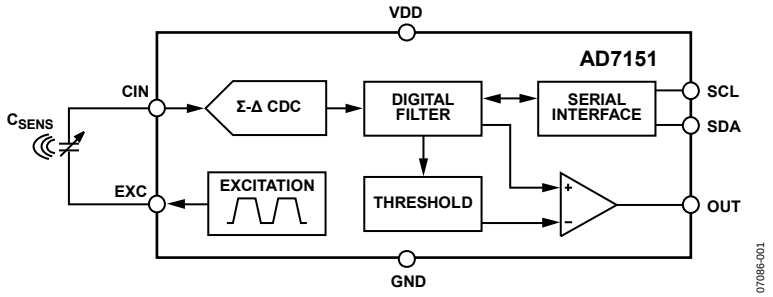


Figure 1.

Rev. 0
Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113 **©2007 Analog Devices, Inc. All rights reserved.**

TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Functional Block Diagram ... 1
Revision History ... 2
Specifications ... 3
Timing Specifications ... 4
Absolute Maximum Ratings ... 5
ESD Caution ... 5
Pin Configuration and Function Descriptions ... 6
Typical Performance Characteristics ... 7
Architecture and Main Features ... 10
Capacitance-to-Digital Converter ... 10
CAPDAC ... 10
Comparator and Threshold Modes ... 11
Adaptive Threshold ... 11
Data Average ... 11
Sensitivity ... 12
Hysteresis ... 12
Timeout ... 12
AutoCAPDAC Adjustment ... 13
Power-Down Timer ... 13
Power Supply Monitor ... 13
Register Descriptions ... 14
Status Register ... 15
Data Register ... 16
Average Register ... 16
Fixed Threshold Register ... 16
Sensitivity Register ... 16
Timeout Register ... 17
Setup Register ... 18
Configuration Register ... 19
Power-Down Timer Register ... 20
CAPDAC Register ... 20
Serial Number Register ... 20
Chip ID Register ... 20
Serial Interface ... 21
Read Operation ... 21
Write Operation ... 21
AD7151 Reset ... 22
General Call ... 22
Hardware Design Considerations ... 23
Overview ... 23
Parasitic Capacitance to Ground ... 23
Parasitic Resistance to Ground ... 23
Parasitic Parallel Resistance ... 23
Parasitic Serial Resistance ... 24
Input Overvoltage Protection ... 24
Input EMC Protection ... 24
Power Supply Decoupling and Filtering ... 24
Application Examples ... 25
Outline Dimensions ... 26
Ordering Guide ... 26

REVISION HISTORY

11/07—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 3.6 V; GND = 0 V; −40°C to +85°C, single-ended capacitance mode, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
CAPACITIVE INPUT					
Conversion Input Range CIN to EXC[2]	3.2	4		pF	4 pF input range
	1.6	2		pF	2 pF input range
	0.8	1		pF	1 pF input range
	0.4	0.5		pF	0.5 pF input range
Resolution[3]		2.0		fF	4 pF input range
		1.6		fF	2 pF input range
		1.4		fF	1 pF input range
		1.0		fF	0.5 pF input range
Allowed Capacitance CIN to GND[3]			150	pF	
Allowed Resistance CIN to GND[3]	15			MΩ	
Allowed Serial Resistance[3]			200	kΩ	
Gain Error	−20		+20	%	
Gain Deviation over Temperature[3]		0.5		%	
Gain Matching Between Ranges[3]	−2		+2	%	
Offset Error[3]		50		fF	CIN and EXC pins disconnected
Offset Deviation over Temperature[3]		5		fF	CIN and EXC pins disconnected
Integral Nonlinearity (INL)[3]		0.1		%	
Power Supply Rejection[3]		4		fF/V	
CAPDAC[2]					
Full Range	10	12.5		pF	
Resolution (LSB)[3]		200		fF	
Differential Nonlinearity (DNL)[3]			0.25	LSB	
AutoDAC Increment/Decrement[3]	25		75	% of C_{IN} Range	
EXCITATION					
Voltage		±V_{DD}/2		V	
Frequency	15.4	16	16.3	kHz	
Allowed Capacitance EXC to GND[3]			300	pF	
Allowed Resistance EXC to GND[3]	1			MΩ	
LOGIC OUTPUT (OUT)					
Output Low Voltage (V_{OL})			0.4	V	I_{SINK} = −4 mA
Output High Voltage (V_{OH})	V_{DD} − 0.6			V	I_{SOURCE} = 4 mA
SERIAL INTERFACE INPUTS (SCL, SDA)					
Input High Voltage (V_{IH})	1.5			V	
Input Low Voltage (V_{IL})			0.8	V	
Input Leakage Current		±0.1	±5	µA	
Input Pin Capacitance		6		pF	
OPEN-DRAIN OUTPUT (SDA)					
Output Low Voltage (V_{OL})			0.4	V	I_{SINK} = −6.0 mA
Output High Leakage Current (I_{OH})		0.1	5	µA	V_{OUT} = V_{DD}
POWER SUPPLY MONITOR					
V_{DD} Threshold Voltage		2.45	2.65	V	

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
POWER REQUIREMENTS					
V_{DD}-to-GND Voltage	2.7		3.6	V	V_{DD} = 3.3 V, nominal
I_{DD} Current[4]		70	80	µA	
I_{DD} Current Power-Down Mode[4]		1	5	µA	Temperature ≤ 25°C
		3	10	µA	Temperature = 85°C

[1] Capacitance units: one picofarad (1 pF) = 1×10^{-12} farad (F); one femtofarad (1 fF) = 10^{-15} farad (F).
[2] The CAPDAC can be used to shift (offset) the input range. The total capacitance of the sensor can, therefore, be up to the sum of the CAPDAC value and the conversion input range. With the autoCAPDAC feature, the CAPDAC is adjusted automatically when the CDC input value is lower than 25% or higher than 75% of the CDC nominal input range.
[3] Specification is not production tested but is supported by characterization data at initial product release.
[4] Digital inputs equal to V_{DD} or GND.

TIMING SPECIFICATIONS

V_{DD} = 2.7 V to 3.6 V; GND = 0 V; Input Logic 0 = 0 V; Input Logic 1 = V_{DD}; –40°C to +85°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CONVERTER					
Conversion Time			10	ms	
Wake-Up Time from Power-Down Mode[1, 2]		0.3		ms	
Power-Up Time[1, 3]		2		ms	
Reset Time[1, 4]		2		ms	
SERIAL INTERFACE[5, 6]					See Figure 2.
SCL Frequency	0		400	kHz	
SCL High Pulse Width, t_{HIGH}	0.6			µs	
SCL Low Pulse Width, t_{LOW}	1.3			µs	
SCL, SDA Rise Time, t_R			0.3	µs	
SCL, SDA Fall Time, t_F			0.3	µs	
Hold Time (Start Condition), $t_{HD;STA}$	0.6			µs	After this period, the first clock is generated.
Setup Time (Start Condition), $t_{SU;STA}$	0.6			µs	Relevant for repeated start condition.
Data Setup Time, $t_{SU;DAT}$	0.1			µs	
Setup Time (Stop Condition), $t_{SU;STO}$	0.6			µs	
Data Hold Time (Master), $t_{HD;DAT}$	10			ns	
Bus-Free Time (Between Stop and Start Condition), t_{BUF}	1.3			µs	

[1] Specification is not production tested but is supported by characterization data at initial product release.
[2] Wake-up time is the maximum delay between the last SCL edge writing the configuration register and the start of conversion.
[3] Power-up time is the maximum delay between the V_{DD} crossing the minimum level (2.7 V) and either the start of conversion or when ready to receive a serial interface command.
[4] Reset time is the maximum delay between the last SCL edge writing the reset command and either the start of conversion or when ready to receive a serial interface command.
[5] Sample tested during initial release to ensure compliance.
[6] All input signals are specified with input rise/fall times = 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Output load = 10 pF.

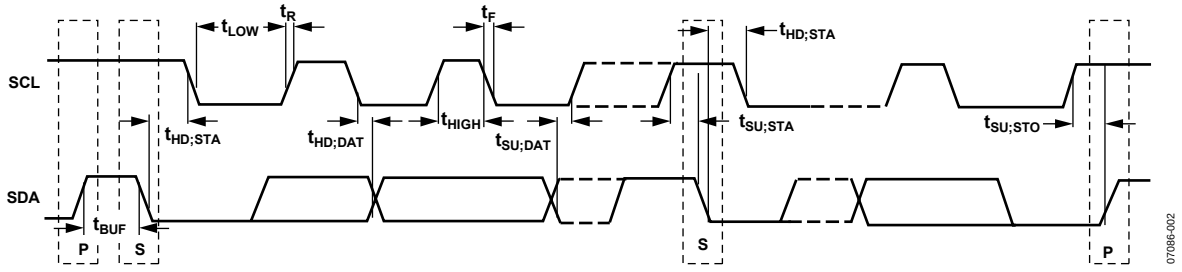


Figure 2. Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
Positive Supply Voltage V_{DD} to GND	−0.3 V to +3.9 V
Voltage on Any Input or Output to GND	−0.3 V to V_{DD} + 0.3 V
ESD Rating HBM (ESD Association Human Body Model, S5.1)	4 kV
ESD Rating FICDM (Field-Inducted Charged Device Model)	1 kV
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
MSOP Package	
θ_{JA}, Thermal Impedance-to-Air	206°C/W
θ_{JC}, Thermal Impedance-to-Case	44°C/W
Reflow Soldering (Pb-Free)	
Peak Temperature	260(+0/−5)°C
Time at Peak Temperature	10 sec to 40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

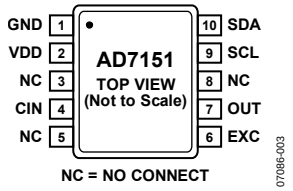


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Ground Pin.
2	VDD	Power Supply Voltage. This pin should be decoupled to GND using a low impedance capacitor, for example, 0.1 µF X7R multilayer ceramic.
3	NC	This pin should be left as an open circuit or connected to GND.
4	CIN	CDC Capacitive Input. The measured capacitance (sensor) is connected between the EXC pin and the CIN pin.
5	NC	This pin should be left as an open circuit.
6	EXC	CDC Excitation Output. The measured capacitance is connected between the EXC pin and the CIN pin.
7	OUT	Logic Output. High level on this output indicates proximity detected on the capacitive input.
8	NC	This pin should be left as an open circuit.
9	SCL	Serial Interface Clock Input. Connects to the master clock line. Requires a pull-up resistor if not provided elsewhere in the system.
10	SDA	Serial Interface Bidirectional Data. Connects to the master data line. Requires a pull-up resistor if not provided elsewhere in the system.

TYPICAL PERFORMANCE CHARACTERISTICS

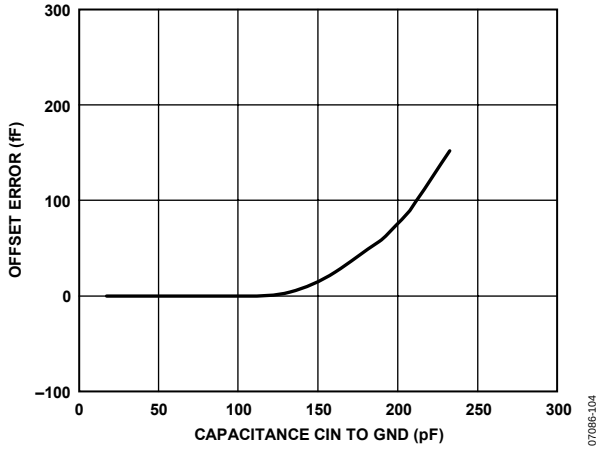


Figure 4. Capacitance Input Offset Error vs. Capacitance CIN to GND, V_{DD} = 3.3 V, EXC Pin Open Circuit

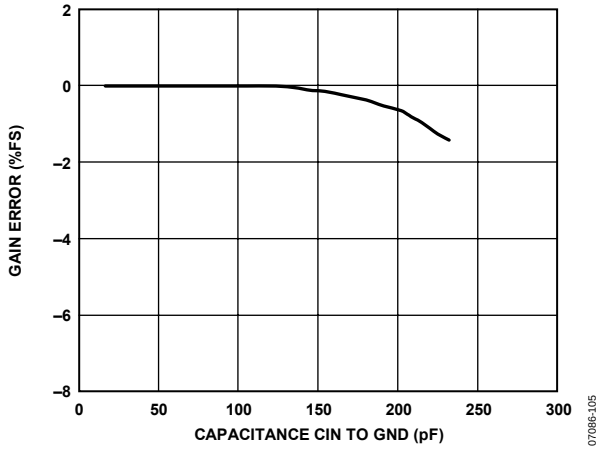


Figure 5. Capacitance Input Gain Error vs. Capacitance CIN to GND, V_{DD} = 3.3 V, CIN to EXC = 2 pF

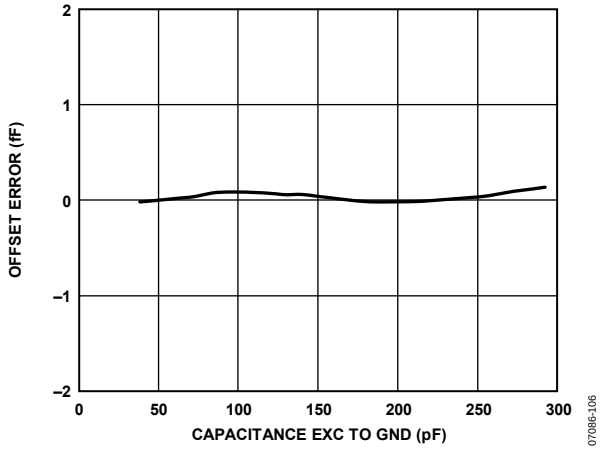


Figure 6. Capacitance Input Offset Error vs. Capacitance EXC to GND, V_{DD} = 3.3 V, CIN Pin Open Circuit

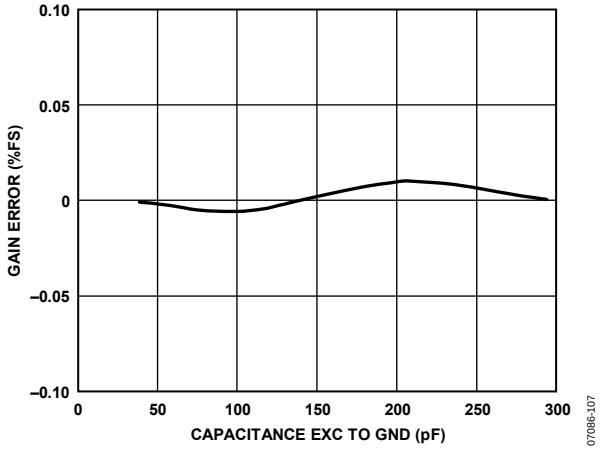


Figure 7. Capacitance Input Gain Error vs. Capacitance EXC to GND, V_{DD} = 3.3 V, CIN to EXC = 2 pF

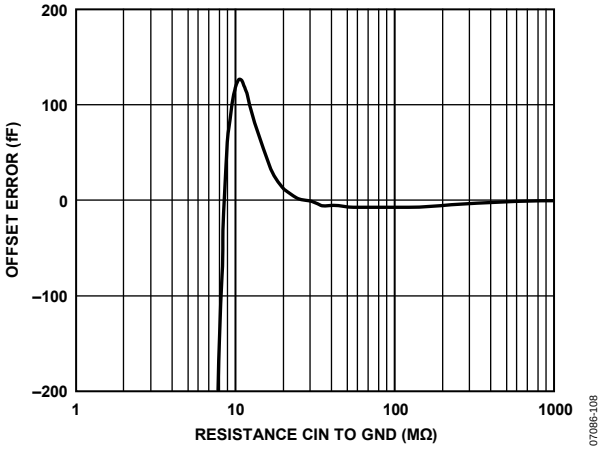


Figure 8. Capacitance Input Offset Error vs. Resistance CIN to GND, V_{DD} = 3.3 V, EXC Pin Open Circuit

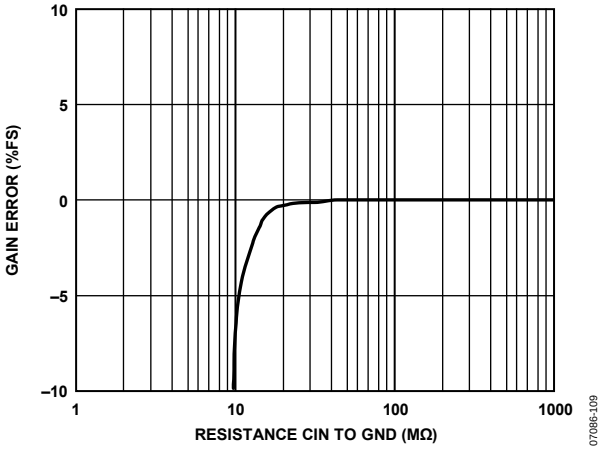


Figure 9. Capacitance Input Gain Error vs. Resistance CIN to GND, V_{DD} = 3.3 V, CIN to EXC = 2 pF

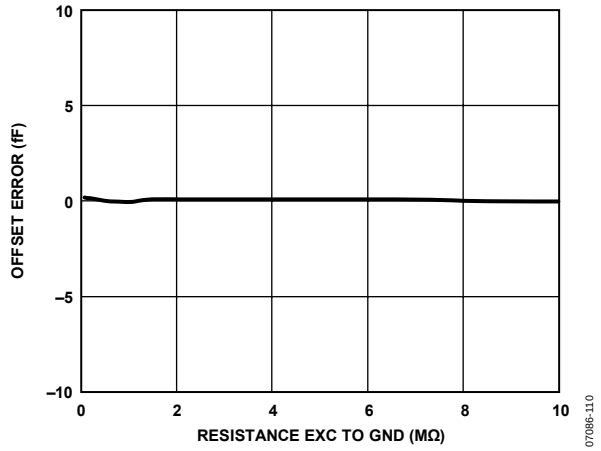


Figure 10. Capacitance Input Offset Error vs. Resistance EXC to GND, V_{DD} = 3.3 V, CIN Pin Open Circuit

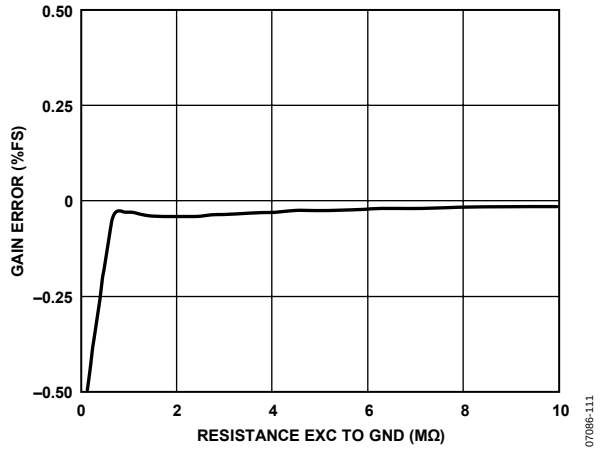


Figure 11. Capacitance Input Gain Error vs. Resistance EXC to GND, V_{DD} = 3.3 V, CIN to EXC = 2 pF

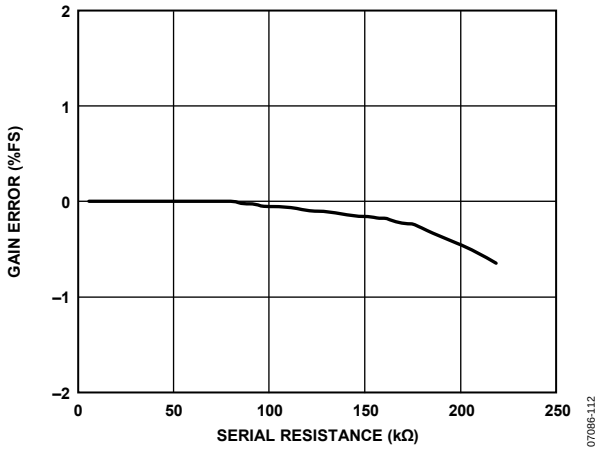


Figure 12. Capacitance Input Gain Error vs. Serial Resistance V_{DD} = 3.3 V, CIN to EXC = 2 pF

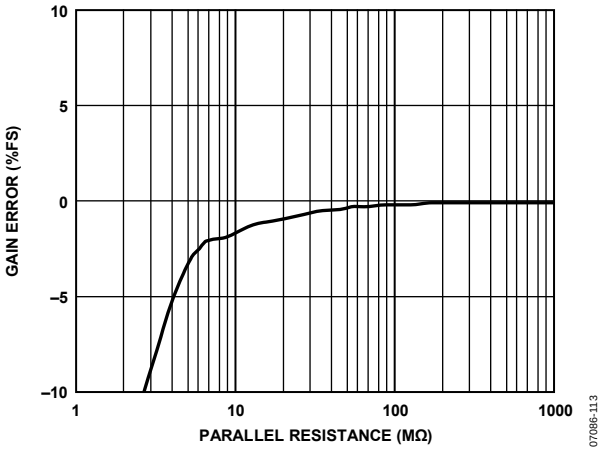


Figure 13. Capacitance Input Gain Error vs. Parallel Resistance, V_{DD} = 3.3 V, CIN to EXC = 2 pF

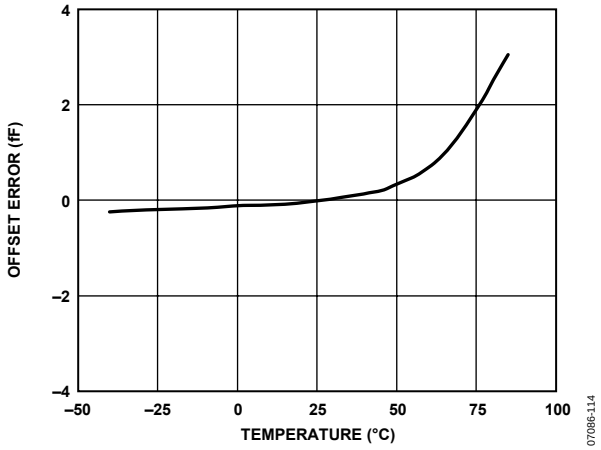


Figure 14. Capacitance Input Offset Error vs. Temperature, V_{DD} = 3.3 V, CIN and EXC Pins Open Circuit

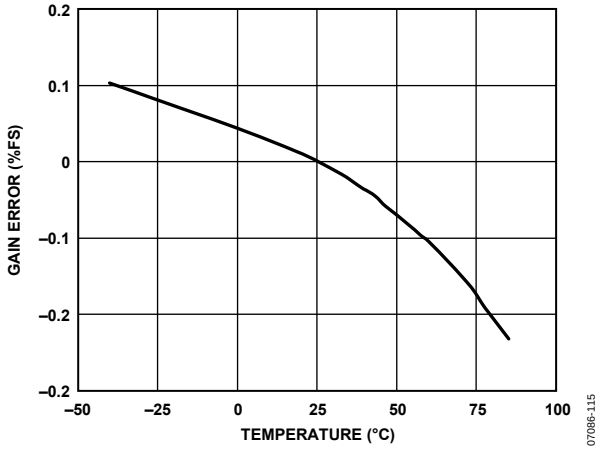


Figure 15. Capacitance Input Gain Error vs. Temperature, V_{DD} = 3.3 V, CIN to EXC = 2 pF

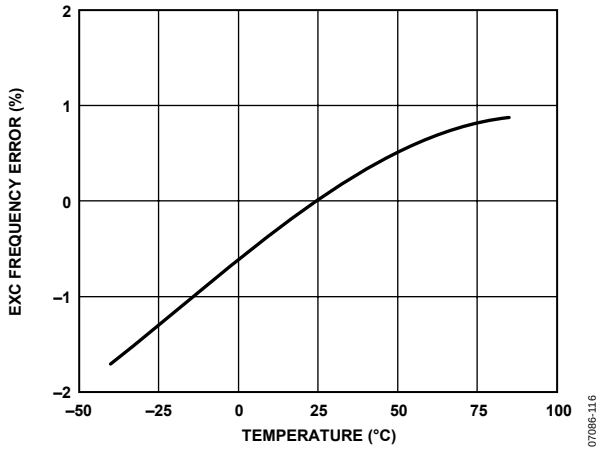


Figure 16. EXC Frequency Error vs. Temperature, V_{DD} = 3.3 V

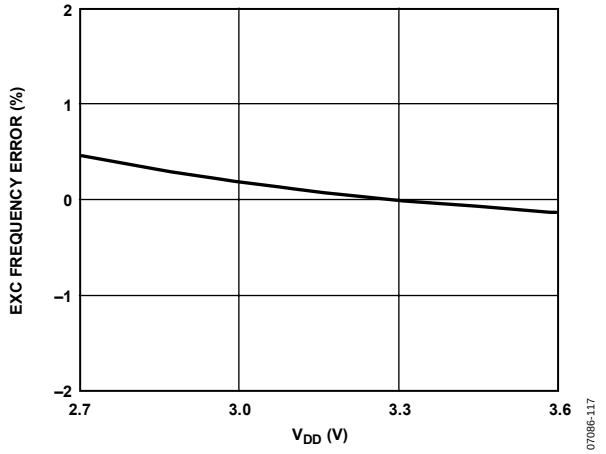


Figure 17. EXC Frequency Error vs. V_{DD}

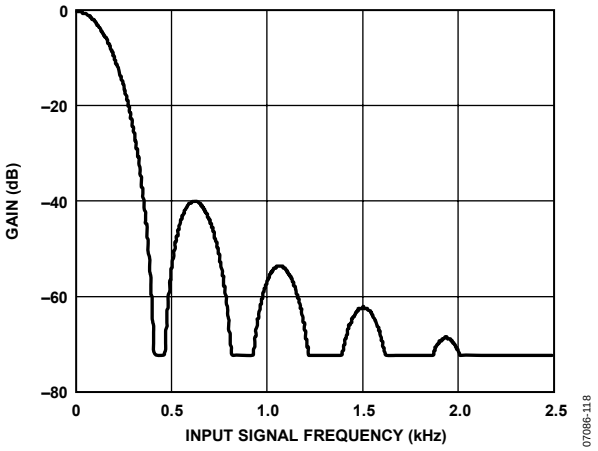


Figure 18. Capacitance to Digital Converter Frequency Response

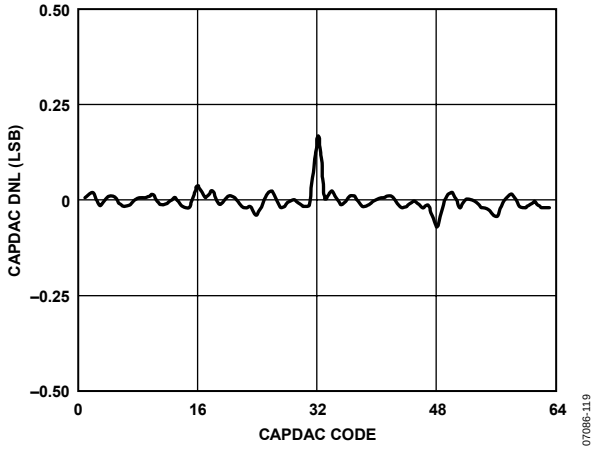


Figure 19. CAPDAC Differential Nonlinearity (DNL), V_{DD} = 3.3 V

ARCHITECTURE AND MAIN FEATURES

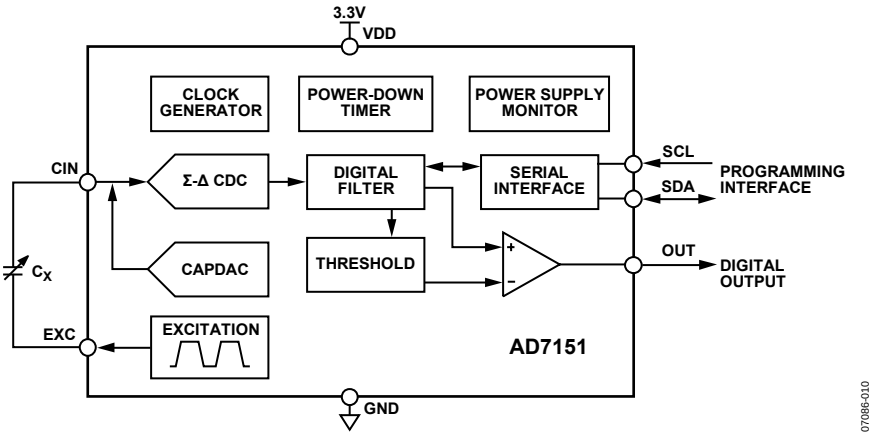


Figure 20. AD7151 Block Diagram

The AD7151 core is a high performance capacitance-to-digital converter (CDC) that allows the part to be interfaced directly to a capacitive sensor.

The comparator compares the CDC result with thresholds, either fixed or dynamically adjusted by the on-chip adaptive threshold algorithm engine. Thus, the output indicates a defined change in the input sensor capacitance.

The AD7151 also integrates an excitation source and CAPDAC for the capacitive inputs, an input multiplexer, a complete clock generator, a power-down timer, a power supply monitor, control logic, and an I²C®-compatible serial interface for configuring the part and accessing the internal CDC data and status, if required in the system (see Figure 20).

CAPACITANCE-TO-DIGITAL CONVERTER

Figure 21 shows the CDC simplified functional diagram. The converter consists of a second-order sigma delta (Σ-Δ), charge balancing modulator and a third-order digital filter. The measured capacitance C_X is connected between an excitation source and the Σ-Δ modulator input. The excitation signal is applied on the C_X during the conversion, and the modulator continuously samples the charge going through the C_X. The digital filter processes the modulator output, which is a stream of 0s and 1s containing the information in 0 and 1 density. The data is processed by the adaptive threshold engine and output comparators; the data can be also read through the serial interface.

The AD7151 is designed for floating capacitive sensors. Therefore, both C_X plates have to be isolated from ground or any other fixed potential node in the system.

The AD7151 features slew rate limiting on the excitation voltage output, which decreases the energy of higher harmonics on the excitation signal and dramatically improves the system electromagnetic compatibility (EMC).

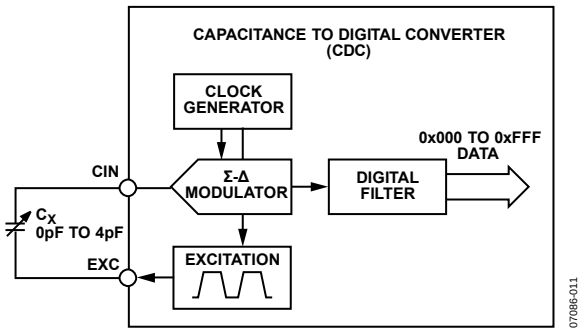


Figure 21. CDC Simplified Block Diagram

CAPDAC

The AD7151 CDC core maximum full-scale input range is 4 pF. However, the part can accept a higher capacitance on the input, and the offset (nonchanging component) capacitance of up to 10 pF can be balanced by a programmable on-chip CAPDAC.

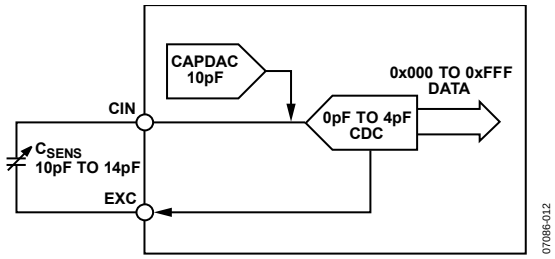


Figure 22. Using CAPDAC

The CAPDAC can be understood as a negative capacitance connected internally to the CIN pin. The CAPDAC has a 6-bit resolution and a monotonic transfer function. Figure 22 shows how to use the CAPDAC to shift the CDC 4 pF input range to measure capacitance between 10 pF and 14 pF.

COMPARATOR AND THRESHOLD MODES

The AD7151 comparator and its threshold can be programmed to operate in several different modes. In an adaptive mode, the threshold is dynamically adjusted and the comparator output indicates fast changes and ignores slow changes in the input (sensor) capacitance. Alternatively, the threshold can be programmed as a constant (fixed) value, and the output then indicates any change in the input capacitance that crosses the defined fixed threshold.

The AD7151 logic output (active high) indicates either a positive or a negative change in the input capacitance, in both adaptive and fixed threshold modes (see Figure 23 and Figure 24).

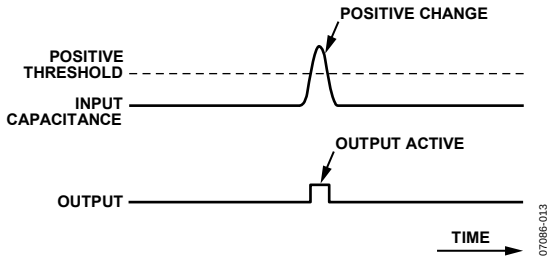


Figure 23. Positive Threshold Mode
Indicates Positive Change in Input Capacitance

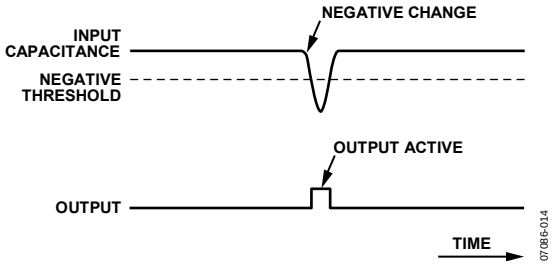


Figure 24. Negative Threshold Mode
Indicates Negative Change in Input Capacitance

Additionally, for the adaptive mode only, the comparator can work as window comparator, indicating input either inside or outside a selected sensitivity band (see Figure 25 and Figure 26).

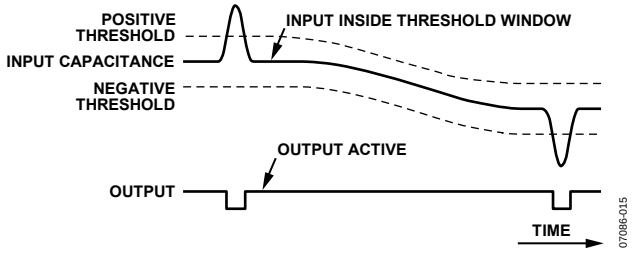


Figure 25. In-Window (Adaptive) Threshold Mode

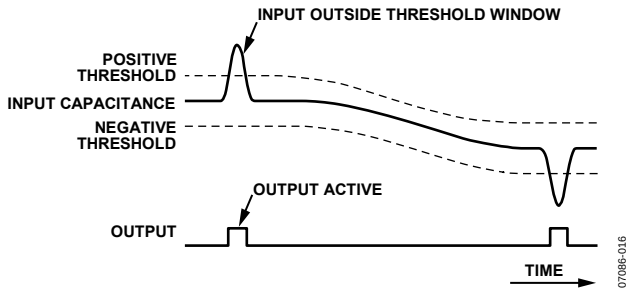


Figure 26. Out-Window (Adaptive) Threshold Mode

ADAPTIVE THRESHOLD

In an adaptive mode, the thresholds are dynamically adjusted, ensuring indication of fast changes (for example an object moving close to a capacitive proximity sensor) and eliminating slow changes in the input (sensor) capacitance, usually caused by environment changes such as humidity or temperature or changes in the sensor dielectric material over time (see Figure 27).

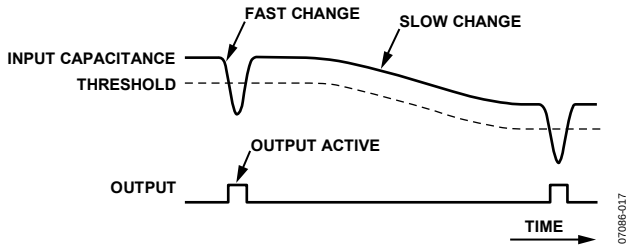


Figure 27. Adaptive Threshold
Indicates Fast Changes and Eliminates Slow Changes in Input Capacitance

DATA AVERAGE

The adaptive threshold algorithm is based on an average calculated from previous CDC output data. The response of the average to an input capacitance step change (more exactly, response to the change in the CDC output data) is an exponential settling curve, which can be characterized by the following equation:

$$Average(N) = Average(0) + Change(1 - e^{N / TimeConst})$$

where:
Average(*N*) is the value of average N complete CDC conversion cycles after a step change on the input.
Average(0) is the value before the step change.
TimeConst can be selected in the range between 2 and 65,536, in steps of power of 2, by programming the ThrSettling bits in the setup register.

See Figure 28 and the Register Descriptions section.

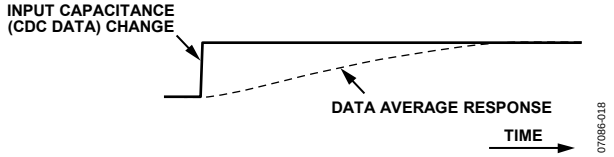


Figure 28. Data Average Response to Data Step Change

SENSITIVITY

In adaptive threshold mode, the output comparator threshold is set as a defined distance (sensitivity) above the data average, below the data average, or both, depending on the selected threshold mode of operation (see Figure 29). The sensitivity value is programmable in the range 0 to 255 LSBs of the 12-bit CDC converter (see the Register Descriptions section).

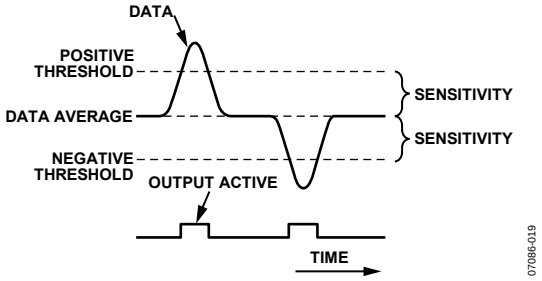


Figure 29. Threshold Sensitivity

HYSTERESIS

In adaptive threshold mode, the comparator features hysteresis. The hysteresis is fixed to one-fourth of the threshold sensitivity and can be programmed on or off. The comparator does not have hysteresis in the fixed threshold mode.

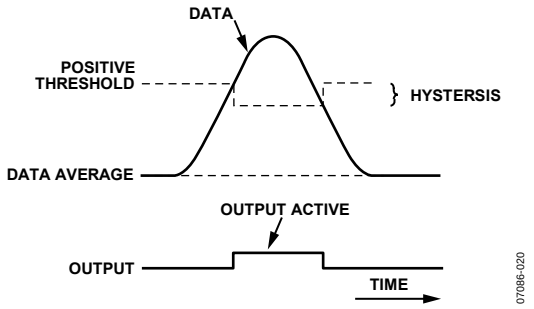


Figure 30. Threshold Hysteresis

TIMEOUT

In the case of a large, long change in the capacitive input, when the data average adapting to a new condition may take too long, a timeout can be set.

The timeout becomes active (counting) when the CDC data goes outside the band of data average ± sensitivity. When the timeout elapses (a defined number of CDC conversions is counted), the data average (and thus the threshold) is forced to follow the new CDC data value immediately (see Figure 31).

The timeout can be set independently for approaching (for change in data toward the threshold) and for receding (for change in data away from the threshold). See Figure 32, Figure 33, and the Register Descriptions section.

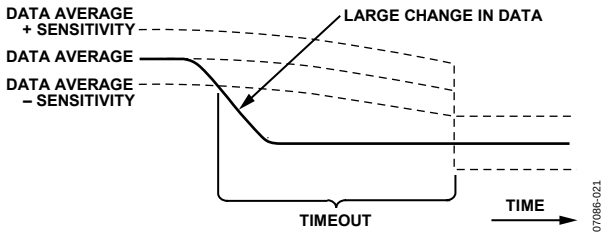


Figure 31. Threshold Timeout After a Large Change in CDC Data

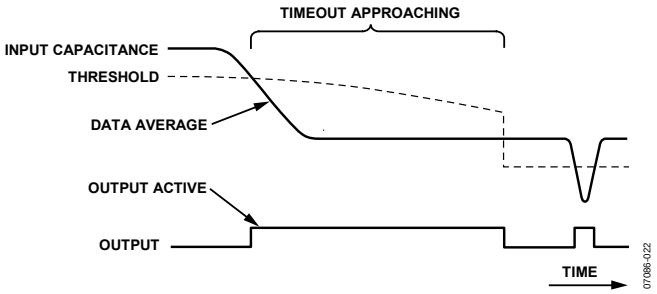


Figure 32. Approaching Timeout in Negative Threshold Mode Shortens False Output Trigger

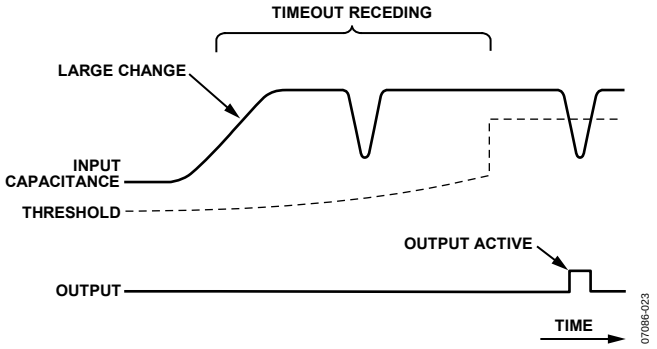


Figure 33. Positive Timeout in Negative Threshold Mode Shortens Period of Missing Output Trigger

AUTOCAPDAC ADJUSTMENT

In adaptive threshold mode, the part can dynamically adjust the CAPDAC to keep the CDC in an optimal operating capacitive range. When the AutoDAC function is enabled, the CAPDAC value is automatically incremented when the data average exceeds three-fourths of the CDC full range, and the CAPDAC value is decremented when the data average goes below one-fourth of the CDC full range. The AutoDAC increment or decrement step depends on the selected CDC capacitive input range. See the Setup Register section.

POWER-DOWN TIMER

In power sensitive applications, the AD7151 can be set to automatically enter power-down mode after a programmed period of time in which the output has not been activated. The AD7151 can be then returned to a normal operational mode either via the serial interface or by the power supply off/on sequence.

POWER SUPPLY MONITOR

When the AD7151 V_{DD} power supply voltage drops below a defined level needed for correct CDC operation, the on-chip power supply monitor stops the adaptive threshold logic and holds it in reset. After the V_{DD} reaches the required level, the threshold logic is released, and the data average is reset to the value of the first conversion finished at the correct power supply voltage.

This feature prevents the adaptive threshold from being set incorrectly after a very slow rise of the V_{DD} voltage or from being corrupted by accidental drops in the V_{DD} voltage.

The other AD7151 functions continue working below the power supply monitor threshold, down to approximately 1.0V..1.8V, the exact level depending on the manufacturing process variation. In the region of the low V_{DD} voltage, the part is still accessible via the serial interface and continues conversion. However, the conversion results may be incorrect and, therefore, the data should not be considered valid if the part operates below the power supply monitor threshold.

The status of the power supply monitor can be determined by reading the PwrDown bit in the AD7151 status register.

REGISTER DESCRIPTIONS

Table 5. Register Summary

Register	Pointer (Dec)	Pointer (Hex)	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				Default Value							
Status	0	0x00	R	PwrDown	–	–	$\overline{\text{DacStep}}$	OUT	–	–	$\overline{\text{RDY}}$
				0	1	0	1	0	0	1	1
Data High	1	0x01	R	0x00							
Data Low	2	0x02	R	0x00							
–	3	0x03	R	0x00							
–	4	0x04	R	0x00							
Average High	5	0x05	R	0x00							
Average Low	6	0x06	R	0x00							
–	7	0x07	R	0x00							
–	8	0x08	R	0x00							
Sensitivity Threshold High	9	0x09	R/W	Sensitivity (in adaptive threshold mode)/Threshold High Byte (in fixed threshold mode)							
				0x08							
Timeout Threshold Low	10	0x0A	R/W	Timeout (in adaptive threshold mode)/Threshold Low Byte (in fixed threshold mode)							
				0x86							
Setup	11	0x0B	R/W	RngH	RngL	–	$\overline{\text{Hyst}}$	ThrSettling (4-bit value)			
				0	0	0	0	0x0B			
–	12	0x0C	R/W	0x00							
–	13	0x0D	R/W	0x00							
–	14	0x0E	R/W	0x00							
Configuration	15	0x0F	R/W	ThrFixed	ThrMD1	ThrMD0	EnConv	–	MD2	MD1	MD0
				0	0	0	1	0	0	0	1
Power-Down Timer	16	0x10	R/W	–	–	Power-Down Timeout (6-bit value)					
				0	0	0x00					
CAPDAC	17	0x11	R/W	DacEn	DacAuto	DacValue (6-bit value)					
				1	1	0x00					
–	18	0x12	R/W	0x00							
Serial Number 3	19	0x13	R	Serial Number – Byte 3 (MSB)							
Serial Number 2	20	0x14	R	Serial Number – Byte 2							
Serial Number 1	21	0x15	R	Serial Number – Byte 1							
Serial Number 0	22	0x16	R	Serial Number – Byte 0 (LSB)							
Chip ID	23	0x17	R	Chip Identification Code							

STATUS REGISTER

Address Pointer 0x00
8 Bits, Read-Only, Default Value 0x53 Before Conversion, 0x52 After Conversion

The status register indicates the status of the part. The register can be read via the 2-wire serial interface to query the status of the outputs, check the CDC finished conversion, and check whether the CAPDAC has been changed by the autoCAPDAC function.

Table 6. Status Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	PwrDown	–	–	$\overline{\text{DacStep}}$	OUT	–	–	$\overline{\text{RDY}}$
Default	0	1	0	1	0	0	1	1

Table 7. Status Register Bit Descriptions

Bit	Mnemonic	Description
7	PwrDown	PwrDown = 1 indicates that the part is in a power-down mode or that the part V_{DD} is below the power supply monitor threshold voltage.
6	–	Bit not used, always reads 1.
5	–	Bit not used, always reads 0.
4	$\overline{\text{DacStep}}$	$\overline{\text{DacStep}}$ = 0 indicates that the CAPDAC value was changed during the last conversion as part of the AutoDac function. The bit value is updated after each finished CDC conversion.
3	OUT	OUT = 1 indicates that the data (CIN capacitance) crossed the threshold, according to the selected comparator mode of operation. The bit value is updated after each finished CDC conversion.
2	–	Bit not used, always reads 0.
1	–	Bit not used, always reads 1.
0	$\overline{\text{RDY}}$	$\overline{\text{RDY}}$ = 0 indicates a finished CDC conversion. The bit is reset back to 1 when the data register is read via the serial interface or after the part reset or power-up.

DATA REGISTER

Address Pointer 0x01, 0x02
16 Bits, Read-Only, Default Value 0x0000

Data from the last complete capacitance-to-digital conversion reflects the capacitance on the input. Only the 12 MSBs (most significant bits) of the data register are used for the CDC result. The 4 LSBs (least significant bits) are always 0, as shown in Figure 34.

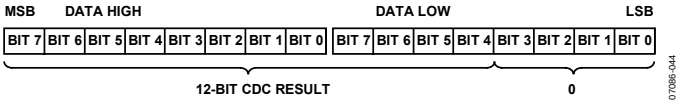


Figure 34. CDC Data Register

The nominal AD7151 CDC transfer function (an ideal transfer function excluding offset and/or gain error) maps the input capacitance between zero scale and full scale to output data codes between 0x3000 and 0xCFF0 only (see Table 8).

Table 8. AD7151 Capacitance-to-Data Mapping

Data	Input Capacitance
0x0000	Not valid, underrange
0x3000	Zero-scale (0 pF)
0x8000	Mid-scale (+1 pF)
0xCFF0	Full-scale (+2 pF)
0xFFF0	Not valid, overrange

The input capacitance can be calculated from the output data using the following equation:

$$C(\text{pF}) = \frac{Data - 12288}{40944} \times Input_Range$$

where *Input_Range* = 4 pF, 2 pF, 1 pF, or 0.5 pF.

The following is the same equation written with hexadecimal numbers:

$$C(\text{pF}) = \frac{Data - 0\text{x}3000}{0\text{x}9FF0} \times Input_Range$$

The data register is updated after a finished conversion, with one exception: when the serial interface read operation from the data register is in progress, the data register is not updated and the new capacitance conversion result is lost.

The stop condition on the serial interface is considered to be the end of the read operation. Therefore, to prevent incorrect data reading through the serial interface, the two bytes of the data register should be read sequentially using the register address pointer auto-increment feature of the serial interface.

AVERAGE REGISTER

Address Pointer 0x05, 0x06
16 Bits, Read-Only, Default Value 0x0000

This register shows the average calculated from the previous CDC data. The 12-bit CDC result corresponds to the 12 MSBs of the average register.

The settling time of the average can be set by programming the ThrSettling bits in the setup register. The average register is overwritten directly with the CDC output data, that is, the history is forgotten if the timeout is enabled and elapses.

FIXED THRESHOLD REGISTER

Address Pointer 0x09, 0x0A
16 Bits, Read/Write, Factory Preset 0x0886

A constant threshold for the output comparator in the fixed threshold mode can be set using this register. The 12-bit CDC result corresponds to the 12 MSBs of the threshold register. The fixed threshold register shares the address pointer and location on-chip with the sensitivity and timeout registers. The fixed threshold register is not accessible in the adaptive threshold mode.

SENSITIVITY REGISTER

Address Pointer 0x09
8 Bits, Read/Write, Factory Preset 0x08

The sensitivity register sets the distance of the positive threshold above the data average, and the distance of the negative threshold below the data average, in the adaptive threshold mode.

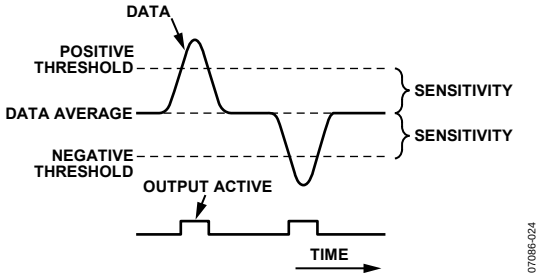


Figure 35. Threshold Sensitivity

The sensitivity is an 8-bit value and is mapped to the lower eight bits of the 12-bit CDC data, that is, it corresponds to the 16-bit data register as shown in Figure 36.

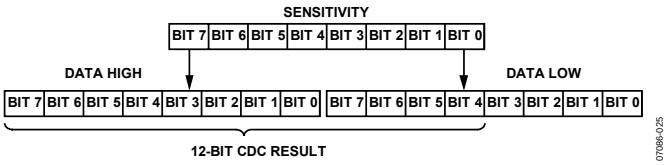


Figure 36. Relation Between Sensitivity Register and CDC Data Register

TIMEOUT REGISTER

Address Pointer 0x0A
8 Bits, Read/Write, Factory Preset 0x86

Table 9. Timeout Register Bit Map

Bit	Bits [7:4]	Bits [3:0]
Mnemonic	TimeOutApr	TimeOutRec
Default	0x08	0x06

The register sets timeouts for the adaptive threshold mode.

The approaching timeout starts when the CDC data crosses the data average ± sensitivity band toward the threshold, according to the selected positive, negative, or window threshold mode. The approaching timeout elapses after the number of conversion cycles equals $2^{TimeOutApr}$, where TimeOutApr is the value of the four most significant bits of the timeout register.

The receding timeout starts when the CDC data crosses the data average ± sensitivity band away from the threshold, according to the selected positive or negative threshold mode. The receding timeout is not used in the window threshold mode. The receding timeout elapses after the number of conversion cycles equals $2^{TimeOutRec}$, where TimeOutRec is the value of the four least significant bits of the timeout register.

When either the approaching or receding timeout elapses (that is, after the defined number of CDC conversions is counted), the data average (and thus the thresholds) is forced to follow the new CDC data value immediately.

When the timeout register equals 0, timeouts are disabled.

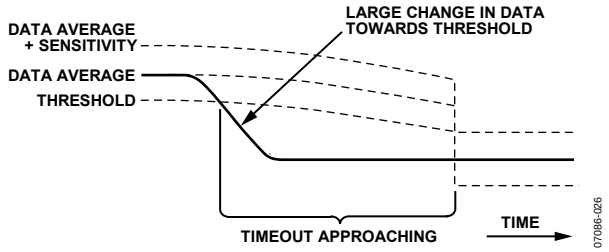


Figure 37. Threshold Timeout Approaching After a Large Change in CDC Data Toward Threshold

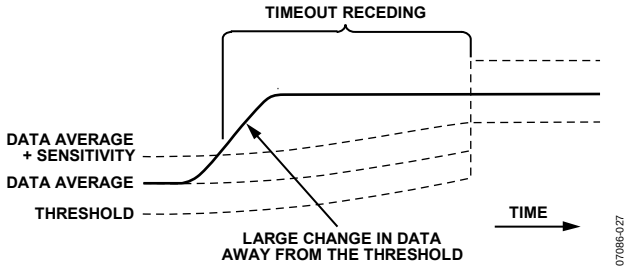


Figure 38. Threshold Timeout Receding After a Large Change in CDC Data Away from Threshold

SETUP REGISTER

Address Pointer 0x0B
8 Bits, Read/Write, Factory Preset 0x0B

Table 10. Setup Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	RngH	RngL	–	$\overline{\text{Hyst}}$	ThrSettling (4-Bit Value)			
Default	0	0	0	0	0x0B			

Table 11. Setup Register Bit Descriptions

Bit	Mnemonic	Description
7 6	RngH RngL	Range bits set the CDC input range and determine the step for the AutoDAC function.

RngH	RngL	Capacitive Input Range (pF)	AutoDAC Step (CAPDAC LSB)
0	0	2	4
0	1	0.5	1
1	0	1	2
1	1	4	8

5	–	This bit should be 0 for the specified operation.
4	$\overline{\text{Hyst}}$	$\overline{\text{Hyst}}$ = 1 disables hysteresis in adaptive threshold mode. This bit has no effect in fixed threshold mode; hysteresis is always disabled in the fixed threshold mode.
3 2 1 0	ThrSettling	Determines the settling time constant of the data average and thus the settling time of the adaptive thresholds. The response of the average to an input capacitance step change (that is, response to the change in the CDC output data) is an exponential settling curve characterized by the following equation: $Average(N) = Average(0) + Change(1 - e^{N / TimeConst})$ where: *Average(N)* is the value of average N complete CDC conversion cycles after a step change on the input *Average*(0) is the value before the step change *TimeConst* can be selected in the range between 2 and 65,536 conversion cycle multiples, in steps of power of 2, by programming the ThrSettling bits. $TimeConst = 2^{(ThrSettling+1)}$ See Figure 39.

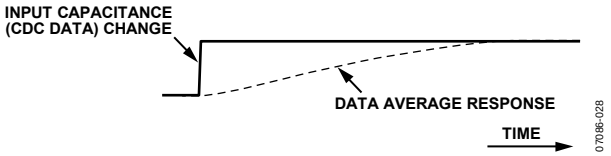


Figure 39. Data Average Response to Data Step Change

CONFIGURATION REGISTER

Address Pointer 0x0F
8 Bits, Read/Write, Factory Preset 0x19

Table 12. Configuration Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	ThrFixed	ThrMD1	ThrMD0	EnConv	–	MD2	MD1	MD0
Default	0	0	0	1	0	0	0	1

Table 13.Configuration Register Bit Descriptions

<table>
<tr><th>Bit</th><th>Mnemonic</th><th colspan="6">Description</th></tr>
<tr><td>7</td><td>ThrFixed</td><td colspan="6">ThrFixed = 1 sets the fixed threshold mode. The output reflects comparison of data and a fixed (constant) value of the threshold register.
ThrFixed = 0 sets the adaptive threshold mode. The output reflects comparison of data to the adaptive threshold. The adaptive threshold is set dynamically, based on the history of the previous data.</td></tr>
<tr><td>6
5</td><td>ThrMD1
ThrMD0</td><td colspan="6">These bits set the output comparator mode.
<table>
<tr><th rowspan="2">ThrMD1</th><th rowspan="2">ThrMD0</th><th rowspan="2">Threshold Mode</th><th colspan="2">Output Active When</th></tr>
<tr><th>Adaptive Threshold Mode</th><th>Fixed Threshold Mode</th></tr>
<tr><td>0</td><td>0</td><td>Negative</td><td>data < average – sensitivity</td><td>Data < Threshold</td></tr>
<tr><td>0</td><td>1</td><td>Positive</td><td>data > average + sensitivity</td><td>Data > Threshold</td></tr>
<tr><td>1</td><td>0</td><td>In-Window</td><td>data > average – sensitivity
AND
data < average + sensitivity</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>Out-Window</td><td>data < average – sensitivity
OR
data > average + sensitivity</td><td>-</td></tr>
</table></td></tr>
<tr><td>4</td><td>EnConv</td><td colspan="6">Enables conversion. This bit must be 1 for proper operation.</td></tr>
<tr><td>3</td><td>–</td><td colspan="6">This bit must be 0 for proper operation.</td></tr>
<tr><td>2
1
0</td><td>MD2
MD1
MD0</td><td colspan="6">Converter mode of operation setup.
<table>
<tr><th>MD2</th><th>MD1</th><th>MD0</th><th>Mode</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Idle</td><td>Part is fully powered up but performing no conversion.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Continuous Conversion</td><td>Part is repeatedly performing conversions, provided the EnConv bit is set.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Single Conversion</td><td>Part performs a single conversion, provided the EnConv bit is set. After finishing the conversion(s), the part goes to the idle mode.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Power-Down</td><td>Powers down the on-chip circuits, except the digital interface.</td></tr>
<tr><td>1</td><td>X</td><td>X</td><td>Reserved</td><td>Do not use these modes.</td></tr>
</table></td></tr>
</table>

POWER-DOWN TIMER REGISTER

Address Pointer 0x10
8 Bits, Read/Write, Factory Preset 0x00

Table 14. Power-Down Timer Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	–	–	Power-Down Timeout (6-Bit Value)					
Default	0	0	0x00					

Table 15. Power-Down Timer Register Bit Descriptions

Bit	Mnemonic	Description
[7:6]	-	These bits must be 0 for proper operation
[5:0]	Power-Down Timeout	Defines the period duration of the power-down timeout. If the output comparator output has not been activated during the programmed period, the part enters power-down mode automatically. The part can be then returned to a normal operational mode either via the serial interface or by the power supply off/on sequence. The period is programmable in steps of four hours. For example, setting the value to 0x06 sets the duration to 24 hours. The maximum value of 0x3F corresponds to approximately 10.5 days. The value of 0x00 disables the power-down timeout, and the part does not enter power-down mode automatically.

CAPDAC REGISTER

Address Pointer 0x11
8 Bits, Read/Write, Factory Preset 0x00

Table 16. CAPDAC Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	DacEn	DacAuto	DacValue (6-Bit Value)					
Default	1	1	0x00					

Table 17. CAPDAC Register Bit Descriptions

Bit	Mnemonic	Description
7	DacEn	DacEn = 1 enables capacitive DAC.
6	DacAuto	DacAuto = 1 enables the AutoDAC function in the adaptive threshold mode. When the AutoDAC function is enabled, the part dynamically adjusts the CAPDAC to keep the CDC in an optimal operating capacitive range. The CAPDAC value is automatically incremented when the data average exceeds ¾ of the CDC full range, and the CAPDAC value is decremented when the data average goes below ¼ of the CDC full range. The AutoDAC increment or decrement step depends on the selected CDC capacitive input range. Bit has no effect in fixed threshold mode; the AutoDAC function is always disabled in the fixed threshold mode.
[5:0]	DacValue	CAPDAC value, Code 0x00 ≈ 0 pF, Code 0x3F ≈ CAPDAC full range.

SERIAL NUMBER REGISTER

Address Pointer 0x13, 0x14, 0x15, 0x16
32 Bits, Read Only, 0xXXXX

This register holds a serial number, unique for each individual part.

CHIP ID REGISTER

Address Pointer 0x17
8 Bits, Read Only, 0xXX

This register holds the chip identification code, used in factory manufacturing and testing.

SERIAL INTERFACE

The AD7151 supports an I²C-compatible 2-wire serial interface. The two wires on the serial bus (interface) are called SCL (clock) and SDA (data). These two wires carry all addressing, control, and data information one bit at a time over the bus to all connected peripheral devices. The SDA wire carries the data, while the SCL wire synchronizes the sender and receiver during the data transfer. The devices on the bus are classified as either master or slave devices. A device that initiates a data transfer message is called a master, while a device that responds to this message is called a slave.

To control the AD7151 device on the bus, the following protocol must be followed. First, the master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that the start byte follows. This 8-bit start byte is made up of a 7-bit address plus an R/W bit indicator.

All peripherals connected to the bus respond to the start condition and shift in the next eight bits (7-bit address + R/W bit). The bits arrive MSB first. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as the acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. An exception to this is the general call address, which is described in the General Call section. In the idle condition, the device monitors the SDA and SCL lines waiting for the start condition and the correct address byte.

The R/W bit determines the direction of the data transfer. A Logic 0 LSB in the start byte means that the master writes information to the addressed peripheral. In this case, the AD7151 becomes a slave receiver. A Logic 1 LSB in the start byte means that the master reads information from the addressed peripheral. In this case, the AD7151 becomes a slave transmitter. In all instances, the AD7151 acts as a standard slave device on the serial bus.

The start byte address for the AD7151 is 0x90 for a write and 0x91 for a read.

READ OPERATION

When a read is selected in the start byte, the register that is currently addressed by the address pointer is transmitted to the SDA line by the AD7151. This is then clocked out by the master device, and the AD7151 awaits an acknowledge from the master.

If an acknowledge is received from the master, the address auto-incrementer automatically increments the address pointer register and outputs the next addressed register content to the SDA line for transmission to the master. If no acknowledge is received, the AD7151 returns to the idle state and the address pointer is not incremented. The address pointers' auto-incrementer allows block data to be written to or read from the starting address and subsequent incremental addresses.

In continuous conversion mode, the address pointers' auto-incrementer should be used for reading a conversion result. This means that the two data bytes should be read using one multibyte read transaction rather than two separate single-byte transactions. The single-byte data read transaction may result in the data bytes from two different results being mixed.

The user can also access any unique register (address) on a one-to-one basis without having to update all the registers. The address pointer register contents cannot be read.

If an incorrect address pointer location is accessed or if the user allows the auto-incrementer to exceed the required register address, the following applies:

- In read mode, the AD7151 continues to output various internal register contents until the master device issues a no acknowledge, start, or stop condition. The address pointers' auto-incrementer contents are reset to point to the status register at the 0x00 address when a stop condition is received at the end of a read operation. This allows the status register to be read (polled) continually without having to constantly write to the address pointer.
- In write mode, the data for the invalid address is not loaded into the AD7151 registers, but an acknowledge is issued by the AD7151.

WRITE OPERATION

When a write is selected, the byte following the start byte is always the register address pointer (subaddress) byte, which points to one of the internal registers on the AD7151. The address pointer byte is automatically loaded into the address pointer register and acknowledged by the AD7151. After the address pointer byte acknowledge, a stop condition, a repeated start condition, or another data byte can follow from the master. A stop condition is defined by a low-to-high transition on SDA while SCL remains high. If a stop condition is encountered by the AD7151, it returns to its idle condition and the address pointer is reset to 0x00.

If a data byte is transmitted after the register address pointer byte, the AD7151 loads this byte into the register that is currently addressed by the address pointer register and sends an acknowledge, and the address pointer auto-incrementer automatically increments the address pointer register to the next internal register address. Thus, subsequent transmitted data bytes are loaded into sequentially incremented addresses.

If a repeated start condition is encountered after the address pointer byte, all peripherals connected to the bus respond exactly as outlined previously for a start condition; that is, a repeated start condition is treated the same as a start condition. When a master device issues a stop condition, it relinquishes control of the bus, allowing another master device to take control of the bus. Therefore, a master wanting to retain control of the bus issues successive start conditions known as repeated start conditions.

AD7151 RESET

To reset the AD7151 without having to reset the entire serial bus, an explicit reset command is provided. This uses a particular address pointer word as a command word to reset the part and upload all default settings. The AD7151 does not respond to the serial bus commands (do not acknowledge) during the default values upload for approximately 2 ms.

The reset command address word is 0xBF.

GENERAL CALL

When a master issues a slave address consisting of seven 0s with the eighth bit (R/W bit) set to 0, this is known as the general call address. The general call address is for addressing every device connected to the serial bus. The AD7151 acknowledges this address and reads in the following data byte.

If the second byte is 0x06, the AD7151 is reset, completely uploading all default values. The AD7151 does not respond to the serial bus commands (do not acknowledge) during the default values upload for approximately 2 ms.

The AD7151 does not acknowledge any other general call commands.

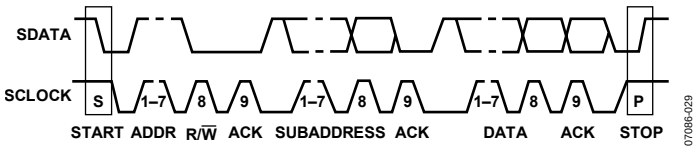


Figure 40. Bus Data Transfer

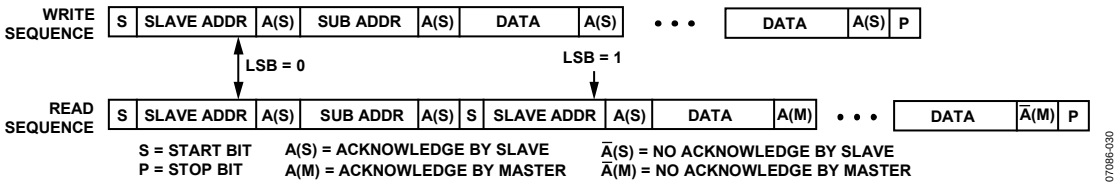


Figure 41. Write and Read Sequences

HARDWARE DESIGN CONSIDERATIONS

OVERVIEW

The AD7151 is an interface to capacitive sensors.

On the input side, the sensor (C_X) can be connected directly between the AD7151 EXC and CIN pins. The way it is connected and the electrical parameters of the sensor connection, such as parasitic resistance or capacitance, can affect the system performance. Therefore, any circuit with additional components in the capacitive front end, such as overvoltage protection, has to be carefully designed considering the AD7151 specified limits and information provided in this section.

On the output side, the AD7151 can work as a standalone device, using the power-up default register settings and flagging the result on digital outputs. Alternatively, the AD7151 can be interfaced to a microcontroller via the 2-wire serial interface, offering flexibility by overwriting the AD7151 register values from the host with a user-specific setup.

PARASITIC CAPACITANCE TO GROUND

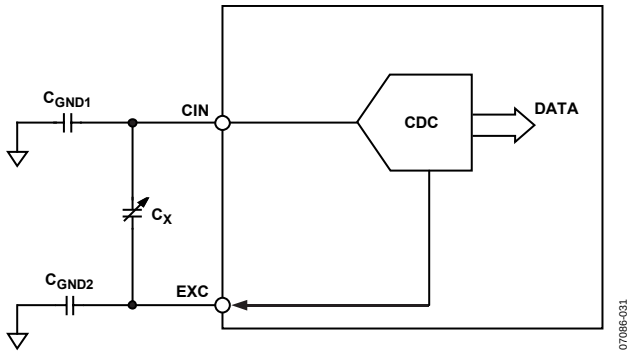


Figure 42. Parasitic Capacitance to Ground

The CDC architecture used in the AD7151 measures the capacitance C_X connected between the EXC pin and the CIN pin. In theory, any capacitance C_{GND} to ground should not affect the CDC result (see Figure 42).

The practical implementation of the circuitry in the chip implies certain limits, and the result is gradually affected by capacitance to ground (see Table 1 for information about the allowed capacitance to GND for CIN and information about excitation).

See Figure 4, Figure 5, Figure 6, and Figure 7.

PARASITIC RESISTANCE TO GROUND

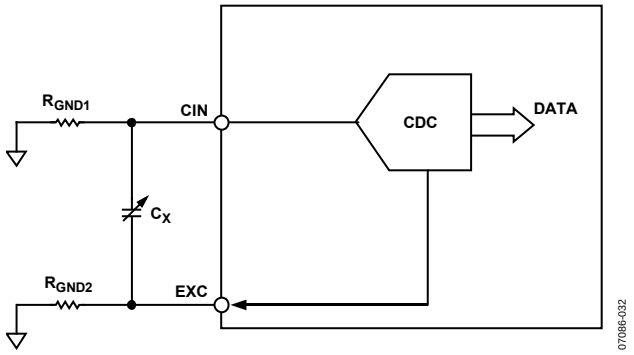


Figure 43. Parasitic Resistance to Ground

The AD7151 CDC result is affected by a leakage current from C_X to ground; therefore, C_X should be isolated from the ground. The equivalent resistance between C_X and ground should be maximized (see Figure 43).

See Figure 8, Figure 9, Figure 10, and Figure 11.

PARASITIC PARALLEL RESISTANCE

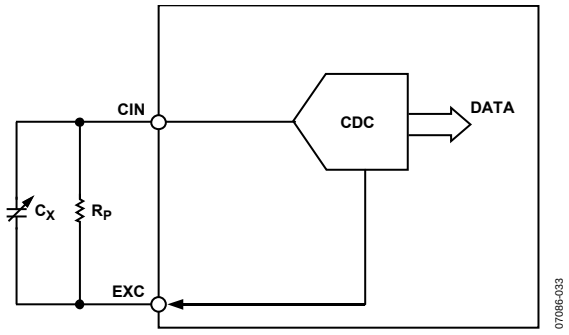


Figure 44. Parasitic Parallel Resistance

The AD7151 CDC measures the charge transfer between the EXC and CIN pins. Any resistance connected in parallel to the measured capacitance C_X (see Figure 44), such as the parasitic resistance of the sensor, also transfers charge. Therefore, the parallel resistor is seen as an additional capacitance in the output data. The equivalent parallel capacitance (or error caused by the parallel resistance) can be approximately calculated as

$$C_P = \frac{1}{R_P \times f_{EXC} \times 4}$$

where R_P is the parallel resistance and f_{EXC} is the excitation frequency.

See Figure 13.

PARASITIC SERIAL RESISTANCE

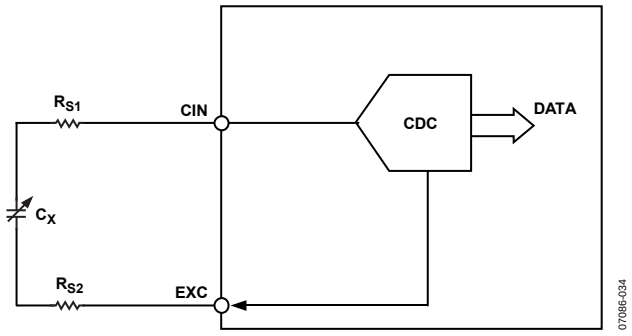


Figure 45. Parasitic Serial Resistance

The AD7151 CDC result is affected by a resistance in series with the measured capacitance. The total serial resistance (R_{S1} + R_{S2} in Figure 45) should be on the order of hundreds of Ω.

See Figure 12.

INPUT OVERVOLTAGE PROTECTION

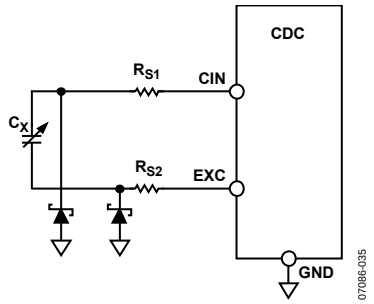


Figure 46. AD7151 CIN Overvoltage Protection

The AD7151 capacitive input has an internal ESD protection. However, some applications may require an additional overvoltage protection, depending on the application-specific requirements. Any additional circuit in the capacitive front end must be carefully designed, especially with respect to the limits recommended for maximum capacitance to ground, maximum serial resistance, maximum leakage, and so on.

INPUT EMC PROTECTION

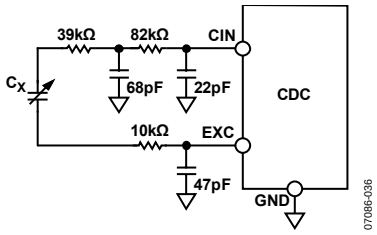


Figure 47. AD7151 CIN EMC Protection

Some applications may require an additional input filter for improving electromagnetic compatibility (EMC). Any input filter must be carefully designed, considering the balance between the system capacitance performance and system electromagnetic immunity.

Figure 47 shows one of the possible input circuit configurations significantly improving the system immunity against high frequency noise and slightly affecting the AD7151 performance in terms of additional gain and offset error.

POWER SUPPLY DECOUPLING AND FILTERING

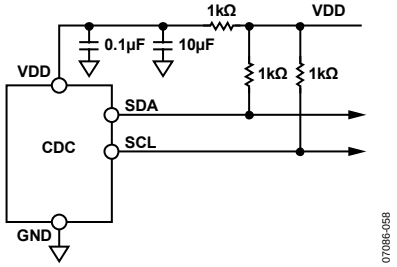


Figure 48. AD7151 V_{DD} Decoupling and Filtering

The AD7151 has good dc and low frequency power supply rejection but may be sensitive to higher frequency ripple and noise, specifically around the excitation frequency and its harmonics. Figure 48 shows a possible circuit configuration for improving the system immunity against ripple and noise coupled to the AD7151 via the power supply.

If the serial interface is connected to the other circuits in the system, it is better to connect the pull-up resistors on the other side of the V_{DD} filter than connect to the AD7151. If the AD7151 is used in standalone mode and the serial interface is not used, it is better to connect the pull-up resistors directly to the AD7151 V_{DD}.

APPLICATION EXAMPLES

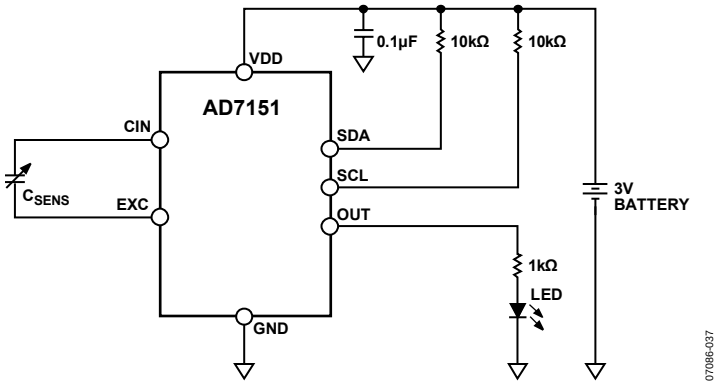


Figure 49. AD7151 Standalone Operation Application Diagram

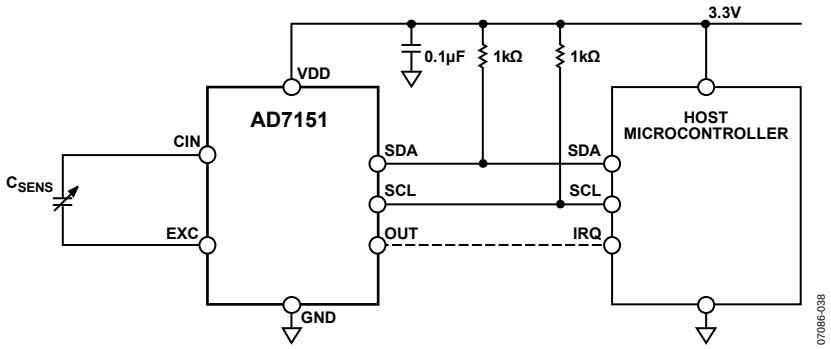


Figure 50. AD7151 Interfaced to a Host Microcontroller

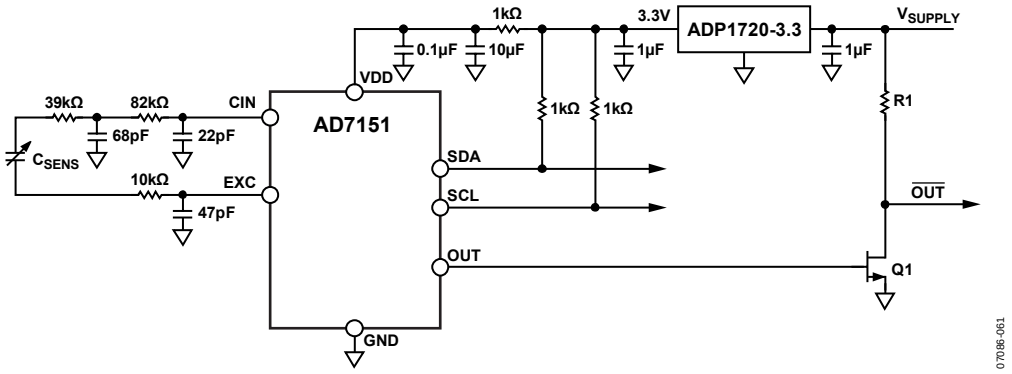


Figure 51. AD7151 Standalone Operation with EMC Protection and Optional Serial Interface

OUTLINE DIMENSIONS

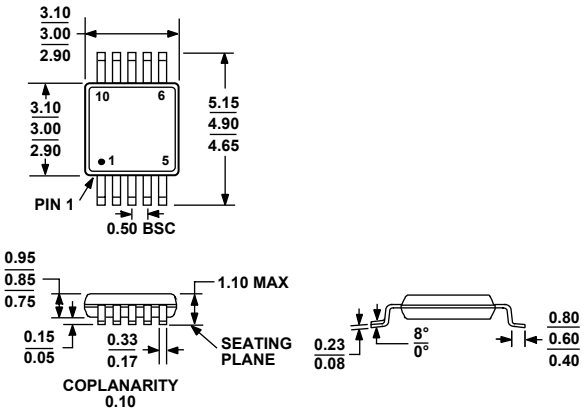


Figure 52. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD7151BRMZ[1]	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	C5M
AD7151BRMZ-REEL[1]	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	C5M

[1] Z = RoHS Compliant Part.

NOTES

NOTES

Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

©2007 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D07086-0-11/07(0)

ANALOG DEVICES

www.analog.com