80 MHz Bandwidth, IF Receiver

Data Sheet

AD6677

FEATURES

- JESD204B Subclass 0 or Subclass 1 coded serial digital outputs
- Signal-to-noise ratio (SNR) = 71.9 dBFS at 185 MHz AIN and 250 MSPS with noise shaping requantizer (NSR) set to 33%
- Spurious-free dynamic range (SFDR) = 87 dBc at 185 MHz A_{IN} and 250 MSPS
- Total power consumption: 435 mW at 250 MSPS
- 1.8 V supply voltages
- Integer 1 to 8 input clock divider
- Sample rates of up to 250 MSPS
- IF sampling frequencies of up to 400 MHz
- Internal analog-to-digital converter (ADC) voltage reference
- Flexible analog input range
  - 1.4 V p-p to 2.0 V p-p (1.75 V p-p nominal)
- ADC clock duty cycle stabilizer (DCS)
- Serial port control
- Energy saving power-down modes

APPLICATIONS

- Communications
- Diversity radio and smart antenna multiple input, multiple output (MIMO) systems
- Multimode digital receivers (3G)
  - TD-SCDMA, WiMAX, W-CDMA, CDMA2000, GSM, EDGE, LTE
- I/Q demodulation systems
- General-purpose software radios

GENERAL DESCRIPTION

The AD6677 is an 11-bit, 250 MSPS, intermediate frequency (IF) receiver specifically designed to support multi-antenna systems in telecommunication applications where high dynamic range performance, low power, and small size are desired.

The device consists of a high performance ADC and an NSR digital block. The ADC consists of a multistage, differential pipelined architecture with integrated output error correction logic, and each ADC features a wide bandwidth switched capacitor sampling network within the first stage of the differential pipeline. An integrated voltage reference eases design considerations. A duty cycle stabilizer compensates for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

The ADC output is connected internally to an NSR block. The integrated NSR circuitry allows for improved SNR performance in a smaller frequency band within the Nyquist bandwidth. The device supports two different output modes selectable via the serial port interface (SPI). With the NSR feature enabled, the output of the ADC is processed such that the AD6677 supports enhanced SNR performance within a limited portion of the Nyquist bandwidth while maintaining an 11-bit output resolution.

FUNCTIONAL BLOCK DIAGRAM

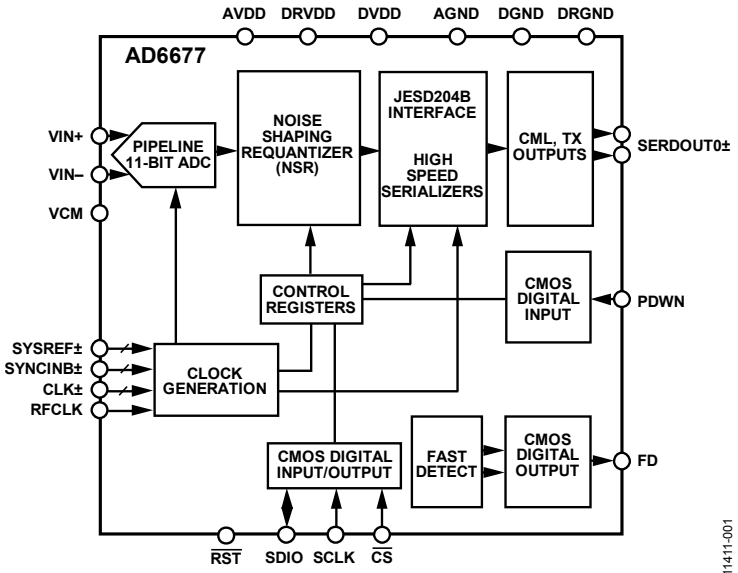

Figure 1.

Rev. C

Document Feedback

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REVISION HISTORY

1/16—Rev. B to Rev. C

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5/14—Rev. A to Rev. B

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3/14—Rev. 0 to Rev. A

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4/13—Revision 0: Initial Version

The NSR block can be programmed to provide a bandwidth of either 22% or 33% of the sample clock. For example, with a sample clock rate of 250 MSPS, the AD6677 can achieve up to 76.3 dBFS SNR for a 55 MHz bandwidth in the 22% mode and up to 73.5 dBFS SNR for an 82 MHz bandwidth in the 33% mode.

When the NSR block is disabled, the ADC data is provided directly to the output at a resolution of 11 bits. The AD6677 can achieve up to 65.9 dBFS SNR for the entire Nyquist bandwidth when operated in this mode. This allows the AD6677 to be used in telecommunication applications such as a digital predistortion observation path where wider bandwidths are required.

The output data is routed directly to an external JESD204B serial output lane. This output is at current mode logic (CML) voltage levels. Only one JESD204B lane configuration such that the output coded data is sent through one lane (L = 1; F = 4). Synchronization input controls (SYNCINB± and SYSREF±) are provided.

The AD6677 receiver digitizes a wide spectrum of IF frequencies. This IF sampling architecture greatly reduces component cost and complexity compared with traditional analog techniques or less integrated digital methods.

Flexible power-down options allow significant power savings, when desired. Programmable overrange level detection is supported via dedicated fast detect pins.

Programming for setup and control is accomplished using a 3-wire SPI-compatible serial interface with numerous modes to support board level system testing.

The AD6677 is available in a 32-lead LFCSP and is specified over the industrial temperature range of −40°C to +85°C.

PRODUCT HIGHLIGHTS

1. The configurable JESD204B output block with an integrated phase-locked loop (PLL) to support lane rates up to 5 Gbps.
2. The IF receiver includes an 11-bit, 250 MSPS ADC with programmable NSR function that allows for improved SNR within a reduced bandwidth of 22% or 33% of the sample rate.
3. Support for an optional radio frequency (RF) clock input to ease system board design.
4. Proprietary differential input maintains excellent SNR performance for input frequencies of up to 400 MHz.
5. An on-chip integer, 1-to-8 input clock divider and SYNC input allow synchronization of multiple devices.
6. Operation from a single 1.8 V power supply.
7. Standard SPI that supports various product features and functions, such as controlling the clock DCS, power-down, test modes, voltage reference mode, overrange fast detection, and serial output configuration.

SPECIFICATIONS

ADC DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, DVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.75 V p-p full-scale input range, duty cycle stabilizer enabled, default SPI, unless otherwise noted.

Table 1.

Parameter	Temperature	Min	Typ	Max	Unit
RESOLUTION	Full	11			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full			±9.0	mV
Gain Error	Full	−5.3		+1.2	%FSR
Differential Nonlinearity (DNL)	Full			±0.6	LSB
	25°C		±0.25		LSB
Integral Nonlinearity (INL)[1]	Full			±0.7	LSB
	25°C		±0.3		LSB
TEMPERATURE DRIFT					
Offset Error	Full		±7		ppm/°C
Gain Error	Full		±39		ppm/°C
INPUT REFERRED NOISE					
VREF = 1.75 V	25°C		0.46		LSB rms
ANALOG INPUT					
Input Span	Full		1.75		V p-p
Input Capacitance[2]	Full		2.5		pF
Input Resistance[3]	Full		20		kΩ
Input Common-Mode Voltage	Full		0.9		V
POWER SUPPLIES					
Supply Voltage					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
DVDD	Full	1.7	1.8	1.9	V
Supply Current					
I_{AVDD}	Full		149	163	mA
$I_{DRVDD} + I_{DVDD}$	Full				mA
NSR Disabled	Full		93		mA
NSR Enabled, 22% Mode	Full		120	128	mA
NSR Enabled, 33% Mode	Full		129		mA
POWER CONSUMPTION					
Sine Wave Input	Full				
NSR Disabled	Full		435		mW
NSR Enabled, 22% Mode	Full		484		mW
NSR Enabled, 33% Mode	Full		500		mW
Standby Power[4]	Full		266		mW
Power-Down Power[5]	Full		9		mW

[1] Measured with a low input frequency, full-scale sine wave.
[2] Input capacitance refers to the effective capacitance between one differential input pin and the complement.
[3] Input resistance refers to the effective resistance between one differential input pin and the complement.
[4] Standby power is measured with a low input frequency, full-scale sine wave and the CLK± pins active. Address 0x08 is set to 0x20, and the PDWN pin is asserted.
[5] Power-down power is measured with a low input frequency, full-scale sine wave, RFCLK pulled high, and the CLK± pins active. Address 0x08 is set to 0x00 and the PDWN pin is asserted.

ADC AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, DVDD = 1.8 V, maximum sample, VIN = −1.0 dBFS differential input, 1.75 V p-p full-scale input range, duty cycle stabilizer enabled, default SPI, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
SIGNAL-TO-NOISE-RATIO (SNR)					
NSR Disabled					
f_{IN} = 30 MHz	25°C		66.6		dBFS
f_{IN} = 90 MHz	25°C		66.4		dBFS
f_{IN} = 140 MHz	25°C		66.2		dBFS
f_{IN} = 185 MHz	25°C		66.1		dBFS
	Full	65.8			dBFS
f_{IN} = 220 MHz	25°C		65.9		dBFS
NSR Enabled 22% Bandwidth Mode					
f_{IN} = 30 MHz	25°C		76.3		dBFS
f_{IN} = 90 MHz	25°C		75.7		dBFS
f_{IN} = 140 MHz	25°C		74.8		dBFS
f_{IN} = 185 MHz	25°C		74.2		dBFS
	Full	73.6			dBFS
f_{IN} = 220 MHz	25°C		73.6		dBFS
NSR Enabled 33% Bandwidth Mode					
f_{IN} = 30 MHz	25°C		73.5		dBFS
f_{IN} = 90 MHz	25°C		72.1		dBFS
f_{IN} = 140 MHz	25°C		72.6		dBFS
f_{IN} = 185 MHz	25°C		71.9		dBFS
	Full	70.6			dBFS
f_{IN} = 220 MHz	25°C		71.4		dBFS
SIGNAL-TO-NOISE AND DISTORTION (SINAD)					
f_{IN} = 30 MHz	25°C		65.6		dBFS
f_{IN} = 90 MHz	25°C		65.3		dBFS
f_{IN} = 140 MHz	25°C		65.2		dBFS
f_{IN} = 185 MHz	25°C		65.1		dBFS
	Full	64.7			dBFS
f_{IN} = 220 MHz	25°C		64.8		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 30 MHz	25°C		10.6		Bits
f_{IN} = 90 MHz	25°C		10.6		Bits
f_{IN} = 140 MHz	25°C		10.5		Bits
f_{IN} = 185 MHz	25°C		10.5		Bits
f_{IN} = 220 MHz	25°C		10.5		Bits
WORST SECOND OR THIRD HARMONIC					
f_{IN} = 30 MHz	25°C		−87		dBc
f_{IN} = 90 MHz	25°C		−82		dBc
f_{IN} = 140 MHz	25°C		−86		dBc
f_{IN} = 185 MHz	25°C		−87		dBc
	Full			−80	dBc
f_{IN} = 220 MHz	25°C		−84		dBc

Parameter[1]	Temperature	Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 30 MHz	25°C		87		dBc
f_{IN} = 90 MHz	25°C		82		dBc
f_{IN} = 140 MHz	25°C		86		dBc
f_{IN} = 185 MHz	25°C		87		dBc
	Full	80			dBc
f_{IN} = 220 MHz	25°C		84		dBc
WORST OTHER (HARMONIC OR SPUR)					
f_{IN} = 30 MHz	25°C		−94		dBc
f_{IN} = 90 MHz	25°C		−85		dBc
f_{IN} = 140 MHz	25°C		−88		dBc
f_{IN} = 185 MHz	25°C		−90		dBc
	Full			−82	dBc
f_{IN} = 220 MHz	25°C		−87		dBc
TWO-TONE SFDR					
f_{IN1} = 184.12 MHz (−7 dBFS), f_{IN2} =187.12 MHz (−7 dBFS)	25°C		86		dBc
FULL POWER BANDWIDTH[2]	25°C		1000		MHz

[1] See the Application Note AN-835, *Understanding High Speed ADC Testing and Evaluation,* for a complete set of definitions.
[2] Full power bandwidth is the bandwidth of operation determined by where the spectral power of the fundamental frequency is reduced by 3 dB.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, DVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.75 V p-p full-scale input range, duty cycle stabilizer enabled, default SPI, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK−)					
Input CLK± Clock Rate	Full	40		625	MHz
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND		AVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	0		+60	µA
Low Level Input Current	Full	−60		0	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
RF CLOCK INPUT (RFCLK)					
RF Clock Rate	Full	500		1500	MHz
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Bias	Full		0.9		V
Input Voltage Range	Full	AGND		AVDD	V
High Input Voltage Level	Full	1.2		AVDD	V
Low Input Voltage Level	Full	AGND		0.6	V
High Level Input Current	Full	0		+150	µA
Low Level Input Current	Full	−150		0	µA
Input Capacitance	Full		1		pF
Input Resistance (AC-Coupled)	Full	8	10	12	kΩ

Parameter	Temperature	Min	Typ	Max	Unit
SYNCIN INPUTS (SYNCINB+/SYNCINB−)					
Logic Compliance			CMOS/LVDS		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage Range	Full	0.3		3.6	V p-p
Input Voltage Range	Full	DGND		DVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	−5		+5	µA
Low Level Input Current	Full	−10		+10	µA
Input Capacitance	Full		1		pF
Input Resistance	Full	12	16	20	kΩ
SYSREF INPUTS (SYSREF+, SYSREF−)					
Logic Compliance			LVDS		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage Range	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND		AVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	−5		+5	µA
Low Level Input Current	Full	−10		+10	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
LOGIC INPUT ($\overline{RST}$)[1]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−5		+5	µA
Low Level Input Current	Full	−100		−45	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUTS (SCLK, PDWN, $\overline{CS}$[2])[3]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	45		100	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (SDIO)[3]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	45		100	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
DIGITAL OUTPUTS (SERDOUT0+/SERDOUT0−)					
Logic Compliance			CML		
Differential Output Voltage (V_{OD})	Full	400	600	750	mV
Output Offset Voltage (V_{OS})	Full	0.75	DRVDD/2	1.05	V
DIGITAL OUTPUTS (SDIO/FD[4])					
High Level Output Voltage (V_{OH})	Full				
I_{OH} = 50 µA	Full	1.79			V
I_{OH} = 0.5 mA	Full	1.75			V
I_{OH} = 2.0 mA	Full	1.6			V

Parameter	Temperature	Min	Typ	Max	Unit
Low Level Output Voltage (V_{OL})	Full				
I_{OL} = 2.0 mA	Full			0.25	V
I_{OL} = 1.6 mA	Full			0.2	V
I_{OL} = 50 µA	Full			0.05	V

[1] Pull-up.
[2] Needs an external pull-up.
[3] Pull-down.
[4] Compatible with JEDEC standard JESD8-7A.

SWITCHING SPECIFICATIONS

Table 4.

Parameter	Symbol	Temperature	Min	Typ	Max	Unit
CLOCK INPUT PARAMETERS						
Conversion Rate[1]	f_S	Full	40		250	MSPS
SYSREF± Setup Time to Rising Edge CLK±[2]	t_{REFS}	Full		300		ps
SYSREF± Hold Time from Rising Edge CLK±[2]	t_{REFH}	Full		40		ps
SYSREF± Setup Time to Rising Edge RFCLK±[2]	t_{REFSRF}	Full		400		ps
SYSREF± Hold Time from Rising Edge RFCLK±[2]	t_{REFHRF}	Full		0		ps
CLK± Pulse Width High	t_{CH}					
Divide by 1 Mode, DCS Enabled		Full	1.8	2.0	2.2	ns
Divide by 1 Mode, DCS Disabled		Full	1.9	2.0	2.1	ns
Divide by 2 Mode Through Divide by 8 Mode		Full	0.8			ns
Aperture Delay	t_A	Full		1.0		ns
Aperture Uncertainty (Jitter)	t_J	Full		0.16		ps rms
DATA OUTPUT PARAMETERS						
Data Output Period or Unit Interval (UI)		Full		$20 \times f_S$		Seconds
Data Output Duty Cycle		25°C		50		%
Data Valid Time		25°C		0.78		UI
PLL Lock Time	t_{LOCK}	25°C		25		µs
Wake-Up						
Time (Standby)		25°C		10		µs
Time ADC (Power-Down)[3]		25°C		250		ms
Time Output (Power-Down)[4]		25°C		50		ms
Subclass 0: SYNCINB± Falling Edge to First Valid K.28 Characters (Delay Required for Rx CGS Start)		Full	5			Multiframes
Subclass 1: SYSREF± Rising Edge to First Valid K.28 Characters (Delay Required for SYNCB± Rising Edge/Rx CGS Start)		Full	6			Multiframes
CGS Phase K.28 Characters Duration		Full	1			Multiframe
Pipeline Delay						
JESD204B (Latency)		Full		36		Cycles[5]
Additional Pipeline Latency with NSR Enabled		Full		2		Cycles
Fast Detect (Latency)		Full		7		Cycles
Lane Rate		Full			5	Gbps
Uncorrelated Bounded High Probability (UBHP) Jitter		Full		12		ps
Random Jitter at 5 Gbps		Full		1.7		ps rms
Output Rise/Fall Time		Full		60		ps
Differential Termination Resistance		25°C		100		Ω
Out of Range Recovery Time		Full		3		Cycles

[1] Conversion rate is the clock rate after the divider.
[2] Refer to Figure 3 for timing diagram.
[3] Wake-up time ADC is defined as the time required for the ADC to return to normal operation from power-down mode.
[4] Wake-up time output is defined as the time required for JESD204B output to return to normal operation from power-down mode.
[5] Cycles refers to ADC conversion rate cycles.

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SPI TIMING REQUIREMENTS (See Figure 58)					
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between $\overline{CS}$ and SCLK	2			ns
t_H	Hold time between $\overline{CS}$ and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK must be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK must be in a logic low state	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in figures)	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in figures)	10			ns
t_{SPI_RST}	Time required after hard or soft reset until SPI access is available (not shown in figures)	500			µs

Timing Diagrams

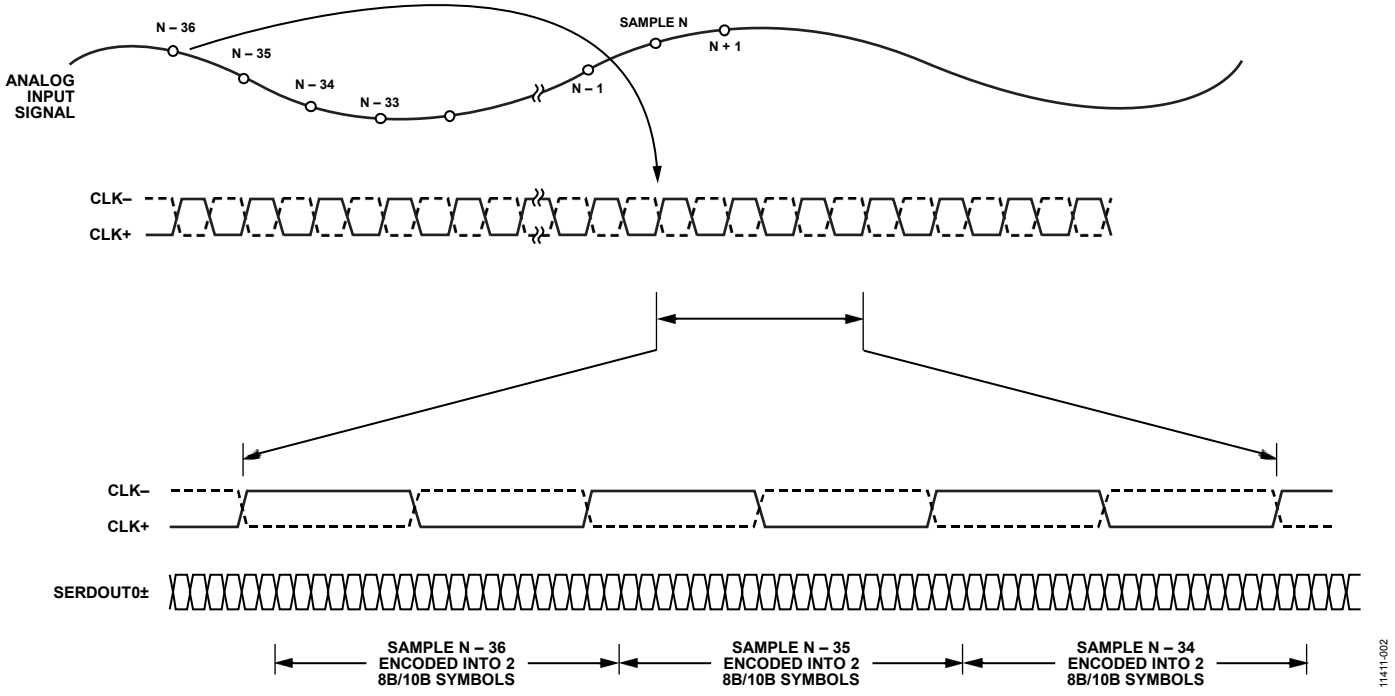

Figure 2. Data Output Timing

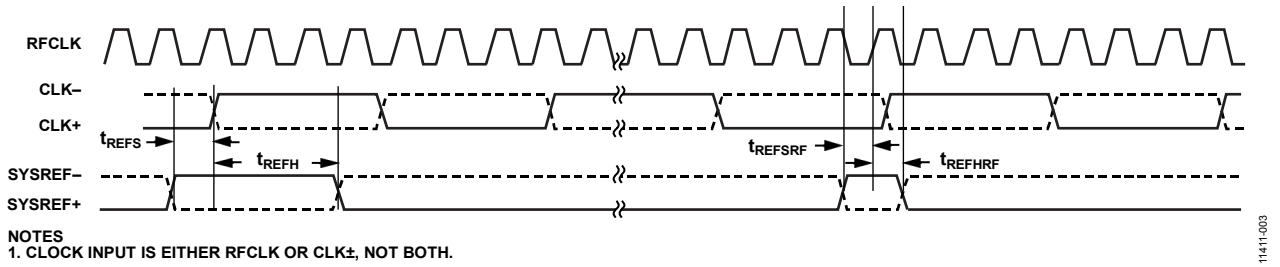

Figure 3. SYSREF± Setup and Hold Timing (Clock Input Either RFCLK or CLK±, Not Both)

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to DRGND	−0.3 V to +2.0 V
DVDD to DGND	−0.3 V to +2.0 V
VIN+, VIN− to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
RFCLK to AGND	−0.3 V to AVDD + 0.2 V
VCM to AGND	−0.3 V to AVDD + 0.2 V
$\overline{CS}$, PDWN to DGND	−0.3 V to DVDD + 0.3 V
SCLK to DGND	−0.3 V to DVDD + 0.3 V
SDIO to DGND	−0.3 V to DVDD + 0.3 V
$\overline{RST}$ to DGND	−0.3 V to DVDD + 0.3 V
FD to DGND	−0.3 V to DVDD + 0.3 V
SERDOUT0+, SERDOUT0− to AGND	−0.3 V to DRVDD + 0.3 V
SYNCINB+, SYNCINB− to DGND	−0.3 V to DVDD + 0.3 V
SYSREF+, SYSREF− to AGND	−0.3 V to AVDD + 0.3 V
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +125°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

The exposed pad must be soldered to the ground plane of the LFCSP package. This increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1,2]	θ_{JC}[1,3,4]	θ_{JB}[1,4,5]	Unit
32-Lead LFCSP 5 mm × 5 mm (CP-32-12)	0	37.1	3.1	20.7	°C/W
	1.0	32.4	N/A	N/A	°C/W
	2.5	29.1	N/A	N/A	°C/W

[1] Per JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-STD-883, Method 1012.1.
[4] N/A means not applicable.
[5] Per JEDEC JESD51-8 (still air).

Typical θ_{JA} is specified for a 4-layer printed circuit board (PCB) with a solid ground plane. As shown in Table 7, airflow increases heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

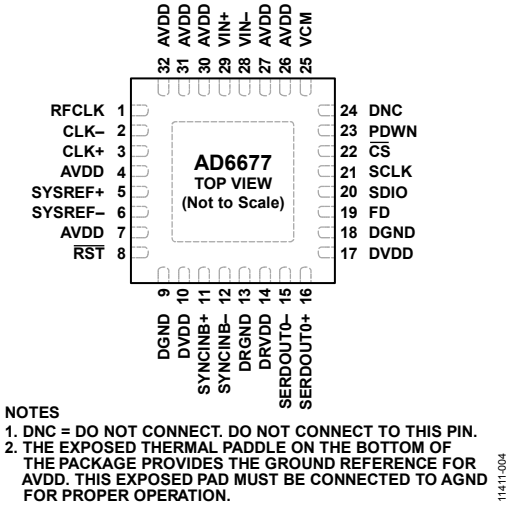

Figure 4. Pin Configuration (Top View)

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
4, 7, 26, 27, 30, 31, 32	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
9, 18	DGND	Ground	Ground Reference for DVDD.
10, 17	DVDD	Supply	Digital Power Supply (1.8 V Nominal).
13	DRGND	Ground	Ground Reference for DRVDD.
14	DRVDD	Supply	JESD204B PHY Serial Output Driver Supply (1.8 V Nominal). Note that the DRVDD power is referenced to the AGND plane.
24	DNC		Do Not Connect.
	EPAD (AGND)	Ground	Expose Pad. The exposed thermal pad on the bottom of the package provides the ground reference for AVDD. This exposed pad must be connected to AGND for proper operation.
ADC Analog			
1	RFCLK	Input	ADC RF Clock Input.
2	CLK–	Input	ADC Nyquist Clock Input—Complement.
3	CLK+	Input	ADC Nyquist Clock Input—True.
25	VCM	Output	Common-Mode Level Bias Output for Analog Inputs. Decouple this pin to ground using a 0.1 µF capacitor.
28	VIN–	Input	Differential Analog Input (Negative).
29	VIN+	Input	Differential Analog Input (Positive).
ADC Fast Detect Output			
19	FD	Output	Fast Detect Indicator (CMOS Levels).
Digital Inputs			
5	SYSREF+	Input	JESD204B LVDS SYSREF Input—True.
6	SYSREF–	Input	JESD204B LVDS SYSREF Input—Complement.
11	SYNCINB+	Input	JESD204B LVDS Sync Input—True/JESD204B CMOS Sync Input.
12	SYNCINB–	Input	JESD204B LVDS Sync Input—Complement.
Data Outputs			
15	SERDOUT0–	Output	CML Output Data—Complement.
16	SERDOUT0+	Output	CML Output Data—True.

Pin No.	Mnemonic	Type	Description
Device Under Test (DUT) Controls			
8	$\overline{\text{RST}}$	Input	Digital Reset (Active Low).
20	SDIO	Input/output	SPI Serial Data Input/Output.
21	SCLK	Input	SPI Serial Clock.
22	$\overline{\text{CS}}$	Input	SPI Chip Select (Active Low). This pin needs an external pull-up.
23	PDWN	Input	Power-Down Input (Active High). The operation of this pin depends on SPI mode and can be configured as power-down or standby (see Table 17).

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, DVDD = 1.8 V, sample rate is 250 MSPS, duty cycle stabilizer enabled, 1.75 V p-p differential input, VIN = −1.0 dBFS, 16k sample, T_A = 25°C, default SPI, unless otherwise noted.

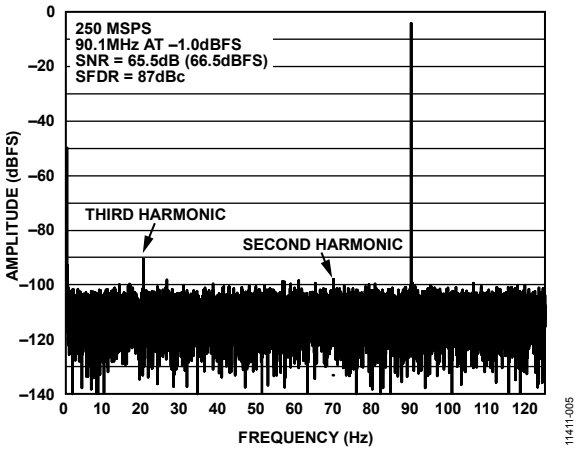

Figure 5. Single-Tone FFT with f_{IN} = 90.1 MHz

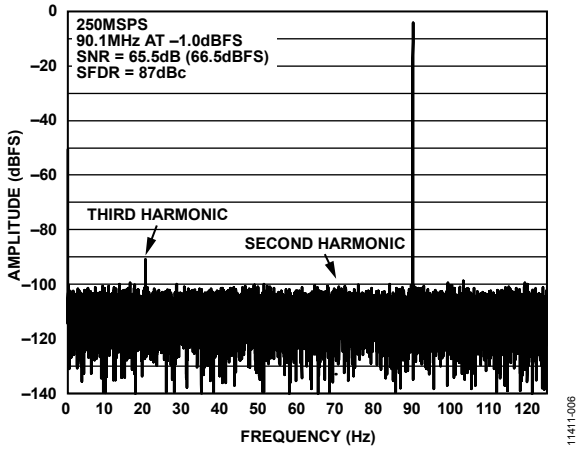

Figure 6. Single-Tone FFT with f_{IN} = 90.1 MHz, RFCLK = 1.0 GHz with Divide by 4 (Address 0x09 = 0x21)

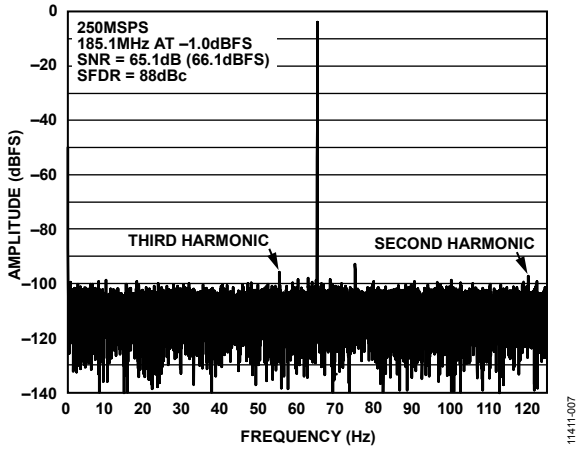

Figure 7. Single-Tone FFT with f_{IN} = 185.1 MHz

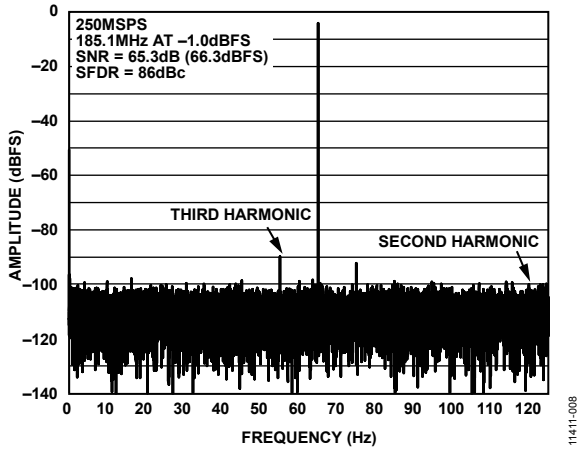

Figure 8. Single-Tone FFT with f_{IN} = 185.1 MHz, RFCLK = 1.0 GHz with Divide by 4 (Address 0x09 = 0x21)

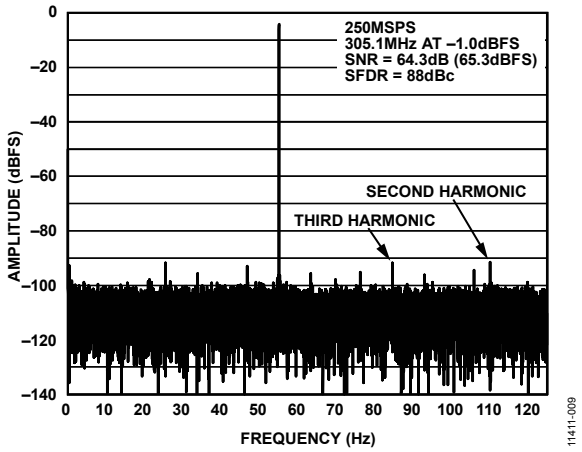

Figure 9. Single-Tone FFT with f_{IN} = 305.1 MHz

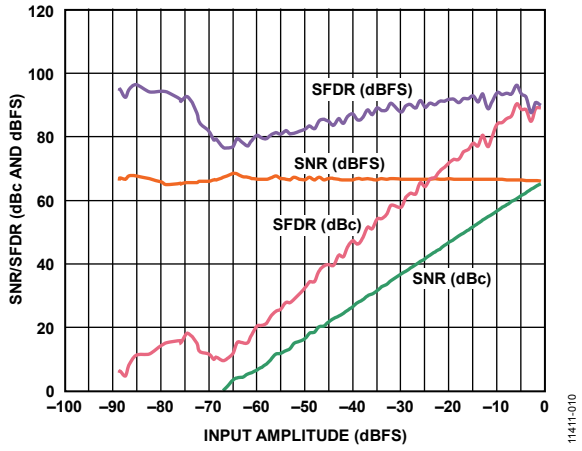

Figure 10. Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 185.1 MHz

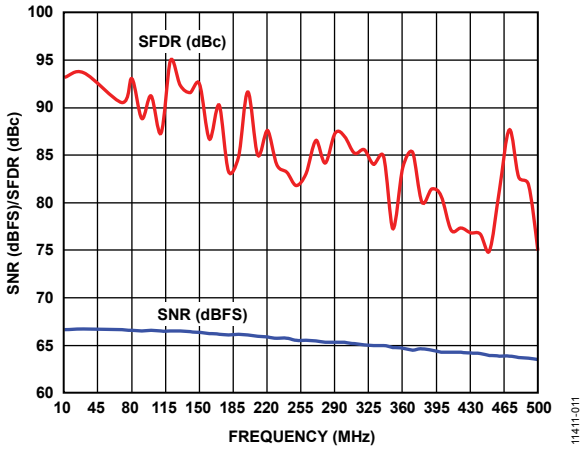

Figure 11. Single-Tone SNR/SFDR vs. Input Frequency (f_{IN})

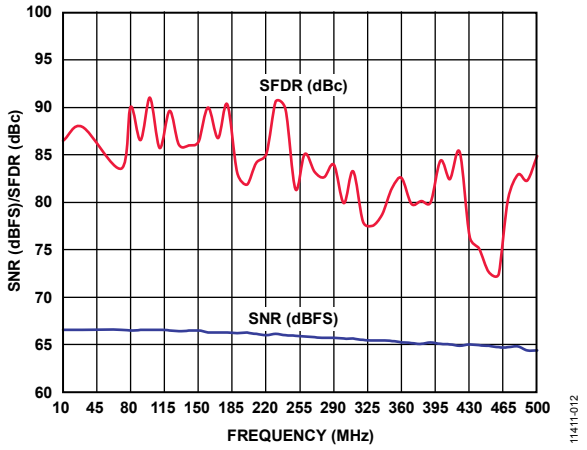

Figure 12. Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}), RFCLK = 1.0 GHz with Divide by 4 (Address 0x09 = 0x21)

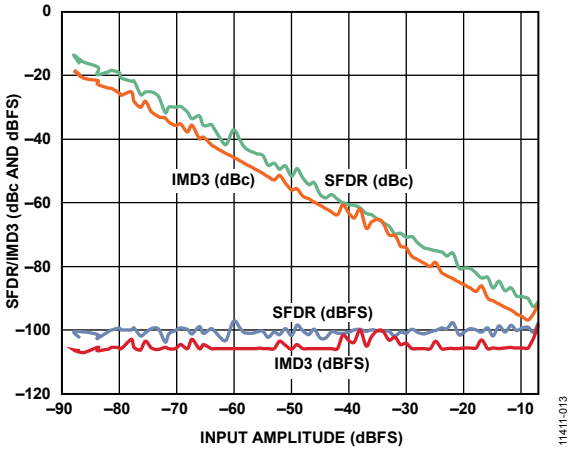

Figure 13. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz

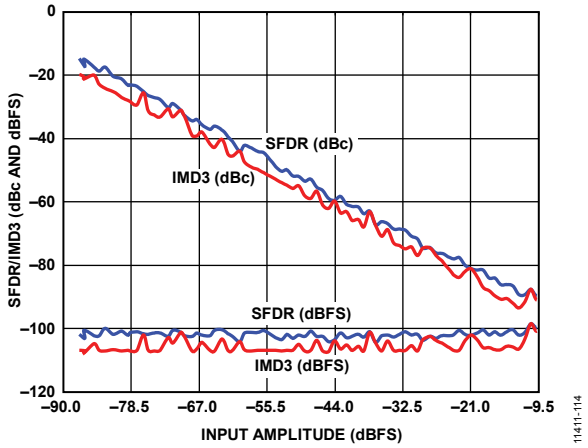

Figure 14. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz

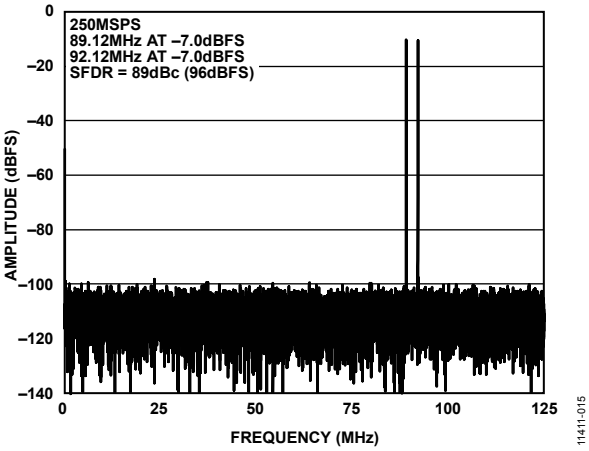

Figure 15. Two-Tone FFT with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz

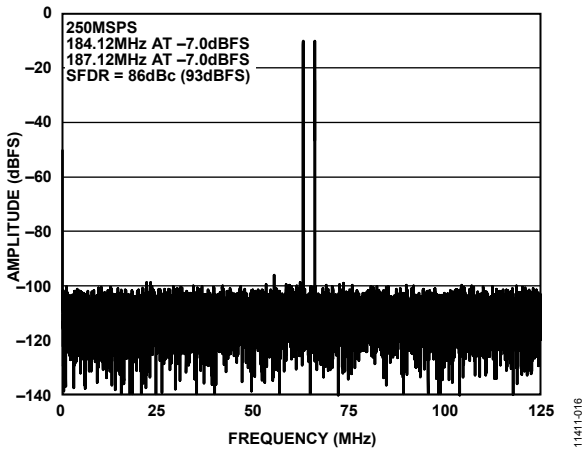

Figure 16. Two-Tone FFT with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz

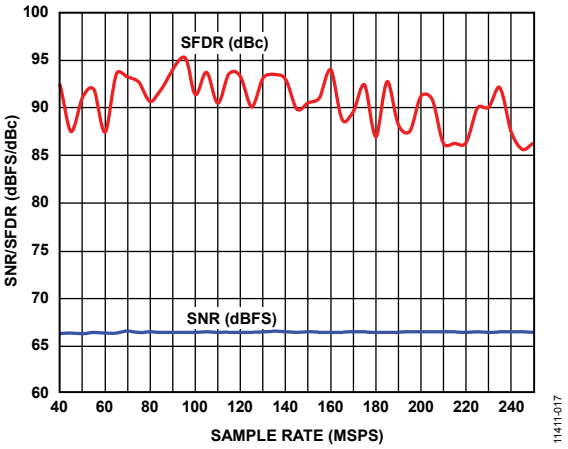

Figure 17. Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 90.1 MHz

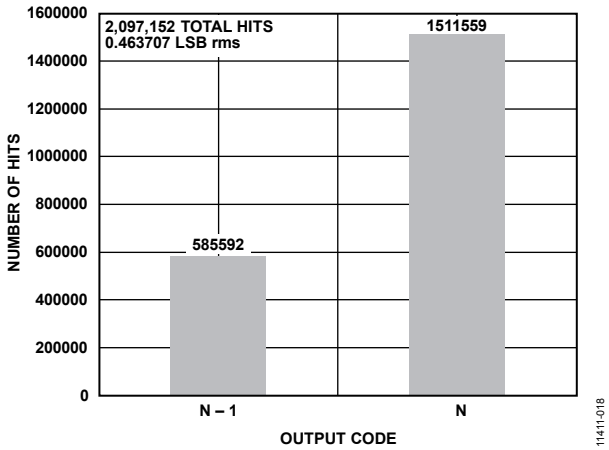

Figure 18. Grounded Input Histogram

EQUIVALENT CIRCUITS

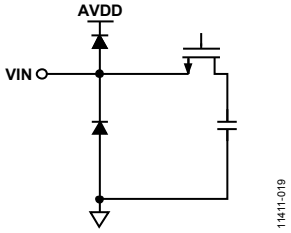

Figure 19. Equivalent Analog Input Circuit

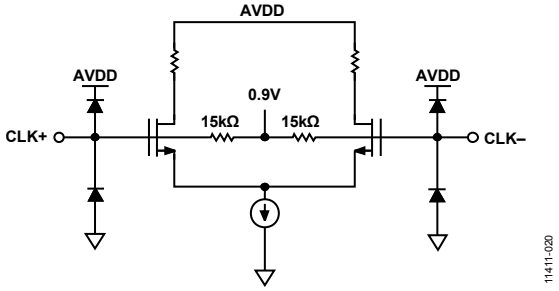

Figure 20. Equivalent Clock Input Circuit

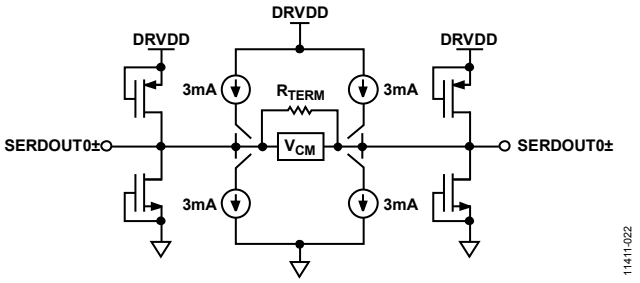

Figure 21. Digital CML Output Circuit

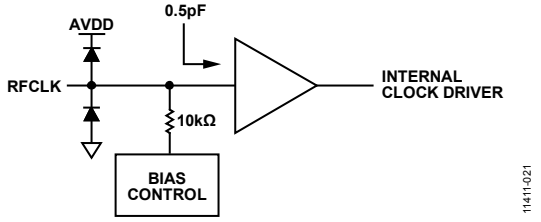

Figure 22. Equivalent RF Clock Input Circuit

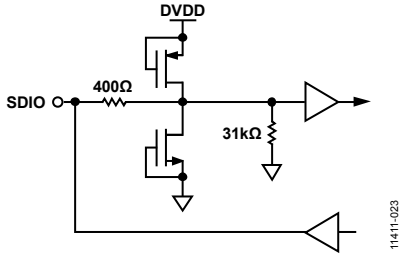

Figure 23. Equivalent SDIO Circuit

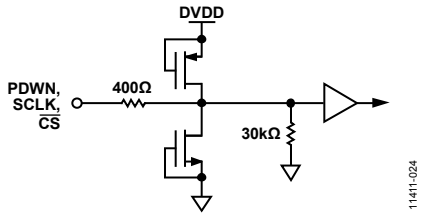

Figure 24. Equivalent PDWN, SCLK, or $\overline{CS}$ Input Circuit

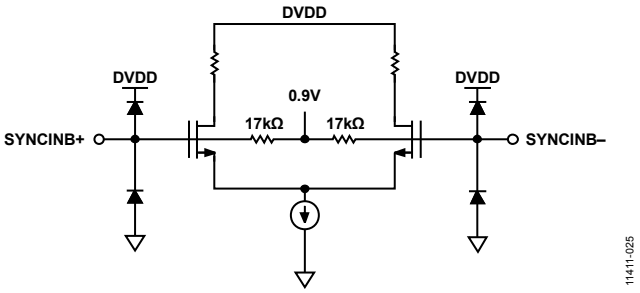

Figure 25. Equivalent SYNCINB± Input Circuit

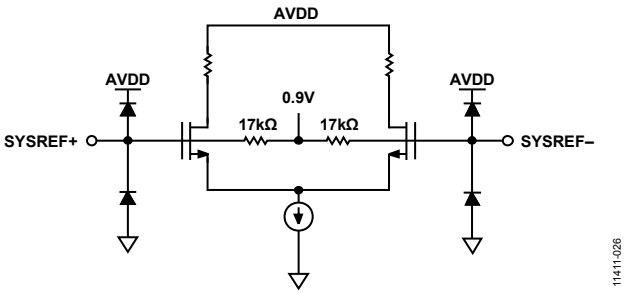

Figure 26. Equivalent SYSREF± Input Circuit

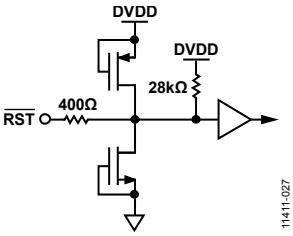

Figure 27. Equivalent $\overline{RST}$ Input Circuit

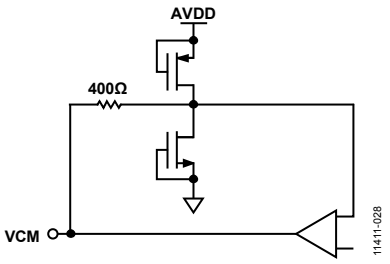

Figure 28. Equivalent VCM Circuit

THEORY OF OPERATION

The AD6677 has one analog input channel and one JESD204B output lane. The signal passes through several stages before appearing at the output port.

The dual ADC design can be used for diversity reception of signals, where the ADCs operate identically on the same carrier but from two separate antennae. The ADCs can also operate with independent analog inputs. The user can sample frequencies from dc to 400 MHz using appropriate low-pass or band-pass filtering at the ADC inputs with little loss in ADC performance. Operation above 400 MHz analog input is permitted but occurs at the expense of increased ADC noise and distortion.

A synchronization capability is provided to allow synchronized timing between multiple devices.

Programming and control of the AD6677 are accomplished using a 3-pin, SPI-compatible serial interface.

ADC ARCHITECTURE

The AD6677 architecture consists of a front-end, sample-and-hold circuit, followed by a pipelined switched capacitor ADC. The quantized outputs from each stage are combined into a final 11-bit result in the digital correction logic. Alternately, the 11-bit result can be processed through the NSR block before it is sent to the digital correction logic.

The pipelined architecture permits the first stage to operate on a new input sample, and the remaining stages to operate on the preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor digital-to-analog converter (DAC) and an interstage residue amplifier (MDAC). The MDAC magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage contains a differential sampling circuit that can be ac- or dc-coupled in differential or single-ended modes. The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing digital output noise to be separated from the analog core.

The user can input frequencies from dc to 300 MHz using appropriate low-pass or band-pass filtering at the ADC inputs, with little loss in performance. Operation to a 400 MHz analog input is permitted; however, it occurs at the expense of increased ADC noise and distortion. A synchronization capability is provided to allow synchronized timing between multiple devices. Programming and control of the AD6677 are accomplished using a 3-wire SPI-compatible serial interface.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD6677 is a differential, switched capacitor circuit that has been designed for optimum performance while processing a differential input signal.

The clock signal alternatively switches the input between sample mode and hold mode (see the configuration shown in Figure 29). When the input is switched into sample mode, the signal source must be capable of charging the sampling capacitors and settling within 1/2 clock cycle.

A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. A shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC input; therefore, the precise values are dependent on the application.

In IF undersampling applications, reduce the shunt capacitors. In combination with the driving source impedance, the shunt capacitors limit the input bandwidth. Refer to the Application Note AN-742, *Frequency Domain Response of Switched-Capacitor ADCs*; the Application Note AN-827, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*; and the *Analog Dialogue* article, "Transformer-Coupled Front-End for Wideband A/D Converters," for more information.

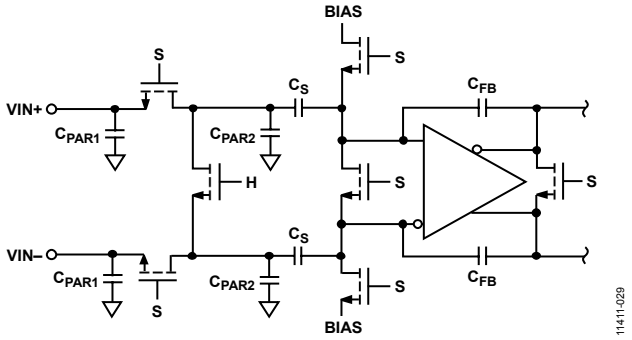

Figure 29. Switched Capacitor Input

For best dynamic performance, match the source impedances driving VIN+ and VIN− and differentially balance the inputs.

Input Common Mode

The analog inputs of the AD6677 are not internally dc biased. In ac-coupled applications, the user must provide this bias externally. Configuring the input so that V_{CM} = 0.5 × AVDD (or 0.9 V) is recommended for optimum performance. An on-board common-mode voltage reference is included in the design and is available from the VCM pin. Using the VCM output to set the input common mode is recommended. Optimum performance is achieved when the common-mode voltage of the analog input is set by the VCM pin voltage (typically 0.5 × AVDD). Decouple the VCM pin to ground by using a 0.1 µF capacitor, as described in the Applications Information section. Place this decoupling capacitor close to the pin to minimize the series resistance and inductance between the device and this capacitor.

Differential Input Configurations

Optimum performance is achieved while driving the AD6677 in a differential input configuration. For baseband applications, the AD8138, ADA4937-1, ADA4938-1, and ADA4930-1 differential drivers provide excellent performance and a flexible interface to the ADC.

The output common-mode voltage of the ADA4930-1 is easily set with the VCM pin of the AD6677 (see Figure 30), and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

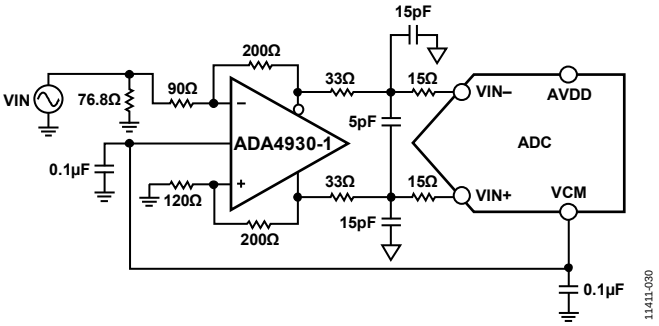

Figure 30. Differential Input Configuration Using the ADA4930-1

For baseband applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example is shown in Figure 31. To bias the analog input, the VCM voltage can be connected to the center tap of the secondary winding of the transformer.

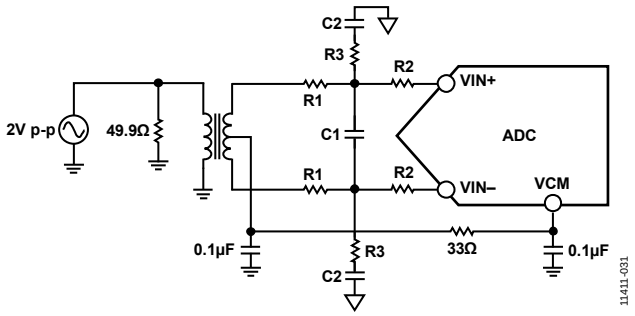

Figure 31. Differential Transformer-Coupled Configuration

Consider the signal characteristics when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz. Excessive signal power can also cause core saturation, which leads to distortion.

At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD6677. For applications where SNR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 32). In this configuration, the input is ac-coupled and the VCM voltage is provided to each input through a 33 Ω resistor. These resistors compensate for losses in the input baluns to provide a 50 Ω impedance to the driver.

In the double balun and transformer configurations, the value of the input capacitors and resistors is dependent on the input frequency and source impedance. Based on these parameters, the value of the input resistors and capacitors may need to be adjusted or some components may need to be removed. Table 9 displays recommended values to set the RC network for different input frequency ranges. However, these values are dependent on the input signal and bandwidth and must only be used as a starting guide. Note that the values given in Table 9 are for each R1, R2, C1, C2, and R3 components shown in Figure 31 and Figure 32.

Table 9. Example RC Network

Frequency Range (MHz)	R1 Series (Ω)	C1 Differential (pF)	R2 Series (Ω)	C2 Shunt (pF)	R3 Shunt (Ω)
0 to 100	33	8.2	0	15	24.9
100 to 400	15	8.2	0	8.2	24.9
>400	15	≤3.9	0	≤3.9	24.9

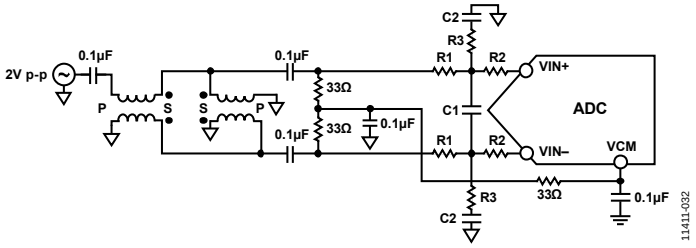

Figure 32. Differential Double Balun Input Configuration

An alternative to using a transformer-coupled input at frequencies in the second Nyquist zone is to use an amplifier with variable gain. The AD8375 digital variable gain amplifier (DVGA) provides good performance for driving the AD6677. Figure 33 shows an example of the AD8375 driving the AD6677 through a band-pass antialiasing filter.

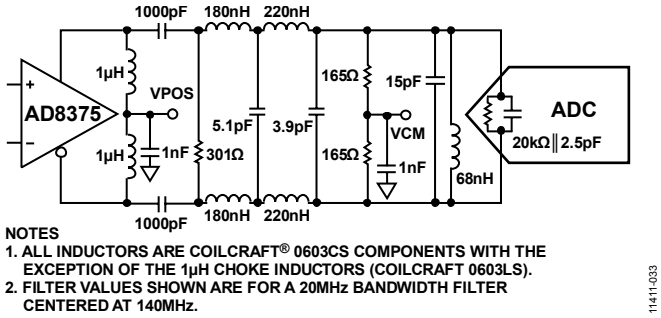

Figure 33. Differential Input Configuration Using the AD8376

VOLTAGE REFERENCE

A stable and accurate voltage reference is built into the AD6677. The full-scale input range can be adjusted by varying the reference voltage via the SPI. The input span of the ADC tracks the reference voltage changes linearly.

CLOCK INPUT CONSIDERATIONS

The AD6677 has two options for deriving the input sampling clock: a differential Nyquist sampling clock input or an RF clock input (which is internally divided by 2 or 4). The clock input is selected in Address 0x09 and, by default, is configured for the Nyquist clock input. For optimum performance, clock the AD6677 Nyquist sample clock input, CLK+ and CLK−, with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK− pins via a transformer or capacitors. These pins are biased internally (see Figure 34) and require no external bias. If the clock inputs are floated, CLK− is pulled slightly lower than CLK+ to prevent spurious clocking.

Nyquist Clock Input Options

The AD6677 Nyquist clock input supports a differential clock between 40 MHz to 625 MHz. The clock input structure supports differential input voltages from 0.3 V to 3.6 V and is, therefore, compatible with various logic family inputs, such as CMOS, LVDS, and LVPECL. A sine wave input is also accepted, but higher slew rates typically provide optimal performance. Clock source jitter is a critical parameter that can affect performance, as described in the Jitter Considerations section. If the inputs are floated, pull the CLK− pin low to prevent spurious clocking.

The Nyquist clock input pins, CLK+ and CLK−, are internally biased to 0.9 V and have a typical input impedance of 4 pF in parallel with 10 kΩ (see Figure 34). The input clock is typically ac-coupled to CLK+ and CLK−. Some typical clock drive circuits are presented in Figure 35 through Figure 38 for reference.

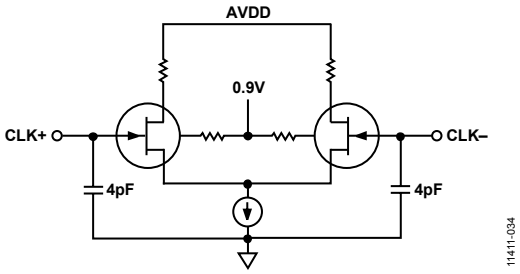

Figure 34. Equivalent Nyquist Clock Input Circuit

For applications where a single-ended low jitter clock between 40 MHz to 200 MHz is available, an RF transformer is recommended. Figure 35 shows an example of using an RF transformer in the clock network. At frequencies above 200 MHz, an RF balun is recommended, as seen in Figure 36. The back to back Schottky diodes across the transformer secondary limit clock excursions into the AD6677 to approximately 0.8 V p-p differential. This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD6677, yet preserves the fast rise and fall times of the clock, which are critical to low jitter performance.

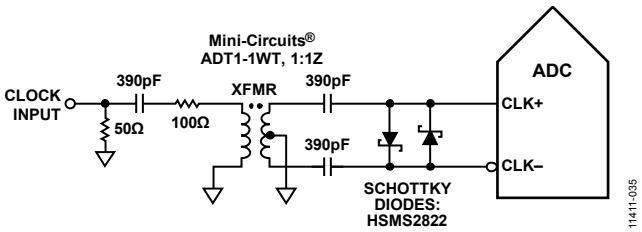

Figure 35. Transformer-Coupled Differential Clock (Up to 200 MHz)

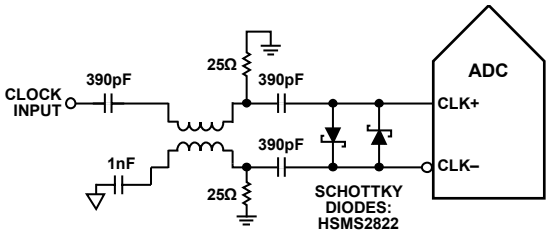

Figure 36. Balun-Coupled Differential Clock (Up to 625 MHz)

In some cases, it is desirable to buffer or generate multiple clocks from a single source. In those cases, Analog Devices, Inc., offers clock drivers with excellent jitter performance. Figure 37 shows a typical PECL driver circuit that uses PECL drivers such as the AD9510, AD9511, AD9512, AD9513, AD9514, AD9515, the AD9516-0 through AD9516-5 device family, the AD9517-0 through AD9517-4 device family, the AD9518-0 through AD9518-4 device family, the AD9520-0 through AD9520-5 device family, the AD9522-0 through AD9522-5 device family, AD9523, AD9524, and ADCLK905/ADCLK907/ADCLK925.

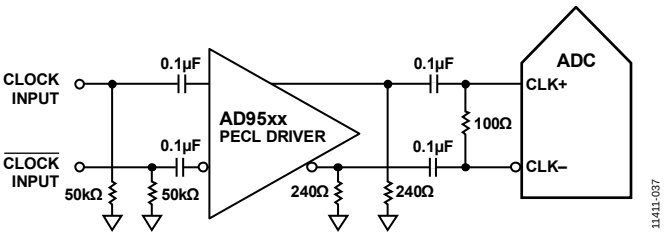

Figure 37. Differential PECL Sample Clock (Up to 625 MHz)

Analog Devices also offers LVDS clock drivers with excellent jitter performance. Figure 38 shows a typical circuit. This illustrates using LVDS drivers such as the AD9510, AD9511, AD9512, AD9513, AD9514, AD9515, the AD9516-0 through AD9516-5 device family, the AD9517-0 through AD9517-4 device family, the AD9518-0 through AD9518-4 device family, the AD9520-0 through AD9520-5 device family, the AD9522-0 through AD9522-5 device family, AD9523, and AD9524.

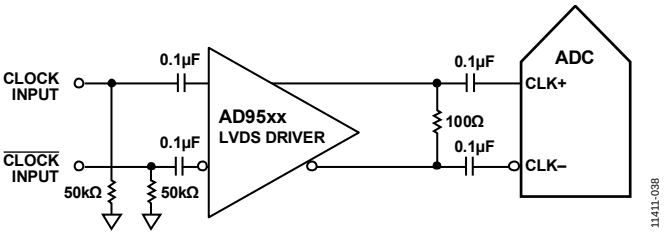

Figure 38. Differential LVDS Sample Clock (Up to 625 MHz)

RF Clock Input Options

The AD6677 RF clock input supports a single-ended clock between 500 MHz to 1.5 GHz. The equivalent RF clock input circuit is shown in Figure 39. The input is self biased to 0.9 V and is typically ac-coupled. The input has a typical input impedance of 10 kΩ in parallel with 0.5 pF at the RFCLK pin.

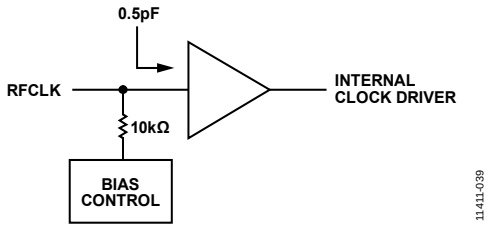

Figure 39. Equivalent RF Clock Input Circuit

It is recommended that the RF clock input of the AD6677 be driven with a PECL or sine wave signal with a minimum signal amplitude of 600 mV p-p. Regardless of the type of signal used, clock source jitter is of the most concern, as described in the Jitter Considerations section. Figure 40 shows the preferred method of clocking when using the RF clock input on the AD6677. Due to the high frequency nature of the signal, it is recommended to use a 50 Ω transmission line to route the clock signal to the RF clock input of the AD6677 and terminate the transmission line close to the RF clock input.

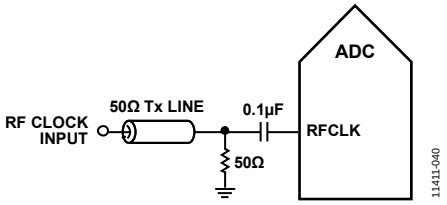

Figure 40. Typical RF Clock Input Circuit

Figure 41 shows the RF clock input of the AD6677 being driven from the LVPECL outputs of the AD9515. The differential LVPECL output signal from the AD9515 is converted to a single-ended signal using an RF balun or RF transformer. The RF balun configuration is recommended for clock frequencies associated with the RF clock input.

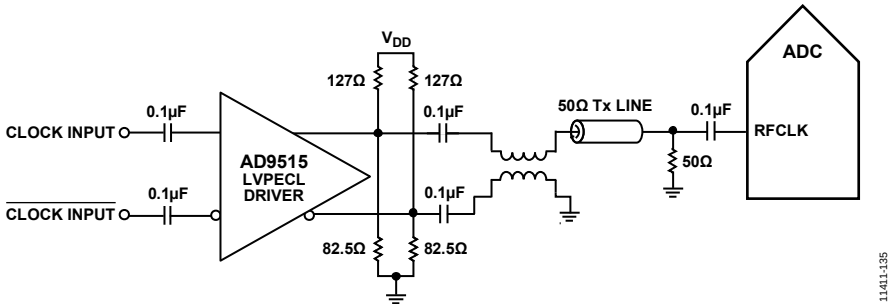

Figure 41. Differential PECL RF Clock Input Circuit

Input Clock Divider

The AD6677 contains an input clock divider with the ability to divide the Nyquist input clock by integer values between 1 and 8. The RF clock input uses an on-chip predivider to divide the clock input by four before it reaches the 1 to 8 divider. This allows higher input frequencies to be achieved on the RF clock input. The divide ratios can be selected using Address 0x09 and Address 0x0B. Address 0x09 sets the RF clock input and Address 0x0B can set the divide ratio of the 1 to 8 divider for both the RF clock input and the Nyquist clock input. For divide ratios other than 1, the duty cycle stabilizer is automatically enabled.

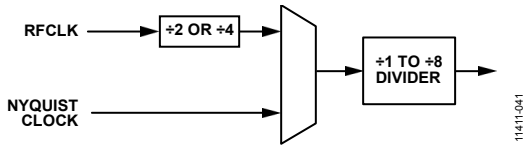

Figure 42. AD6677 Clock Divider Circuit

The AD6677 clock divider can be synchronized using the external SYSREF input. Bit 1 and Bit 2 of Address 0x3A allow the clock divider to be resynchronized on every SYSREF signal or only on the first signal after the register is written. A valid SYSREF causes the clock divider to reset to the initial state. This synchronization feature allows multiple devices to align the clock dividers to guarantee simultaneous input sampling.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD6677 contains a DCS that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD6677.

Jitter on the rising edge of the input clock is still of paramount concern and is not reduced by the DCS. The duty cycle control loop does not function for clock rates of less than 40 MHz nominally. The loop has a time constant associated with it that must be considered when the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal. During the time that the loop is not locked, the DCS loop is bypassed, and the internal device timing is dependent on the duty cycle of the input clock signal. In such applications, it may be appropriate to disable the DCS. In all other applications, enabling the DCS circuit is recommended to maximize ac performance.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_{IN}) due to jitter (t_J) can be calculated by

$$SNR_{HF} = -10 \log[(2\pi \times f_{IN} \times t_{JRMS})^2 + 10^{(-SNR_{LF}/10)}]$$

In the equation, the rms aperture jitter represents the root-mean-square of all jitter sources, which include the clock input, the analog input signal, and the ADC aperture jitter specification. IF undersampling applications are particularly sensitive to jitter, as shown in Figure 43.

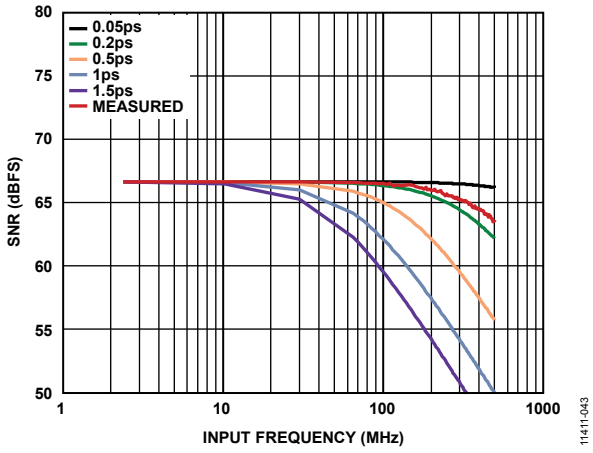

Figure 43. SNR vs. Input Frequency and Jitter

Treat the clock input as an analog signal in cases where aperture jitter may affect the dynamic range of the AD6677. Separate the power supplies for the clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), retime it by using the original clock at the last step.

Refer to the Application Note AN-501, *Aperture Uncertainty and ADC System Performance*, and the Application Note AN-756, *Sampled Systems and the Effects of Clock Phase Noise and Jitter*, for more information about jitter performance as it relates to ADCs.

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 44, the power dissipated by the AD6677 is proportional to the sample rate. The data in Figure 44 was taken using the same operating conditions as those used for the Typical Performance Characteristics section. I_{DVDD} in Figure 44 is a summation of I_{DVDD} and I_{DRVDD}.

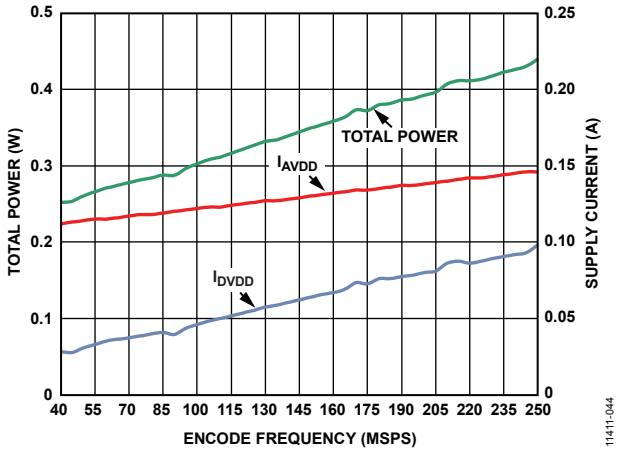

Figure 44. Power vs. Encode Rate

By asserting PDWN (either through the SPI port or by asserting the PDWN pin high), the AD6677 is placed in power-down mode. In this state, the ADC typically dissipates about 9 mW. Asserting the PDWN pin low returns the AD6677 to the normal operating mode.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. Internal capacitors are discharged when entering power-down mode and then must be recharged when returning to normal operation. As a result, wake-up time is related to the time spent in power-down mode, and shorter power-down cycles result in proportionally shorter wake-up times.

When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the Memory Map Register Descriptions section and theApplication Note AN-877, *Interfacing to High Speed ADCs via SPI*, for additional details.

NOISE SHAPING REQUANTIZER

The AD6677 features a NSR to allow higher than 11-bit SNR to be maintained in a subset of the Nyquist band. The harmonic performance of the receiver is unaffected by the NSR feature. When enabled, the NSR contributes an additional 0.6 dB of loss to the input signal, such that a 0 dBFS input is reduced to −0.6 dBFS at the output pins.

Two different bandwidth modes are provided; the mode can be selected from the SPI port. In each of the two modes, the center frequency of the band can be tuned such that IFs can be placed anywhere in the Nyquist band.

22% BANDWIDTH MODE (>40 MHZ AT 184.32 MSPS)

The first bandwidth mode offers excellent noise performance over 22% of the ADC sample rate (44% of the Nyquist band) and can be centered by setting the NSR mode bit in the NSR control register (Address 0x3C) to 0. In this mode, the useful frequency range can be set using the 6-bit tuning word in the NSR tuning words register (Address 0x3E). There are 57 possible tuning words (TW); each step is 0.5% of the ADC sample rate. The following three equations describe the left band edge (f_0), the channel center (f_{CENTER}), and the right band edge (f_1), respectively:

$$f_0 = f_{ADC} \times 0.005 \times TW$$

$$f_{CENTER} = f_0 + 0.11 \times f_{ADC}$$

$$f_1 = f_0 + 0.22 \times f_{ADC}$$

Figure 45 to Figure 47 show the typical spectrum that can be expected from the AD6677 in the 22% bandwidth mode for three different tuning words.

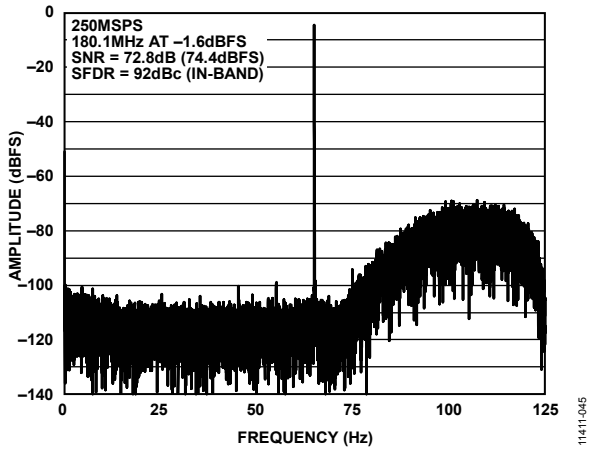

Figure 45. 22% Bandwidth Mode, Tuning Word = 13

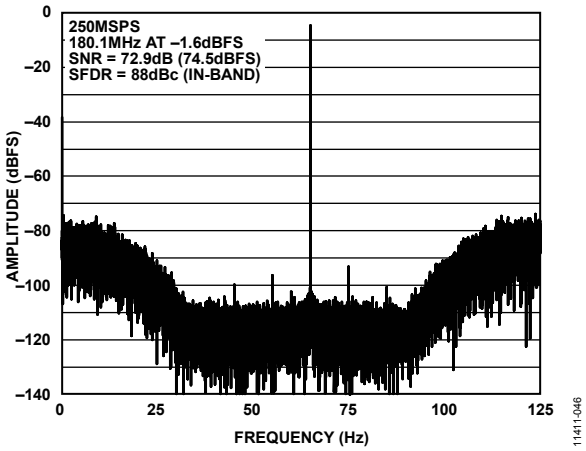

Figure 46. 22% Bandwidth Mode, Tuning Word = 28 (f_S/4 Tuning)

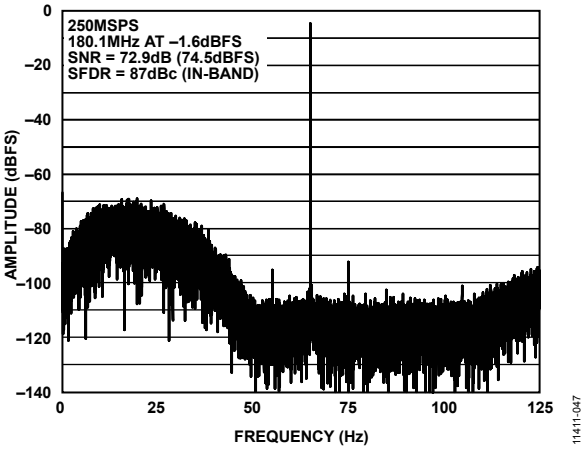

Figure 47. 22% Bandwidth Mode, Tuning Word = 41

33% BANDWIDTH MODE (>60 MHz AT 184.32 MSPS)

The second bandwidth mode offers excellent noise performance over 33% of the ADC sample rate (66% of the Nyquist band) and can be centered by setting the NSR mode bit in the NSR control register (Address 0x3C) to 1. In this mode, the useful frequency range can be set using the 6-bit tuning word in the NSR tuning register (Address 0x3E). There are 57 possible tuning words (TW); each step is 0.5% of the ADC sample rate. The following three equations describe the left band edge (f_0), the channel center (f_{CENTER}), and the right band edge (f_1), respectively:

$$f_0 = f_{ADC} \times .005 \times TW$$

$$f_{CENTER} = f_0 + 0.165 \times f_{ADC}$$

$$f_1 = f_0 + 0.33 \times f_{ADC}$$

Figure 48 to Figure 50 show the typical spectrum that can be expected from the AD6677 in the 33% bandwidth mode for three different tuning words.

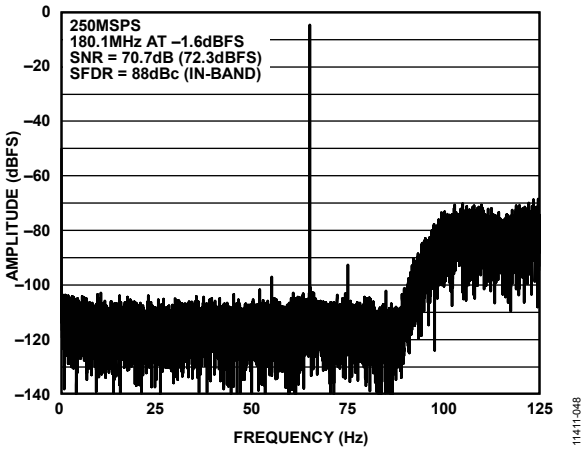

Figure 48. 33% Bandwidth Mode, Tuning Word = 5

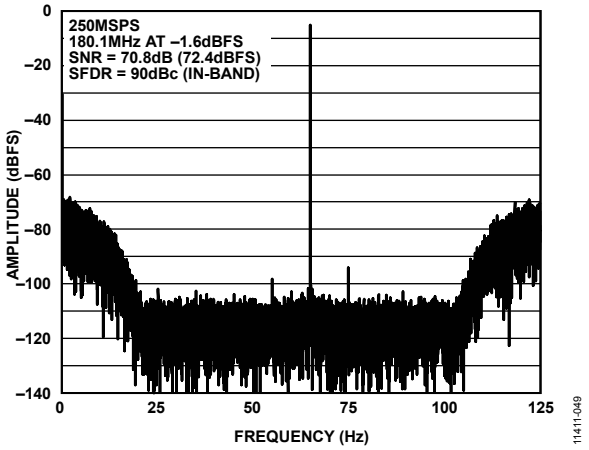

Figure 49. 33% Bandwidth Mode, Tuning Word = 17 (f_S/4 Tuning)

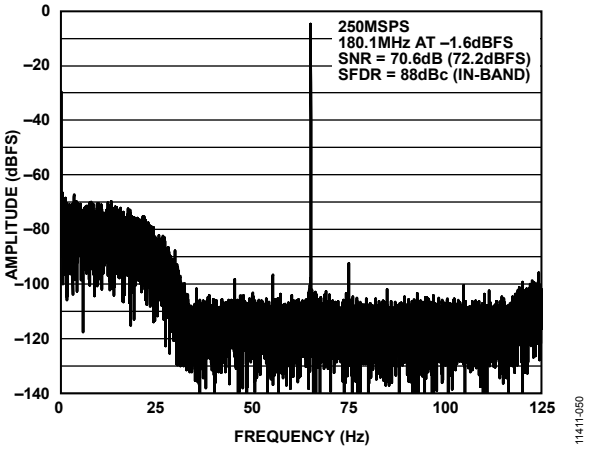

Figure 50. 33% Bandwidth Mode, Tuning Word = 27

DIGITAL OUTPUTS

JESD204B TRANSMIT TOP LEVEL DESCRIPTION

The AD6677 digital output uses the JEDEC Standard No. JESD204B, *Serial Interface for Data Converters*. JESD204B is a protocol to link the AD6677 to a digital processing device over a serial interface of up to 5 Gbps link speeds. The benefits of the JESD204B interface include a reduction in required board area for data interface routing and the enabling of smaller packages for converter and logic devices. The AD6677 supports single or dual lane interfaces.

JESD204B Overview

The JESD204B data transmit block assembles the parallel data from the ADC into frames and uses 8B/10B encoding as well as optional scrambling to form serial output data. Lane synchronization is supported using special characters during the initial establishment of the link and additional synchronization is embedded in the data stream thereafter. A matching external receiver is required to lock onto the serial data stream and recover the data and clock. For additional details on the JESD204B interface, refer to the JESD204B standard.

The AD6677 JESD204B transmit block maps the output of the ADC over a single link. The link is configured to use a single pair of serial differential outputs that is called a lane. The JESD204B specification refers to a number of parameters to define the link, and these parameters must match between the JESD204B transmitter (AD6677 output) and receiver.

The JESD204B link is described according to the following parameters:

- S = samples transmitted per single converter per frame cycle (AD6677 value = 1)
- M = number of converters per converter device (AD6677 value = 1)
- L = number of lanes per converter device (AD6677 value = 1)
- N = converter resolution (AD6677 value = 11)
- N' = total number of bits per sample (AD6677 value = 16)
- CF = number of control words per frame clock cycle per converter device (AD6677 value = 0)
- CS = number of control bits per conversion sample (configurable on the AD6677 up to 2 bits)
- K = number of frames per multiframe (configurable on the AD6677)
- HD = high density mode (AD6677 value = 0)
- F = octets/frame (AD6677 value = 2)
- C = control bit (overrange, overflow, underflow; available on the AD6677)
- T = tail bit (available on the AD6677)
- SCR = scrambler enable/disable (configurable on the AD6677)
- FCHK = checksum for the JESD204B parameters (automatically calculated and stored in register map)

Figure 51 shows a simplified block diagram of the AD6677 JESD204B link. The AD6677 is configured to use one converter and one lane. Converter data is output to SERDOUT0+/ SERDOUT0−. The AD6677 allows for other configurations such as combining the outputs of both converters onto a single lane or changing the mapping of the A and B digital output paths. These modes are set up through a quick configuration register in the register map, along with additional customizable options.

By default, in the AD6677, the 11-bit converter word is divided into two octets (8 bits of data). Bit 10 (MSB) through Bit 3 are in the first octet. The second octet contains Bit 2 through Bit 0 (LSB), followed by three bits that can be programmed as 0 or pseudo-random numbers with two tail bits added to fill the second octet. The tail bits can be configured as zeros, a pseudo-random number sequence, or control bits indicating overrange, underrange, or valid data conditions.

The two resulting octets can be scrambled. Scrambling is optional, however, it is available to avoid spectral peaks when transmitting similar digital data patterns. The scrambler uses a self synchronizing, polynomial-based algorithm defined by the $1 + x^{14} + x^{15}$ equation. The descrambler in the receiver must be a self synchronizing version of the scrambler polynomial.

The two octets are then encoded with an 8B/10B encoder. The 8B/10B encoder works by taking eight bits of data (an octet) and encoding them into a 10-bit symbol. Figure 52 shows how the 11-bit data is taken from the ADC, the tail bits are added, the two octets are scrambled, and how the octets are encoded into two 10-bit symbols. Figure 52 illustrates the default data format.

At the data link layer, in addition to the 8B/10B encoding, the character replacement allows the receiver to monitor frame alignment. The character replacement process occurs on the frame and multiframe boundaries. Implementation depends on which boundary is occurring and if scrambling is enabled.

If scrambling is disabled, the following applies:

- If the last scrambled octet of the last frame of the multiframe equals the last octet of the previous frame, the transmitter replaces the last octet with the control character /A/ = /K28.3/.
- On other frames within the multiframe, if the last octet in the frame equals the last octet of the previous frame, the transmitter replaces the last octet with the control character /F/ = /K28.7/.

If scrambling is enabled, the following applies:

- If the last octet of the last frame of the multiframe equals 0x7C, the transmitter replaces the last octet with the control character /A/ = /K28.3/.
- On other frames within the multiframe, if the last octet equals 0xFC, the transmitter replaces the last octet with the control character /F/ = /K28.7/.

Refer to JEDEC Standard, No. 204B, July 2011, for additional information about the JESD204B interface. Section 5.1 covers the transport layer and data format details, and Section 5.2 covers scrambling and descrambling.

JESD204B Synchronization Details

The AD6677 is a JESD204B Subclass 1 device that establishes synchronization of the link through two control signals, SYSREF and SYNC, and, typically, a common device clock. SYSREF and SYNC are common to all converter devices for alignment purposes at the system level.

The synchronization process is accomplished over three phases: code group synchronization (CGS), initial lane alignment sequence (ILAS), and data transmission. If scrambling is enabled, the bits are not actually scrambled until the data transmission phase, and the CGS phase and ILAS phase do not use scrambling.

CGS Phase

In the CGS phase, the JESD204B transmit block transmits /K28.5/ characters. The receiver (external logic device) must locate /K28.5/ characters in the input data stream using clock and data recovery (CDR) techniques.

When a certain number of consecutive /K28.5/ characters are detected on the link lane, the receiver initiates a SYSREF edge so that the AD6677 transmit data establishes a local multiframe clock (LMFC) internally.

The SYSREF edge also resets any sampling edges within the ADC to align sampling instances to the LMFC. This is important to maintain synchronization across multiple devices.

The receiver or logic device deasserts the sync signal (SYNCINB±), and the transmitter block begins the ILAS phase.

ILAS Phase

In the ILAS phase, the transmitter sends out a known pattern, and the receiver aligns the lanes in the link and verifies the parameters of the link.

The ILAS phase begins after SYNC has been deasserted (goes high). The transmit block begins to transmit four multiframes. Dummy samples are inserted between the required characters so that full multiframes are transmitted. The four multiframes include the following:

- Multiframe 1 begins with an /R/ character [K28.0] and ends with an /A/ character [K28.3].
- Multiframe 2 begins with an /R/ character followed by a /Q/ [K28.4] character, followed by link configuration parameters over 14 configuration octets (see Table 10), and ends with an /A/ character.
- Multiframe 3 is the same as Multiframe 1.
- Multiframe 4 is the same as Multiframe 1.

Data Transmission Phase

In the data transmission phase, frame alignment is monitored with control characters. Character replacement is used at the end of frames. Character replacement in the transmitter occurs in the following instances:

- If scrambling is disabled and the last octet of the frame or multiframe equals the octet value of the previous frame
- If scrambling is enabled and the last octet of the multiframe is equal to 0x7C, or the last octet of a frame is equal to 0xFC

Table 10. Fourteen Configuration Octets of the ILAS Phase

No.	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	DID[7:0]							
1					BID[3:0]			
2				LID[4:0]				
3	SCR			L[4:0]				
4	F[7:0]							
5				K[4:0]				
6	M[7:0]							
7	CS[1:0]			N[4:0]				
8	Subclass[2:0]			N'[4:0]				
9	JESDV[2:0]			S[4:0]				
10				CF[4:0]				
11	Reserved, don't care							
12	Reserved, don't care							
13	FCHK[7:0]							

Link Setup Parameters

The following sections demonstrate how to configure the AD6677 JESD204B interface. The steps to configure the output include the following:

1. Disable the lane before changing the configuration.
2. Select a quick configuration option.
3. Configure detailed options.
4. Check FCHK, the checksum of the JESD204B interface parameters.
5. Set additional digital output configuration options.
6. Reenable the lane.

Disable Lane Before Changing Configuration

Before modifying the JESD204B link parameters, disable the link and hold it in reset. This is accomplished by writing Logic 1 to Address 0x5F, Bit 0.

Configure Detailed Options

Configure the tail bits and control bits as follows.

- With N' = 16 and N = 11, there are two bits available per sample for transmitting additional information over the JESD204B link. The options are tail bits or control bits. By default, tail bits of 0b00 value are used.
- Tail bits are dummy bits sent over the link to complete the two octets and do not convey any information about the input signal. Tail bits can be fixed zeros (default) or pseudo-random numbers (Address 0x5F, Bit 6).
- One or two control bits can be used instead of the tail bits using Address 0x72, Bits[7:6]. The tail bits can be set using Address 0x14, Bits[7:5], and the tail bits are enabed using Address 0x5F, Bit 6.

Set the lane identification values.

- JESD204B allows parameters to identify the device and lane. These parameters are transmitted during the ILAS phase, and they are accessible in the internal registers.
- There are three identification values: device identification (DID), bank identification (BID), and lane identification (LID). DID and BID are device specific; therefore, they can be used for link identification.

Set the number of frames per multiframe, K.

- Per the JESD204B specification, a multiframe is defined as a group of K successive frames, where K is between 1 and 32, and it requires that the number of octets be between 17 and 1024. The K value is set to 32 by default in Address 0x70, Bits[7:0]. Note that the K value is the register value plus 1.
- The K value can be changed; however, it must comply with a few conditions. The AD6677 uses a fixed value for octets per frame (F) based on the JESD204B quick configuration setting. K must also be a multiple of 4 and conform to the following equation:

$$32 \geq K \geq Ceil\ (17/F)$$

- The JESD204B specification also requires the number of octets per multiframe (K × F) to be between 17 and 1024. The F value is fixed through the quick configuration setting to ensure that this relationship is true.

Table 11. JESD204B Configurable Identification Values

ID Value	Register, Bits	Value Range
LID	0x67, [4:0]	0 to 31
DID	0x64, [7:0]	0 to 255
BID	0x65, [3:0]	0 to 15

Scramble, SCR.

- Scrambling can be enabled or disabled by setting Address 0x6E, Bit 7. By default, scrambling is enabled. Per the JESD204B protocol, scrambling is functional only after the lane synchronization has completed.

Select lane synchronization options.

Most of the synchronization features of the JESD204B interface are enabled by default for typical applications. In some cases, these features can be disabled or modified as follows:

- ILAS enabling is controlled in Address 0x5F, Bits[3:2] and, by default, is enabled. Optionally, to support some unique instances of the interfaces (such as NMCDA-SL), the JESD204B interface can be programmed to either disable the ILAS sequence or continually repeat the ILAS sequence.

The AD6677 has fixed values of some of the JESD204B interface parameters, and they are as follows:

- N = 11, number of bits per converter is 11 in Address 0x72, Bits[3:0]
- N' = 16, number of bits per sample is 16 in Address 0x73, Bits[3:0]
- CF = 0, number of control words per frame clock cycle per converter is 0 in Address 0x75, Bits[4:0]

Verify read only values: lanes per link (L), octets per frame (F), number of converters (M), and samples per converter per frame (S). The AD6677 calculates values for some JESD204B parameters based on other settings, particularly the quick configuration register selection. The read only values here are available in the register map for verification.

- L = lanes per link is 1; read the values from Address 0x6E, Bits[4:0]
- F = octets per frame can be 1, 2, or 4; read the value from Address 0x6F, Bits[7:0]
- HD = high density mode can be 0 or 1; read the value from Address 0x75, Bit 7
- M = number of converters per link can be 1 or 2; read the value from Address 0x71, Bits[7:0]
- S = samples per converter per frame can be 1 or 2; read the value from Address 0x74, Bits[4:0]

Check FCHK, Checksum of JESD204B Interface Parameters

The JESD204B parameters can be verified through the checksum value (FCHK) of the JESD204B interface parameters. Each lane has a FCHK value associated with it. The FCHK value is transmitted during the ILAS second multiframe and can be read from the internal registers.

The checksum value is the modulo 256 sum of the parameters listed in the No. column of Table 12. The checksum is calculated by adding the parameter fields before they are packed into the octets shown in Table 12.

The FCHK value for the lane configuration for data coming out of Lane 0 can be read from Address 0x79.

Table 12. JESD204B Configuration Table Used in ILAS and CHKSUM Calculation

No.	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	DID[7:0]							
1					BID[3:0]			
2				LID[4:0]				
3	SCR			L[4:0]				
4	F[7:0]							
5				K[4:0]				
6	M[7:0]							
7	CS[1:0]			N[4:0]				
8	Subclass[2:0]			N′[4:0]				
9	JESDV[2:0]			S[4:0]				
10				CF[4:0]				

Set Additional Digital Output Configuration Options

Other data format controls include the following:

- Invert polarity of serial output data, Address 0x60, Bit 1
- ADC data format select (offset binary or twos complement), Address 0x14, Bits[1:0]
- Options for interpreting signal on SYNCINB± and SYSREF±, Address 0x3A, Bits[4:0]

Reenable Lane After Configuration

After modifying the JESD204B link parameters, enable the link so that the synchronization process can begin. This is accomplished by writing Logic 0 to Address 0x5F, Bit 0.

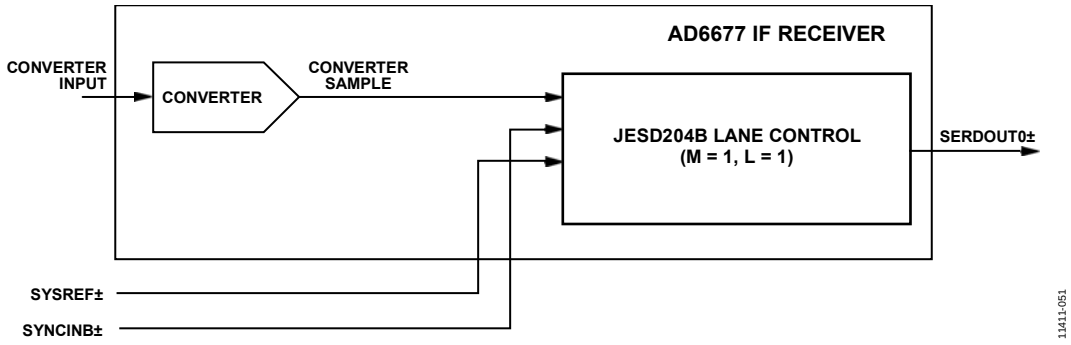

Figure 51. Transmit Link Simplified Block Diagram

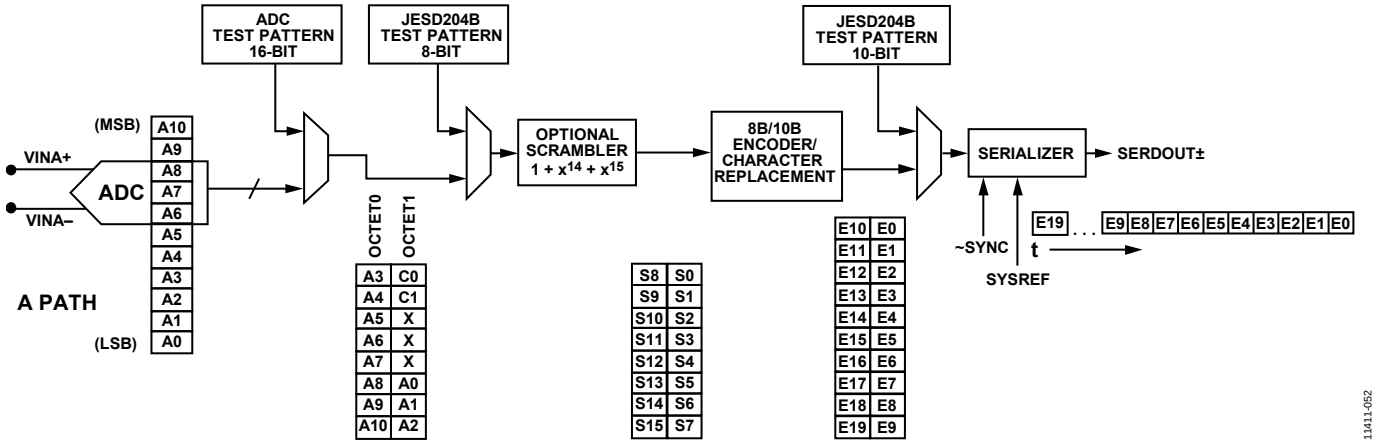

Figure 52. Digital Processing of JESD204B Lane The Octet 0/1

Table 13. JESD204B Typical Configurations

JESD204B Configure Setting	M (No. of Converters), Address 0x71, Bits[7:0]	L (No. of Lanes), Address 0x6E, Bits[4:0]	F (Octets/Frame), Address 0x6F, Bits[7:0], Read Only	S (Samples/ADC/Frame), Address 0x74, Bits[4:0], Read Only	HD (High Density Mode), Address 0x75, Bit 7, Read Only
0x11 (Default)	1	1	2	1	0

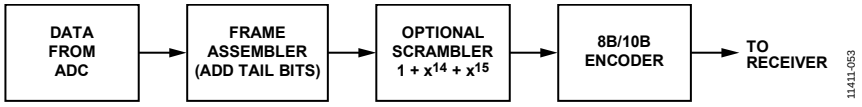

Figure 53. ADC Output Data Path

Table 14. JESD204B Frame Alignment Monitoring and Correction Replacement Characters

Scrambling	Lane Synchronization	Character to be Replaced	Last Octet in Multiframe	Replacement Character
Off	On	Last octet in frame repeated from previous frame	No	K28.7
Off	On	Last octet in frame repeated from previous frame	Yes	K28.3
Off	Off	Last octet in frame repeated from previous frame	Not applicable	K28.7
On	On	Last octet in frame equals D28.7	No	K28.7
On	On	Last octet in frame equals D28.3	Yes	K28.3
On	Off	Last octet in frame equals D28.7	Not applicable	K28.7

Frame and Lane Alignment Monitoring and Correction

Frame alignment monitoring and correction is part of the JESD204B specification. The 11-bit word requires two octets to transmit all the data. The two octets (MSB and LSB), where F = 2, make up a frame. During normal operating conditions, frame alignment is monitored via alignment characters, which are inserted under certain conditions at the end of a frame. Table 14 summarizes the conditions for character insertion along with the expected characters under the various operation modes. If lane synchronization is enabled, the replacement character value depends on whether the octet is at the end of a frame or at the end of a multiframe.

Based on the operating mode, the receiver can ensure that it is still synchronized to the frame boundary by correctly receiving the replacement characters.

Digital Outputs and Timing

The AD6677 has differential digital outputs that power up by default. The driver current is derived on chip and sets the output current at each output equal to a nominal 3 mA. Each output presents a 100 Ω dynamic internal termination to reduce unwanted reflections.

Place a 100 Ω differential termination resistor at each receiver input to result in a nominal 600 mV p-p swing at the receiver (see Figure 54). Alternatively, single-ended 50 Ω termination can be used. When single-ended termination is used, the termination voltage must be DRVDD/2; otherwise, ac coupling capacitors can be used to terminate to any single-ended voltage.

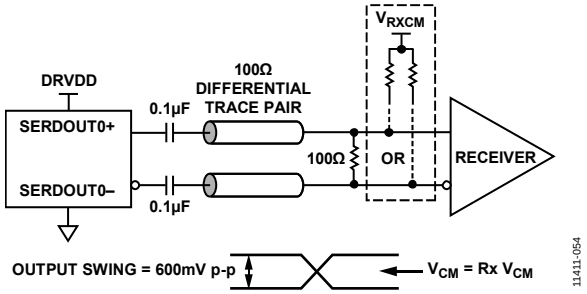

Figure 54. AC-Coupled Digital Output Termination Example

The AD6677 digital outputs can interface with custom ASICs and FPGA receivers, providing superior switching performance in noisy environments.

Single point-to-point network topologies are recommended with a single differential 100 Ω termination resistor placed as close to the receiver logic as possible. The common mode of the digital output automatically biases itself to half the supply of the AD6677 (that is, the common-mode voltage is 0.9 V for a supply of 1.8 V) if a dc-coupled connection is used (see Figure 55). For a receiver logic that is not within the bounds of the DRVDD supply, use an ac-coupled connection. Simply place a 0.1 µF capacitor on each output pin and derive a 100 Ω differential termination close to the receiver side.

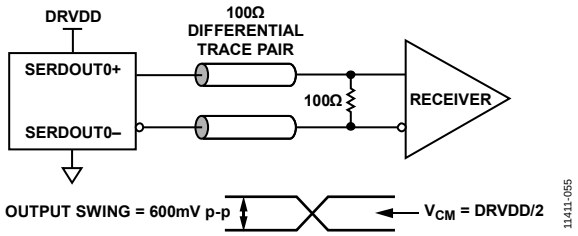

Figure 55. DC-Coupled Digital Output Termination Example

If there is no far-end receiver termination, or if there is poor differential trace routing, timing errors may result. To avoid such timing errors, it is recommended that the trace length be less than 6 inches, and that the differential output traces be close together and at equal lengths.

Figure 56 shows an example of the digital output (default) data eye and time interval error (TIE) jitter histogram and bathtub curve for the AD6677 lane running at 5 Gbps.

Additional SPI options allow the user to further increase the output driver voltage swing or enable preemphasis to drive longer trace lengths (see Address 0x15 in Table 17). The power dissipation of the DRVDD supply increases when this option is used. See the Memory Map section for more details.

The format of the output data is twos complement by default. To change the output data format to offset binary, see the Memory Map section (Address 0x14 in Table 17).

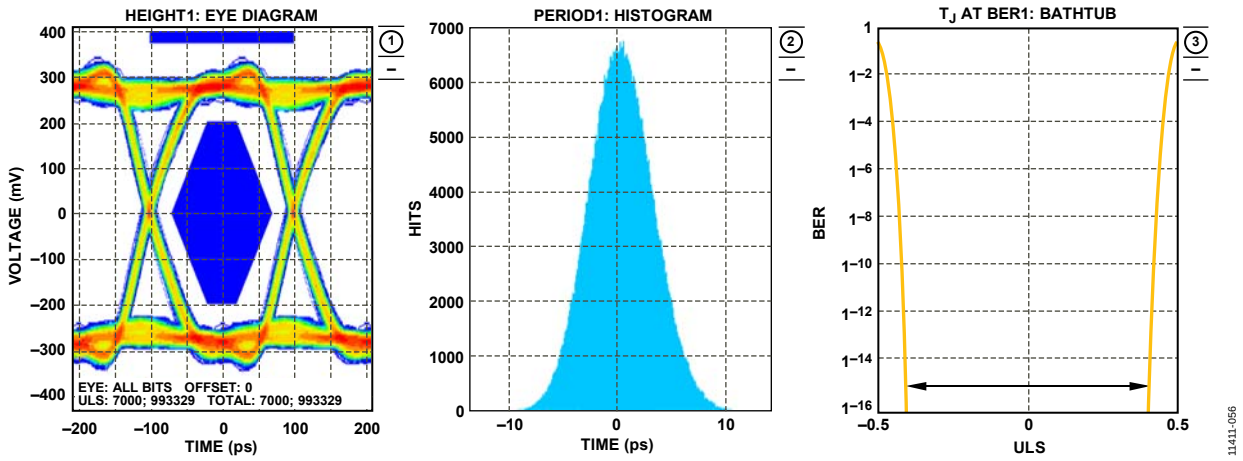

Figure 56. AD6677 Digital Outputs Data Eye, Histogram, and Bathtub, External 100 Ω Terminations at 5 Gbps

ADC OVERRANGE AND GAIN CONTROL

In receiver applications, it is desirable to have a mechanism to reliably determine when the converter is about to be clipped. The standard overflow indicator provides delayed information on the state of the analog input that is of limited value in preventing clipping. Therefore, it is helpful to have a programmable threshold below full scale that allows time to reduce the gain before the clip occurs. In addition, because input signals can have significant slew rates, latency of this function is of concern.

Using the SPI port, the user can provide a threshold above which the FD output is active. Bit 0 of Address 0x45 enables the fast detect feature. Address 0x47 to Address 0x4A allow the user to set the threshold levels. As long as the signal is below the selected threshold, the FD output remains low. In this mode, the magnitude of the data is considered in the calculation of the condition, but the sign of the data is not considered. The threshold detection responds identically to positive and negative signals outside the desired range (magnitude).

ADC Overrange (OR)

The ADC overrange indicator is asserted when an overrange is detected on the input of the ADC. The overrange condition is determined at the output of the ADC pipeline and, therefore, is subject to a latency of 36 ADC clock cycles. An overrange at the input is indicated by this bit 36 clock cycles after it occurs.

Gain Switching

The AD6677 includes circuitry that is useful in applications either where large dynamic ranges exist, or where gain ranging amplifiers are employed. This circuitry allows digital thresholds to be set such that an upper threshold and a lower threshold can be programmed.

One such use is to detect when an ADC is about to reach full scale with a particular input condition. The result is to provide an indicator that can be used to quickly insert an attenuator that prevents ADC overdrive.

Fast Threshold Detection (FD)

The FD indicator is asserted if the input magnitude exceeds the value programmed in the fast detect upper threshold registers, located in Address 0x47 and Address 0x48. The selected threshold register is compared with the signal magnitude at the output of the ADC. The fast upper threshold detection has a latency of four clock cycles. The approximate upper threshold magnitude is defined by

$$\textit{Upper Threshold Magnitude}\ (\text{dBFS}) = 20 \log (\textit{Threshold Magnitude}/2^{13})$$

The FD indicators are not cleared until the signal drops below the lower threshold for the programmed dwell time. The lower threshold is programmed in the fast detect lower threshold registers, located at Address 0x49 and Address 0x4A. The fast detect lower threshold register is a 16-bit register that is compared with the signal magnitude at the output of the ADC. This comparison is subject to the ADC pipeline latency but is accurate in terms of converter resolution. The lower threshold magnitude is defined by

$$\textit{Lower Threshold Magnitude}\ (\text{dBFS}) = 20 \log (\textit{Threshold Magnitude}/2^{13})$$

For example, to set an upper threshold of −6 dBFS, write 0x0FFF to those registers, and to set a lower threshold of −10 dBFS, write 0x0A1D to those registers.

The dwell time can be programmed from 1 to 65,535 sample clock cycles by placing the desired value in the fast detect dwell time registers, located in Address 0x4B and Address 0x4C.

The operation of the upper threshold and lower threshold registers, along with the dwell time registers, is shown in Figure 57.

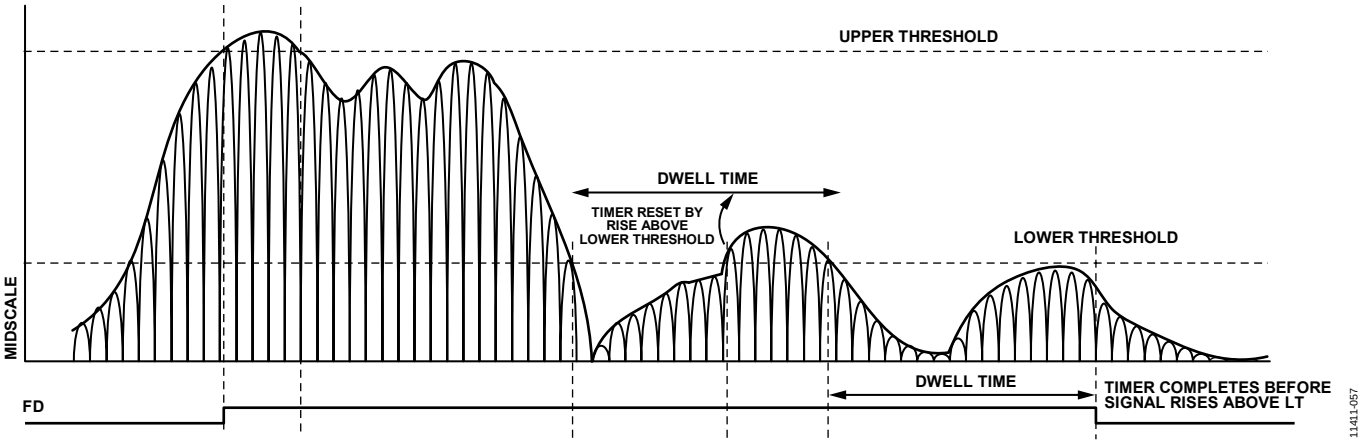

Figure 57. Threshold Settings for FD Signals

DC CORRECTION (DCC)

Because the dc offset of the ADC may be significantly larger than the signal being measured, a dc correction circuit is included to null the dc offset before measuring the power. The dc correction circuit can also be switched into the main signal path; however, this may not be appropriate if the ADC is digitizing a time-varying signal with significant dc content, such as GSM.

DC CORRECTION BANDWIDTH

The dc correction circuit is a high-pass filter with a programmable bandwidth (ranging between 0.29 Hz and 2.387 kHz at 245.76 MSPS). The bandwidth is controlled by writing to the four dc correction bandwidth select bits, located at Address 0x40, Bits[5:2]. The following equation can be used to compute the bandwidth value for the dc correction circuit:

$$DC_Corr_BW = 2^{-k-14} \times f_{CLK}/(2 \times \pi)$$

where:
k is the 4-bit value programmed in Bits[5:2] of Address 0x40 (values between 0 and 13 are valid for k).
f_{CLK} is the AD6677 ADC sample rate in hertz.

DC CORRECTION READBACK

The current dc correction value can be read back in Address 0x41 and Address 0x42. The dc correction value is a 16-bit value that can span the entire input range of the ADC.

DC CORRECTION FREEZE

Setting Bit 6 of Address 0x40 freezes the dc correction at the current state and continues to use the last updated value as the dc correction value. Clearing this bit restarts dc correction and adds the currently calculated value to the data.

DC CORRECTION ENABLE BITS

Setting Bit 1 of Address 0x40 enables dc correction for use in the output data signal path.

SERIAL PORT INTERFACE (SPI)

The AD6677 SPI allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section. For detailed operational information, see the Application Note AN-877, *Interfacing to High Speed ADCs via SPI*.

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK pin, the SDIO pin, and the $\overline{CS}$ pin (see Table 15). The SCLK (serial clock) pin is used to synchronize the read and write data presented from/to the ADC. The SDIO (serial data input/output) pin is a dual-purpose pin that allows data to be sent to and read from the internal ADC memory map registers. The $\overline{CS}$ (chip select bar) pin is an active low control that enables or disables the read and write cycles.

Table 15. Serial Port Interface Pins

Pin	Function
SCLK	Serial clock. The serial shift clock input, which is used to synchronize the serial interface reads and writes.
SDIO	Serial data input/output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
$\overline{CS}$	Chip select bar. An active low control that gates the read and write cycles.

The falling edge of $\overline{CS}$, in conjunction with the rising edge of SCLK, determines the start of the framing. An example of the serial timing and definitions can be found in Figure 58 and Table 5.

Other modes involving $\overline{CS}$ are available. $\overline{CS}$ can be held low indefinitely, which permanently enables the device; this is called streaming. $\overline{CS}$ can stall high between bytes to allow for additional external timing. When $\overline{CS}$ is tied high, SPI functions are placed in a high impedance mode. This mode turns on any SPI pin secondary functions.

During an instruction phase, a 16-bit instruction is transmitted. Data follows the instruction phase, and the length is determined by the W0 and the W1 bits.

All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued. This allows the SDIO pin to change direction from an input to an output.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to both program the chip and read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDIO pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or in LSB first mode. MSB first is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the Application Note AN-877, *Interfacing to High Speed ADCs via SPI*.

HARDWARE INTERFACE

The pins described in Table 15 comprise the physical interface between the user programming device and the serial port of the AD6677. The SCLK pin and the $\overline{CS}$ pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the Application Note AN-812, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

Do not activate the SPI port during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the $\overline{CS}$ signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD6677 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

SPI ACCESSIBLE FEATURES

Table 16 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the Application Note AN-877, *Interfacing to High Speed ADCs via SPI*. The AD6677 device-specific features are described in the Memory Map Register Descriptions section.

Table 16. Features Accessible Using the SPI

Feature Name	Description
Mode	Allows the user to set either power-down mode or standby mode
Clock	Allows the user to access the DCS via the SPI
Offset	Allows the user to digitally adjust the converter offset
Test Input/Output	Allows the user to set test modes to have known data on output bits
Output Mode	Allows the user to set up outputs
Output Phase	Allows the user to set the output clock polarity
Output Delay	Allows the user to vary the DCO delay
VREF	Allows the user to set the reference voltage

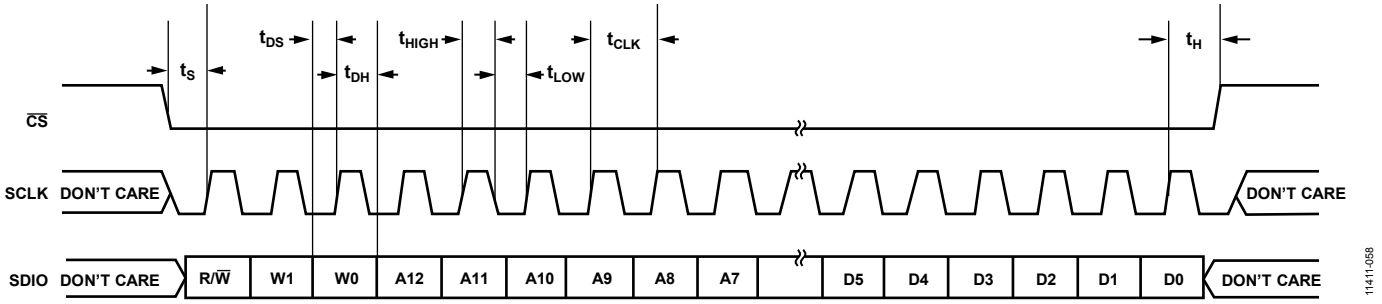

Figure 58. Serial Port Interface Timing Diagram

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is roughly divided into three sections: the chip configuration registers (Address 0x00 to Address 0x02); the ADC functions registers, including setup, control, and test (Address 0x08 to Address 0xA8); and the transfer register (Address 0xFF).

The memory map register table (see Table 17) documents the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For example, Address 0x14, the output mode register, has a hexadecimal default value of 0x01. This means that Bit 0 = 1 and the remaining bits are 0s. This setting is the default output format value, which is twos complement. For more information on this function and others, see the Application Note AN-877, *Interfacing to High Speed ADCs via SPI*. This application note details the functions controlled by Address 0x00 to Address 0x21 and Address 0xFF, with the exception of Address 0x08 and Address 0x14. The remaining registers, Address 0x08, Address 0x14, and Address 0x3A through Address 0xA8, are documented in the Memory Map Register Descriptions section.

Open and Reserved Locations

All address and bit locations that are not included in Table 17 are not currently supported for this device. Unused bits of a valid address location must be written with 0s. Writing to these locations is required only when part of an address location is open (for example, Address 0x18). If the entire address location is open (for example, Address 0x13), do not write to this address location.

Default Values

After the AD6677 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table (see Table 17).

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

Transfer Register Map

Address 0x09, Address 0x0B, Address 0x0D, Address 0x10, Address 0x14, Address 0x18, Address 0x21, and Address 0x3A to Address 0x4C are shadowed. Writes to these addresses do not affect device operation until a transfer command is issued by writing 0x01 to Address 0xFF, setting the transfer bit. This allows these registers to be updated internally and simultaneously when the transfer bit is set. The internal update takes place when the transfer bit is set, and then the bit autoclears.

MEMORY MAP REGISTER TABLE

All address and bit locations that are not included in Table 17 are not currently supported for this device.

Table 17. Memory Map Registers

Reg Addr (Hex)	Reg Addr Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x00	SPI port configuration	0	LSB first	Soft reset	1	1	Soft reset	LSB first	0	0x18	
0x01	Chip ID	AD6677 8-bit Chip ID is 0xC4								0xC4	Read only
0x02	Chip grade			Speed grade: 00 = 250 MSPS			Reserved for chip die revision currently 0x0			0x00	
0x08	PDWN modes			External PDWN mode: 0 = PDWN is full power-down, 1 = PDWN puts device in standby	JESD204B standby mode (when external PDWN is used): 0 = JESD204B core is unaffected, 1 = JESD204B core is powered down except for PLL	JESD204B power modes: 00 = normal mode (power-up); 01 = power-down mode, PLL off, serializer off, clocks stopped, digital held in reset; 10 = standby mode: PLL on, serializer off, clocks stopped, digital circuitry held in reset		ADC power modes: 00 = normal mode (power-up), 01 = power-down mode, 10 = standby mode, does not affect JESD204B digital circuitry		0x00	
0x09	Global clock	Reserved		Clock selection: 00 = Nyquist clock, 01 = RF clock divide by 2, 10 = RF clock divide by 4, 11 = clock off					Clock duty cycle stabilizer enable	0x01	DCS enabled if clock divider enabled
0x0A	PLL status	PLL locked status							JESD204B link is ready		Read only
0x0B	Clock divider			Clock divide phase relative to the encode clock: 0x0 = 0 input clock cycles delayed, 0x1 = 1 input clock cycles delayed, 0x2 = 2 input clock cycles delayed, … 0x7 = 7 input clock cycles delayed			Clock divider ratio relative to the encode clock: 0x00 = divide by 1, 0x01 = divide by 2, 0x02 = divide by 3, … 0x07 = divide by 8			0x00	Clock divide values other than 0x00 automatically cause the DCS to become active
0x0D	Test mode	User test mode cycle: 00 = repeat pattern (user pattern 1, 2, 3, 4, 1, 2, 3, 4, 1, …); 10 = single pattern (user pattern 1, 2, 3, 4, then all zeros)		Long pseudo-random number generator reset: 0 = long PRN enabled, 1 = long PRN held in reset	Short pseudo-random number generator reset: 0 = short PRN enabled, 1 = short PRN held in reset	Data output test generation mode: 0000 = off (normal mode), 0001 = midscale short, 0010 = positive full scale, 0011 = negative full scale, 0100 = alternating checkerboard, 0101 = PN sequence long, 0110 = PN sequence short, 0111 = 1/0 word toggle, 1000 = user test mode (use with Address 0x0D, Bits[7:6] and user pattern 1, 2, 3, 4), 1001 to 1110 = unused, 1111 = ramp output				0x00	
0x10	Customer offset			Offset adjust in LSBs from +31 to −32 (twos complement format): 01 1111 = adjust output by +31, 01 1110 = adjust output by +30, … 00 0001 = adjust output by +1, 00 0000 = adjust output by 0 (default), … 10 0001 = adjust output by −31, 10 0000 = adjust output by −32						0x00	
0x14	Output mode	JESD204B CS bits assignment (in conjunction with Address 0x72): 000 = {overrange||underrange, valid}, 001 = {overrange, underrange}, 010 = {overrange||underrange, blank}, 011 = {blank, valid}, 100 = {blank, blank}, 101 = {underrange, overrange}, 110 = {valid, overange||underrange}, 111 = {valid, blank}			ADC output disable		ADC data invert: 0 = normal (default), 1 = inverted	Data format select (DFS): 00 = offset binary, 01 = twos complement		0x01	

Reg Addr (Hex)	Reg Addr Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x15	CML output adjust						JESD204B CML differential output drive level adjustment: 000 = 75% of nominal (438 mV p-p), 001 = 83% of nominal (488 mV p-p), 010 = 91% of nominal (538 mV p-p), 011 = nominal (default) (588 mV p-p), 100 = 109% of nominal (638 mV p-p), 101 = 117% of nominal (690 mV p-p), 110 = 126% of nominal (740 mV p-p), 111 = 134% of nominal (790 mV p-p)			0x03	
0x18	Input span select				Main reference full-scale VREF adjustment: 0 1111 = internal 2.087 V p-p, ... 0 0001 = internal 1.772 V p-p, 0 0000 = internal 1.75 V p-p (default), 1 1111 = internal 1.727 V p-p, … 1 0000 = internal 1.383 V p-p					0x00	
0x19	User Test Pattern 1 LSB	User Test Pattern 1 LSB; use in conjunction with Address 0x0D and Address 0x61									
0x1A	User Test Pattern 1 MSB	User Test Pattern 1 MSB									
0x1B	User Test Pattern 2 LSB	User Test Pattern 2 LSB									
0x1C	User Test Pattern 2 MSB	User Test Pattern 2 MSB									
0x1D	User Test Pattern 3 LSB	User Test Pattern 3 LSB									
0x1E	User Test Pattern 3 MSB	User Test Pattern 3 MSB									
0x1F	User Test Pattern 4 LSB	User Test Pattern 4 LSB									
0x20	User Test Pattern 4 MSB	User Test Pattern 4 MSB									
0x21	PLL low encode				00 = for lane speeds of >2 Gbps, 01 = for lane speeds of <2 Gbps					0x00	
0x3A	SYNCINB±/ SYSREF± control				JESD204B realign SYNCINB±: 0 = normal mode, 1 = realigns lane on every active SYNCINB±	JESD204B realign SYSREF±: 0 = normal mode, 1 = realigns lane on every active SYSREF±	SYSREF± mode: 0 = continuous reset clock dividers, 1 = sync on next SYSREF± rising edge only	SYSREF± enable: 0 = disabled, 1 = enabled Note: This bit self-clears after SYSREF if SYSREF± mode = 1	Enable internal SYSREF± buffer; 0 = buffer disabled, external SYSREF± pin ignored; 1 = buffer enabled, use external SYSREF± pin	0x00	
0x3C	NSR control							Bandwidth mode (NSR): 0 = 22%, 1 = 33%	NSR enable	0x00	
0x3E	NSR tuning word			Noise shaped requantizer tuning word; selects the center frequency of the noise transfer function (NTF); 57 possible tuning words (TW) exist for 22% mode and 34 possible tuning words (TW) exist for 33% mode; each step is 0.5% of the ADC sample rate						0x1C	

Reg Addr (Hex)	Reg Addr Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x40	DC correction control		Freeze dc correction: 0 = calculate, 1 = freeze value	DC correction bandwidth select; correction bandwidth is 2387.32 Hz/reg value; there are 14 possible values: 0000 = 2387.32 Hz, 0001 = 1193.66 Hz, 0010 = 596.83 Hz, 0011 = 298.42 Hz, 0100 = 149.21 Hz, 0101 = 74.60 Hz, 0110 = 37.30 Hz, 0111 = 18.65 Hz, 1000 = 9.33 Hz, 1001 = 4.66 Hz, 1010 = 2.33 Hz, 1011 = 1.17 Hz, 1100 = 0.58 Hz, 1101 = 0.29 Hz, 1110 = reserved, 1111 = reserved			Enable dc correction		0x00	
0x41	DC Correction Value 0	DC correction value LSB[7:0]								0x00	
0x42	DC Correction Value 1	DC correction value MSB[15:8]								0x00	
0x45	Fast detect control				FD pin function: 0 = fast detect, 1 = overrange	Force FD output enable: 0 = normal function, 1 = force to value	Forced FD output value; if force FD pin is true, this value is output on the FD pin		Enable fast detect output		
0x47	Fast detect upper threshold	Fast detect upper threshold[7:0]									
0x48			Fast detect upper threshold[14:8]								
0x49	Fast detect lower threshold	Fast detect lower threshold[7:0]									
0x4A			Fast detect lower threshold[14:8]								
0x4B	Fast detect dwell time	Fast detect dwell time[7:0]									
0x4C		Fast detect dwell time[15:8]									
0x5E	JESD204B quick config	JESD204B quick configuration, always reads back 0x00; 0x11 = M =1, L = 1; one converter, one lane								0x00	Always reads back 0x00
0x5F	JESD204B Link Control 1		Serial tail bit enable: 0 = extra bits are 0, 1 = extra bits are 9-bit PN	JESD204B test sample enable	Reserved; set to 1	ILAS mode: 01 = ILAS normal mode enabled, 11 = ILAS always on, test mode		Reserved; set to 1	JESD204B link power-down; set high while configuring link parameters	0x16	
0x60	JESD204B Link Control 2	Reserved; set to 0	Reserved; set to 0	Reserved; set to 0	SYNCINB± logic type: 0 = LVDS (differential), 1 = CMOS (single-ended)		Reserved; set to 0	Invert transmit bits	Reserved; set to 0	0x00	
0x61	JESD204B Link Control 3	Reserved; set to 0	Reserved; set to 0	Test data injection point: 01 = 10-bit data at 8B/10B output, 10 = 8-bit data at scrambler input		JESD204B test mode patterns: 0000 = normal operation (test mode disabled), 0001 = alternating checkerboard, 0010 = 1/0 word toggle, 0011 = PN Sequence PN23, 0100 = PN Sequence PN9, 0101= continuous/repeat user test mode, 0110 = single user test mode, 0111 = reserved, 1100 = PN Sequence PN7, 1101 = PN Sequence PN15, other setting are unused				0x00	
0x64	JESD204B DID config	JESD204B DID value									

Reg Addr (Hex)	Reg Addr Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x65	JESD204B BID config					JESD204B BID value					
0x67	JESD204B LID config				JESD204B LID value						
0x6E	JESD204B scrambler (SCR) and lane (L) configuration	JESD204B scrambling (SCR): 0 = disabled, 1 = enabled			JESD204B number of lanes (L); 0 = one lane per link (L = 1)					0x80	
0x6F	JESD204B parameter, F	JESD204B number of octets per frame (F); calculated value; read only [Note that this value is in x – 1 format]								0x01	Read only
0x70	JESD204B parameter, K	JESD204B number of frames per multiframe (K); set value of K per JESD204B specifications, but must also be a multiple of four octets [Note that this value is in x – 1 format]								0x1F	
0x71	JESD204B parameter, M	JESD204B number of converters (M); 0 = 1 converter								0x00	
0x72	JESD204B parameters, N/CS	Number of control bits (CS): 00 = no control bits (CS = 0), 01 = 1 control bit (CS = 1), 10 = 2 control bits (CS = 2)				ADC converter resolution (N), 0xA = 11-bit converter (N = 11) [Note that this value is in x – 1 format]				0x0D	
0x73	JESD204B parameter, subclass/N'		JESD204B subclass: 00 = Subclass 0, 01 = Subclass 1 (default)			JESD204B N' value; 0xF = N' = 16 [Note that this value is in x – 1 format]				0x2F	
0x74	JESD204B parameter, S			Reserved; set to 1	JESD204B samples per converter per frame cycle (S); read only [Note that this value is in x – 1 format]					0x20	
0x75	JESD204B parameters, HD and CF	JESD204B HD value; read only			JESD204B control words per frame clock cycle per link (CF); read only [Note that this value is in x – 1 format]					0x00	Read only
0x76	JESD204B RESV1	JESD204B Reserved Field 1									
0x77	JESD204B RESV2	JESD204B Reserved Field 2									
0x79	JESD204B CHKSUM	JESD204B checksum value for the output lane									
0x80	JESD204B output driver control								JESD204B driver power-down: 0 = enabled, 1 = powered down	0x00	
0x8B	JESD204B LMFC offset				Local multiframe clock (LMFC) phase offset value; reset value for LMFC phase counter when SYSREF± is asserted; used for deterministic delay applications					0x00	
0xA8	JESD204B preemphasis	JESD204B preemphasis enable option (consult factory for more details); set value to 0x04 for preemphasis off, and set value to 0x14 for preemphasis on								0x04	Typically not required
0xFF	Device update (global)								Transfer settings		

MEMORY MAP REGISTER DESCRIPTIONS

For more information on functions controlled in Address 0x00 to Address 0x21 and Address 0xFF, with the exception of Address 0x08 and Address 0x14, see the Application Note AN-877, *Interfacing to High Speed ADCs via SPI*.

PDWN Modes (Address 0x08)

Bits[7:6]—Reserved

Bit 5—External PDWN mode

This bit controls the function of the PDWN pin. When this bit is 0, asserting the PDWN pin results in a full power-down of the device. When this bit is 1, asserting the PDWN pin places the device in standby.

Bit 4—JESD204B standby mode

This bit controls the state of the JESD204B digital circuitry when the external PDWN pin places the device into standby. If this bit is 0, the JES204B digital circuitry is not placed into standby. When this bit is 1, the JESD204B circuitry is placed into standby when the PDWN pin is asserted and Bit 5 is 1.

Bits[3:2]—JESD204B power modes

These bits control the power modes of the JESD204B digital circuitry. When Bits[3:2] = 00, the JESD204B digital circuitry is in normal mode. When Bits[3:2] = 01, the JESD204B digital circuitry is in power-down mode with the PLL off, serializer off, clocks stopped, and the digital circuitry held in reset. When Bits[3:2] = 10, the JESD204B digital circuitry is placed into standby mode with the PLL on, serializer off, clocks stopped, and the digital circuitry held in reset.

Bits[1:0]—ADC power modes

These bits select power mode for the ADC excluding the JESD204B digital circuitry. When Bits[1:0] = 00, the ADC is in normal mode. When Bits[1:0] = 01, the ADC is placed into power-down mode, and when Bits[1:0] = 10, the ADC is placed into standby mode.

Output Mode (Address 0x14)

Bits[7:5]—JESD204B CS bits assignment

These bits control the function of the CS bits in the JESD204B serial data stream.

Bit 4—ADC output disable

If this bit is set, the output data from the ADC is disabled.

Bit 3—Open

Bit 2—ADC data invert

If this bit is set, the output data from the ADC is inverted.

Bits[1:0]—Data format select

These bits select the output data format. When Bits[1:0] = 00, the output data is in offset binary format, and when Bits[1:0] = 01, the output data is in twos complement format.

SYNCINB±/SYSREF± Control (Address 0x3A)

Bits[7:5]—Reserved

Bit 4—JESD204B realign SYNCINB±

When this bit is set low, the JESD204B link operates in normal mode. When this bit is high, the JESD204B link realigns on every active SYNCINB± assertion.

Bit 3—JESD204B realign SYSREF±

When this bit is set low, the JESD204B link operates in normal mode. When this bit is high, the JESD204B link realigns on every active SYSREF± assertion.

Bit 2—SYSREF± mode

When this bit is set low, the clock dividers are continuously reset on each SYSREF± assertion. When this bit is high, the clock dividers are reset on the next rising edge of SYSREF± only.

Bit 1—SYSREF± enable

When this bit is set low, the SYSREF± input is disabled. When this bit is high, the SYSREF± input is enabled.

Bit 0—Enable SYNCINB± buffer

When this bit is set low, the SYNCINB± input buffer is disabled. When this bit is high, the SYNCINB± input buffer is enabled.

NSR Control (Address 0x3C)

Bits[7:2]—Reserved

Bit 1—Bandwidth mode (NSR)

Bit 1 determines the bandwidth mode of the NSR. When Bit 1 is set to 0, the NSR is configured for 22% bandwidth mode, which provides enhanced SNR performance over 22% of the sample rate. When Bit 1 is set to 1, the NSR is configured for 33% bandwidth mode, which provides enhanced SNR performance over 33% of the sample rate.

Bit 0—NSR enable

The NSR is enabled when Bit 0 is high and disabled when Bit 0 is low.

NSR Tuning Word (Address 0x3E)

Bits[7:6]—Reserved

Bits[5:0]—Noise shaped requantizer tuning word

The NSR tuning word sets the band edges of the NSR band. In 22% bandwidth mode, there are 57 possible tuning words, and in 33% bandwidth mode, there are 34 possible tuning words. In either mode, each step represents 0.5% of the ADC sample rate. For the equations that calculate the tuning word based on the bandwidth mode of operation, see the Noise Shaping Requantizer section.

DC Correction Control (Address 0x40)

Bit 7—Reserved

Bit 6—Freeze dc correction

When Bit 6 is set low, the dc correction is continuously calculated. When Bit 6 is set high, the dc correction is no longer updated to the signal monitor block, which holds the last dc value calculated.

Bits[5:2]—DC correction bandwidth select

Bits[5:2] set the averaging time of the signal monitor dc correction function. This 4-bit word sets the bandwidth of the correction block, according to the following equation:

$$DC_Corr_BW = 2^{-k-14} \times \frac{f_{CLK}}{2 \times \pi}$$

where:
k is the 4-bit value programmed in Bits[5:2] of Address 0x40 (values between 0 and 13 are valid for k; programming 14 or 15 provides the same result as programming 13).
f_{CLK} is the AD6677 ADC sample rate in hertz.

Bit 1—Enable dc correction

Setting this bit high causes the output of the dc measurement block to be summed with the data in the signal path to remove the dc offset from the signal path.

Bit 0—Reserved

DC Correction Value 0 (Address 0x41)

Bits[7:0]—DC correction value LSB[7:0]

These bits are the LSBs of the dc correction value.

DC Correction Value 1 (Address 0x42)

Bits[7:0]—DC correction value MSB[15:8]

These bits are the MSBs of the dc correction value.

Fast Detect Control (Address 0x45)

Bits[7:5]—Reserved

Bit 4—FD pin function

When this bit is set low, the FD pin functions as the fast detect output. When this pin is set high, the FD pin functions as the overrange indicator.

Bit 3—Force FD output enable

Setting this bit high forces the FD output pin to the value written to Bit 2 of this register (Address 0x45). This enables the user to force a known value on the FD pin for debugging.

Bit 2—Forced FD output value

The value written to Bit 2 is forced on the FD output pin when Bit 3 is written high.

Bit 1—Reserved

Bit 0—Enable fast detect output

Setting this bit high enables the output of the upper threshold FD comparator to drive the FD output pin.

Fast Detect Upper Threshold (Address 0x47 and Address 0x48)

Address 0x48, Bit 7—Reserved

Address 0x48, Bits[6:0]—Fast detect upper threshold[14:8]

Address 0x47, Bits[7:0]—Fast detect upper threshold[7:0]

These registers provide an upper limit threshold. The 15-bit value is compared with the output magnitude from the ADC block. If the ADC magnitude exceeds this threshold value, the FD output pin is set if Bit 0 in Address 0x45 is set.

Fast Detect Lower Threshold (Address 0x49 and Address 0x4A)

Address 0x4A, Bit 7—Reserved

Address 0x4A, Bits[6:0]—Fast detect lower threshold[14:8]

Address 0x49, Bits[7:0]—Fast detect lower threshold[7:0]

These registers provide a lower limit threshold. The 15-bit value is compared with the output magnitude from the ADC block. If the ADC magnitude is less than this threshold value for the number of cycles programmed in the fast detect dwell time register, the FD output bit is cleared.

Fast Detect Dwell Time (Address 0x4B and Address 0x4C)

Address 0x4C, Bits[7:0]—Fast detect dwell time[15:8]

Address 0x4B, Bits[7:0]—Fast detect dwell time[7:0]

These register values set the minimum time in ADC sample clock cycles (after clock divider) that a signal must stay below the lower threshold limit before the FD output bits are cleared.

JESD204B Quick Configuration (Address 0x5E)

Bits [7:0]—JESD204B quick configuration

These bits serve to quickly set up the default JESD204B link parameters for M = 1 and L = 1.

JESD204B Link Control 1 (Address 0x5F)

Bit 7—Open

Bit 6—Serial tail bit enable

If this bit is set and the CS bits are not enabled, unused tail bits are padded with a pseudo-random number sequence from a 9-bit LFSR (see JESD204B 5.1.4).

Bit 5—JESD204B test sample enable

If set, JESD204B test samples are enabled, and the long transport layer test sample sequence (as specified in JESD204B Section 5.1.6.3) sent on all link lanes.

Bit 4—Reserved; set to 1

Bits[3:2]—ILAS mode

01 = initial lane alignment sequence enabled.

11 = initial lane alignment sequence always on in test mode; JESD204B data link layer test mode where repeated lane alignment sequence (as specified in JESD204B Section 5.3.3.8.2) is sent on all lanes.

Bit 1—Reserved; set to 1

Bit 0—JESD204B link power-down

If Bit 0 is set high, the serial transmit link is held in reset with the clock gated off. The JESD204B transmitter must be powered down when changing any of the link configuration bits.

JESD204B Link Control 2 (Address 0x60)

Bits[7:5]—Reserved; set to 0

Bit 4—SYNCINB± logic type

0 = LVDS differential pair SYNCINB± input (default).

1 = CMOS single-ended SYNCINB± using the SYNCINB+ input. If operating in this mode, leave the SYNCINB− floating.

Bit 3—Open

Bit 2—Reserved; set to 0

Bit 1—Invert transmit bits

Setting this bit inverts the 10 serial output bits. This effectively inverts the output signals.

Bit 0—Reserved; set to 0

JESD204B Link Control 3 (Address 0x61)

Bit [7:6]—Reserved; set to 0

Bits[5:4]—Test data injection point

01 = 10-bit test generation data injected at output of 8B/10B encoder (at input to PHY).

10 = 8-bit test generation data injected at input of scrambler.

Bits[3:0]—JESD204B Test Mode Patterns

0000 = normal operation (test mode disabled).

0001 = alternating checkerboard.

0010 = 1/0 word toggle.

0011 = PN23 sequence.

0100 = PN9 sequence.

0101 = continuous/repeat user test mode. The most significant bits from the user patterns (1, 2, 3, 4) are placed on the output for one clock cycle and then the output user patterns are repeated (1, 2, 3, 4, 1, 2, 3, 4, 1, 2, 3, 4….).

0110 = single user test mode. The most significant bits from the user patterns (1, 2, 3, 4) are placed on the output for one clock cycle and then all zeros are output (output user patterns 1, 2, 3, 4; then output all zeros).

0111 = reserved.

1100 = PN7 sequence.

1101 = PN15 sequence.

Others = unused.

JESD204B Device Identification (DID) Configuration (Address 0x64)

Bits[7:0]—JESD204B device identification (DID) value

JESD204B Bank Identification (BID) Configuration (Address 0x65)

Bits[7:4]—Open

Bits[3:0]—JESD204B bank identification (BID) value

JESD204B Lane Identification (LID) Configuration (Address 0x67)

Bits[7:5]—Open

Bits[4:0]—JESD204B lane identification (LID) value

JESD204B Scrambler (SCR) and Lane (L) Configuration (Address 0x6E)

Bit 7—JESD204B scrambling (SCR)

When this bit is set to low, it disables the scrambler (SCR = 0). When this bit is set to high, it enables the scrambler (SCR = 1).

Bits[6:5]—Open

Bits[4:0]—JESD204B number of lanes

0 = one lane per link (L = 1).

JESD204B Parameters, F (Address 0x6F, Read Only)

Bits[7:0]—JESD204B number of octets per frame (F)

The readback from this register is calculated from the following equation: $F = (M \times 2)/L$.

The valid value for F is F = 2, with M = 1 and L = 1.

JESD204B Parameters, K (Address 0x70)

Bits[7:0]—JESD204B number of frames per multiframe (K)

This register sets the K value for the JESD204B interface which defines the number of frames per multiframe. The value must be a multiple of 4.

JESD204B Parameters, M (Address 0x71)

Bit [7:0]—JESD204B number of converters (M)

0 = link connected to one ADC. Only primary input used (M = 1).

JESD204B Parameters, N/CS (Address 0x72)

Bits[7:6]—Number of control bits (CS)

00 = no control bits sent per sample (CS = 0).

01 = one control bit sent per sample—overrange bit enabled (CS = 1).

10 = two control bits sent per sample—overflow/underflow bits enabled (CS = 2).

Bit [5:4]—Open

Bits [3:0]—ADC converter resolution (N)

Read only bits showing the converter resolution (reads back 13 (0xD) for 14-bit resolution).

JESD204B Parameters, Subclass/N' (Address 0x73)

Bit 7—Reserved

Bits[6:5]—JESD204B subclass

When Bits[6:5] are 00, the device operates in Subclass 0 mode, and when Bits[6:5] are 01, the device operates in Subclass 1 mode.

Bit 4—Reserved

Bits[3:0]—JESD204B N' Value

Read only bits showing the total number of bits per sample, minus 1 (reads back 15 (0xF) for 16 bits per sample).

JESD204B Samples per Converter per Frame Cycle (S) (Address 0x74)

Bits[7:6]—Open

Bit 5—Reserved; set to 1

Bits[4:0]—JESD204B samples per converter per frame cycle (S)

Read only bits showing the number of samples per converter frame cycle, minus 1 (reads back 0 (0x0) for one sample per converter frame).

JESD204B Parameters, HD and CF (Address 0x75)

Bit 7—JESD204B high density (HD) value (read only)

Read only bit. Always set to 0.

Bits[6:5]—Open

Bits[4:0]—JESD204B control words per frame clock cycle per link (CF)

Read only bits. Reads back 0x0.

JESD204B Reserved 1 (Address 0x76)

Bits[7:0]—JESD204B Reserved Field 1

This read/write register is available for customer use.

JESD204B Reserved 2 (Address 0x77)

Bits[7:0]—JESD204B Reserved Field 2

This read/write register is available for customer use.

JESD204B Checksum (Address 0x79)

Bits[7:0]—JESD204B checksum value for the output lane

This read only register is automatically calculated for the lane. Checksum equals sum (all link configuration parameters for the lane) modulus 256.

JESD204B Output Driver Control (Address 0x80)

Bits[7:1]—Reserved

Bit 1—JESD204B driver power-down

When this bit is set low, the JESD204B output drivers are enabled. When this bit is set high, the JESD204B output drivers are powered down.

JESD204B LMFC Offset (Address 0x8B)

Bits[7:5]—Reserved

Bits[4:0]—Local multiframe clock phase offset value

These bits are the reset value for the local multiframe clock (LMFC) phase counter when SYSREF± is asserted. These bits are used in applications requiring deterministic delay.

JESD204B Preemphasis (Address 0xA8)

Bits[7:0]—JESD204B preemphasis enable option

These bits enable the preemphasis feature on the JESD204B output drivers. Setting Bits[7:0] to 0x04 disables preemphasis, and setting Bits[7:0] to 0x14 enables preemphasis.

APPLICATIONS INFORMATION

DESIGN GUIDELINES

Before starting system level design and layout of the AD6677, it is recommended that the designer become familiar with these guidelines, which discuss the special circuit connections and layout requirements needed for certain pins.

Power and Ground Recommendations

When connecting power to the AD6677, it is recommended that two separate 1.8 V power supplies be used. The power supply for AVDD can be isolated, and the power supply for DVDD and DRVDD can be tied together, in which case, an isolation inductor of approximately 1 µH is recommended. Alternatively, the JESD204B PHY power (DRVDD) and analog (AVDD) supplies can be tied together, and a separate supply can be used for the digital outputs (DVDD).

The designer can employ several different decoupling capacitors to cover both high and low frequencies. Place these capacitors close to the point of entry at the PCB level and close to the pins of the device with minimal trace length.

When using the AD6677, a single PCB ground plane is sufficient. With proper decoupling and smart partitioning of the PCB analog, digital, and clock sections, optimum performance is easily achieved.

Exposed Pad Thermal Heat Slug Recommendations

It is mandatory that the exposed pad on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance. Mate a continuous, exposed (no solder mask) copper plane on the PCB to the AD6677 exposed pad.

The copper plane must have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. Fill or plug these vias with nonconductive epoxy.

To maximize the coverage and adhesion between the ADC and the PCB, overlay a silkscreen to partition the continuous plane on the PCB into several uniform sections. This provides several tie points between the ADC and the PCB during the reflow process. Using one continuous plane with no partitions guarantees only one tie point between the ADC and the PCB. See the evaluation board for a PCB layout example. For detailed information about the packaging and PCB layout of chip scale packages, refer to the Application Note AN-772, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

VCM

Decouple the VCM pin to ground with 0.1 µF capacitors, as shown in Figure 31. It is recommended to place one 0.1 µF capacitor as close as possible to the VCM pin and another at the VCM connection to the analog input network.

SPI Port

Do not activate the SPI port during periods when the full dynamic performance of the converter is required. Because the SCLK, $\overline{\text{CS}}$, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD6677 to keep these signals from transitioning at the converter input pins during critical sampling periods.

OUTLINE DIMENSIONS

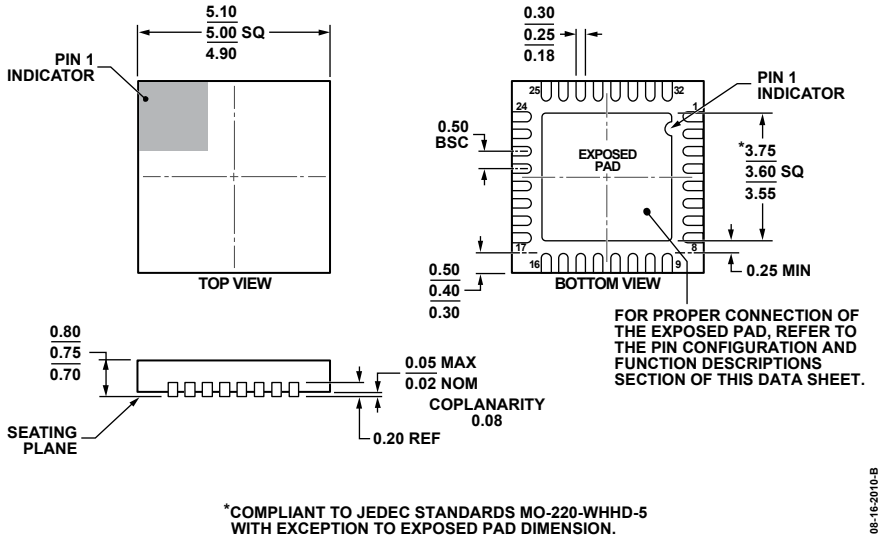

Figure 59. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD6677BCPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
AD6677BCPZRL7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
AD6677EBZ		Evaluation Board with AD6677	

[1] Z = RoHS Compliant Part.

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