IF Receiver

Data Sheet

AD6672

FEATURES

- 11-bit, 250 MSPS output data rate
- Performance with NSR enabled
  - SNR: 75.2 dBFS in a 55 MHz band to 185 MHz at 250 MSPS
  - SNR: 72.8 dBFS in an 82 MHz band to 185 MHz at 250 MSPS
- Performance with NSR disabled
  - SNR: 66.4 dBFS up to 185 MHz at 250 MSPS
  - SFDR: 87 dBc up to 185 MHz at 250 MSPS
- Total power consumption: 358 mW at 250 MSPS
- 1.8 V supply voltages
- LVDS (ANSI-644 levels) outputs
- Integer 1-to-8 input clock divider (625 MHz maximum input)
- Internal ADC voltage reference
- Flexible analog input range
  - 1.4 V p-p to 2.0 V p-p (1.75 V p-p nominal)
- Serial port control
- Energy saving power-down modes

APPLICATIONS

- Communications
- Diversity radio and smart antenna (MIMO) systems
- Multimode digital receivers (3G)
  - WCDMA, LTE, CDMA2000
  - WiMAX, TD-SCDMA
- I/Q demodulation systems
- General-purpose software radios

GENERAL DESCRIPTION

The AD6672 is an 11-bit intermediate receiver with sampling speeds of up to 250 MSPS. The AD6672 is designed to support communications applications, where low cost, small size, wide bandwidth, and versatility are desired.

The ADC core features a multistage, differential pipelined architecture with integrated output error correction logic. The ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. A duty cycle stabilizer is provided to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

The ADC core output is connected internally to a noise shaping requantizer (NSR) block. The device supports two output modes that are selectable via the serial port interface (SPI). With the NSR feature enabled, the outputs of the ADCs are processed such that the AD6672 supports enhanced SNR performance within a limited region of the Nyquist bandwidth while maintaining an 11-bit output resolution. The NSR block is programmed to provide a bandwidth of up to 33% of the sample clock. For example, with a sample clock rate of 250 MSPS, the AD6672 can achieve up to 73.6 dBFS SNR for an 82 MHz bandwidth at 185 MHz f_{IN}.

With the NSR block disabled, the ADC data is provided directly to the output with an output resolution of 11 bits. The AD6672 can achieve up to 66.6 dBFS SNR for the entire Nyquist bandwidth when operated in this mode.

FUNCTIONAL BLOCK DIAGRAM

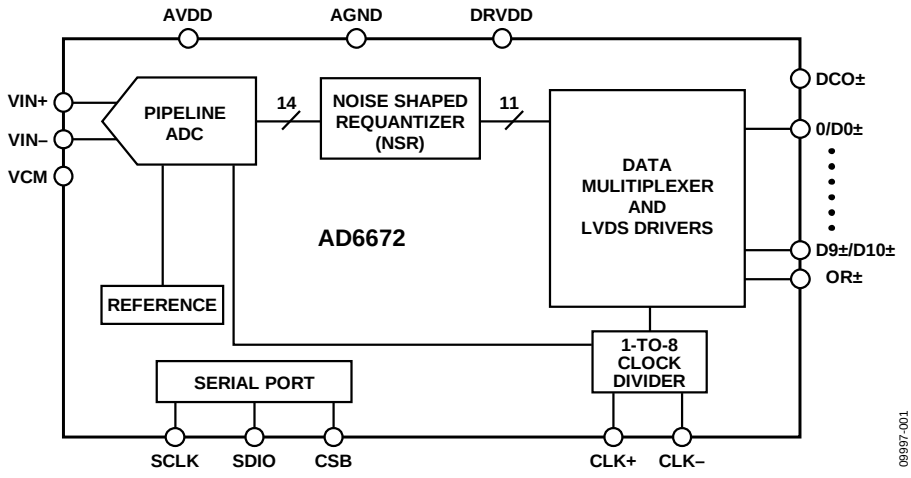


Figure 1.

Rev. C

Document Feedback

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REVISION HISTORY

12/14—Rev. B to Rev. C

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Changes to 33% BW NSR Mode (>82 MHz BW at 250 MSPS) Section ... 21
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7/14—Rev. A to Rev. B

Changes to Features Section and Figure 1 ... 1
Changes to Full Power Bandwidth Parameter, Table 2 ... 6
Deleted Noise Bandwidth Parameter, Table 2 ... 6

11/12—Rev. 0 to Rev. A

Changes to Features Section ... 1

7/11—Revision 0: Initial Version

When the NSR block is disabled, the ADC data is provided directly to the output at a resolution of 11 bits. This allows the AD6672 to be used in telecommunication applications, such as a digital predistortion observation path, where wider bandwidths are required.

After digital signal processing, multiplexed output data is routed into one 11-bit output port such that the maximum data rate is 500 Mbps (DDR). This output is LVDS and supports ANSI-644 levels.

The AD6672 receiver digitizes a wide spectrum of IF frequencies. This IF sampling architecture greatly reduces component cost and complexity compared with traditional analog techniques or less integrated digital methods.

Flexible power-down options allow significant power savings. Programming for device setup and control is accomplished using a 3-wire, SPI-compatible serial interface with numerous modes to support board level system testing.

The AD6672 is available in a 32-lead, RoHS-compliant LFCSP and is specified over the industrial temperature range of −40°C to +85°C. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. Integrated 11-bit, 250 MSPS ADC with a noise shaping requantizer option.
2. Operation from a single 1.8 V supply and a separate digital output driver supply accommodating LVDS outputs.
3. On-chip 1-to-8 integer clock divider function to support a wide range of clocking.
4. Noise shaping requantizer function allows attaining improved SNR within a reduced frequency band. With NSR enabled, the AD6672 supports up to 82 MHz at 250 MSPS.
5. Standard serial port interface (SPI) that supports various product features and functions, such as data formatting (offset binary, twos complement, or gray coding), enabling the clock DCS, power-down, test modes, and voltage reference mode.

SPECIFICATIONS

ADC DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.75 V p-p full-scale input range, DCS enabled, unless otherwise noted.

Table 1.

Parameter	Temperature	Min	Typ	Max	Unit
RESOLUTION	Full	11			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full			±11	mV
Gain Error	Full			+3/−6.5	% FSR
Differential Nonlinearity (DNL)	Full			±0.2	LSB
	25°C		±0.1		LSB
Integral Nonlinearity (INL)[1]	Full			±0.3	LSB
	25°C		±0.12		LSB
TEMPERATURE DRIFT					
Offset Error	Full		±7		ppm/°C
Gain Error	Full		±85		ppm/°C
INPUT-REFERRED NOISE					
VREF = 1.0 V	25°C		0.65		LSB rms
ANALOG INPUT					
Input Span	Full		1.75		V p-p
Input Capacitance[2]	Full		5		pF
Input Resistance	Full		20		kΩ
Input Common-Mode Voltage	Full		0.9		V
POWER SUPPLIES					
Supply Voltage					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
Supply Current					
I_{AVDD}[1]	Full		136	145	mA
I_{DRVDD}[1] (NSR Disabled)	Full		63	68	mA
I_{DRVDD}[1] (NSR Enabled, 22% Bandwidth Mode)	Full		89		mA
I_{DRVDD}[1] (NSR Enabled, 33% Bandwidth Mode)	Full		99		mA
POWER CONSUMPTION					
Sine Wave Input (DRVDD = 1.8 V, NSR Disabled)	Full		358	385	mW
Sine Wave Input (DRVDD = 1.8 V, NSR Enabled, 22% Bandwidth Mode)	Full		405		mW
Sine Wave Input (DRVDD = 1.8 V, NSR Enabled, 33% Bandwidth Mode)	Full		423		mW
Standby Power[3]	Full		50		mW
Power-Down Power	Full		5		mW

[1] Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND. See Figure 18 for the equivalent analog input structure.
[3] Standby power is measured with a dc input, the CLK pin inactive (set to AVDD or AGND).

ADC AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.75 V p-p full-scale input range, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
SIGNAL-TO-NOISE-RATIO (SNR)					
NSR Disabled					
f_{IN} = 30 MHz	25°C		66.6		dBFS
f_{IN} = 90 MHz	25°C		66.6		dBFS
f_{IN} = 140 MHz	25°C		66.5		dBFS
f_{IN} = 185 MHz	25°C		66.4		dBFS
	Full	65.4			dBFS
f_{IN} = 220 MHz	25°C		66.3		dBFS
NSR Enabled					
22% Bandwidth Mode					
f_{IN} = 30 MHz	25°C		75.8		dBFS
f_{IN} = 90 MHz	25°C		75.7		dBFS
f_{IN} = 140 MHz	25°C		75.6		dBFS
f_{IN} = 185 MHz	25°C		75.2		dBFS
	Full	72.2			dBFS
f_{IN} = 220 MHz	25°C		74.8		dBFS
33% Bandwidth Mode					
f_{IN} = 30 MHz	25°C		73.4		dBFS
f_{IN} = 90 MHz	25°C		73.3		dBFS
f_{IN} = 140 MHz	25°C		73.2		dBFS
f_{IN} = 185 MHz	25°C		72.8		dBFS
	Full	69.2			dBFS
f_{IN} = 220 MHz	25°C		72.4		dBFS
SIGNAL-TO-NOISE RATIO AND DISTORTION (SINAD)					
f_{IN} = 30 MHz	25°C		65.7		dBFS
f_{IN} = 90 MHz	25°C		65.7		dBFS
f_{IN} = 140 MHz	25°C		65.6		dBFS
f_{IN} = 185 MHz	25°C		65.3		dBFS
	Full	64.4			dBFS
f_{IN} = 220 MHz	25°C		65.2		dBFS
WORST SECOND OR THIRD HARMONIC					
f_{IN} = 30 MHz	25°C		−88		dBc
f_{IN} = 90 MHz	25°C		−88		dBc
f_{IN} = 140 MHz	25°C		−89		dBc
f_{IN} = 185 MHz	25°C		−87		dBc
	Full			−80	dBc
f_{IN} = 220 MHz	25°C		−88		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 30 MHz	25°C		88		dBc
f_{IN} = 90 MHz	25°C		88		dBc
f_{IN} = 140 MHz	25°C		89		
f_{IN} = 185 MHz	25°C		87		dBc
	Full	80			dBc
f_{IN} = 220 MHz	25°C		88		dBc

Parameter[1]	Temperature	Min	Typ	Max	Unit
WORST OTHER (HARMONIC OR SPUR)					
f_{IN} = 30 MHz	25°C		−96		dBc
f_{IN} = 90 MHz	25°C		−97		dBc
f_{IN} = 140 MHz	25°C		−97		dBc
f_{IN} = 185 MHz	25°C		−98		dBc
	Full			−81	dBc
f_{IN} = 220 MHz	25°C		−97		dBc
TWO-TONE SFDR					
f_{IN} = 184.12 MHz, 187.12 MHz (−7 dBFS)	25°C		88		dBc
FULL POWER BANDWIDTH	25°C		1000		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK–)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND		AVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	10		+22	µA
Low Level Input Current	Full	−22		−10	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	12	15	18	kΩ
LOGIC INPUT (CSB)[1]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	50		71	µA
Low Level Input Current	Full	−5		+5	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (SCLK)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	45		70	µA
Low Level Input Current	Full	−5		+5	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUTS (SDIO)[1]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	45		70	µA
Low Level Input Current	Full	−5		+5	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
DIGITAL OUTPUTS (OR+, OR–)					
LVDS Data and OR Outputs					
Differential Output Voltage (V_{OD}), ANSI Mode	Full	250	350	450	mV
Output Offset Voltage (V_{OS}), ANSI Mode	Full	1.15	1.25	1.35	V
Differential Output Voltage (V_{OD}), Reduced Swing Mode	Full	150	200	280	mV
Output Offset Voltage (V_{OS}), Reduced Swing Mode	Full	1.15	1.25	1.35	V

[1] Pull-up.
[2] Pull-down.

SWITCHING SPECIFICATIONS

Table 4.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK INPUT PARAMETERS					
Input Clock Rate	Full			625	MHz
Conversion Rate[1]	Full	40		250	MSPS
CLK Period—Divide-by-1 Mode (t_{CLK})	Full	4			ns
CLK Pulse Width High (t_{CH})					
Divide-by-1 Mode, DCS Enabled	Full	1.8	2.0	2.2	ns
Divide-by-1 Mode, DCS Disabled	Full	1.9	2.0	2.1	ns
Divide-by-2 Mode Through Divide-by-8 Mode	Full	0.8			ns
Aperture Delay (t_A)	Full		1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.1		ps rms
DATA OUTPUT PARAMETERS					
Data Propagation Delay (t_{PD})	Full	4.1	4.7	5.2	ns
DCO Propagation Delay (t_{DCO})	Full	4.7	5.3	5.8	ns
DCO-to-Data Skew (t_{SKEW})	Full	0.3	0.5	0.7	ns
Pipeline Delay (Latency)—NSR Disabled	Full		10		Cycles
Pipeline Delay (Latency)—NSR Enabled	Full		13		Cycles
Wake-Up Time (from Standby)	Full		10		µs
Wake-Up Time (from Power-Down)	Full		100		µs
Out-of-Range Recovery Time	Full		3		Cycles

[1] Conversion rate is the clock rate after the divider.

Timing Diagram

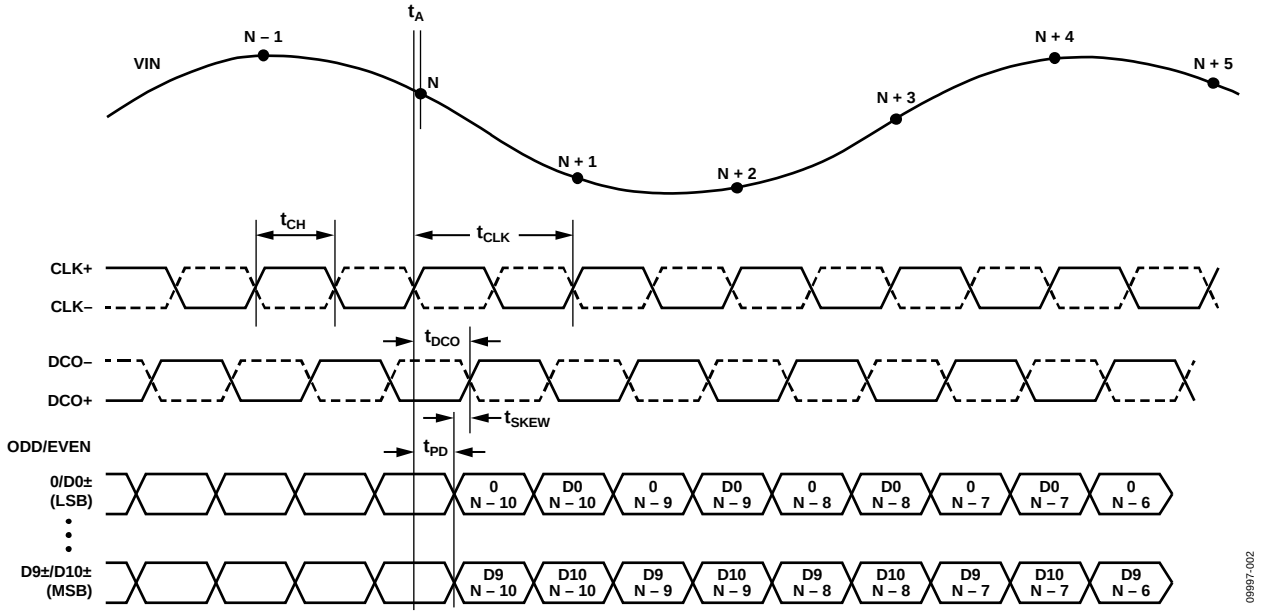


Figure 2. LVDS Data Output Timing

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SPI TIMING REQUIREMENTS	See Figure 42 for the SPI timing diagram				
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK should be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK should be in a logic low state	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 42)	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 42)	10			ns

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
VIN+, VIN− to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
VCM to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to DRVDD + 0.3 V
SCLK to AGND	−0.3 V to DRVDD + 0.3 V
SDIO to AGND	−0.3 V to DRVDD + 0.3 V
0/D0−, 0/D0 + Through D9−/D10−, D9+/D10+ to AGND	−0.3 V to DRVDD + 0.3 V
OR+/OR− to AGND	−0.3 V to DRVDD + 0.3 V
DCO+, DCO− to AGND	−0.3 V to DRVDD + 0.3 V
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +125°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the customer board increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	θ_{JC}[1, 3]	θ_{JB}[1, 4]	Unit
32-Lead LFCSP 5 mm × 5 mm (CP-32-12)	0	37.1	3.1	20.7	°C/W
	1.0	32.4			°C/W
	2.0	29.1			°C/W

[1] Per JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane. As shown in Table 7, airflow increases heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces—through holes, ground, and power planes—reduces the θ_{JA}.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

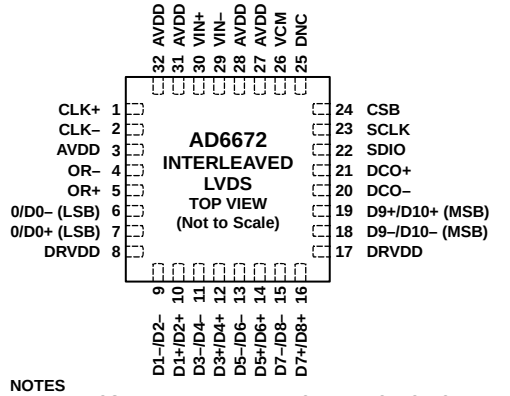


Figure 3. LFCSP Pin Configuration (Top View)

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
8, 17	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
3, 27, 28, 31, 32	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
0	AGND, Exposed Paddle	Ground	Analog Ground. The exposed thermal paddle on the bottom of the package provides the analog ground for the part. This exposed paddle must be connected to ground for proper operation.
25	DNC		Do Not Connect. Do not connect to this pin.
ADC Analog			
30	VIN+	Input	Differential Analog Input Pin (+).
29	VIN–	Input	Differential Analog Input Pin (–).
26	VCM	Output	Common-Mode Level Bias Output for Analog Inputs. This pin should be decoupled to ground using a 0.1 µF capacitor.
1	CLK+	Input	ADC Clock Input—True.
2	CLK–	Input	ADC Clock Input—Complement.
Digital Outputs			
5	OR+	Output	Overrange indicator—True.
4	OR–	Output	Overrange indicator—Complement.
7	0/D0+ (LSB)	Output	DDR LVDS Output Data 0—True. The output bit on the rising edge of the data clock output (DCO) from this output is always a Logic 0 (see Figure 2).
6	0/D0– (LSB)	Output	DDR LVDS Output Data 0—Complement. The output bit on the rising edge of the data clock output (DCO) from this output is always a Logic 0 (see Figure 2).
10	D1+/D2+	Output	DDR LVDS Output Data 1/2—True.
9	D1–/D2–	Output	DDR LVDS Output Data 1/2—Complement.
12	D3+/D4+	Output	DDR LVDS Output Data 3/4—True.
11	D3–/D4–	Output	DDR LVDS Output Data 3/4—Complement.
14	D5+/D6+	Output	DDR LVDS Output Data 5/6—True.
13	D5–/D6–	Output	DDR LVDS Output Data 5/6—Complement.
16	D7+/D8+	Output	DDR LVDS Output Data 7/8—True.
15	D7–/D8–	Output	DDR LVDS Output Data 7/8—Complement.
19	D9+/D10+ (MSB)	Output	DDR LVDS Output Data 9/10—True.
18	D9–/D10– (MSB)	Output	DDR LVDS Output Data 9/10—Complement.
21	DCO+	Output	LVDS Data Clock Output—True.
20	DCO–	Output	LVDS Data Clock Output—Complement.
SPI Control			
23	SCLK	Input	SPI Serial Clock.
22	SDIO	Input/output	SPI Serial Data I/O.
24	CSB	Input	SPI Chip Select (Active Low).

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, sample rate = 250 MSPS, DCS enabled, 1.75 V p-p differential input, VIN = −1.0 dBFS, 32k sample, T_A = 25°C, unless otherwise noted.

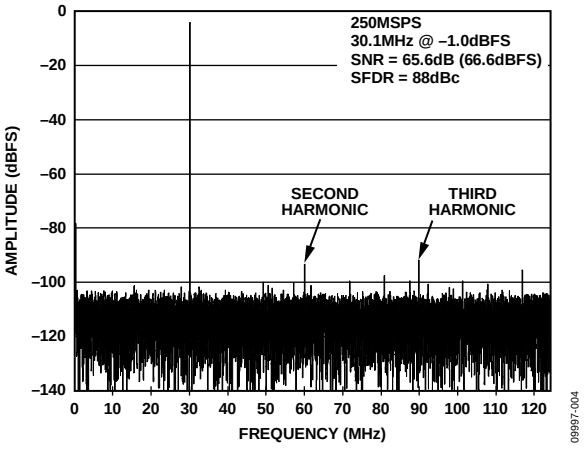


Figure 4. Single-Tone FFT with f_{IN} = 30.1 MHz

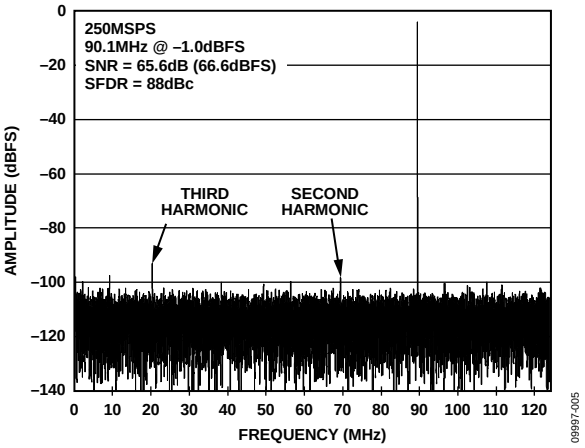


Figure 5. Single-Tone FFT with f_{IN} = 90.1 MHz

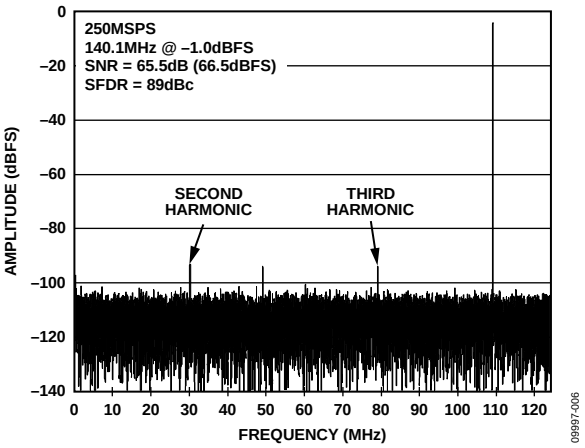


Figure 6. Single-Tone FFT with f_{IN} = 140.1 MHz

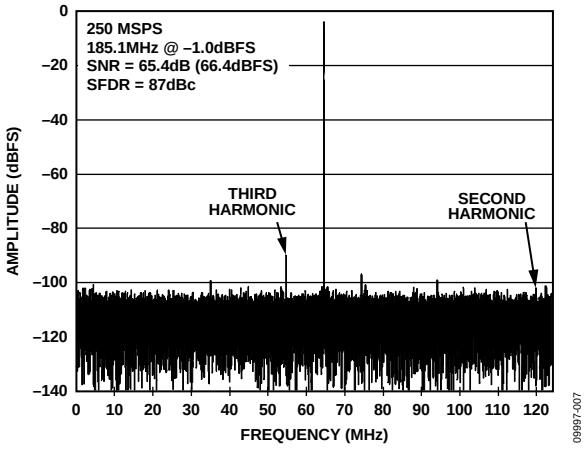


Figure 7. Single-Tone FFT with f_{IN} = 185.1 MHz

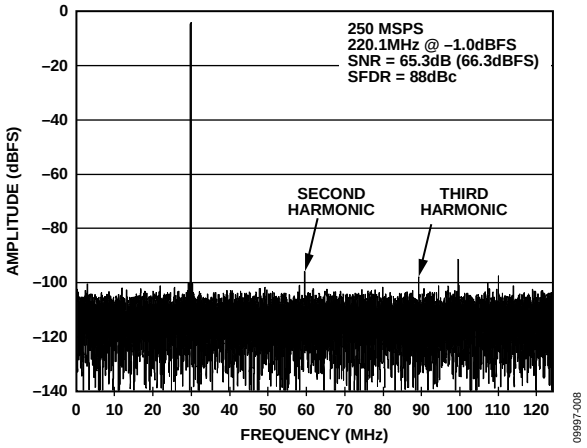


Figure 8. Single-Tone FFT with f_{IN} = 220.1 MHz

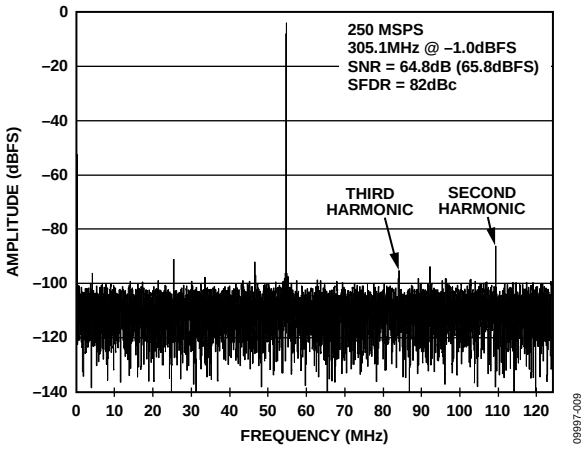


Figure 9. Single-Tone FFT with f_{IN} = 305.1 MHz

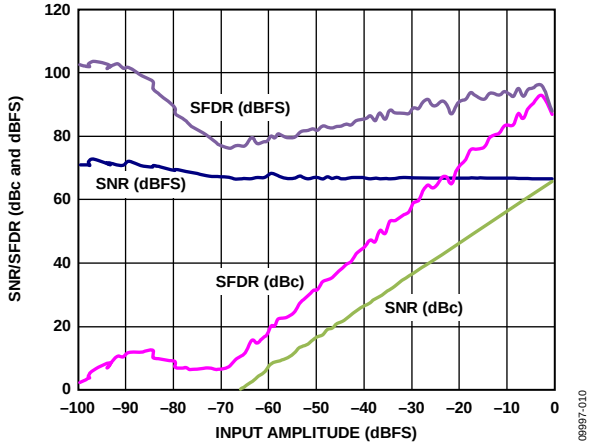


Figure 10. Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 90.1 MHz, f_S = 250 MSPS

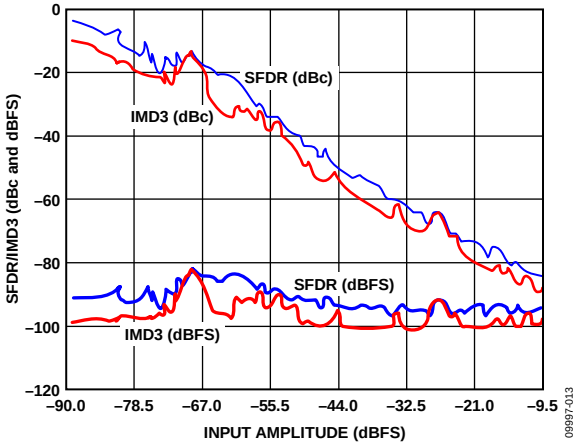


Figure 13. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz, f_S = 250 MSPS

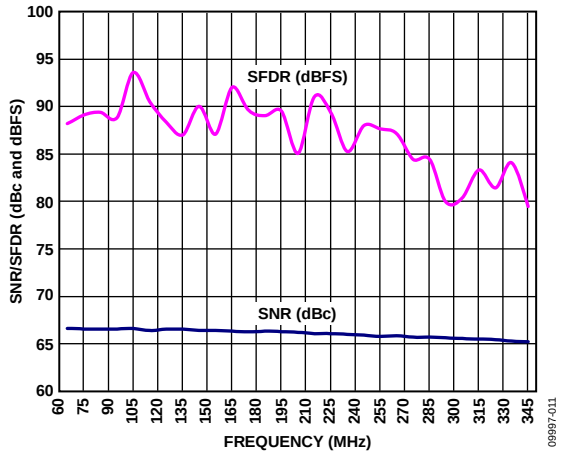


Figure 11. Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}), f_S = 250 MSPS

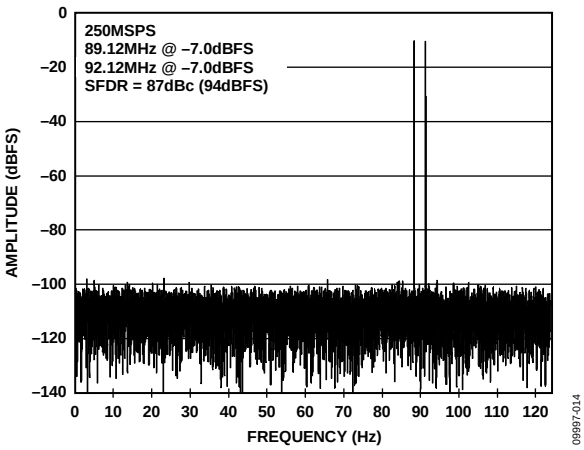


Figure 14. Two-Tone FFT with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz

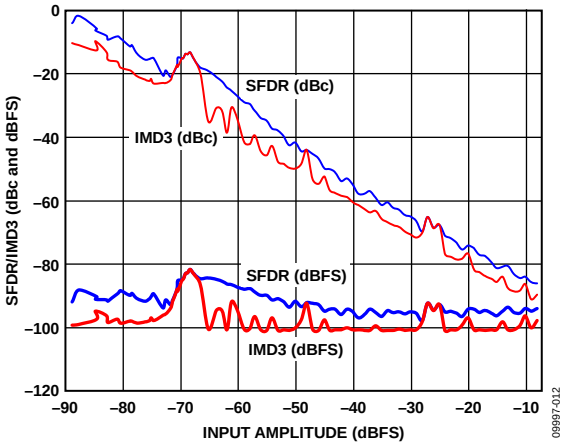


Figure 12. Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz, f_S = 250 MSPS

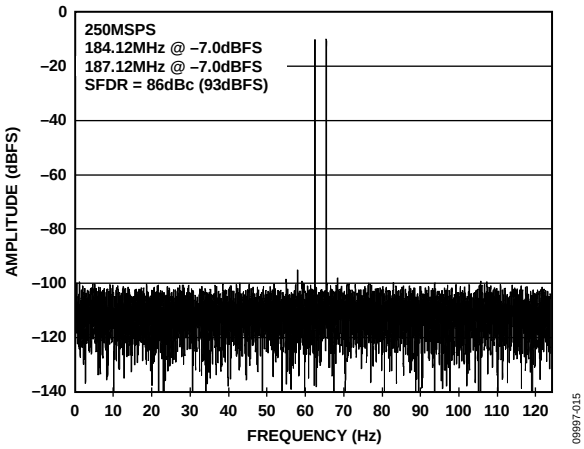


Figure 15. Two-Tone FFT with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz

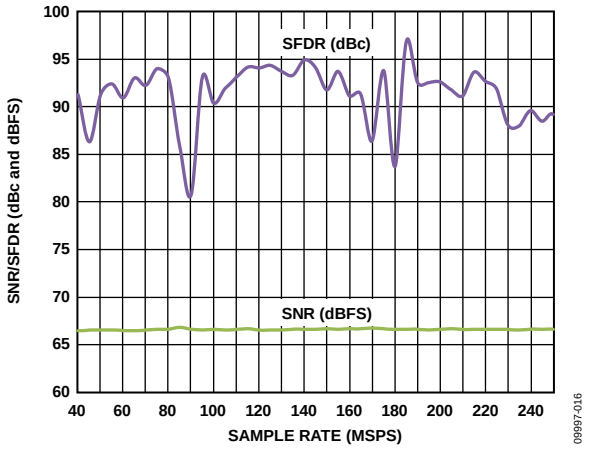


Figure 16. Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 90 MHz

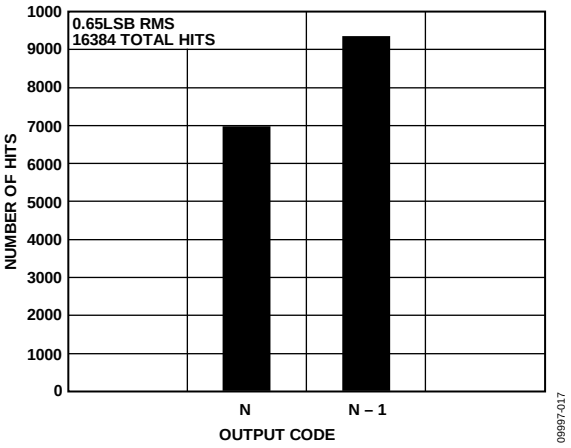


Figure 17. Grounded Input Histogram, f_S = 250 MSPS

EQUIVALENT CIRCUITS

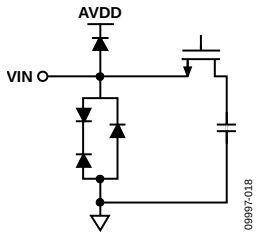


Figure 18. Equivalent Analog Input Circuit

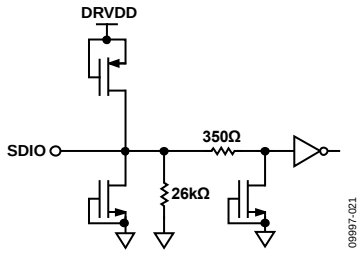


Figure 21. Equivalent SDIO Circuit

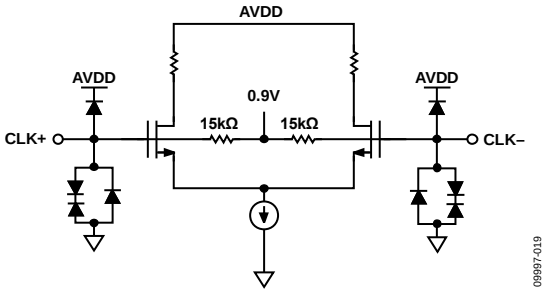


Figure 19. Equivalent Clock Input Circuit

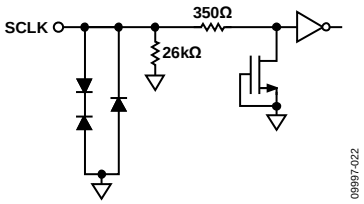


Figure 22. Equivalent SCLK Input Circuit

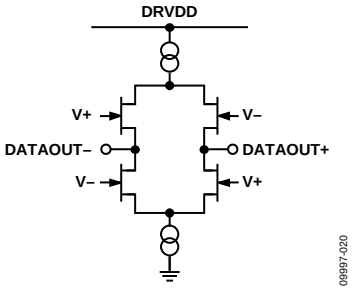


Figure 20. Equivalent LVDS Output Circuit

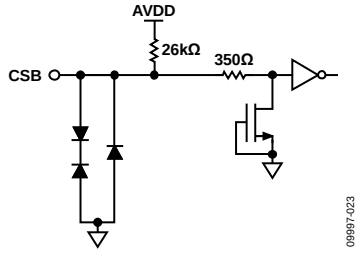


Figure 23. Equivalent CSB Input Circuit

THEORY OF OPERATION

The AD6672 can sample any $f_S/2$ frequency segment from dc to 250 MHz using appropriate low-pass or band-pass filtering at the ADC inputs with little loss in ADC performance.

Programming and control of the AD6672 are accomplished using a 3-pin, SPI-compatible serial interface.

ADC ARCHITECTURE

The AD6672 architecture consists of a front-end sample-and-hold circuit, followed by a pipelined switched-capacitor ADC. The quantized outputs from each stage are combined into a final 11-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample and the remaining stages to operate on the preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor digital-to-analog converter (DAC) and an interstage residue amplifier (MDAC). The MDAC magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage of the AD6672 contains a differential sampling circuit that can be ac- or dc-coupled in differential or single-ended modes. The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing digital output noise to be separated from the analog core. During power-down, the output buffers go into a high impedance state.

The AD6672 features a noise shaping requantizer (NSR) to allow higher than 11-bit SNR to be maintained in a subset of the Nyquist band.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD6672 is a differential switched-capacitor circuit that has been designed to attain optimum performance when processing a differential input signal.

The clock signal alternatively switches the input between sample mode and hold mode (see the configuration shown in Figure 24). When the input is switched into sample mode, the signal source must be capable of charging the sampling capacitors and settling within 1/2 clock cycle.

A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. A shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC input; therefore, the precise values are dependent on the application.

In intermediate frequency (IF) undersampling applications, the shunt capacitors should be reduced. In combination with the driving source impedance, the shunt capacitors limit the input bandwidth. Refer to the AN-742 Application Note, *Frequency Domain Response of Switched-Capacitor ADCs*; the AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*; and the *Analog Dialogue* article, "Transformer-Coupled Front-End for Wideband A/D Converters," for more information on this subject.

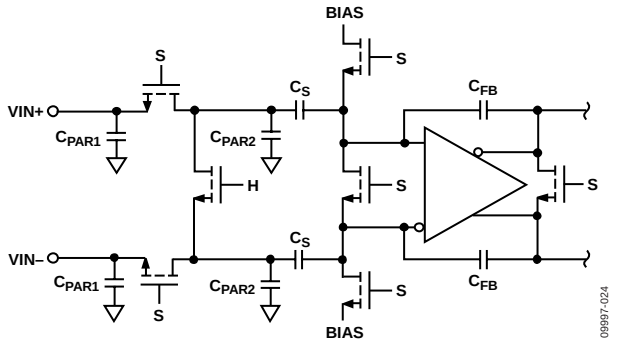


Figure 24. Switched-Capacitor Input

For best dynamic performance, match the source impedances driving VIN+ and VIN− and differentially balance the inputs.

Input Common Mode

The analog inputs of the AD6672 are not internally dc biased. In ac-coupled applications, the user must provide this bias externally. Setting the device so that V_{CM} = 0.5 × AVDD (or 0.9 V) is recommended for optimum performance. An on-board common-mode voltage reference is included in the design and is available from the VCM pin. Using the VCM output to set the input common mode is recommended. Optimum performance is achieved when the common-mode voltage of the analog input is set by the VCM pin voltage (typically 0.5 × AVDD). The VCM pin must be decoupled to ground by a 0.1 µF capacitor, as described in the Applications Information section. Place this decoupling capacitor close to the pin to minimize the series resistance and inductance between the part and this capacitor.

Differential Input Configurations

Optimum performance can be achieved when driving the AD6672 in a differential input configuration. For baseband applications, the AD8138, ADA4937-1, and ADA4930-1 differential drivers provide excellent performance and a flexible interface to the ADC.

The output common-mode voltage of the ADA4930-1 is easily set with the VCM pin of the AD6672 (see Figure 25), and the driver can be configured in a Sallen-Key filter topology to provide band-limiting of the input signal.

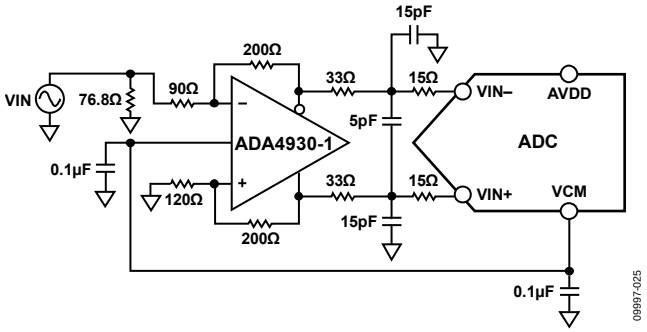


Figure 25. Differential Input Configuration Using the ADA4930-1

For baseband applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example is shown in Figure 26. To bias the analog input, connect the VCM voltage to the center tap of the secondary winding of the transformer.

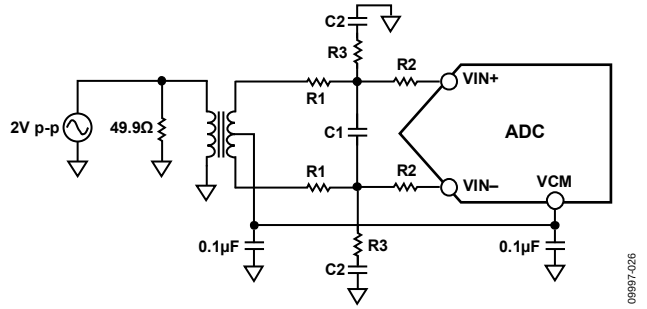


Figure 26. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz. Excessive signal power can also cause core saturation, which leads to distortion.

At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD6672. For applications where SNR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 28). In this configuration, the input is ac-coupled and the VCM voltage is provided to the input through a 33 Ω resistor. This resistor compensates for losses in the input baluns to provide a 50 Ω impedance to the driver.

In the double balun and transformer configurations, the value of the input capacitors and resistors is dependent on the input frequency and source impedance. Based on these parameters, the value of the input resistors and capacitors may need to be adjusted or some components may need to be removed. Table 9 displays recommended values to set the RC network for different input frequency ranges. However, these values are dependent on the input signal and bandwidth and should be used only as a starting guide. Note that the values given in Table 9 are for each R1, R2, C2, and R3 component shown in Figure 26 and Figure 28.

Table 9. Example RC Network

Frequency Range (MHz)	R1 Series (Ω)	C1 Differential (pF)	R2 Series (Ω)	C2 Shunt (pF)	R3 Shunt (Ω)
0 to 100	33	8.2	0	15	49.9
100 to 300	15	3.9	0	8.2	49.9

An alternative to using a transformer-coupled input at frequencies in the second Nyquist zone is to use an amplifier with variable gain. The AD8375 digital variable gain amplifier (DVGA) provides good performance for driving the AD6672. Figure 27 shows an example of the AD8375 driving the AD6672 through a band-pass antialiasing filter.

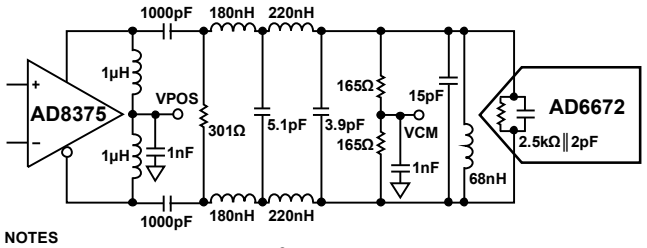


Figure 27. Differential Input Configuration Using the AD8375

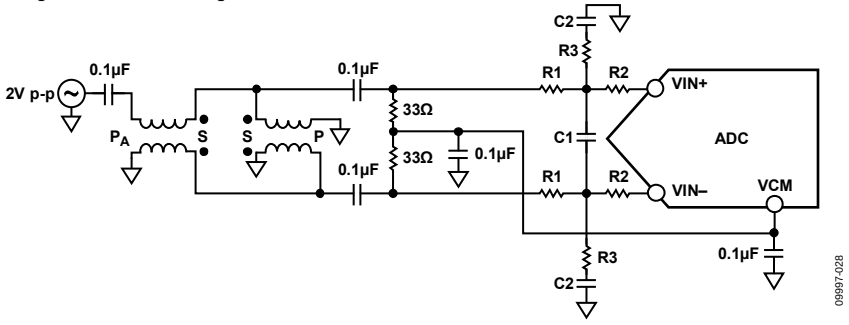


Figure 28. Differential Double Balun Input Configuration

VOLTAGE REFERENCE

A stable and accurate voltage reference is built into the AD6672. The full-scale input range can be adjusted by varying the reference voltage via SPI. The input span of the ADC tracks reference voltage changes linearly.

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD6672 sample clock inputs, CLK+ and CLK−, should be clocked with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK− pins via a transformer or via capacitors. These pins are biased internally (see Figure 29) and require no external bias. If the inputs are floated, the CLK− pin is pulled low to prevent spurious clocking.

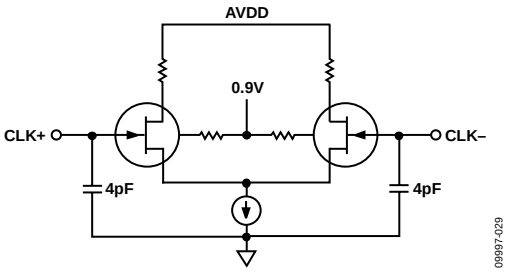


Figure 29. Simplified Equivalent Clock Input Circuit

Clock Input Options

The AD6672 has a very flexible clock input structure. Clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of the most concern, as described in the Jitter Considerations section.

Figure 30 and Figure 31 show two preferable methods for clocking the AD6672 (at clock rates of up to 625 MHz). A low jitter clock source is converted from a single-ended signal to a differential signal using an RF balun or RF transformer.

The RF balun configuration is recommended for clock frequencies between 125 MHz and 625 MHz, and the RF transformer is recommended for clock frequencies from 10 MHz to 250 MHz. The back-to-back Schottky diodes across the secondary winding of the transformer limit clock excursions into the AD6672 to approximately 0.8 V p-p differential. This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD6672 while preserving the fast rise and fall times of the signal, which are critical for low jitter performance.

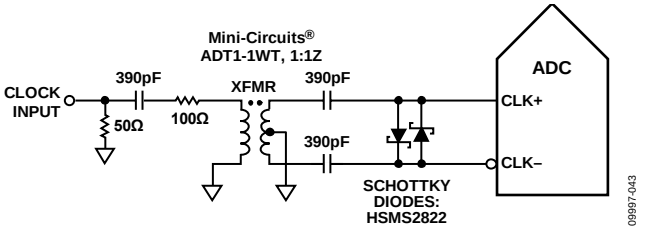


Figure 30. Transformer-Coupled Differential Clock (Up to 250 MHz)

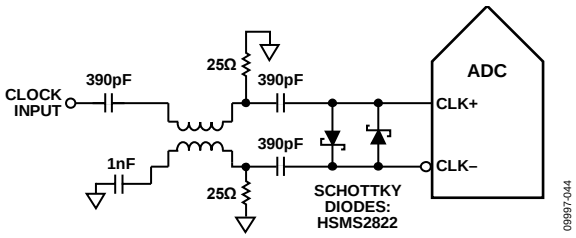


Figure 31. Balun-Coupled Differential Clock (Up to 625 MHz)

If a low jitter clock source is not available, another option is to ac-couple a differential PECL signal to the sample clock input pins as shown in Figure 32. The AD9510, AD9511, AD9512, AD9513, AD9514, AD9515, AD9516, AD9517, AD9518, AD9520, AD9522, AD9523, AD9524, and ADCLK905/ADCLK907/ADCLK925 clock drivers offer excellent jitter performance.

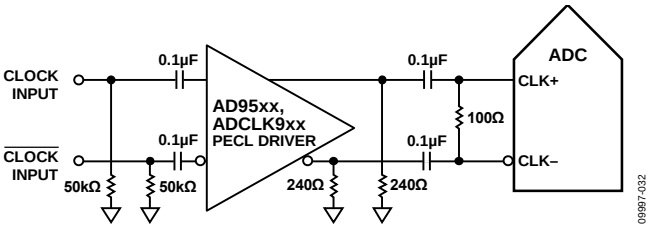


Figure 32. Differential PECL Sample Clock (Up to 625 MHz)

A third option is to ac-couple a differential LVDS signal to the sample clock input pins, as shown in Figure 33. The AD9510, AD9511, AD9512, AD9513, AD9514, AD9515, AD9516, AD9517, AD9518, AD9520, AD9522, AD9523, and AD9524 clock drivers offer excellent jitter performance.

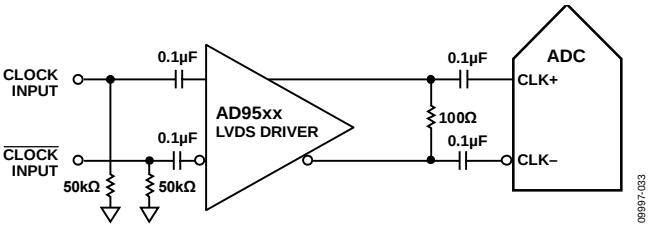


Figure 33. Differential LVDS Sample Clock (Up to 625 MHz)

Input Clock Divider

The AD6672 contains an input clock divider with the ability to divide the input clock by integer values between 1 and 8. For divide ratios other than 1, the duty cycle stabilizer (DCS) is enabled by default on power-up.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD6672 contains a DCS that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD6672.

Jitter on the rising edge of the input clock is still of paramount concern and is not reduced by the duty cycle stabilizer. The duty cycle control loop does not function for clock rates less than 40 MHz nominally. The loop has a time constant associated with it that must be considered when the clock rate may change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal. During the time that the loop is not locked, the DCS loop is bypassed, and internal device timing is dependent on the duty cycle of the input clock signal. In such applications, it may be appropriate to disable the duty cycle stabilizer. In all other applications, enabling the DCS circuit is recommended to maximize ac performance.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_{IN}) due to jitter (t_J) can be calculated by

$$SNR_{HF} = -10 \log[(2\pi \times f_{IN} \times t_{JRMS})^2 + 10^{(-SNR_{LF}/10)}]$$

In the equation, the rms aperture jitter represents the root-mean-square of all jitter sources, which include the clock input, the analog input signal, and the ADC aperture jitter specification. IF undersampling applications are particularly sensitive to jitter, as shown in Figure 34.

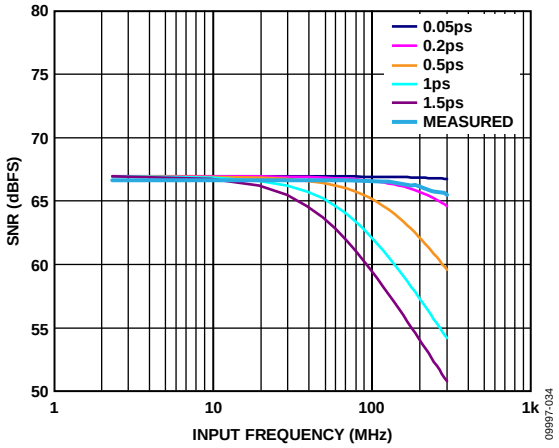


Figure 34. SNR vs. Input Frequency and Jitter

In cases where aperture jitter may affect the dynamic range of the AD6672, treat the clock input as an analog signal. In addition, use separate power supplies for the clock drivers and the ADC output driver to avoid modulating the clock signal with digital noise. Low jitter, crystal controlled oscillators provide the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), it should be retimed by the original clock during the last step.

Refer to the AN-501 Application Note, *Aperture Uncertainty and ADC System Performance*, and the AN-756 Application Note, *Sampled Systems and the Effects of Clock Phase Noise and Jitter*, for more information about jitter performance as it relates to ADCs.

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 35, the power dissipated by the AD6672 is proportional to its sample rate. The data in Figure 35 was taken using the same operating conditions as those used for the Typical Performance Characteristics section.

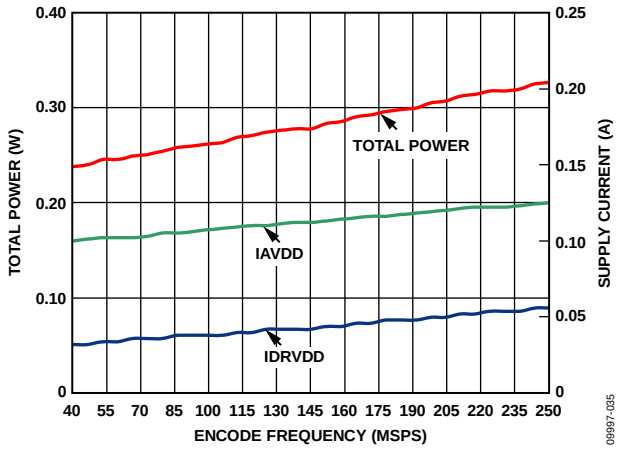


Figure 35. AD6672-250 Power and Current vs. Sample Rate

By setting the internal power-down mode bits (Bits[1:0]) in the power modes register (Address 0x08) to 01, the AD6672 is placed in power-down mode. In this state, the ADC typically dissipates 2.5 mW. During power-down, the output drivers are placed in a high impedance state.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. Internal capacitors are discharged when entering power-down mode and then must be recharged when returning to normal operation. As a result, the wake-up time is related to the time spent in power-down mode, and shorter power-down cycles result in proportionally shorter wake-up times.

When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. To put the part into standby mode, set the internal power-down mode bits (Bits[1:0]) in the power modes register (Address 0x08) to 10. See the Memory Map section and the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, for additional details.

DIGITAL OUTPUTS

The AD6672 output drivers can be configured for either ANSI LVDS or reduced swing LVDS using a 1.8 V DRVDD supply.

As detailed in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, the data format can be selected for offset binary, twos complement, or gray code when using the SPI control.

Digital Output Enable Function (OEB)

The AD6672 has a flexible three-state ability for the digital output pins. The three-state mode is enabled using the SPI interface. The data outputs can be three-stated by using the output enable bar bit (Bit 4) in Register 0x14. This OEB function is not intended for rapid access to the data bus.

Timing

The AD6672 provides latched data with a pipeline delay of 10 input sample clock cycles when NSR is disabled and provides 13 input sample clock cycles when NSR is enabled. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal.

Minimize the length of the output data lines as well as the loads placed on these lines to reduce transients within the AD6672. These transients may degrade converter dynamic performance.

The lowest typical conversion rate of the AD6672 is 40 MSPS. At clock rates below 40 MSPS, dynamic performance may degrade.

Data Clock Output (DCO)

The AD6672 also provides the data clock output (DCO) intended for capturing the data in an external register. Figure 2 shows a timing diagram of the AD6672 output modes.

ADC OVERRANGE (OR)

The ADC overrange indicator is asserted when an overrange is detected on the input of the ADC. The overrange condition is determined at the output of the ADC pipeline and, therefore, is subject to a latency of 10 ADC clock cycles. An overrange at the input is indicated by this bit 10 clock cycles after it occurs.

Table 10. Output Data Format

Input (V)	VIN+ – VIN–, Input Span = 1.75 V p-p (V)	Offset Binary Output Mode	Twos Complement Mode (Default)	OR
VIN+ – VIN–	<–0.875	000 0000 0000	100 0000 0000	1
VIN+ – VIN–	–0.875	000 0000 0000	100 0000 0000	0
VIN+ – VIN–	0	100 0000 0000	000 0000 0000	0
VIN+ – VIN–	+0.875	111 1111 1111	011 1111 1111	0
VIN+ – VIN–	>+0.875	111 1111 1111	011 1111 1111	1

NOISE SHAPING REQUANTIZER

The AD6672 features a noise shaping requantizer (NSR) to allow more than an 11-bit SNR to be maintained in a subset of the Nyquist band. The harmonic performance of the receiver is unaffected by the NSR feature. When enabled, the NSR contributes an additional 0.6 dB of loss to the input signal, such that a 0 dBFS input is reduced to −0.6 dBFS at the output pins.

Two bandwidth (BW) modes are provided; the mode can be selected from the SPI port. In each mode, the center frequency of the band can be tuned such that IFs can be placed anywhere in the Nyquist band.

22% BW NSR MODE (55 MHz BW AT 250 MSPS)

The first bandwidth mode offers excellent noise performance over 22% of the ADC sample rate (44% of the Nyquist band) and can be centered by setting the NSR mode bits (Bits[3:1]) in the NSR control register (Address 0x3C) to 000. In this mode, the useful frequency range can be set using the 6-bit tuning word (Bits[5:0]) in the NSR tuning register (Address 0x3E). There are 57 possible tuning words (TW); each step is 0.5% of the ADC sample rate. The following equations describe the left band edge (f_0), the channel center (f_{CENTER}), and the right band edge (f_1), respectively:

$$f_0 = f_{ADC} \times 0.005 \times TW$$

$$f_{CENTER} = f_0 + 0.11 \times f_{ADC}$$

$$f_1 = f_0 + 0.22 \times f_{ADC}$$

Figure 36 to Figure 38 show the typical spectrum that can be expected from the AD6672 in the 22% bandwidth mode for three tuning words.

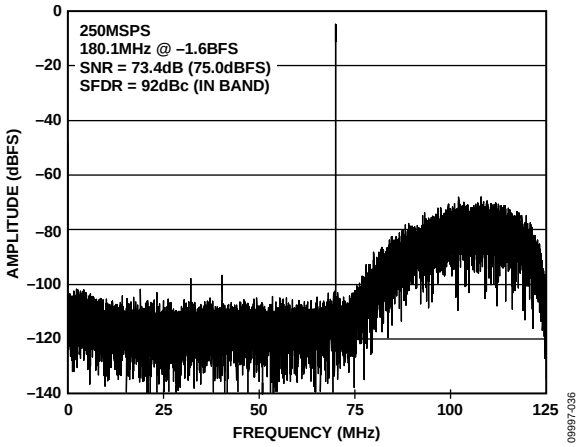


Figure 36. 22% Bandwidth Mode, Tuning Word = 13

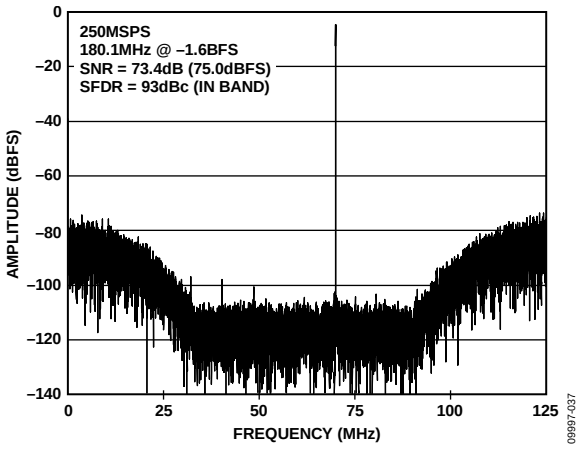


Figure 37. 22% Bandwidth Mode, Tuning Word = 28

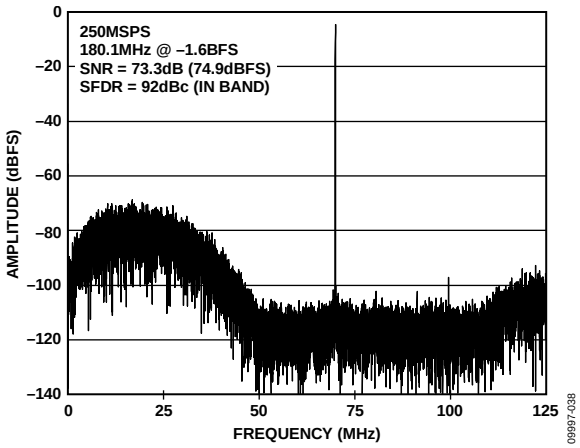


Figure 38. 22% Bandwidth Mode, Tuning Word = 41

33% BW NSR MODE (>82 MHZ BW AT 250 MSPS)

The second bandwidth mode offers excellent noise performance over 33% of the ADC sample rate (66% of the Nyquist band) and can be centered by setting the NSR mode bits in the NSR control register (Address 0x3C) to 001. In this mode, the useful frequency range can be set using the 6-bit tuning word (TW) in the NSR tuning register (Address 0x3E). There are 34 possible tuning words; each step is 0.5% of the ADC sample rate. The following three equations describe the left band edge (f_0), the channel center (f_{CENTER}), and the right band edge (f_1), respectively:

$$f_0 = f_{ADC} \times 0.005 \times TW$$

$$f_{CENTER} = f_0 + 0.165 \times f_{ADC}$$

$$f_1 = f_0 + 0.33 \times f_{ADC}$$

Figure 39 to Figure 41 show the typical spectrum that can be expected from the AD6672 with the 33% bandwidth NSR mode enabled for three filter settings.

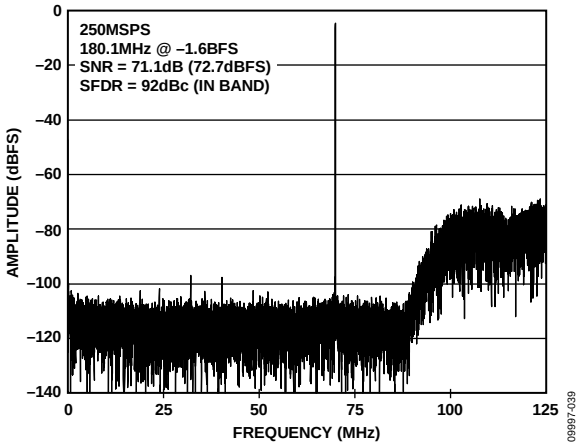


Figure 39. 33% Bandwidth Mode, Tuning Word = 5

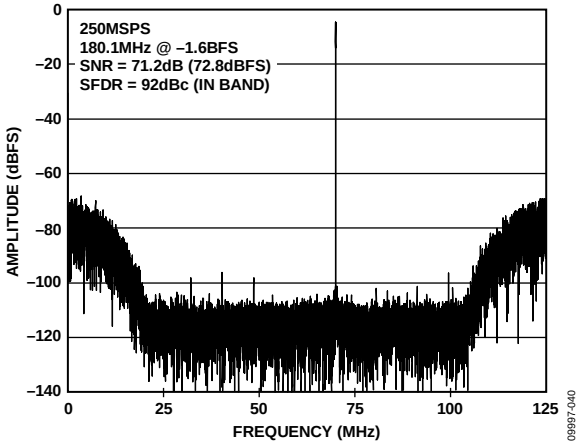


Figure 40. 33% Bandwidth Mode, Tuning Word = 17

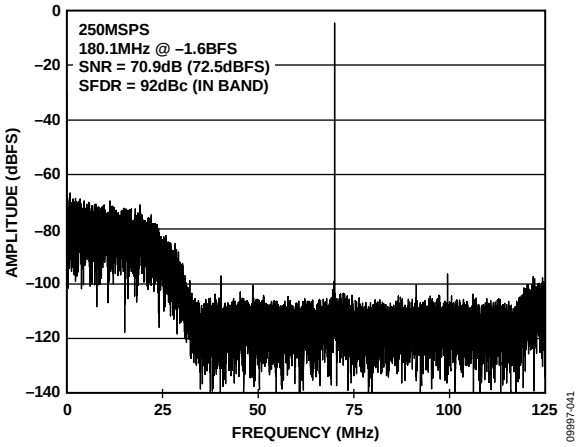


Figure 41. 33% Bandwidth Mode, Tuning Word = 27

SERIAL PORT INTERFACE (SPI)

The AD6672 serial port interface (SPI) allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI offers added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section. For detailed operational information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK pin, the SDIO pin, and the CSB pin (see Table 11). The SCLK (serial clock) pin is used to synchronize the read and write data presented from and to the ADC. The SDIO (serial data input/output) pin is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB (chip select bar) pin is an active low control that enables or disables the read and write cycles.

Table 11. Serial Port Interface Pins

Pin	Function
SCLK	Serial clock. The serial shift clock input, which is used to synchronize serial interface reads and writes.
SDIO	Serial data input/output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip select bar. An active low control that gates the read and write cycles.

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 42 and Table 5.

Other modes involving the CSB are available. The CSB can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB can stall high between bytes to allow for additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode. This mode turns on any SPI pin secondary functions.

During an instruction phase, a 16-bit instruction is transmitted. Data follows the instruction phase, and its length is determined by the W0 and W1 bits.

All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued. This allows the serial data input/output (SDIO) pin to change direction from an input to an output.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or in LSB first mode. MSB first mode is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

HARDWARE INTERFACE

The pins described in Table 11 comprise the physical interface between the user programming device and the serial port of the AD6672. The SCLK pin and the CSB pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD6672 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

SPI ACCESSIBLE FEATURES

Table 12 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. The AD6672 part-specific features are described in the Memory Map Register Description section.

Table 12. Features Accessible Using the SPI

Feature Name	Description
Mode	Allows the user to set either power-down mode or standby mode
Clock	Allows the user to access the DCS via the SPI
Offset	Allows the user to digitally adjust the converter offset
Test I/O	Allows the user to set test modes to have known data on output bits
Output Mode	Allows the user to set up outputs
Output Phase	Allows the user to set the output clock polarity
Output Delay	Allows the user to vary the DCO delay
VREF	Allows the user to set the reference voltage
Digital Processing	Allows the user to enable the synchronization features

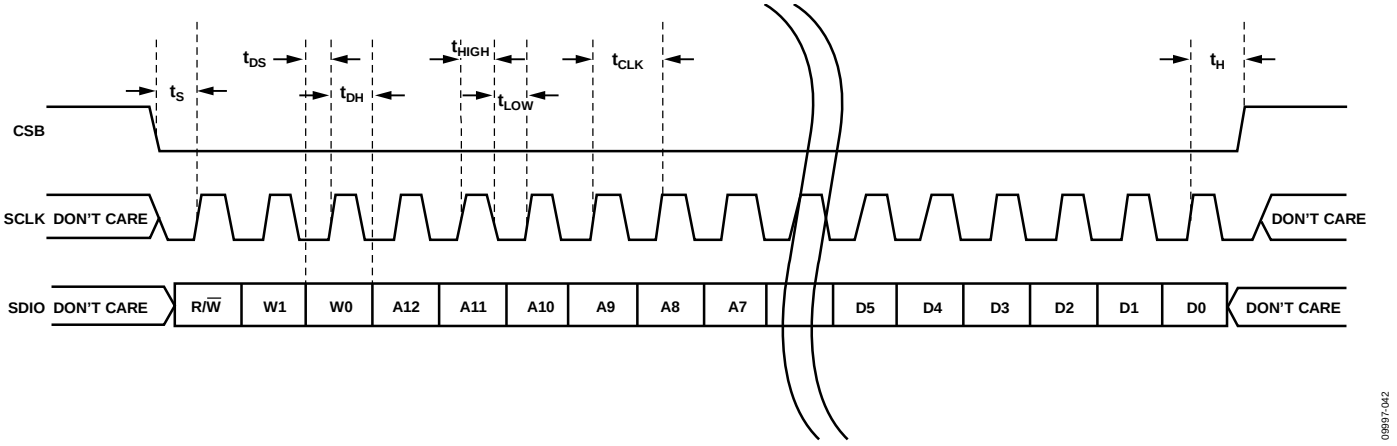


Figure 42. Serial Port Interface Timing Diagram

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is roughly divided into four sections: the chip configuration registers (Address 0x00 to Address 0x02); the transfer register (Address 0xFF); the ADC functions registers, including setup, control, and test (Address 0x08 to Address 0x20); and the digital feature control registers (Address 0x3C and Address 0x3E).

The memory map register table (Table 13) documents the default hexadecimal value for each hexadecimal address shown. The Bit 7 (MSB) column is the start of the default hexadecimal value given. For example, Address 0x14, the output mode register, has a hexadecimal default value of 0x01. This means that Bit 0 = 1 and the remaining bits are 0s. This setting is the default output format value, which is twos complement. For more information on this function and others, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. This document details the functions controlled by Register 0x00 to Register 0x20. The remaining registers, Register 0x3C and Register 0x3E, are documented in the Memory Map Register Description section.

Open Locations

All address and bit locations that are not included in Table 13 are not currently supported for this device. Write 0s to unused bits of a valid address location. Writing to these locations is required only when part of an address location is open (for example, Address 0x18). If the entire address location is open (for example, Address 0x13), this address location should not be written.

Default Values

After the AD6672 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table (Table 13).

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

Transfer Register Map

Address 0x08 to Address 0x20, as well as Address 0x3C and Address 0x3E, are shadowed. Writes to these addresses do not affect part operation until a transfer command is issued by writing 0x01 to Address 0xFF, setting the transfer bit. This allows these registers to be updated internally and simultaneously when the transfer bit is set. The internal update takes place when the transfer bit is set, and then the bit autoclears.

MEMORY MAP REGISTER TABLE

All address and bit locations that are not included in Table 13 are not currently supported for this device.

Table 13. Memory Map Registers

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
Chip Configuration Registers											
0x00	SPI port configuration	0	LSB first	Soft reset	1	1	Soft reset	LSB first	0	0x18	Nibbles are mirrored so that LSB first mode or MSB first mode is set correctly, regardless of shift mode.
0x01	Chip ID	8-bit chip ID[7:0] (AD6672 = 0xA4) (default)								0xA4	Read only.
0x02	Chip grade	Open	Open	Speed grade ID 00 = 250 MSPS		Open	Open	Open	Open		Speed grade ID used to differentiate devices; read only.
Transfer Register											
0xFF	Transfer	Open	Open	Open	Open	Open	Open	Open	Transfer	0x00	Synchronously transfers data from the master shift register to the slave.
ADC Functions Registers											
0x08	Power modes	Open	Open	Open	Open	Open	Open	Internal power-down mode 00 = normal operation 01 = full power-down 10 = standby 11 = reserved		0x00	Determines various generic modes of chip operation.
0x09	Global clock	Open	Open	Open	Open	Open	Open	Open	Duty cycle stabilizer (default)	0x01	
0x0B	Clock divide	Open	Open	Input clock divider phase adjust 000 = no delay 001 = 1 input clock cycle 010 = 2 input clock cycles 011 = 3 input clock cycles 100 = 4 input clock cycles 101 = 5 input clock cycles 110 = 6 input clock cycles 111 = 7 input clock cycles			Clock divide ratio 000 = divide by 1 001 = divide by 2 010 = divide by 3 011 = divide by 4 100 = divide by 5 101 = divide by 6 110 = divide by 7 111 = divide by 8			0x00	Clock divide values other than 000 automatically cause the duty cycle stabilizer to become active.
0x0D	Test mode	User test mode control 0 = continuous/ repeat pattern 1 = single pattern, then 0s	Open	Reset PN long gen	Reset PN short gen	Output test mode 0000 = off (default) 0001 = midscale short 0010 = positive FS 0011 = negative FS 0100 = alternating checkerboard 0101 = PN long sequence 0110 = PN short sequence 0111 = one/zero word toggle 1000 = user test mode 1001 to 1110 = unused 1111 = ramp output				0x00	When this register is set, the test data is placed on the output pins in place of normal data.
0x10	Offset adjust	Open	Open	Offset adjust in LSBs from +31 to −32 (twos complement format)						0x00	

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
0x14	Output mode	Open	Open	Open	Output enable bar 0 = on 1 = off	Open	Output invert 0 = normal (default) 1 = inverted	Output format 00 = offset binary 01 = twos complement (default) 10 = gray code 11 = reserved		0x01	Configures the outputs and the format of the data.
0x15	Output adjust	Open	Open	Open	Open	LVDS output drive current adjust 0000 = 3.72 mA output drive current 0001 = 3.5 mA output drive current (default) 0010 = 3.30 mA output drive current 0011 = 2.96 mA output drive current 0100 = 2.82 mA output drive current 0101 = 2.57 mA output drive current 0110 = 2.27 mA output drive current 0111 = 2.0 mA output drive current (reduced range) 1000 to 1111 = reserved				0x01	
0x16	Clock phase control	Invert DCO clock	Open	Open	Open	Open	Open	Open	Open	0x00	
0x17	DCO output delay	Enable DCO clock delay	Open	Open	DCO clock delay [delay = (3100 ps × register value/31 +100)] 00000 = 100 ps 00001 = 200 ps 00010 = 300 ps … 11110 = 3100 ps 11111 = 3200 ps					0x00	
0x18	Input span select	Open	Open	Open	Full-scale input voltage selection 01111 = 2.087 V p-p … 00001 = 1.772 V p-p 00000 = 1.75 V p-p (default) 11111 = 1.727 V p-p … 10000 = 1.383 V p-p					0x00	Full-scale input adjustment in 0.022 V steps.
0x19	User Test Pattern 1 LSB	User Test Pattern 1[7:0]								0x00	
0x1A	User Test Pattern 1 MSB	User Test Pattern 1[15:8]								0x00	
0x1B	User Test Pattern 2 LSB	User Test Pattern 2[7:0]								0x00	
0x1C	User Test Pattern 2 MSB	User Test Pattern 2[15:8]								0x00	
0x1D	User Test Pattern 3 LSB	User Test Pattern 3[7:0]								0x00	
0x1E	User Test Pattern 3 MSB	User Test Pattern 3[15:8]								0x00	
0x1F	User Test Pattern 4 LSB	User Test Pattern 4[7:0]								0x00	
0x20	User Test Pattern 4 MSB	User Test Pattern 4[15:8]								0x00	
Digital Feature Control Registers											
0x3C	NSR control	Open	Open	Open	Open	NSR mode 000 = 22% bandwidth mode 001 = 33% bandwidth mode			NSR enable 0 = off 1 = on	0x00	NSR controls.
0x3E	NSR tuning word	Open	Open	NSR tuning word (see the Noise Shaping Requantizer section; equations for the tuning word are dependent on the NSR mode)						0x1C	NSR frequency tuning word.

MEMORY MAP REGISTER DESCRIPTION

For more information on functions controlled in Register 0x00 to Register 0x20, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

NSR Control (Register 0x3C)

Bits[7:4]—Reserved

Bits[3:1]—NSR Mode

Bits[3:1] determine the bandwidth mode of the NSR. When Bits[3:1] are set to 000, the NSR is configured for 22% bandwidth mode, which provides enhanced SNR performance over 22% of the sample rate. When Bits[3:1] are set to 001, the NSR is configured for 33% bandwidth mode, which provides enhanced SNR performance over 33% of the sample rate.

Bit 0—NSR Enable

The NSR is enabled when Bit 0 is high and disabled when Bit 0 is low.

NSR Tuning Word (Register 0x3E)

Bits[7:6]—Reserved

Bits[5:0]—NSR Tuning Word

The NSR tuning word sets the band edges of the NSR band. In 22% bandwidth mode, there are 57 possible tuning words; in 33% bandwidth mode, there are 34 possible tuning words. In either mode, each step represents 0.5% of the ADC sample rate. For the equations that are used to calculate the tuning word based on the bandwidth mode of operation, see the Noise Shaping Requantizer section.

APPLICATIONS INFORMATION

DESIGN GUIDELINES

Before starting system level design and layout of the AD6672, it is recommended that the designer become familiar with these guidelines, which discuss the special circuit connections and layout requirements for certain pins.

Power and Ground Recommendations

When connecting power to the AD6672, it is recommended that two separate 1.8 V supplies be used: use one supply for analog (AVDD) and a separate supply for the digital outputs (DRVDD). The designer can employ several different decoupling capacitors to cover both high and low frequencies. Locate these capacitors close to the point of entry at the PC board level and close to the pins of the part with minimal trace length.

A single PCB ground plane should be sufficient when using the AD6672. With proper decoupling and smart partitioning of the PCB analog, digital, and clock sections, optimum performance can be easily achieved.

Exposed Paddle Thermal Heat Slug Recommendations

It is mandatory that the exposed paddle on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance. A continuous, exposed (no solder mask) copper plane on the PCB should mate to the AD6672 exposed paddle, Pin 0.

The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be filled or plugged with nonconductive epoxy.

To maximize the coverage and adhesion between the ADC and the PCB, overlay a silkscreen to partition the continuous plane on the PCB into several uniform sections. This provides several tie points between the ADC and the PCB during the reflow process. Using one continuous plane with no partitions guarantees only one tie point between the ADC and the PCB. See the evaluation board for a PCB layout example. For detailed information about the packaging and PCB layout of chip scale packages, refer to the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

VCM

Decouple the VCM pin to ground with a 0.1 µF capacitor, as shown in Figure 26.

SPI Port

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK, CSB, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD6672 to keep these signals from transitioning at the converter input pins during critical sampling periods.

OUTLINE DIMENSIONS

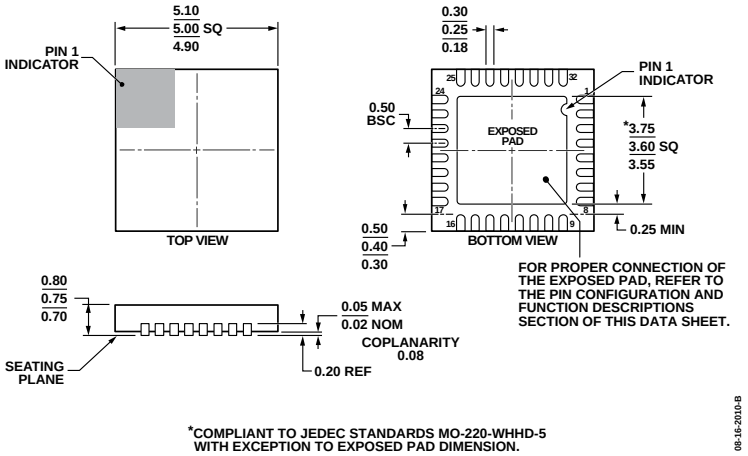


Figure 43. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD6672BCPZ-250	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
AD6672BCPZRL7-250	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
AD6672-250EBZ	−40°C to +85°C	Evaluation Board with AD6672 and Software	

[1] Z = RoHS Compliant Part.

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