AD6650 Diversity IF-to-Baseband GSM/EDGE Narrow-Band Receiver

AD6650

FEATURES

116 dB dynamic range
Digital VGA
I/Q demodulators
Active low-pass filters
Dual wideband ADC
Programmable decimation and channel filters
VCO and phase-locked loop circuitry
Serial data output ports
Intermediate frequencies of 70 MHz to 260 MHz
10 dB noise figure
+43 dBm input IP2 at 70 MHz IF
–9.5 dBm input IP3 at 70 MHz IF
3.3 V I/O and CMOS core
Microprocessor interface
JTAG boundary scan

APPLICATIONS

PHS or GSM/EDGE single carrier, diversity receivers
Microcell and picocell systems
Wireless local loop
Smart antenna systems
Software radios
In-building wireless telephony

PRODUCT DESCRIPTION

The AD6650 is a diversity intermediate frequency-to-baseband (IF-to-baseband) receiver for GSM/EDGE. This narrow-band receiver consists of an integrated DVGA, IF-to-baseband I/Q demodulators, low-pass filtering, and a dual wideband ADC. The chip can accommodate IF input from 70 MHz to 260 MHz. The receiver architecture is designed such that only one external surface acoustic wave (SAW) filter for main and one for diversity are required in the entire receive signal path to meet GSM/EDGE blocking requirements.

Digital decimation and filtering circuitry provided on-chip remove unwanted signals and noise outside the channel of interest. Programmable RAM coefficient filters allow antialiasing, matched filtering, and static equalization functions to be combined in a single cost-effective filter. The output of the channel filters is provided to the user via serial output I/Q data streams.

FUNCTIONAL BLOCK DIAGRAM

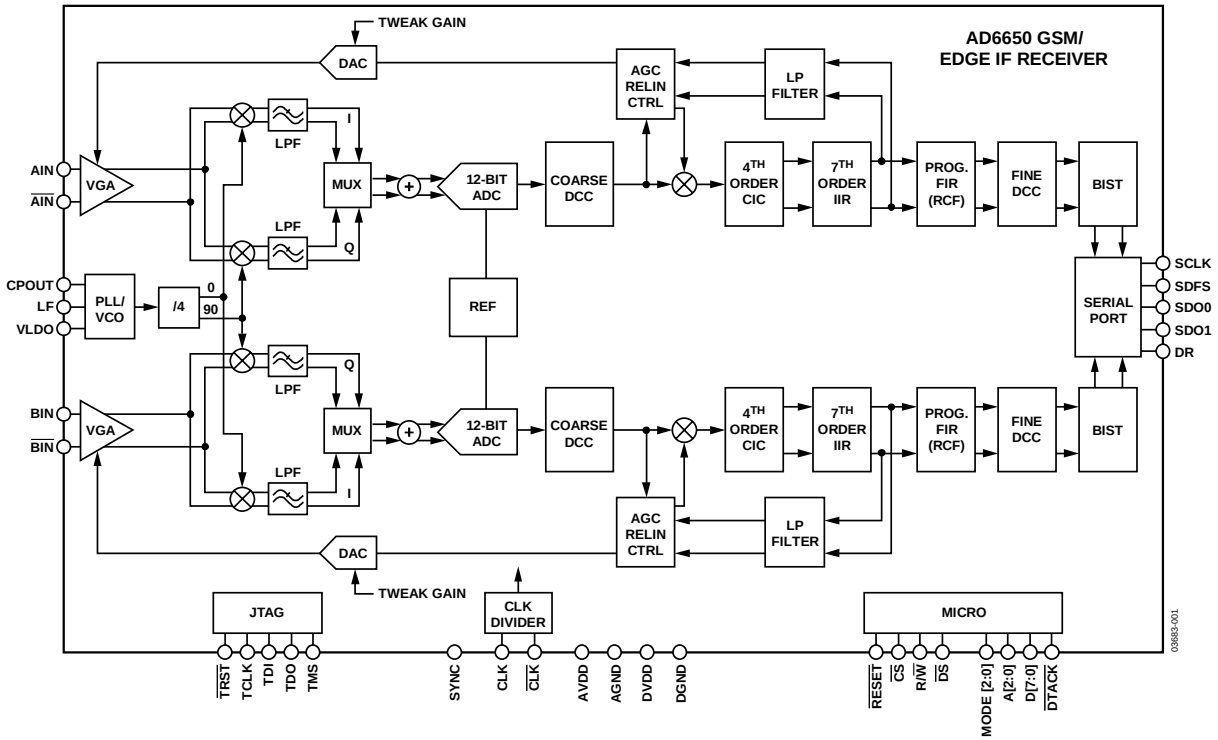


Figure 1.

Rev. A
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REVISION HISTORY

1/07—Rev. 0 to Rev. A

Updated Format ... Universal
Changes to Specifications ... 3
Changes to Figure 18 ... 13
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3/06—Revision 0: Initial Version

SPECIFICATIONS

EXPLANATION OF TEST LEVELS

I. 100% production tested.
II. 100% production tested at 25°C; sample tested at specified temperatures.
III. Sample tested only.
IV. Parameter guaranteed by design and analysis.
V. Parameter is typical value only.
VI. 100% production tested at 25°C; sample tested at temperature extreme.
VII. 100% production tested at +85°C.

C_{LOAD} = 40 pF on all outputs, unless otherwise specified. All timing specifications valid over VDD range of 3.0 V to 3.45 V and VDDIO range of 3.0 V to 3.45 V.

AC SPECIFICATIONS

AVDD and DVDD = 3.3 V, CLK = 52 MSPS (driven differentially), 50% duty cycle, unless otherwise noted. All minimum ac specifications are guaranteed from −25°C to +85°C. AC minimum specifications degrade slightly from −25°C to −40°C.

Table 1.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
OVERALL FUNCTION						
Frequency Range	Full	V	70		260	MHz
GAIN CONTROL						
Gain Step Size	25°C	V		0.094		dB
Gain Step Accuracy	25°C	V		±0.047		dB
AGC Range	25°C	V		36		dB
BASEBAND FILTERS						
Bandwidth	Full	IV	3.36	3.5	3.64	MHz
Alias Rejection at 25.9 MHz	25°C	V		77		dB
LO PHASE NOISE						
At 10 kHz Offset	25°C	V		−79		dBc/Hz
At 20 kHz Offset	25°C	V		−87		dBc/Hz
At 50 kHz Offset	25°C	V		−103		dBc/Hz
At 100 kHz Offset	25°C	V		−112		dBc/Hz
At 200 kHz Offset	25°C	V		−119		dBc/Hz
At 400 kHz Offset	25°C	V		−125		dBc/Hz
At 600 kHz Offset	25°C	V		−130		dBc/Hz
At 800 kHz Offset	25°C	V		−133		dBc/Hz
At 1600 kHz Offset	25°C	V		−138		dBc/Hz
At 3000 kHz Offset	25°C	V		−143		dBc/Hz
GAIN ERROR	25°C	V		−0.7		dB
PSRR (AVDD with 20 mV RMS Ripple)[1]						
At 5 kHz	25°C	V		−13.4		dBc
At 10 kHz	25°C	V		−17		dBc
At 50 kHz	25°C	V		−34		dBc
At 100 kHz	25°C	V		−39.8		dBc
At 150 kHz	25°C	V		−45.7		dBc
f = 70 MHz						
Coarse DC Correction		V		−70		dB
Noise Figure[2]		V		10		dB
Input IP2[2]	Full	IV	24	43		dBm
Input IP3[2]	Full	IV	−15	−9.5		dBm
Image Rejection	Full	IV		−49	−33	dBc
Full-Scale Input Power		V		4		dBm
Input Impedance		V		189.6 – j33.6		Ω

Parameter	Temp	Test Level	Min	Typ	Max	Unit
f = 150 MHz						
Coarse DC Correction		V		−70		dB
Noise Figure[2]		V		10		dB
Input IP2[2]	Full	IV	24	37		dBm
Input IP3[2]	Full	IV	−15	−11.5		dBm
Image Rejection	Full	IV		−46.5	−33	dBc
Full-Scale Input Power		V		4		dBm
Input Impedance		V		169.3 – j59.2		Ω
f = 200 MHz						
Coarse DC Correction		V		−70		dB
Noise Figure[2]		V		10		dB
Input IP2[2]	Full	IV	24	35		dBm
Input IP3[2]	Full	IV	−16	−12		dBm
Image Rejection	Full	IV		−46.5	−33	dBc
Full-Scale Input Power		V		4		dBm
Input Impedance		V		159.3 – j66.9		Ω
f = 250 MHz						
Coarse DC Correction		V		−70		dB
Noise Figure[2]		V		10		dB
Input IP2[2]	Full	VII	24	33		dBm
Input IP3[2]	Full	VII	−16	−13		dBm
Image Rejection	Full	VII		−45	−33	dBc
Full-Scale Input Power		V		4		dBm
Input Impedance		V		137.1 – j72.7		Ω

[1] See Figure 40 and Figure 41 for additional PSRR specifications.
[2] This measurement applies for maximum gain (36 dB).

DIGITAL SPECIFICATIONS

AVDD and DVDD = 3.3 V, CLK = 52 MSPS, unless otherwise noted.

Table 2.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
DVDD	Full	IV	3.0	3.3	3.45	V
AVDD	Full	IV	3.0	3.3	3.45	V
$T_{AMBIENT}$[1]		IV	−25	+25	+85	°C

[1] The AD6650 is guaranteed fully functional from −40°C to +85°C. All ac minimum specifications are guaranteed from −25°C to +85°C, but degrade slightly from −25°C to −40°C.

ELECTRICAL CHARACTERISTICS

Table 3.

Parameter (Conditions)	Temp	Test Level	Min	Typ	Max	Unit
LOGIC INPUTS						
Logic Compatibility	Full	IV		3.3 V CMOS		
Digital Logic						
Logic 1 Voltage	Full	IV	2.0		VDD	V
Logic 0 Voltage	Full	IV	0		0.8	V
Logic 1 Current	25°C	V		60		µA
Logic 0 Current	25°C	V		7		µA
Input Capacitance	25°C	V		5		pF
CLOCK INPUTS						
Differential Input Voltage[1]	25°C	V	0.4		3.6	V p-p
Common-Mode Input Voltage	25°C	V		DVDD/2		V
Differential Input Resistance	25°C	V		7.5		kΩ
Differential Input Capacitance	25°C	V		5		pF
LOGIC OUTPUTS						
Logic Compatibility	Full			3.3 V CMOS/TTL		
Logic 1 Voltage (I_{OH} = 0.25 mA)	Full	IV	2.4	VDD − 0.2		V
Logic 0 Voltage (I_{OL} = 0.25 mA)	Full	IV		0.2	0.8	V
IDD SUPPLY CURRENT						
CLK = 52 MHz (GSM Example)						
I_{DVDD}	Full	VII		155		mA
I_{AVDD}	Full	VII		360		mA
POWER DISSIPATION						
CLK = 52 MHz (GSM/EDGE Example)	Full	VII		1.7	2.1	W

[1] All ac specifications are tested by driving CLK and $\overline{CLK}$ differentially.

GENERAL TIMING CHARACTERISTICS

Table 4.

Parameter (Conditions)	Symbol	Temp	Test Level	Min	Typ	Max	Unit
CLK TIMING REQUIREMENTS							
CLK Period[1]	t_{CLK}	Full	I	9.6		19.2	ns
CLK Width Low	t_{CLKL}	Full	IV		0.5 × t_{CLK}		ns
CLK Width High	t_{CLKH}	Full	IV		0.5 × t_{CLK}		ns
$\overline{RESET}$ TIMING REQUIREMENTS							
$\overline{RESET}$ Width Low	t_{SSF}	Full	IV	30			ns
PIN_SYNC TIMING REQUIREMENTS							
SYNC to ↑ CLK Setup Time	t_{SS}	Full	IV	−3			ns
SYNC to ↑ CLK Hold Time	t_{HS}	Full	IV	6			ns
SERIAL PORT TIMING REQUIREMENTS: SWITCHING CHARACTERISTICS[2]							
↑ CLK to ↑ SCLK Delay (Divide-by-1)	t_{DSCLK1}	Full	IV	3.2		12.5	ns
↑ CLK to ↑ SCLK Delay (For Any Other Divisor)	t_{DSCLKH}	Full	IV	4.4		16	ns
↑ CLK to ↓ SCLK Delay (Divide-by-2 or Even Number)	t_{DSCLKL}	Full	IV	4.7		16	ns
↓ CLK to ↓ SCLK Delay (Divide-by-3 or Odd Number)	$t_{DSCLKLL}$	Full	IV	4		14	ns
↑ SCLK to SDFS Delay	t_{DSDFS}	Full	IV	1		2.6	ns
↑ SCLK to SDO0 Delay	t_{DSDO0}	Full	IV	0.5		3.5	ns
↑ SCLK to SDO1 Delay	t_{DSDO1}	Full	IV	0.5		3.5	ns
↑ SCLK to DR Delay	t_{DSDR}	Full	IV	1		3.5	ns

[1] Minimum specification is based on a 104 MSPS clock rate (an internal divide-by-2 must be used with a 104 MSPS clock rate); maximum specification is based on a 52 MSPS clock rate. This device is optimized to operate at a clock rate of 52 MSPS or 104 MSPS.
[2] The timing parameters for SCLK, SDFS, SDO0, SDO1, and DR apply to both Channel 0 and Channel 1.

MICROPROCESSOR PORT TIMING CHARACTERISTICS

All timing specifications valid over VDD range of 3.0 V to 3.45 V and VDDIO range of 3.0 V to 3.45 V.

Table 5. Microprocessor Port, Mode INM (MODE = 0); Asynchronous Operation

Parameter	Symbol	Temp	Test Level	Min	Typ	Max	Unit
WRITE TIMING							
$\overline{WR}$ (R/$\overline{W}$) to RDY ($\overline{DTACK}$) Hold Time[1]	t_{HWR}	Full	IV	0.0			ns
Address/Data to $\overline{WR}$ (R/$\overline{W}$) Setup Time[1]	t_{SAM}	Full	IV	0.0			ns
Address/Data to RDY ($\overline{DTACK}$) Hold Time[1]	t_{HAM}	Full	IV	0.0			ns
$\overline{WR}$ (R/$\overline{W}$) to RDY ($\overline{DTACK}$) Delay	t_{DRDY}[2]	Full	IV	9.0		15.0	ns
$\overline{WR}$ (R/$\overline{W}$) to RDY ($\overline{DTACK}$) High Delay[1]	t_{ACC}	Full	IV	$4 \times t_{CLK}$		$13 \times t_{CLK}$	ns
READ TIMING							
Address to $\overline{RD}$ ($\overline{DS}$) Setup Time[1]	t_{SAM}	Full	IV	0.0			ns
Address to Data Hold Time[1]	t_{HAM}	Full	IV	0.0			ns
Data Three-state Delay[1]	t_{ZD}	Full	V		12		ns
RDY ($\overline{DTACK}$) to Data Delay[1]	t_{DD}	Full	IV			0.0	ns
$\overline{RD}$ ($\overline{DS}$) to RDY ($\overline{DTACK}$) Delay	t_{DRDY}[2]	Full	IV	9.0		15.0	ns
$\overline{RD}$ ($\overline{DS}$) to RDY ($\overline{DTACK}$) High Delay[1]	t_{ACC}	Full	IV	$4 \times t_{CLK}$		$13 \times t_{CLK}$	ns

[1] Timing is guaranteed by design.
[2] Specification pertains to control signals R/$\overline{W}$, $\overline{WR}$, $\overline{DS}$, $\overline{RD}$, and $\overline{CS}$ such that the minimum specification is valid after the last control signal has reached a valid logic level.

Table 6. Microprocessor Port, Mode MNM (MODE = 1)

Parameter	Symbol	Temp	Test Level	Min	Typ	Max	Unit
WRITE TIMING							
$\overline{DS}$ ($\overline{RD}$) to $\overline{DTACK}$ (RDY) Hold Time	t_{HDS}	Full	IV	15.0			ns
R/$\overline{W}$ ($\overline{WR}$) to $\overline{DTACK}$ (RDY) Hold Time	t_{HRW}	Full	IV	15.0			ns
Address/Data to R/$\overline{W}$ ($\overline{WR}$) Setup Time[1]	t_{SAM}	Full	IV	0.0			ns
Address/Data to R/$\overline{W}$ ($\overline{WR}$) Hold Time[1]	t_{HAM}	Full	IV	0.0			ns
$\overline{DS}$ ($\overline{RD}$) to $\overline{DTACK}$ (RDY) Delay[2]	t_{DDTACK}	Full	V		16		ns
R/$\overline{W}$ ($\overline{WR}$) to $\overline{DTACK}$ (RDY) Low Delay[1]	t_{ACC}	Full	IV	$4 \times t_{CLK}$		$13 \times t_{CLK}$	ns
READ TIMING							
$\overline{DS}$ ($\overline{RD}$) to $\overline{DTACK}$ (RDY) Hold Time	t_{HDS}	Full	IV	15.0			ns
Address to $\overline{DS}$ ($\overline{RD}$) Setup Time[1]	t_{SAM}	Full	IV	0.0			ns
Address to Data Hold Time[1]	t_{HAM}	Full	IV	0.0			ns
Data Three-State Delay	t_{ZD}	Full	V		13		ns
$\overline{DTACK}$ (RDY) to Data Delay[1]	t_{DD}	Full	IV			0.0	ns
$\overline{DS}$ ($\overline{RD}$) to $\overline{DTACK}$ (RDY) Delay[2]	t_{DDTACK}	Full	V		16		ns
$\overline{DS}$ ($\overline{RD}$) to $\overline{DTACK}$ (RDY) Low Delay[1]	t_{ACC}	Full	IV	$4 \times t_{CLK}$		$13 \times t_{CLK}$	ns

[1] Timing is guaranteed by design.
[2] $\overline{DTACK}$ is an open-drain device and must be pulled up with a 1 kΩ resistor.

TIMING DIAGRAMS



Figure 2. $\overline{RESET}$ Timing Requirements

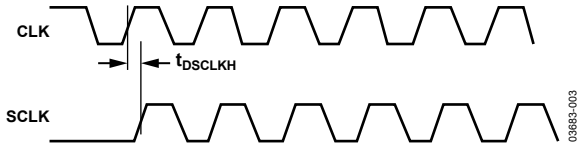


Figure 3. SCLK Switching Characteristics (Divide-by-1)

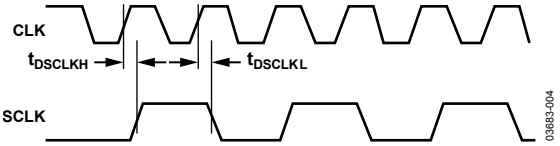


Figure 4. SCLK Switching Characteristics (Divide-by-2 or Even Integer)

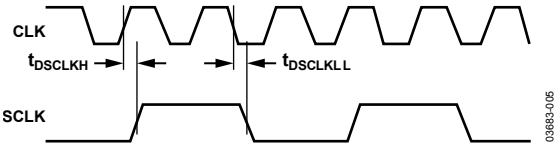


Figure 5. SCLK Switching Characteristics (Divide-by-3 or Odd Integer)

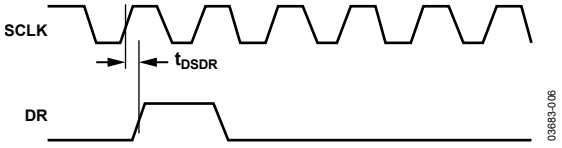


Figure 6. SCLK, DR Switching Characteristics

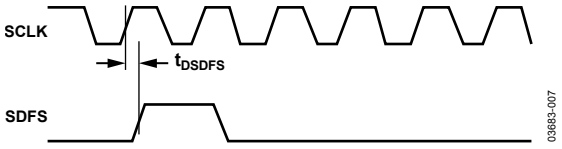


Figure 7. SCLK, SDFS Switching Characteristics

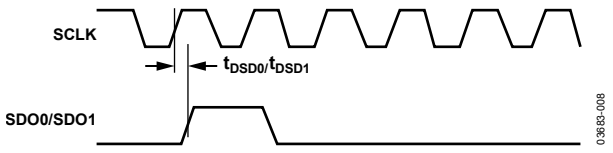


Figure 8. SCLK, SDO0/SDO1 Switching Characteristics

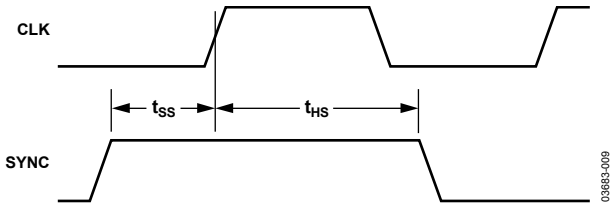
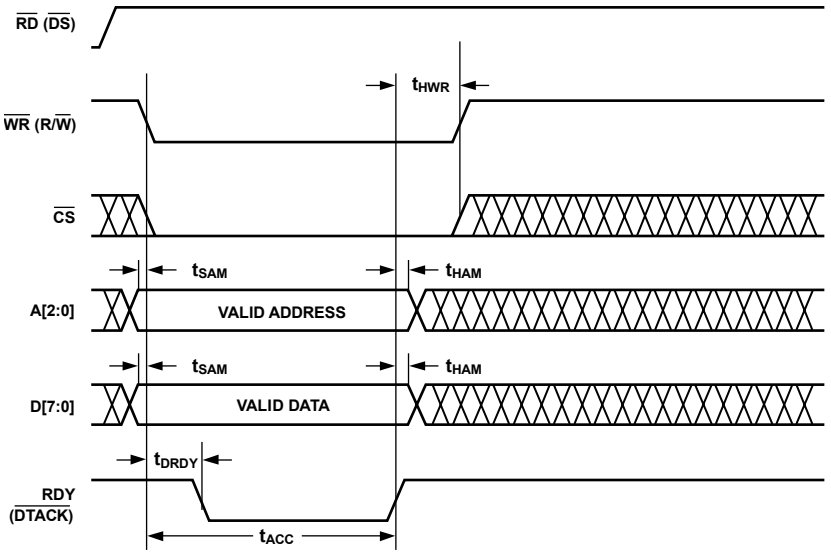


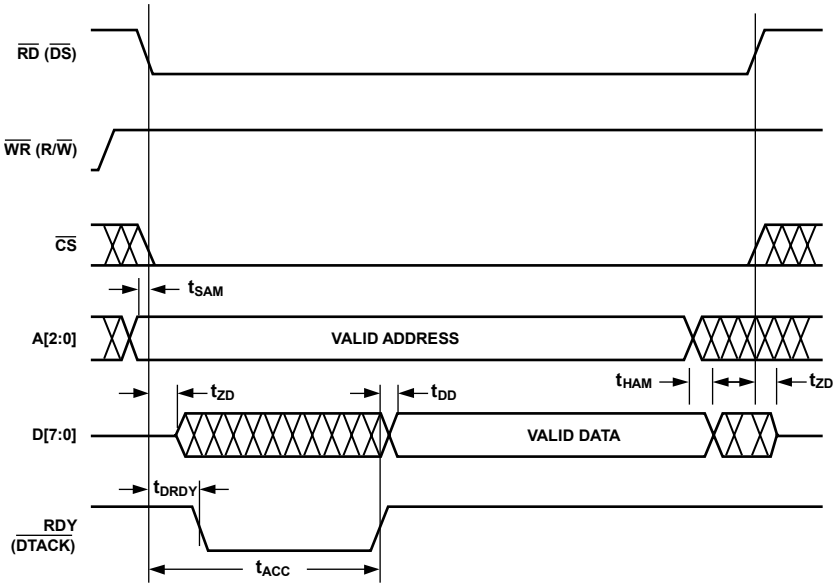
Figure 9. SYNC Timing Inputs



NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FALLING EDGE OF WR TO RISING EDGE OF RDY.
2. t_{ACC} REQUIRES A MAXIMUM OF NINE CLK PERIODS.

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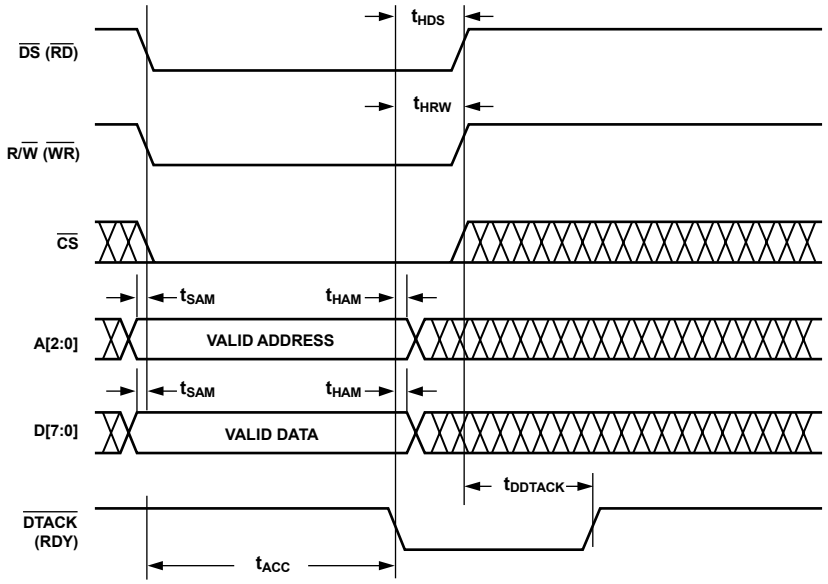
Figure 10. INM Microport Write Timing Requirements



NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FALLING EDGE OF RD TO RISING EDGE OF RDY.
2. t_{ACC} REQUIRES A MAXIMUM OF 13 CLK PERIODS.

03683-011

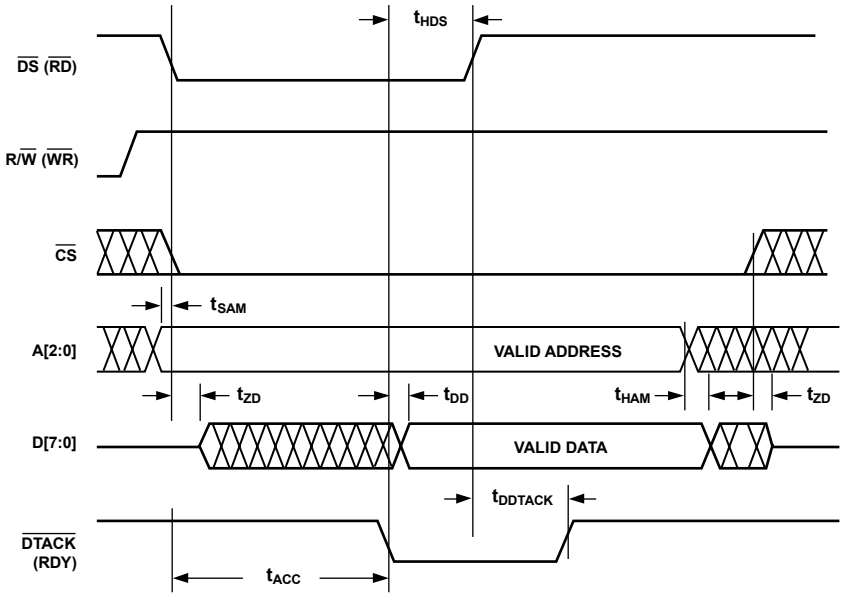
Figure 11. INM Microport Read Timing Requirements



NOTES

1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FALLING EDGE OF $\overline{DS}$ TO FALLING EDGE OF $\overline{DTACK}$.
2. t_{ACC} REQUIRES A MAXIMUM OF NINE CLK PERIODS.

Figure 12. MNM Microport Write Timing Requirements



NOTES

1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FALLING EDGE OF DS TO THE FALLING EDGE OF DTACK.
2. t_{ACC} REQUIRES A MAXIMUM OF 13 CLK PERIODS.

Figure 13. MNM Microport Read Timing Requirements

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Supply Voltage	−0.3 V to +3.6 V
Input Voltage	−0.3 V to +3.6 V
Output Voltage Swing	−0.3 V to VDDIO + 0.3 V
Load Capacitance	200 pF
Junction Temperature Under Bias	125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (5 sec)	280°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

121-lead chip scale package ball grid array:

θ_{JA} = 22.8°C/W, no airflow, measurements made in the horizontal position on a 4-layer board.

θ_{JA} = 20.2°C/W, 200 LFPM airflow, measurements made in the horizontal position on a 4-layer board.

θ_{JA} = 20.7°C/W, no airflow, soldered on an 8-layer board with two layers dedicated as ground planes.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

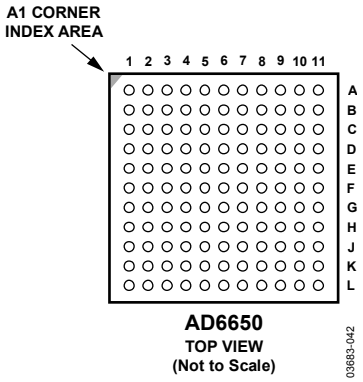


Figure 14. Pin Configuration

Table 8. Pin Configuration

	1	2	3	4	5	6	7	8	9	10	11	
A	DGND	TDI	TMS	$\overline{\text{TRST}}$	$\overline{\text{RESET}}$	DNC	AVDD	CLK	$\overline{\text{CLK}}$	AGND	AGND	**A**
B	SDFS	SCLK	TDO	TCLK	SYNC	DNC	AVDD	AVDD	AGND	AGND	$\overline{\text{BIN}}$	**B**
C	SDO1	SDO0	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AGND	AGND	BIN	**C**
D	D7	DR	DVDD	DGND	DGND	DGND	AVDD	AVDD	AGND	AGND	AGND	**D**
E	D5	D6	DVDD	DGND	DGND	DGND	AVDD	AVDD	AGND	AGND	LF	**E**
F	D3	D4	DVDD	DGND	DGND	DGND	AVDD	AVDD	AGND	DNC	VLDO	**F**
G	D1	D2	DVDD	DGND	DGND	DGND	AVDD	AVDD	AGND	AGND	CPOUT	**G**
H	$\overline{\text{DS}}$ ($\overline{\text{RD}}$)	D0	DVDD	DGND	DGND	DGND	AVDD	AVDD	AGND	AGND	AGND	**H**
J	R/$\overline{\text{W}}$ ($\overline{\text{WR}}$)	$\overline{\text{DTACK}}$ (RDY)	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AGND	AGND	AIN	**J**
K	A2	A1	$\overline{\text{CS}}$	MODE1	CHIP_ID1	DNC	AVDD	REFGND	REFT	AGND	$\overline{\text{AIN}}$	**K**
L	DGND	A0	MODE2	MODE0	CHIP_ID0	DNC	AVDD	VREF	REFB	AGND	AGND	**L**
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	

Table 9. Pin Function Descriptions

Mnemonic	Type	Description	No. of Pins
POWER SUPPLY			
DVDD	Power	3.3 V Digital Supply.	13
AVDD	Power	3.3 V Analog Supply.	19
DGND	Ground	Digital Ground.	17
AGND	Ground	Analog Ground.	22
DIGITAL INPUTS			
$\overline{\text{RESET}}$	Input	Active Low Reset Pin.	1
SYNC	Input	Synchronizes Digital Filters.	1
CHIP_ID[1:0]	Input	Chip ID.	2
SERIAL DATA PORT			
SCLK	Bidirectional	Serial Clock.	1
SDFS	Bidirectional	Serial Data Frame Sync.	1
SDO[1:0]	Output	Serial Data Outputs. Three-stated when inactive.	2
DR	Output	Output Data Ready Indicator.	1
MICROPORTCONTROL			
D[7:0]	Bidirectional	Microport Data.	8
A[2:0]	Input	Microport Address Bits.	3
$\overline{\text{CS}}$	Input	Chip Select.	1
$\overline{\text{DS}}$ ($\overline{\text{RD}}$)	Input	Active Low Data Strobe (Active Low Read).	1

Mnemonic	Type	Description	No. of Pins
$\overline{\text{DTACK}}$ (RDY)	Output	Active Low Data Acknowledge (Microport Status Bit). Open-drain output, requires external pull-up resistor of 1 kΩ.	1
R/$\overline{\text{W}}$ ($\overline{\text{WR}}$)	Input	Read Write (Active Low Write).	1
MODE [2:0]	Input	Selects Control Port Mode.	3
JTAG			
$\overline{\text{TRST}}$	Input	Test Reset Pin.	1
TCLK	Input	Test Clock Input.	1
TMS	Input	Test Mode Select Input.	1
TDO	Output	Test Data Output. Three-stated when JTAG is in reset.	1
TDI	Input	Test Data input.	1
ANALOG INPUTS			
AIN	Input	Main Analog Input.	1
$\overline{\text{AIN}}$	Input	Complement of AIN. Differential analog input.	1
BIN	Input	Diversity Analog Input.	1
$\overline{\text{BIN}}$	Input	Complement of BIN. Differential analog input.	1
PLL INPUTS			
CPOUT	Output	Charge-Pump Output.	1
LF	Input	Loop Filter.	1
VLDO	Output	Compensation for Internal Low Dropout Regulator. Bypass to ground with a 220 nF chip capacitor.	1
REFT	Output	Internal ADC Voltage Reference. Bypass to ground with capacitors. See Figure 39 for recommended connection.	1
REFB	Output	Internal ADC Voltage Reference. Bypass to ground with capacitors. See Figure 39 for recommended connection.	1
VREF	Output	Internal ADC Voltage Reference. Bypass to ground with capacitors. See Figure 39 for recommended connection.	1
REFGND	Ground	ADC Ground Reference. See Figure 39 for recommended connection.	1
CLOCK INPUTS			
CLK	Input	Encode Input. Conversion initiated on rising edge.	1
$\overline{\text{CLK}}$	Input	Complement of Encode.	1
DNC		Do Not Connect.	5

TYPICAL PERFORMANCE CHARACTERISTICS

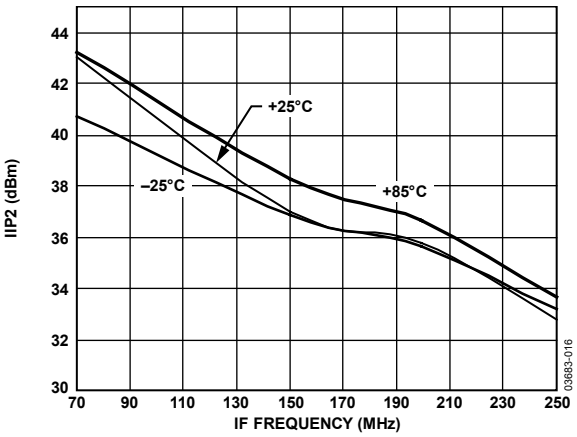


Figure 15. Input IP2 vs. Frequency

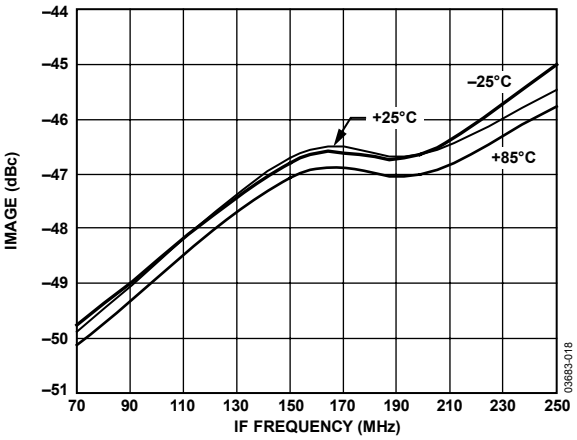


Figure 17. Image vs. Frequency

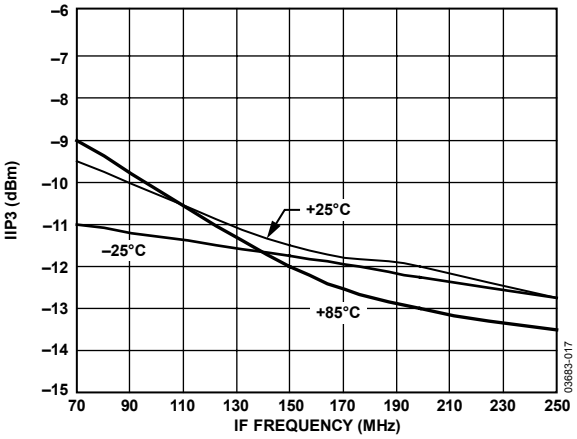


Figure 16. Input IP3 vs. Frequency

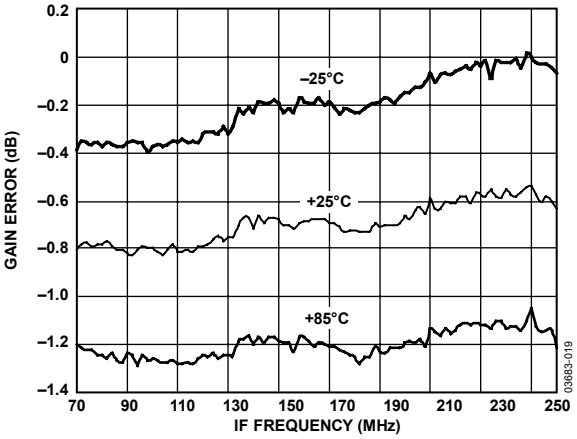


Figure 18. Gain Error vs. Frequency

TERMINOLOGY

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Noise Figure (NF)
The degradation in SNR performance (in dB) of an IF input signal after it passes through a component or system.

The AD6650 noise figure is determined by the equation

$$NF = \left(10 \log\left(\frac{V^2{}_{rms} / Z_{in}}{0.001} \right) - SNR_{FS} \right) - 10 \log\left(\frac{kTB}{0.001} \right) \quad (1)$$

where:

k is the Boltzmann constant = 1.38×10^{-23}.
T is the temperature in kelvin.
B is the channel bandwidth in hertz (200 kHz typical).
V^2_{rms} is the full-scale input voltage.
Z_{in} is the input impedance.
SNR_{FS} is the computed signal-to-noise ratio referred to full scale with a small input signal and the AD6650 in maximum gain.

Input Second-Order Intercept (IIP2)
A figure of merit used to determine a component's or system's susceptibility to intermodulation distortion (IMD) from its second-order nonlinearities. Two unmodulated carriers at a specified frequency relationship (f1 and f2) are injected into a nonlinear system exhibiting second-order nonlinearities producing IMD components at f1 − f2 and f2 − f1. IIP2 graphically represents the extrapolated intersection of the carrier's input power with the second-order IMD component when plotted in decibels.

Input Third-Order Intercept (IIP3)
A figure of merit used to determine a component's or system's susceptibility to intermodulation distortion (IMD) from its third-order nonlinearities. Two unmodulated carriers at a specified frequency relationship (f1 and f2) are injected into a nonlinear system exhibiting third-order nonlinearities producing IMD components at (2 × f1) − f2 and (2 × f2) − f1. IIP3 graphically represents the extrapolated intersection of the carrier's input power with the third-order IMD component when plotted in decibels.

Image
The AD6650 incorporates a quadrature demodulator that mixes the IF frequency to a baseband frequency. The phase and amplitude imbalance of this quadrature demodulator is observed in a complex FFT as an image of the fundamental frequency. The term image arises from the mirror-like symmetry of signal and image frequencies about the beating-oscillator frequency (in this case, this is dc).

Differential Analog Input Resistance, Differential Analog Input Capacitance, and Differential Analog Input Impedance
The real and complex impedances measured at each analog input port. The resistance is measured statically, and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range
The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180° out of phase. The peak-to-peak differential voltage is computed by rotating the phases of the inputs 180° and taking the peak measurement again. Then the difference is computed between both peak measurements.

Full-Scale Input Power
Expressed in dBm. It is computed using the following equation:

$$Power_{Full\,scale} = 10 \log \left(\frac{\frac{V^2{}_{Full\,scale_{rms}}}{Z_{Input}}}{0.001} \right) \quad (2)$$

where Z_{Input} is the input impedance.

Noise
The noise, including both thermal and quantization noise, for any range within the ADC is computed as

$$V_{noise} = \sqrt{Z \times 0.001 \times 10^{\left(\frac{FS_{dBm} - SNR_{dBc} - Signal_{dBFS}}{10} \right)}} \quad (3)$$

where:

Z is the input impedance.
FS_{dBm} is the full scale of the device for the frequency in question.
SNR_{dBc} is the value for the particular input level.
$Signal_{dBFS}$ is the signal level within the ADC reported in decibels below full scale.

EQUIVALENT CIRCUITS

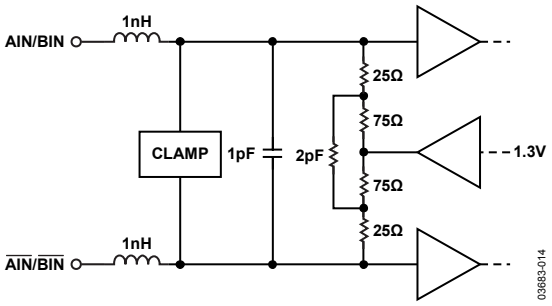


Figure 19. Analog Input

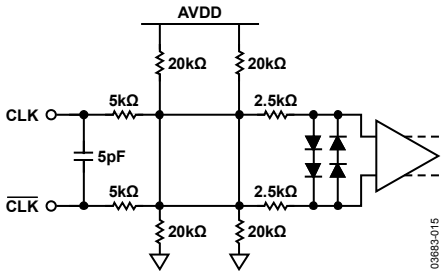


Figure 20. Clock Input

THEORY OF OPERATION

ANALOG FRONT END

The AD6650 is a mixed-signal front-end (MxFE®) component intended for direct IF sampling radios requiring high dynamic range. It is optimized for the demanding performance requirements of GSM and EDGE.

The AD6650 has five signal processing stages: a digital VGA, I/Q demodulators, seventh-order low-pass filters, dual ADCs, and digital filtering. Programming and control are accomplished via a microprocessor interface.

DVGA

A gain-ranging digital VGA is used to extend the dynamic range of the ADC and minimize signal clipping at the ADC input. The VGA has a maximum gain of 36 dB with a nominal step size of 0.094 dB. The amplifier serves as the input stage to the AD6650 and has a nominal input impedance of 200 Ω and a 4 dBm maximum input.

I/Q Demodulators

Frequency translation is accomplished with I/Q demodulators. Real data entering this stage is separated into in-phase (I) and quadrature (Q) components. This stage translates the input signal from an intermediate frequency (IF) of 70 MHz to 260 MHz to a baseband frequency.

Low-Pass Filters

In each I/Q signal path is a seventh-order low-pass active filter with 3.5 MHz bandwidth and automatic resistance-capacitance calibration to ±4%. This filter typically offers greater than 70 dB of alias rejection at 25.9 MHz.

Dual ADCs

The AD6650 has two ADCs. Each is implemented with an AD9238 core preceded by dual track-and-holds that multiplex in the I and Q signals at 26 MSPS each. The full-scale input power into the ADC is 4 dBm.

DIGITAL BACK END

The 12-bit ADC data goes through the coarse dc correction block, which performs a one-time calibration of the dc offsets in the I and Q paths. The output of this block drives the automatic gain control (AGC) loop block, which adjusts the digitally controlled VGA in the analog path. The AGC adjusts the amplitude of the incoming signal of interest to a programmable level and prevents the ADC from clipping. The gain of the VGA is subtracted in the relinearization block so that externally the AD6650 appears to have constant gain. For example, if the VGA must increase the gain from 20 dB to 30 dB due to a decrease in the signal power, the relinearization word changes from a −20 dB to a −30 dB gain so that the total AD6650 response is unchanged. The 19-bit output of the AGC block is then decimated and filtered using the CIC4 filter, the IIR filter, and the programmable RAM coefficient filter (RCF). Either 16-bit or 24-bit data is output through the serial port. With the 36 dB VGA gain, 12-bit ADC performance, and approximately 21 dB of processing gain, the AD6650 is capable of delivering approximately 116 dB of dynamic range or 19 bits of performance. For this reason, it is recommended that the 24-bit serial output be used so that dynamic range is not lost.

A block diagram of the digital signal path is shown in Figure 21.

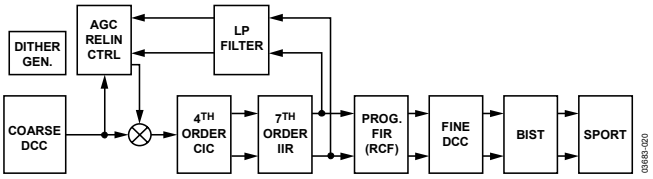


Figure 21. Channel Digital Signal Path

DC CORRECTION

The dc offset in the analog path of the AD6650 comes from three sources: the analog baseband filters, the ADCs, and the LO leakage of the mixers. The dc offsets of the analog filters and the ADCs dominate that of the LO leakage. The dc offsets on the I and Q data for both Channel A and Channel B are different because they use different analog paths. Each path is corrected independently.

The typical uncorrected dc offset is between −32 dB and −35 dB relative to full scale (dBFS) of the ADC. When the AGC range is considered along with this offset, the dc is effectively slid down by the gain setting so that it is approximately −68 dBFS to −71 dBFS or smaller when the AD6650 is in maximum gain.

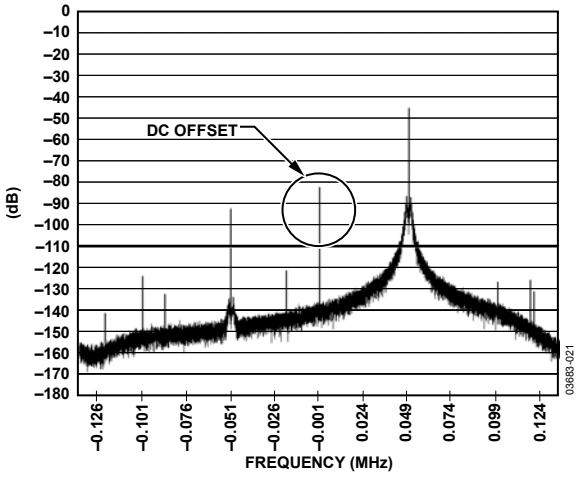


Figure 22. Uncorrected DC Offset

Coarse DC Correction

The coarse dc correction block is a simple integrate-and-dump that integrates the data for 16,384 cycles at the ADC clock rate (typically 26 MSPS) and then updates an estimate of the dc. This estimate is then subtracted from the signal path. The signal is clipped after the subtraction to avoid numerical wrap around with large signals.

The −32 dBFS to −35 dBFS uncorrected offset is sufficient to demodulate large signals, but it does not leave any margin if 30 dB of signal-to-dc is desired. It is essential to consider the dc offset of the signal at the point where the AGC of the AD6650 begins to range. This is important because once the signal or a blocker is in the range of the AGC loop, the dc signal that appears at the output of the AD6650 is modulated by the change in gain of the loop. If the gain decreases, the signal at the output remains at the same power level due to the digital relinearization, but the dc signal at the output is gained up by the relinearization process. For this reason, the coarse dc correction is used to provide additional correction before relinearizing the data to provide additional margin. This block gains another 5 dB to 8 dB (sometimes up to 25 dB) of dc rejection that provides additional margin.

The coarse dc correction is provided for two reasons:

- To provide additional margin on the carrier-to-dc term for large input signals.
- To provide more range for the fine dc correction upper threshold by decreasing the total input power to the block for small input signals. (This is described in more detail in the Fine DC Correction section.)

FOURTH-ORDER CASCADED INTEGRATOR COMB FILTER (CIC4)

The CIC4 processing stage implements a fixed-coefficient decimating filter. It reduces the sample rate of the signal and allows subsequent filtering stages to be implemented more efficiently. The input of the CIC4 is driven by the 19-bit relinearized data at a maximum input rate of 26 MHz (52 MHz clock rate).

The CIC4 decimation ratio, M_{CIC4}, can be programmed from 8 to 32 (all integer values). The CIC4 scale factor, S_{CIC4}, is a programmable unsigned integer between 0 and 8. It serves to control the attenuation of the data into the CIC4 stage in 6 dB increments such that the CIC4 does not overflow. Because this scale factor is in 6 dB steps, the CIC4 filter has a gain between 0 dB and −6.02 dB when properly scaled. For the best dynamic range, S_{CIC4} should be set to the smallest value possible (lowest attenuation) without creating an overflow condition.

$$S_{CIC4} = Ceil\left(4 \times \log_2\left(M_{CIC4}\right)\right) - 12 \quad (4)$$

$$CIC_Gain = \frac{{M_{CIC4}}^4}{2^{S_{CIC4}+12}} \quad (5)$$

The value of 12 that is subtracted in Equation 4 comes from the amount of scaling needed to compensate for the minimum decimation of 8. The frequency response of the CIC4 filter is given by Equation 6 and Equation 7. The gain and pass-band droop of the CIC4 can be calculated using these equations. If the gain and/or droop of the CIC4 filter are not acceptable, they can be compensated for in the programmable RCF filter stage.

$$CIC4(Z) = \left(\frac{1}{M_{CIC4}} \times \frac{1 - Z^{-M_{CIC4}}}{1 - Z^{-1}}\right)^4 \times CIC_Gain \quad (6)$$

$$CIC4(f) = \left(\frac{1}{M_{CIC4}} \times \frac{\sin\left(\pi \times \frac{f \times M_{CIC4}}{f_{ADC}}\right)}{\sin\left(\pi \times \frac{f}{f_{ADC}}\right)}\right)^4 \times CIC_Gain \quad (7)$$

The output rate of this stage is given by Equation 8.

$$f_{SAMP4} \le \frac{f_{ADC}}{M_{CIC4}} \quad (8)$$

CIC4 Rejection

Table 10 shows the amount of bandwidth as a percentage of the input sample rate (ADC sample rate) that can be protected with various decimation rates and alias rejection specifications. The maximum input rate into the CIC4 is 26 MHz. Table 10 shows the half-bandwidth characteristics of the CIC4.

Table 10. SSB CIC4 Alias Rejection Table

	dB					
Rate	**−50**	**−60**	**−70**	**−80**	**−90**	**−100**
8	2.494	1.921	1.473	1.128	0.860	0.651
9	2.224	1.713	1.315	1.007	0.768	0.581
10	2.006	1.546	1.187	0.909	0.693	0.525
11	1.827	1.408	1.081	0.828	0.632	0.478
12	1.676	1.292	0.992	0.760	0.580	0.439
13	1.549	1.194	0.917	0.703	0.536	0.406
14	1.439	1.110	0.852	0.653	0.499	0.378
15	1.344	1.037	0.796	0.610	0.466	0.353
16	1.261	0.972	0.747	0.572	0.437	0.331
17	1.187	0.916	0.703	0.539	0.411	0.312
18	1.122	0.865	0.665	0.509	0.389	0.295
19	1.063	0.820	0.630	0.483	0.369	0.279
20	1.010	0.779	0.599	0.459	0.350	0.265
21	0.962	0.742	0.570	0.437	0.334	0.253
22	0.919	0.709	0.544	0.417	0.319	0.241
23	0.879	0.678	0.521	0.399	0.305	0.231
24	0.842	0.650	0.499	0.383	0.292	0.221
25	0.809	0.624	0.479	0.367	0.281	0.212
26	0.778	0.600	0.461	0.353	0.270	0.204
27	0.749	0.578	0.444	0.340	0.260	0.197
28	0.722	0.557	0.428	0.328	0.251	0.190
29	0.697	0.538	0.413	0.317	0.242	0.183
30	0.674	0.520	0.400	0.306	0.234	0.177
31	0.653	0.503	0.387	0.297	0.226	0.171
32	0.632	0.488	0.375	0.287	0.219	0.166

Table 10 enables the calculation of an upper bound on the decimation ratio (M_{CIC4}), given the desired filter characteristics and input sample rate.

INFINITE IMPULSE RESPONSE (IIR) FILTER

The IIR filter of the AD6650 is a seventh-order low-pass filter with an infinite impulse response. This filter cannot be bypassed and always performs a decimation of 2. As can be seen from the Z-transform, the IIR filter has a gain of −6.02 dB to accommodate signal peaking within the structure. It is designed to be free of limit cycles and is unconditionally stable. The IIR filter is described by the Z-transform and coefficients shown in the following equation:

$$IIR(z) = \frac{\left(n_0 \times z^7 + n_2 \times z^5 + n_3 \times z^3 + n_1 \times z + n_1 \times z^6 + n_3 \times z^4 + n_2 \times z^2 + n_0\right)}{\left(d_7 \times z^7 + d_5 \times z^5 + d_3 \times z^3 + d_1 \times z\right) \times 2} \quad (9)$$

where:

$n_0 = 0.046227$
$n_1 = 0.278961$
$n_2 = 0.76021$
$n_3 = 1.208472$
$d_0 = 0$
$d_1 = 0.12895$
$d_2 = 0$
$d_3 = 0.254698$
$d_4 = 0$
$d_5 = 1.026276$
$d_6 = 0$
$d_7 = 1$

Figure 23 shows the magnitude response of the IIR filter in a typical GSM/EDGE case where the ADCs are sampling at 26 MHz and the CIC filter is decimating by 12 to generate a 2.16 MHz (8× symbol rate) input rate to the IIR.

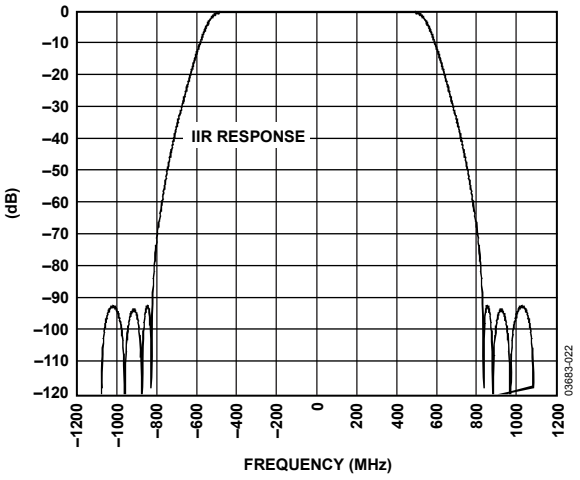


Figure 23. IIR Frequency Response

Figure 24 shows the phase response of the IIR filter over the range of ±100 kHz after a time delay during which ~13.449 input samples of the filter have been removed. The input rate is the same 2.16 MHz from the above GSM/EDGE configuration. Examining the plot shows that the IIR filter is not exactly phase linear. (Linear phase would be flat after the time delay has been removed). It can be seen, however, that the phase response over the band of interest is essentially perfect. From −100 kHz to +100 kHz, the phase distortion is ~0.056° rms. This phase response is several orders of magnitude below the analog LO and analog filter phase distortions.

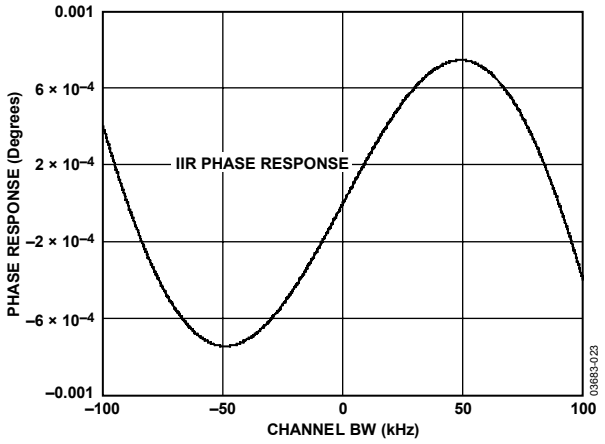


Figure 24. IIR Phase Response

RAM COEFFICIENT FILTER

The final signal processing stage is a sum-of-products decimating filter with programmable coefficients (see Figure 25). The I-RAM and Q-RAM data memories store the most recent complex samples from the IIR filter with 23-bit resolution. The number of samples stored in these memories is equal to the coefficient length (N_{taps}), up to 48 taps. The coefficient memory, CMEM, stores up to 48 coefficients with 20-bit resolution. On every CLK (up to 52 MHz) cycle, one tap for I and one tap for Q are calculated using the same coefficients. The RCF output consists of 16-bit or 24-bit data.

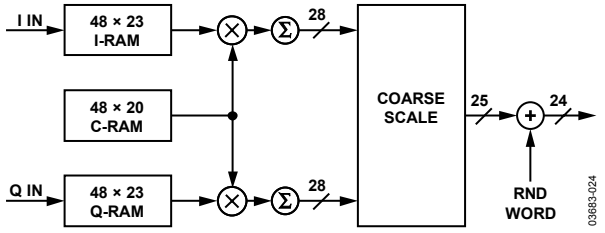


Figure 25. Block Diagram of the RCF

RCF Decimation Register

Each RCF channel can decimate the data rate by a factor of 1 to 8. The decimation register is a 3-bit register. The RCF decimation is stored in Address 0x18 in the form of $M_{RCF} - 1$. The input rate to the RCF is $f_{SAMPIIR}$.

RCF Decimation Phase Register

The AD6650 uses the value stored in this register to preload the RCF counter. Therefore, instead of starting from 0, the counter is loaded with this value, thus creating a time offset in the output data. This data is stored in Address 0x19 as a 3-bit number. Time delays can be achieved in even units of the RCF input rate, which is typically ¼ of the symbol time for GSM.

RCF Filter Length

The maximum number of taps this filter can calculate, N_{taps}, is given by Equation 10. The value $N_{taps} - 1$ is written to the channel register within the AD6650 at Address 0x1B.

$$N_{taps} \le \min\left(\frac{f_{CLK} \times M_{RCF}}{f_{SAMPIIR}}, 48\right) \quad (10)$$

where:

f_{CLK} is the external frequency oscillator.
M_{RCF} is the RCF filter decimation rate.
$f_{SAMPIIR}$ is the input rate to the RCF.

The RCF coefficients are located in Address 0x40 to Address 0x6F, and are interpreted as 20-bit twos complement numbers. When writing the coefficient RAM, the lower addresses are multiplied by relatively older data from the IIR, and the higher coefficient addresses are multiplied by relatively newer data from the IIR. The coefficients need not be symmetric, and the coefficient length, N_{taps}, can be even or odd. If the coefficients are symmetric, both sides of the impulse response must be written into the coefficient RAM.

The RCF stores the data from the IIR into a 46 × 48 RAM. A RAM of 23 × 48 is assigned to I data, and a RAM of 23 × 48 is assigned to Q data.

When the RCF is triggered to calculate a filter output, it starts by multiplying the oldest value in the data RAM by the first coefficient, which is pointed to by the RCF coefficient offset register (Address 0x1A). This value is accumulated with the products of newer data-words multiplied by the subsequent locations in the coefficient RAM until the coefficient address $RCF_{OFF} + N_{taps} - 1$ is reached.

Table 11. Three-Tap Filter

Coefficient Address	Impulse Response	Data
0	h(0)	N(0) oldest
1	h(1)	N(1)
2 = (N_{taps} − 1)	h(2)	N(2) newest

The RCF coefficient offset register can be used for two purposes. The main purpose is to allow multiple filters to be loaded into memory and selected simply by changing the offset. The other is to contribute to the symbol timing adjustment. If the desired filter length is padded with 0s on the ends, the starting point can be adjusted to form slight delays in the time the filter is computed with reference to the high speed clock. This allows for vernier adjustment of the symbol timing. Coarse adjustments can be made with the RCF decimation phase.

The output rate of this filter (f_{SAMPR}) is determined by the output rate of the IIR stage and M_{RCF}.

$$f_{SAMPR} = \frac{f_{SAMPIIR}}{M_{RCF}} \quad (11)$$

where:

$f_{SAMPIIR}$ is the input rate to the RCF.
M_{RCF} is the RCF filter decimation rate.

RCF Output Scale Factor and Control Register

Address 0x1C is used to configure the scale factor for the RCF filter. This 2-bit register is used to scale the output data in 6 dB increments. The possible output scales range from 0 dB to −18 dB.

The AD6650 RCF uses a recirculating multiply accumulator (MAC) to compute the filter. This accumulator has three bits of growth, allowing the output of the accumulator to be up to eight times as large as the input signal. To achieve the best filter performance, the coefficients should be as large as possible without overflowing the accumulator. The gain of a filter is merely the sum of the coefficients; therefore, for normal steady state signals, the sum of the coefficients must be less than 8. If the sum of the coefficients is 8 or slightly less, very rare transient events can overflow the accumulator. To prevent this, the sum of the absolute values of the coefficients should be less than 8. It is then impossible for the RCF filter to overflow.

The RCF filter has a 4-position mux at the output of the accumulator. This mux chooses which 24 bits are propagated to the output and adjusts the rounding appropriately. This can be viewed as a gain block that can be varied in 6 dB steps and is controlled by the 2-bit RCF scale register.

The resulting gain of the RCF (RCFgain) is then represented by the following equation:

$$RCFgain = \sum Coef \times \frac{1}{2^{3 - RCFScale}} \quad (12)$$

where *RCFScale* is the value in the RCF scale register.

COMPOSITE FILTER

The total gain of the digital filters can be calculated with Equation 13 and must be less than or equal to 1 (0 dB). Typically, the RCF coefficient gain is scaled to compensate for the gain of the CIC and IIR, and the RCF scale factor is set to 3.

$$Gain = \frac{M_{CIC4}{}^4}{2^{S_{CIC4}+12}} \times \frac{1}{2} \times \left(\sum Coef \times \frac{1}{2^{3 - RCFScale}}\right) \quad (13)$$

where:

Gain is the gain of the digital filters.
M_{CIC4} is the CIC4 decimation ratio.
S_{CIC4} is the CIC4 scale factor.
RCFScale is the value in the RCF scale register.

The individual responses of the CIC4 and IIR filters, along with the composite response of all the filters, are shown in Figure 26.

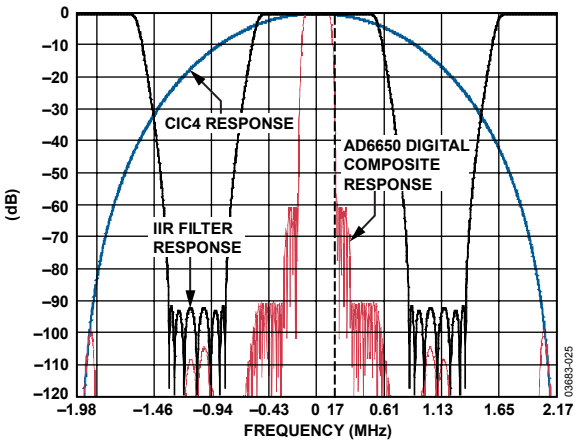


Figure 26. Composite Digital Response with 8× Rate

FINE DC CORRECTION

The fine dc correction block in the AD6650 lies between the RCF and serial output port. While the coarse dc correction block at the front of the channel is included to provide a one-time correction at startup or at rare intervals when commanded by the user, the fine dc correction block is intended to run continuously and track any changes in the dc offsets of the analog front end. To achieve this efficiently under varying signal conditions, this dc estimation process is adaptive.

Adaptive DC Correction Filter

In typical applications where dc offsets are to be corrected, a high-pass filter (HPF) is used to remove the dc and some small percentage of the input signal power. This approach is straightforward and works well when the input signal has a relatively constant power or when the bandwidth of the HPF is extremely small (in the μHz or nHz range) and the dc content does not vary. In general, the more the input signal power can vary, the narrower the bandwidth of the high-pass filter must be to avoid low frequency transients in the filter that are larger than the smallest expected signals. A fundamental trade-off exists because if the high-pass filter has a very low bandwidth, it can only track very slow changes (over hours, days, or weeks) in the dc offsets of the device. On the other hand, if it has a higher bandwidth, it may not be able to estimate the dc properly in the presence of a large baseband signal.

Given the assumption that the signal of interest is uniformly distributed across frequency, the processing gain equation can be used to provide a starting point for system optimization. Enough processing gain must be guaranteed for the dc estimate to be valid for a minimum signal case. This is typically 20 dB to 30 dB but depends on the baseband signal processing of a particular system. For GSM/EDGE, which is distributed over ~100 kHz single sideband (SSB), this implies that the HPF bandwidth must be between 100 Hz to 1 kHz SSB. For every 6 dB that the signal power increases, 6 dB more processing gain is required; therefore, the HPF bandwidth needs to decrease by a factor of 4 or more.

(14)

$$PG = 10 \times \log\left(\frac{f_{BW}}{f_{HPF}}\right) \quad (14)$$

where:

f_{BW} is the channel filter bandwidth.
f_{HPF} is the HPF bandwidth.

In the case of GSM, a simple HPF is not well suited to this problem because the signal power can vary 50 dB or more from time slot to time slot and has a total dynamic range of 91 dB or more. A large time slot would excite the impulse response of the HPF, possibly resulting in a peak occurring later when a small time slot is present. To provide a more optimal dc correction, the AD6650 adaptively adjusts the bandwidth of the HPF based on the signal power. As the signal level decreases, the HPF bandwidth increases. Conversely, as the signal level increases, the HPF bandwidth decreases.

The AD6650 implements this high-pass filter in the form of an accumulator that integrates a number of samples of the output of the RCF and produces an estimate after the samples are accumulated. The estimated dc is then removed from the signal path by a simple subtraction. The subtraction is clamped to avoid overflow problems. The HPF bandwidth is varied by changing the integration time (equivalent to a SYNC 1 filter decimation of the integrator). The integration time is varied based on the output of a peak detector circuit according to the process described in the Peak Detector DC Correction Ranging section.

PEAK DETECTOR DC CORRECTION RANGING

The peak detector of the AD6650 always looks at the maximum signal power present in the I or Q data path. The I and Q paths are treated totally independently in the dc correction circuitry because the analog paths are not guaranteed to match. The first sample that arrives is rectified and preloaded into the peak detector. A control counter is set to the minimum period control register setting. On every input sample, the peak detector determines if the new sample is larger than the currently held sample, and if so, the peak detector is updated. The contents of the peak detector are then examined. If they are below the lower threshold, the control counter counts down and when it reaches 0, it updates the dc estimate, resets the dc accumulator, and reloads the peak detector with the newest input sample magnitude. If the peak detector value is above the upper threshold of the dc correction, the estimate currently being calculated is discarded. When the signal drops below the upper threshold, the calculation of a new dc estimate begins. The current estimate is held, so the last known dc content continues to be removed.

The AI, AQ, BI, and BQ paths of the AD6650 are each treated independently in the dc correction circuitry because the analog paths are not guaranteed to match, and separate dc estimates need to be kept for each. Separate peak detectors, dc estimate accumulators, dc estimate subtractors, and control counters are implemented for each of these paths.

Peak Detector

The peak detector always stores the input sample with the largest magnitude. The absolute value of every input sample is compared to what is currently in the peak detector's holding register. The only exception is when the control counter reaches 0; at this point, the dc offset estimate is updated and the peak detector is set to the current input magnitude. The output of each of the peak detectors is then encoded into a digital word that represents the signal power in 6 dB steps relative to full scale (FS).

DC Accumulator

The dc accumulator accumulates the 24-bit samples input from the RCF filter until the control counter reaches 0. At this time, the dc estimate in the holding register is updated, and the accumulator is directly loaded with the new input sample to begin work on the next estimate.

Control Counter

This counter controls the update of the dc correction block based on the peak detector value and the input control registers. The following three conditions are possible:

- If the digital word from the peak detector indicates that the desired signal is below the lower threshold, the counter merely cycles through at the minimum period.
- If the digital word from the peak detector indicates that the desired signal is above the upper threshold, the control counter is held at the minimum period value and does not count down; therefore, no update is made. When the signal returns below the upper threshold, this counter resumes counting.
- If the digital word from the peak detector indicates that the desired signal is between the lower threshold and the upper threshold, the fine dc correction circuit is in its normal mode of operation. In this mode, the control counter starts with the minimum period but is reloaded with 4× minimum period every time the peak detector output words increment by 6 dB. This errs on the side of caution and ensures that the dc correction integrates long enough to obtain a valid estimate. If smaller integrations are preferred, the minimum period can be decreased or the lower threshold can be raised.

The integration period is given by Equation 15 and Equation 16. The factor of 2 in the exponent shows that as peak signal power increases, the integration time is increased by a factor of 4. This decreases the bandwidth of the estimation filter, thus providing the additional processing gain in the dc estimation term.

When the desired signal power equals the upper threshold,

$$I_P = 2^{Min_Period + Ceil\left(\frac{\left|Upper_Threshold - Lower_Threshold\right|}{6.02}\right) \times 2} \quad (15)$$

When the desired signal power is less than the upper threshold,

$$I_P = 2^{Min_Period + Ceil\left(\frac{\left|Desired_Signal_Power - Lower_Threshold\right|}{6.02}\right) \times 2} \quad (16)$$

where *Min_Period*, *Upper_Threshold*, and *Lower_Threshold* are register-programmable values.

To calculate the time required for the fine dc correction to converge, use the following equation:

$$Fine_DC_Converge = \frac{I_P \times T_{SYM}}{60} \quad (17)$$

where:

T_{SYM} is the output symbol rate of the AD6650.
Fine_DC_Converge is expressed in minutes, and for a GSM application with 1× oversampling, it is 3.69×10^{-6}.

USER-CONFIGURABLE BUILT-IN SELF-TEST (BIST)

The AD6650 includes a BIST to assess digital functionality. This feature verifies the integrity of the main digital signal paths of the AD6650. Each BIST register is independent, meaning that each channel can be tested independently at the same time.

The BIST is a thorough test of the selected AD6650 digital signal path. With this test mode, it is possible to use the internal pseudorandom generator to produce known test data. A signature register follows the fine dc correction block. This register can be read back and compared to a known good signature. If the known good signature matches the register value, the channel is fully operational.

If an error is detected, each internal block can be bypassed and another test can be run to debug the fault. The I and Q paths are tested independently. Use the following steps to perform this test:

1. Reset the AD6650.
2. Program the desired AD6650 channel parameters for the desired application (these parameters include decimation rates, scalars, and RCF coefficients). Also, ensure that the start holdoff counter is set to a nonzero value.
3. Set Register 0xA, Bit 1, to 1 (PN_EN).
4. Set Register 0x21, Bit 8, to 0 (fine DCC to BIST).
5. Start the A and/or B channels with a microprocessor write (Soft_SYNC) or a pulse on the SYNC pin (Pin_SYNC).
6. Wait at least 300 µs.
7. Read the four BIST registers and compare the values to a known good device. This ensures that the AD6650 is programmed correctly and that each channel is functioning correctly.

LO SYNTHESIS

The AD6650 has a fully integrated quadrature LO synthesizer consisting of a voltage-controlled oscillator (VCO) and a phase-locked loop (PLL). Together these blocks generate quadrature IF LO signals for the demodulators.

Figure 27 shows a block diagram of the LO synthesis block. Besides the usual PLL and VCO, there is also a programmable half-rate divider (Div-X and a fixed divide-by-4 quadrature divider that produces the final I and Q LO signals).

VCO

The VCO generates an on-chip RF signal in the range of 2.2 GHz to 2.8 GHz. The only external component required is a bypass capacitor for the low dropout (LDO) voltage regulator used to power the VCO tank core. The VCO uses overlapping bands to achieve the wide tuning range while maintaining excellent phase noise and spurious performance. During band selection, which takes 5 PFD cycles, the VCO V_{TUNE} is disconnected from the output of the loop filter and connected to an internal reference voltage. After band select, normal PLL action resumes. The nominal value of K_V is 65 MHz/V, where K_V is the VCO sensitivity.

Immediately following the VCO is a programmable half-rate divider that has settings of divide-by-2, -2.5, -3, -3.5, and so on, up to divide-by-8. This function divides the VCO frequency down to four times the LO frequency and effectively extends the tuning range of the VCO. The VCO and the half-rate divider can be thought of as a single lower frequency VCO with a frequency range of 280 MHz to 1040 MHz.

Autocalibration selects both the VCO operating band and the oscillator amplitude to ensure peak operating performance across the entire frequency range. The half-rate divide setting is also selected as part of the VCO calibration. Autocalibration is performed whenever PLL Register 3 (the test mode latch) is written; therefore, all other PLL registers should be set first, and Register 3 should be written to last. This is true whenever programming any portion of the LO synthesizer because the VCO may need to recalibrate itself, depending on the changes made to the registers.

PLL

The integer-N type PLL consists of a programmable reference divider (R-divider), a prescaler and feedback divider (N-divider), a phase-frequency detector (PFD), and a charge pump. The output of the charge pump drives an external loop filter, which in turn drives the input of the VCO.

R-Divider

The 14-bit R-divider divides down the input clock frequency to produce the reference frequency for the phase-frequency detector. Although division ratios from 1 to 16,383 are allowed, the maximum update rate for the PFD is 1 MHz. The selected update rate of the PFD and the subsequent charge pump determines the spurious performance of the LO synthesizer; therefore, the PFD reference frequency should be set for optimal placement of spurs.

Prescaler and Feedback Dividers

The dual modulus prescaler, P/(P + 1), and the A and B feedback dividers (5 bits and 13 bits, respectively) combine to provide a wide ranging N-divider in the PLL feedback loop. The feedback division is N = 8B + A. Including the final quadrature divider (divide-by-4), the LO frequency is given by

$$f_{LO} = \frac{f_{CLK} \times (B \times 8 + A)}{4R} \quad (18)$$

where:

f_{LO} is the local oscillator frequency.
f_{CLK} is the external frequency oscillator.
B is the 13-bit divider (3 to 8191).
A is the 5-bit swallow divider (0 to 31).
R is the input reference divider (1 to 16,384).

The $f_{CLK}/4R$ term combines the effects of the reference divider and the final quadrature divider, and determines the frequency spacing for the LO synthesizer. For a typical GSM application, f_{CLK} = 52 MHz and R = 65 result in a 200 kHz PFD update rate, which sets the frequency spacing at a desired 200 kHz. However, this also places LO spurs at offsets of 200 kHz multiples, which might degrade the interferer/blocker performance.

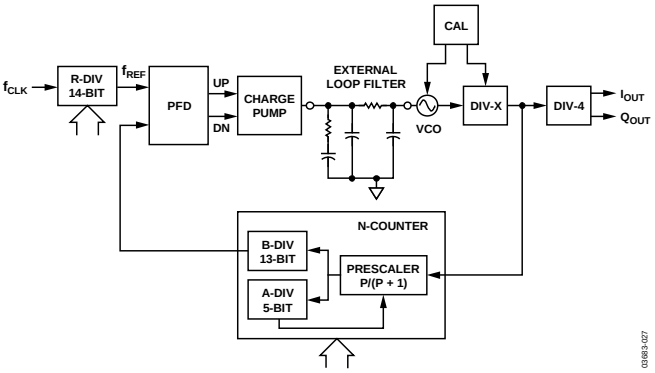


Figure 27. PLL Circuit

PFD and Charge Pump

The phase-frequency detector (PFD) takes inputs from the R-divider and N-divider and produces an output proportional to the phase and frequency difference between them. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes reference spurs.

Loop Filter

The final element in the LO synthesizer is the external loop filter, which is generally a first-order or second-order RC low-pass filter. A filter like the one shown in Figure 28 is recommended to provide a good balance of stability, spurs, and phase noise. This partiular filter is optimized for an update rate of 1 MHz.

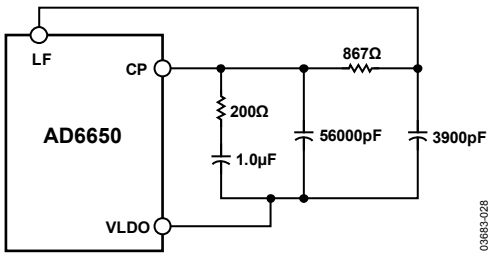


Figure 28. Loop Filter Circuit

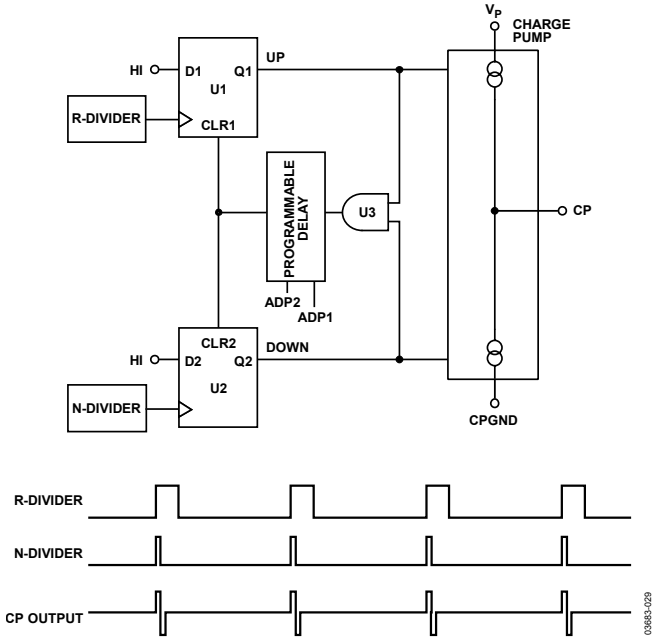


Figure 29. PFD Simplified Schematic and Timing (Locked)

LDO

The AD6650 includes an on-chip 2.6 V low dropout (LDO) voltage regulator that supplies the VCO and other sections of the PLL. A 0.22 µF bypass capacitor is required on the VLDO output to ensure stability. This LDO employs the same technology used in the anyCAP® line of regulators from Analog Devices, Inc., making it insensitive to the type of capacitor used. Driving an external load from the VLDO output is not supported.

AGC LOOP/RELINEARIZATION

The AGC consists of three gain control loops: a slow loop, a fast attack (FA) loop, and a fast decay (FD) loop.

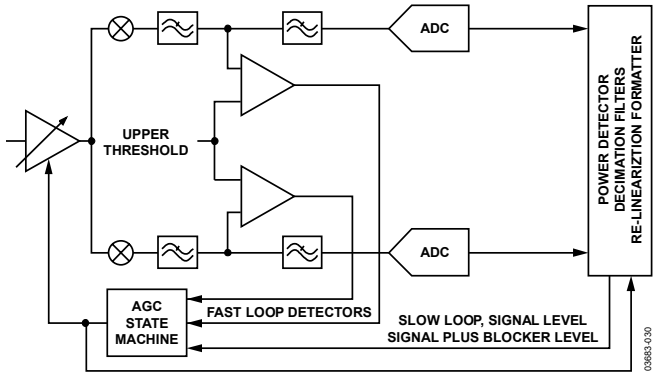


Figure 30. AGC Loop Block Diagram

Slow Loop

The slow loop is the main loop and is associated with a loop gain parameter. This parameter controls the rate of change of the gain and should always be less than 1. To determine the loop gain, Equation 19 should be used.

$$AGCLoopGain = \left(\frac{K_{Mantissa}}{256}\right) \times 2^{-K_{Exponent}} \quad (19)$$

where:

$K_{Mantissa}$ is the loop gain mantissa. Values can range from 0 to 63.
$K_{Exponent}$ is the loop gain exponent. Values can range from 0 to 7.

As the loop gain value increases, the speed of the response of the AGC loop increases; as the loop gain value decreases, so does the speed of the response of the AGC loop. The slow loop attempts to maintain the signal entering the ADC at a given level, referred to as the requested level. This level is specified in dBFS and can be between 0 dBFS and −24 dBFS (in 0.094 dB steps) of the converter resolution. The default value is −6.02 dBFS. The slow loop has a peak detection function, the period of which can be set by the user. This period should be set to ¼ of the symbol period, or greater, to prevent the AGC loop from gaining off the envelope of the EDGE signal. This detection period works because the peak detector's operation is based on dB (max(|I|, |Q|)); therefore, all of the I/Q samples are reflected back into one quadrant of the I/Q plane. At a 26 MHz sampling frequency, one symbol period is 96 clock cycles. Therefore, to obtain a peak detector period that is ¼ of the symbol period, the peak detector period should be set to a minimum of 24 samples. The following equation can also be used:

$$SPB\ Peak\ Samples \geq \tfrac{1}{4} \times \left(f_{SAMP} / f_{SYM}\right) \quad (20)$$

where:

f_{SYM} = 270.833 kHz (GSM symbol rate).
f_{SAMP} = 26 MHz.

Fast Attack (FA) Loop

The FA loop utilizes an analog threshold detector that prevents overdrive of the analog signal path. In a situation that could potentially overdrive the ADC, the FA loop takes over from the slow loop and decreases the gain to the VGA in the front end. The step size used for the FA loop is programmable between 0 dB and 1.504 dB in 0.094 dB steps. The FA loop also has a counter that is programmable between 1 and 16. When initialized to count + 1, the FA loop decreases the gain for count + 1 clock cycles when the threshold is crossed.

Fast Decay (FD) Loop

The FD loop is a fast loop that increases the gain when the signal falls below a threshold during a deep channel fade or on the ramp down. The fast loop accomplishes this task by comparing the peak signal-plus-blocker level at the ADC output (which includes the signal and any blockers that pass through the SAW filter) with a programmable level (SPB_level) that determines when this loop is activated. The SBP_level default

value is −40 dBFS. When the wideband signal is below the SPB level, the FD loop is activated. This loop overrides the slow loop and has a programmable step size (default 0.094 dB) and a programmable peak detect period (defaults four samples at 1.08 MHz).

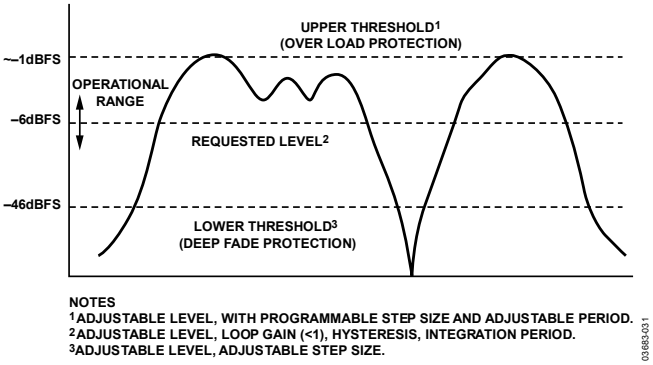


Figure 31. AGC Thresholds

SERIAL OUTPUT DATA PORT

The AD6650 has two configurable serial output ports (SDO0 and SDO1). Both ports must be identically configured and are programmed using the same control register. The ports share a common SFDS, SCLK, and DR pin for connection to an external ASIC or DSP; therefore, the outputs cannot be programmed independently.

Serial Output Data Format

The AD6650 utilizes a twos complement data format with a selectable serial data-word length of 16 bits or 24 bits. The data is shifted out of the device in MSB-first format.

Serial Data Frame Sync

The serial data frame sync (SDFS) pin signals the start of the serial data frame. As channel data becomes available at the output of the AD6650's filters, this data is transferred into the serial data buffer. The internal serial controller initiates the SDFS on the next rising edge of the serial clock. In the AD6650, there are three modes in which the frame sync can be generated, which are described in the SDFS Modes section.

Configuring the Serial Ports

Both serial output ports must function as master serial ports. A serial bus master provides SCLK and SDFS outputs. Serial Port 0 and Serial Port 1 must be programmed as the bus masters by setting Bit 3 of the serial control register high.

Serial Port Data Rate

The SCLK frequency is defined by Equation 21.

$$f_{SCLK} = \frac{f_{CLK}}{SDIV + 1} \quad (21)$$

where:

f_{CLK} is the frequency of the master clock of the AD6650 channel.
SDIV is the serial division word for the channel.

The SDIV for Serial Port 0 and Serial Port 1 can be programmed via Internal Control Register 0x21. Valid SDIV values are between 0 and 7, corresponding to divide ratios between 1 and 8.

Serial Output Frame Timing

The SDFS signal transitions high to signal the start of a data frame. On the next rising edge of SCLK, the port drives the first bit of the serial data on the SDO pin. The falling edge of SCLK or the subsequent rising edge can then be used by the DSP to sample the data until the required number of bits is received (determined by the serial output port word length). If the DSP has the ability to count bits, it can identify when the complete frame is received.

Serial Port Timing Specifications

Figure 32 to Figure 35 indicate the timing required for the AD6650 serial port.

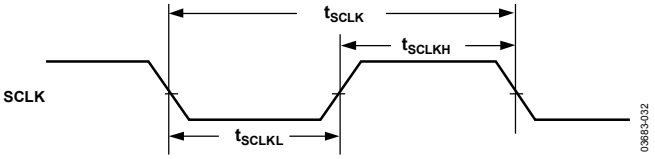


Figure 32. SCLK Timing Requirements

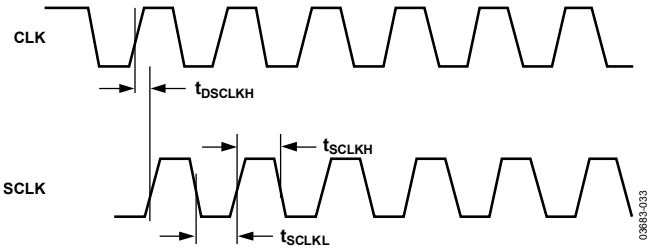


Figure 33. SCLK Switching Characteristics (Divide-by-1)

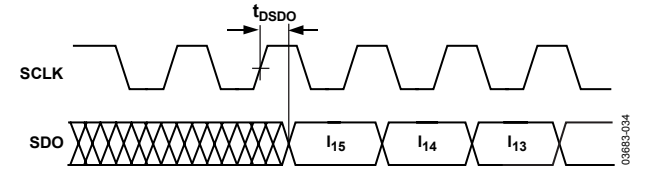


Figure 34. Serial Output Data Switching Characteristics

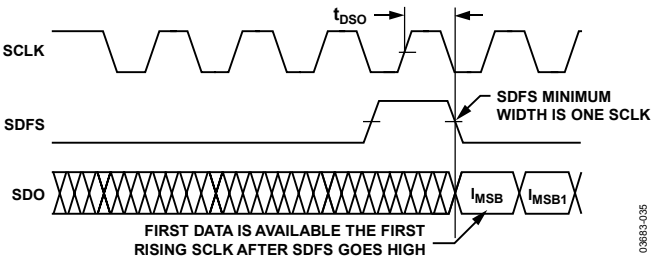


Figure 35. Timing for Serial Output Port

SCLK

SCLK is an output on the AD6650. All outputs are switched on the rising edge of SCLK. The SDFS pin is sampled on the falling edge of SCLK. This allows the AD6650 to recognize the SDFS in time to initiate a frame on the next SCLK rising edge. The maximum speed of this port is 52 MHz.

SDO

SDO is the serial data output. Serial output data is shifted on the rising edge of SCLK. On the next SCLK rising edge after an SDFS, the MSB of the I data from the channel is shifted.

On every subsequent SCLK edge, a new piece of data is shifted out on the SDO pin until the last bit of data is shifted out. The last bit of data shifted is the LSB of the Q data from the channel. SDO is three-stated when the serial port is outside its time slot. This allows the AD6650 to share the SDIN of a DSP with other AD6650s or other devices.

SDFS

SDFS is the serial data frame sync signal. SDFS is configured as an output. SDFS is sampled on the falling edge of SCLK. When SBM is sampled high, the chip functions as a serial bus master. In this mode, the AD6650 is responsible for generating serial control data. Four modes of that operation are set via Channel Address 0x21, Bit 6 to Bit 5.

Serial Word Length

Bit 4 of Address 0x21 determines the length of the serial word (I or Q). If this bit is set to 0, each word is 16 bits wide (16 bits for I and 16 bits for Q). If this bit is set to 1, the serial words are 24 bits wide.

SDFS Modes

As mentioned in the Serial Data Frame Sync section, there are three modes of operation.

Setting Bit 7 of Address 0x21 high indicates that Input Channel A data is output on SDO0 and Input Channel B data is output on SDO1. In this condition, there are three modes of operation. (There are technically four modes, but Mode 0 and Mode 1 are the same).

- Mode 0 and Mode 1 (Address 0x21, Bits[6 :5] = 00; Bit[7] = 1): The SDFS is valid for one complete clock cycle prior to the data shift. This single pulse is valid for Output Channel SDO0 and Output Channel SDO1. On the next clock cycle, the AD6650 begins shifting out the digitally processed data stream. Depending on the bit precision of the serial configuration, either 16 bits or 24 bits of I data are shifted out, followed by 16 bits or 24 bits of Q data.
- Mode 2 (Address 0x21, Bits[6:5] = 10; Bit[7] = 1): Because both SDO0 and SDO1 are used, SDFS pulses high one clock cycle prior to I data and also pulses high one clock cycle prior to Q data for each corresponding input channel. In this mode, there are two SFDS pulses per each output channel.
- Mode 3 (Address 0x21, Bits[6:5] = 11; Bit[7] = 1): The SDFS is high while valid bits are being shifted. On SDO0, SDFS remains high for 16 bits or 24 bits of I data, followed by 16 bits or 24 bits of Q data corresponding to Input Channel A. For SDO1, SDFS remains high for 16 bits or 24 bits of I data, followed by 16 bits or 24 bits of Q data corresponding to Input Channel B. The SDFS bit goes high one complete clock cycle before the first bit is shifted out of the AD6650.

APPLICATION INFORMATION

REQUIRED SETTINGS AND START-UP SEQUENCE FOR DC CORRECTION

On startup, the fine dc correction block may take up to several minutes to converge to a good dc estimate, especially if a large signal is present on the input. To improve this convergence without run-time trade-offs, use a two-step start-up process. The first step is to configure the fine dc correction block with the parameters shown in Table 12. The freeze is set so that the fine dc correction responds after the coarse dc correction has updated. At the same time, the minimum period can be set to a small value, such as 10. This guarantees a quicker convergence because the minimum period is smaller, resulting in a smaller integration period.

Also, setting the registers as described in Table 12, and subsequently programming the AD6650, ensures that the VGA and mixer are powered down during the power-on calibration to keep signals with large dc content from interfering with the estimation of the dc component from the analog path.

After ~500 ms, the freeze bit (Address 0x0B, Bit 0) can be written low. The dc correction then converges and begins removing the offset. If desired, the minimum period can then be set to a larger value.

If the VGA and mixer are not disabled during a power-up using the AutoCalibration control register as recommended, approximately 30 dB of suppression can be achieved, but the user must guarantee that significant content is not present at the IF frequency that will be translated to dc. If enhanced performance is desired from the coarse dc correction, an RF switch or other device can be used to shut off the input of the AD6650 until the correction has been completed.

Overall DC Correction Performance

With the recommended settings, the dc correction performance is approximately −120 dBFS or better for small signals. Once the signal is large enough to trip the AGC loop, the dc component also rises; however, this component has been shown to always be 40 dBc below the signal of interest. Therefore, the carrier-to-dc ratio degrades for small signals. For additional details on the dc correction registers, see the associated bit descriptions in the Register Map section.

CLOCKING THE AD6650

The AD6650 encode signal must be a high quality, low phase noise source to prevent degradation of performance. The AD6650 can be clocked with a single-ended signal, but $\overline{\text{CLK}}$ must be ac-coupled to ground. For optimum performance, the AD6650 must be clocked differentially. The encode signal should be ac-coupled into the CLK and $\overline{\text{CLK}}$ pins via a transformer or capacitors. These pins are biased internally and require no additional bias.

Figure 36 shows the preferred method for clocking the AD6650. The clock source (low jitter) is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the secondary transformer limit clock excursions into the AD6650 to approximately 0.8 V p-p differential. This helps prevent large voltage swings of the clock from feeding through to other portions of the AD6650 and limits the noise presented to the encode inputs.

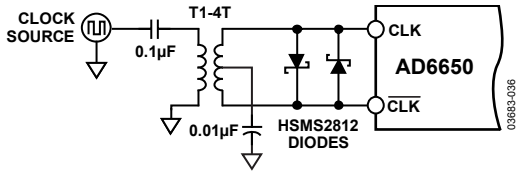


Figure 36. Crystal Clock Oscillator—Differential Encode

Table 12. DC Correction Register Recommendations

Description	Channel Address	Bit	Value
AutoCalibration Control Register	0x22	Bit 0	Enabled (1)
AutoCalibration Control Register	0x22	Bit 1	Power down DACs at startup (0)
AutoCalibration Control Register	0x22	Bit 2	Enabled (1)
AutoCalibration Control Register	0x22	Bit 3	Sync ADCs (0)
Upper Threshold	0x0B	Bit 19 to Bit 13	−48 dBFS
Lower Threshold	0x0B	Bit 12 to Bit 8	−90 dBFS
Minimum Period	0x0B	Bit 7 to Bit 3	+10 sample periods
Freeze	0x0B	Bit 0	Enabled (1)

Another option is to ac-couple a differential ECL/PECL signal to the encode input pins as shown in Figure 37. A device that offers excellent jitter performance is the MC100EL16 (or a device from the same family) from Motorola.

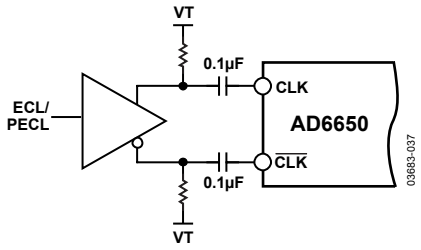


Figure 37. Differential ECL for Encode

DRIVING THE ANALOG INPUTS

As with most new high speed, high dynamic range devices, the analog input to the AD6650 is differential. Differential inputs allow much improvement in performance on-chip because signals are processed through attenuation and gain stages. Most of the improvement is a result of differential analog stages that have high rejection of even-order harmonics. Differential inputs are also beneficial at the PCB level. First, differential inputs have high common-mode rejection of stray signals, such as ground and power noise, and good rejection of common-mode signals, such as local oscillator feedthrough.

The AD6650 analog input voltage range is offset from ground by 1.3 V. The resistor network on the input properly biases the followers for maximum linearity and range. Therefore, the analog source driving the AD6650 should be ac-coupled to the input pins. The input resistance for the AD6650 is 200 Ω, and the input voltage range is 2 V p-p differential. This equates to 4 dBm full-scale input power. The recommended method for driving the analog input of the AD6650 is to use an RF balun.

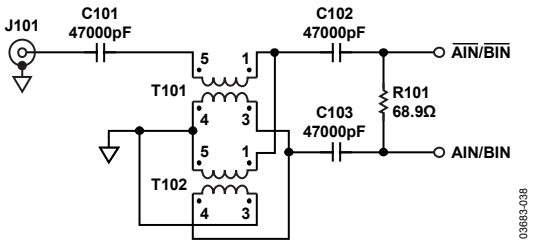


Figure 38. Balun-Coupled Analog Input Circuit

EXTERNAL REFERENCE

The reference should be connected as shown in Figure 39 to achieve the results specified in this data sheet.

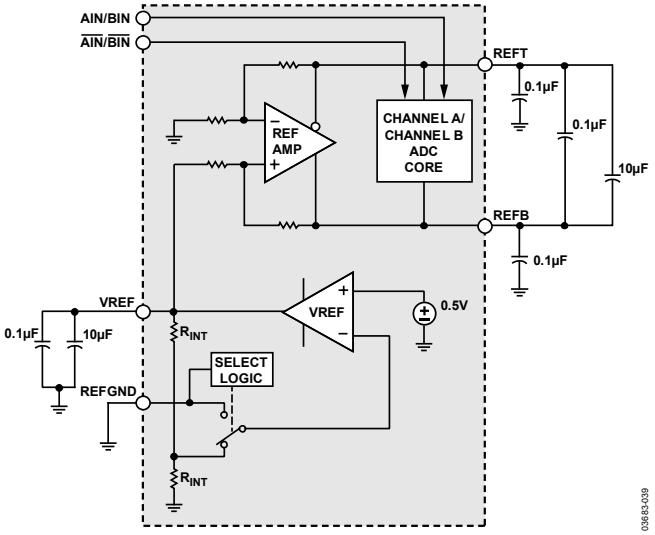


Figure 39. Reference Connection

POWER SUPPLIES

Care should be taken when selecting a power source. Linear supplies are strongly recommended. Switching supplies tend to have radiated components that may be received by the AD6650. Each of the power supply pins should be decoupled as closely to the package as possible using 0.1 µF chip capacitors.

The AD6650 is susceptible to low frequency power supply interference as shown in Figure 40. This low frequency energy is translated into spurious tones in the output signal. Analog power supply ripple couples into the LO through the VCO. This can be observed from the ripple frequency vs. sideband spur level plot (see Figure 40). Note that this plot has the spur level referenced to 1 mV rms supply ripple and is referred to the LO. Thus, this plot shows a transfer function rather than an absolute value. The spurious level can be extrapolated to any supply ripple level from this data using Equation 22.

$$Spur_Lev = Spur_Lev_{1\,mV} \times 20\log(SupRipple(\text{mV})) \quad (22)$$

where:

Spur_Lev is the output spurious level relative to the LO.
$Spur_Lev_{1\,mV}$ is the 1 mV referred level from Figure 40 and Figure 41.
SupRipple (mV) is the RMS ripple on the AVDD power supply.

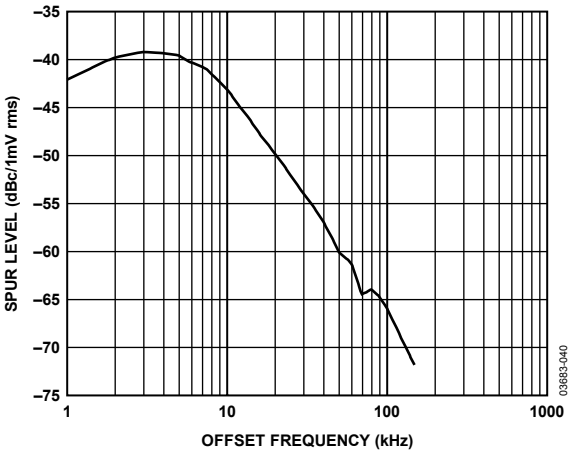


Figure 40. Output Spurious vs. Power Supply Ripple (AIN = 199 MHz)

An additional parameter that strongly impacts the PSRR is the sensitivity to the AVDD voltage level. A plot of spur level versus AVDD is shown below in Figure 41. Note that this plot also has the spur level referenced to 1mV rms supply ripple and is referred to the LO. Thus, this plot shows a transfer function rather than an absolute value. The spurious level can be extrapolated to any supply ripple level from this plot using Equation 21.

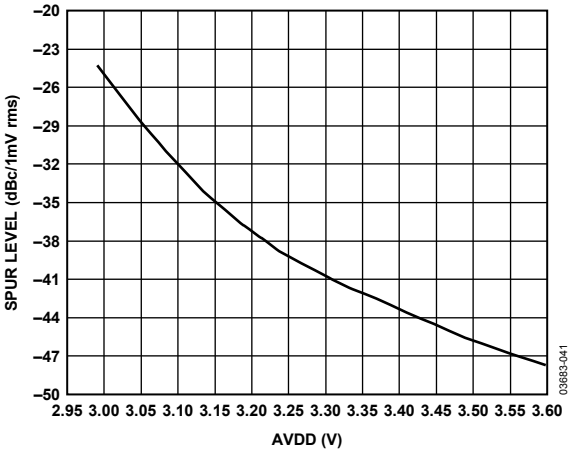


Figure 41. Output Spurious vs. Power Supply Ripple (AIN = 199 MHz)

The AD6650 has separate digital and analog power supply pins. The analog supplies are denoted AVDD, and the digital supply pins are denoted DVDD. Although analog and digital supplies can be tied together, best performance is achieved when the supplies are separate because the fast digital output swings can couple switching current back into the analog supplies. Note that AVDD and DVDD must be held between 3.0 V and 3.45 V.

DIGITAL OUTPUTS

It is recommended that the digital outputs drive a series resistor (for example, 100 Ω). To minimize capacitive loading, the number of gates on each output pin should be limited. The series resistors should be placed as close to the AD6650 as possible to limit the amount of current that can flow into the output stage. These switching currents are confined between ground and the DVDD pin. Also, note that excessive capacitive loading increases output timing and can invalidate timing specifications.

GROUNDING

For optimum performance, it is highly recommended to use a split ground between the analog and digital grounds. AGND should be connected to the analog ground of the RF board, and DGND should be connected to the digital ground of the RF board.

To minimize the potential for noise coupling, it is highly recommended to place multiple ground return traces and vias so that the digital output currents do not flow back toward the analog front end, but instead are routed quickly away from the AD6650. This can be accomplished by simply placing substantial ground connections directly back to the supply at a point between the analog front end and the digital outputs. Judicious use of ceramic chip capacitors between the power supply and ground planes also helps suppress digital noise. The layout should incorporate enough bulk capacitance to supply the peak current requirements during switching periods.

LAYOUT INFORMATION

A multilayer board should be utilized to achieve optimal results. It is highly recommended to use high quality ceramic chip capacitors to decouple each supply pin to ground directly at the device. The pin arrangement of the AD6650 facilitates ease of use in the implementation of high frequency, high resolution design practices. All of the digital outputs are on the opposite side of the package from the analog inputs for isolation purposes.

Care should be taken when routing the digital output traces. To prevent coupling through the digital outputs into the analog portion of the AD6650, minimal capacitive loading should be placed on these outputs.

The layout of the encode circuit is equally critical. Any noise received on this circuitry results in corruption in the digitization process and lower overall performance. The encode clock must be isolated from the digital outputs and the analog inputs.

CHIP SYNCHRONIZATION

The AD6650 is designed to allow synchronization of multiple AD6650s within a system. The AD6650 is synchronized with either a microprocessor write (Soft_SYNC) or a pulse on the SYNC pin (Pin_SYNC). The first sync event starts the device, and subsequent sync events resynchronize the filters of the AD6650. By using a start holdoff counter, it is possible to align the phase of the AD6650 to other devices. To synchronize the AD6650 with external hardware, see the Start with SYNC Pin section.

Start with Soft_SYNC

The AD6650 includes the ability to synchronize channels or chips under microprocessor control. The start holdoff counter (Address 0x14), in conjunction with the SYNC bit (External Memory Address 5, Bit 0), allows this synchronization. The start holdoff counter delays the start and synchronization of a channel(s) by its value (number of AD6650 CLKs).

Use the following method to synchronize the start of a channel via microprocessor control:

1. Set the appropriate channels to sleep mode. A hard reset to the AD6650 ($\overline{\text{RESET}}$ taken low) puts both channels into sleep mode.
2. Enable Channel A and/or Channel B (External Memory Address 3, Bit 0).
3. Write the start holdoff counter(s) (Address 0x14) to the appropriate value (greater than 1 but less than 65,535).
4. Program all other registers of the AD6650 that are not already set.
5. Write the Soft_SYNC bit high (External Memory Address 5, Bit 0).
6. When the Soft_SYNC bit goes high, the start holdoff counter begins to count down using the AD6650 CLK signal after the CLK divider. When the start holdoff counter reaches a count of 1, the selected channel(s) are activated.

Start with SYNC Pin

The AD6650 has a SYNC pin that can be used to provide synchronization between AD6650 devices and external hardware to a resolution of 1 ADC sample cycle. This can be accomplished by providing a 1-CLK-cycle-wide pulse on the SYNC pin when the edge-sensitive bit of the SF1 register is low (External Memory Address 4, Bit 4), which is useful when an FPGA or other external hardware is operating at the CLK rate of the AD6650. Synchronization can also be accomplished by setting the edge-sensitive bit high so that the SYNC input is rising-edge sensitive, which is useful when the external hardware is operating off a clock that is much slower than the AD6650 or is asynchronous to it.

MICROPORT CONTROL

The AD6650 has an 8-bit microprocessor port. The microport interface is a multimode interface that allows flexibility when dealing with the host processor.

There are two modes of bus operation: Intel® nonmultiplexed mode (INM) and Motorola nonmultiplexed mode (MNM). The mode is selected based on the host processor and which mode is best suited for that processor. The microport has an 8-bit data bus (D[7:0]), 3-bit address bus (A[2:0]), three control pin lines ($\overline{CS}$, $\overline{DS}$ or $\overline{RD}$, and R/$\overline{W}$ or $\overline{WR}$), and one status pin ($\overline{DTACK}$ or RDY). The functionality of the control signals and status line changes slightly depending on the selected mode. Refer to the timing diagrams in Figure 10 through Figure 13 and the descriptions in the Programming Modes, Intel Nonmultiplexed Mode (INM), and Motorola Nonmultiplexed Mode (MNM) sections for details on the operation of each mode.

EXTERNAL MEMORY MAP

The external memory map is used to gain access to the channel address space. The 8-bit data and address buses are used to set the eight registers shown in Table 13. These registers are collectively referred to as the external interface registers because they control all access to the channel address space and global chip functions. The use of each register is described in Table 13.

Table 13. External Memory Map

Addr. (Hex)	Mnemonic	Bit No.	Description
7	Access Control Register (ACR)	7	Auto-increment
		6	Reserved (write low)
		5 to 2	Instruction [3:0]
		1 to 0	A[9:8]
6	Channel Address Register (CAR)	7 to 0	A[7:0]
5	Special Function Register 2 (SF2)	6	AGC sync enable
		5	DC correction sync enable
		4	PN sync enable
		3 to 1	Reserved
		0	Issue Soft_SYNC
4	Special Function Register 1 (SF1)	5	First sync only
		4	Enable edge- sensitivity
		3 to 1	Reserved
		0	Enable Pin_SYNC
3	Special Function Register 0 (SF0)	7 to 4	Reserved
		3	Status of Channel B
		2	Enable Channel B
		1	Status of Channel A
		0	Enable Channel A
2	Data Register 2 (DR2)	7 to 4	Reserved
		3 to 0	D[19:16]
1	Data Register 1 (DR1)	15 to 8	D[15:8]
0	Data Register 0 (DR0)	7 to 0	D[7:0]

ACCESS CONTROL REGISTER (ACR)

Bit 7 of the ACR register is the auto-increment bit. If this bit is set to 1, the CAR register, described in the Channel Address Register (CAR) section, increments in value after every access to the channel. This allows blocks of address space, such as coefficient memory, to be initialized more efficiently.

Bit 6 of the ACR register is unused and must be written low.

Bit 5 to Bit 2 of the ACR register are instruction bits that allow multiple AD6650s to receive the same write access. The instruction bits allow a single or multiple (up to four) AD6650 chip(s) to be configured simultaneously. There are seven possible instructions that are defined in Table 14, where x represents disregarded values in the digital decoding.

If multiple AD6650 chips are using the same $\overline{CS}$ line, readback is not valid because of the potential for bus contention. Therefore, if device readback capability is desired, the $\overline{CS}$ lines should be separated for individual control. To facilitate device debug and verification, the use of separate $\overline{CS}$ lines for each AD6650 is recommended.

Bit 1 to Bit 0 of the ACR register are address bits that decode which channel is to be accessed. Because the channels of the AD6650 cannot be programmed independently, these bits should be set to 0.

CHANNEL ADDRESS REGISTER (CAR)

The CAR register represents the 8-bit internal address of each channel. If the auto-increment bit of the ACR is 1, this value is incremented after every access to the DR0 register, which in turn accesses the location pointed to by this address.

SPECIAL FUNCTION REGISTERS

The AD6650 has three special function registers, SF0, SF1, and SF2, that control synchronizing and enabling of the channels. SF0 controls channel enabling, SF1 controls Pin_SYNC, and SF2 controls Soft_SYNC. For SF0, Bit 0 and Bit 2 allow Channel A and Channel B, respectively, to exit sleep mode by the method selected in SF1. Bit 1 and Bit 3 are read-only bits and indicate whether Channel A and Channel B, respectively, are active. A 1 indicates that the channel is active, and a 0 indicates that it is not active. Bits 4 through Bit 7 are unused.

For SF1, if Bit 0 is set to 1, both channels wait for a pulse to appear on the SYNC pin before exiting sleep mode; otherwise, the channels assume a soft start is desired and wait for the start holdoff counter to issue a sync. When Bit 5 is set, both channels ignore all subsequent attempts to resync once they have exited sleep mode.

Table 14. Microport Instructions

Instruction	Description
0xxx	All chips obtain access.
1000	All chips with Chip_ID [1:0] = x0 obtain access.[1]
1001	All chips with Chip_ID [1:0] = x1 obtain access.[1]
1100	All chips with Chip_ID [1:0] = 00 obtain access.[1]
1101	All chips with Chip_ID [1:0] = 01 obtain access.[1]
1110	All chips with Chip_ID [1:0] = 10 obtain access.[1]
1111	All chips with Chip_ID [1:0] = 11 obtain access.[1]

[1] Bits A[9:8] control which channel is decoded for the access.

For SF2, Bit 0 prompts the startup block to run the start hold-off counter from the value programmed in the start holdoff counter control register and to issue a sync when this task is complete. Bit 4 to Bit 6 are used to enable syncs to individual blocks in the channels.

DATA ADDRESS REGISTERS

External Addresses [2:0] form Data Register DR2, Data Register DR1, and Data Register DR0, respectively. All internal data-words have widths that are less than or equal to 22 bits. Access to DR0 triggers an internal access to the AD6650 based on the address indicated in ACR and CAR. Therefore, during writes to the internal registers, DR0 must be written last. At this point, data is transferred to the internal memory location indicated in A[9:0]. Reads are performed in the reverse sequence. Once the address is set, DR0 must be the first data register read to initiate an internal access. DR2 is only six bits wide. Data written to the upper two bits of this register is ignored. Likewise, reading from this register produces only 6 LSBs.

WRITE SEQUENCING

Writing to an internal location is achieved by first writing the upper two bits of the address into Bit 1 and Bit 0 of the ACR (these bits should be set low). Bits[5:2] can be set to select the chips for access as indicated above. The CAR is then written with the lower eight bits of the internal address (it does not matter if the CAR is written to before the ACR, as long as both are written to before the internal access). DR2 and DR1 must be written first because the write to Data Register DR0 triggers the internal access. DR0 must always be the last register written to initiate the internal write.

READ SEQUENCING

Reading from the microport is accomplished in the same manner. The internal address is set up the same way as it is for a write. A read from DR0 activates the internal read; therefore, DR0 must be read first to initiate an internal read followed by reads from DR1 and DR2.

READ/WRITE CHAINING

The microport of the AD6650 allows multiple accesses while $\overline{CS}$ is held low ($\overline{CS}$ can be tied permanently low if the microport is not shared with additional devices). The user can access multiple locations by pulsing the $\overline{WR}$ or $\overline{RD}$ line and changing the contents of the external 3-bit address bus. Access to the external registers listed in Table 13 is accomplished in one of two modes using the $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, and MODE inputs. The access modes are INM mode and MNM mode. These modes are controlled by the MODE input (MODE = 0 for INM, MODE = 1 for MNM). $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ control the access type for each mode.

PROGRAMMING MODES

The AD6650 can be programmed using several different modes. These modes include two microport modes, INM mode and MNM mode. The programming mode is selected by setting the MODE pins. Table 15 identifies how to set the MODE pins to select the desired programming mode.

Table 15. Programming Modes

MODE [2:0]	Description
000	Microport Intel nonmultiplexed mode
001	Microport Motorola nonmultiplexed mode
010	Reserved
011	Reserved
100	Reserved
101	Reserved
110	Reserved
111	Reserved

Intel Nonmultiplexed Mode (INM)

Setting the mode word bits to 000 places the AD6650 in INM mode. The access is controlled by the user with the $\overline{CS}$, $\overline{RD}$ ($\overline{DS}$), and $\overline{WR}$ (R/$\overline{W}$) inputs. The RDY ($\overline{DTACK}$) signal is produced by the microport to communicate to the user that an access has been completed. RDY ($\overline{DTACK}$) goes low at the start of the access and is released when the internal cycle is complete. See Figure 10 and Figure 11 for INM mode read and write timing.

Motorola Nonmultiplexed Mode (MNM)

Setting the mode word bits to 001 places the AD6650 in MNM mode. The access type is controlled by the user with the $\overline{CS}$, $\overline{DS}$ ($\overline{RD}$), and R/$\overline{W}$ ($\overline{WR}$) inputs. The $\overline{DTACK}$ (RDY) signal is generated by the microport to signal the user that an access has been completed. $\overline{DTACK}$ (RDY) goes low when an internal access is complete and returns high after $\overline{DS}$ ($\overline{RD}$) is deasserted. See Figure 12 and Figure 13 for MNM mode read and write timing.

JTAG BOUNDARY SCAN

The AD6650 supports a subset of the IEEE Standard 1149.1 specification. For details of the standard, see the *IEEE Standard Test Access Port and Boundary-Scan Architecture*, an IEEE-1149 publication.

The AD6650 has five pins associated with the JTAG interface. These pins, listed in Table 16, are used to access the on-chip test access port. All input JTAG pins are pull-ups except TCLK, which is a pull-down.

Table 16. Boundary Scan Test Pins

Mnemonic	Description
$\overline{\text{TRST}}$	Test access port reset
TCLK	Test clock
TMS	Test access port mode select
TDI	Test data input
TDO	Test data output

The AD6650 supports three op codes, listed in Table 17. These instructions set the mode of the JTAG interface.

Table 17. Boundary Scan Op Codes

Instruction	Op Code
Bypass	11
Sample/Preload	01
Extest	00

A boundary scan description language (BSDL) file for this device is available. Contact an Analog Devices sales representative for more information.

Bypass (2'b11)

The bypass instruction allows the IC to remain in normal functional mode and selects a 1-bit bypass register between TDI and TDO. During this instruction, serial data is transferred from TDI to TDO without affecting operation of the IC.

Sample/Preload (2'b01)

The sample/preload instruction allows the IC to remain in normal functional mode and selects the boundary scan register to be connected between TDI and TDO. The boundary scan register can be accessed by a scan operation to take a sample of the functional data entering and leaving the IC. Also, test data can be preloaded into the boundary-scan register before an extest instruction.

Extest (2'b00)

The extest instruction places the IC into an external boundary-test mode and selects which boundary scan register is connected between TDI and TDO. During this operation, the boundary scan register is accessed to drive test data off-chip via boundary outputs and receive test data off-chip from boundary inputs.

REGISTER MAP

Table 18. Memory Map

Reg. (Hex)	Mnemonic	Bit Width	Description	Additional Information	
				Code	**Result**
0	Clock Divider Control	1	Power-up value is 1'b1.	0	Bypass
				1	Divide-by-2
1	PLL Register 0	22	PLL Control Register 0.	See Table 19	
2	PLL Register 1	22	PLL Control Register 1.	See Table 20	
3	PLL Register 2	22	PLL Control Register 2.	See Table 21	
4	PLL Register 3	22	PLL Control Register 3.	See Table 22	
5	Clamp Control	6	Various VGA control signals.	Power-up value is 6'b100011	
				Code	**Gain (dB)**
	5 to 2: Tweak Gain	4	Provides ±1.6 dB of additional gain in VGA in 0.2 dB steps.	0	+1.6 dB
				1	+1.4 dB
				2	+1.2 dB
				.	.
				.	.
				7	+0.2 dB
				8	0 dB
				9	−0.2 dB
				.	.
				.	.
				14	−1.2 dB
				15	−1.4 dB
				Code	**Result**
	1: Clamp Disable B	1	Disables clamps at the output of the VGA for Channel B.	0	Enable clamp
				1	Disable clamp
	0: Clamp Disable A	1	Disables clamps at the output of the VGA for Channel A.	0	Enable clamp
				1	Disable clamp
6	Reserved	8	Reserved.	Must be written 8'b00000000	
7	Reserved	8	Reserved.	Must be written 8'b00000000	
8	Reserved	8	Reserved.	Must be written 8'b00010001	
9	Reserved	2	Must be written 0.	Power-up value is 2'b00	
A	Coarse DC Correction	4	Coarse dc correction control registers.	Power-up value is 4'b0000	
				Code	**Result**
	3: Cal Now B	1	Calibrate coarse dc correction for the Channel B. Coarse dc correction occurs automatically at start-up if Bit 0 of the AutoCalibration control register is set high.	0	Disabled
				1	Recalibrate
	2: Cal Now A	1	Calibrate coarse dc correction for the Channel A. Coarse dc correction occurs automatically at start-up if Bit 0 of the AutoCalibration control register is set high.	0	Disabled
				1	Recalibrate
	1: PN_EN	1	Enables the PN sequence generator to test the digital block.	0	Disabled
				1	Enable PN sequence generator
				Code	**Result**
	0: Coarse DCC Enable	1	Enables coarse DCC. This register must be held high during start-up sequence for coarse dc correction to occur.	0	Disabled
				1	DCC enabled

Reg. (Hex)	Mnemonic	Bit Width	Description	Additional Information	
B	DC Correction Control	20	Fine DCC control registers.	Power-up value is 20'b00000000000000000000	
	19 to 13: Upper Threshold	7	Fine DCC upper threshold. No new dc estimation is made if the signal is above the upper threshold.	**Code**	**Level (dBFS)**
				0	0 dBFS
				1	−0.75 dBFS
				2	−1.5 dBFS
				.	.
				.	.
				126	−94.5 dBFS
				127	−95.25 dBFS
	12 to 8: Lower Threshold	5	Fine DCC lower threshold. The maximum range for the lower limit is 0 dBFS to 138.46 dBFS.	0	0 dBFS
				1	−6.02 dBFS
				2	−12.04 dBFS
				.	.
				.	.
				22	−132.44 dBFS
				23	−138.46 dBFS
	7 to 3: Minimum Period	5	Fine DCC integration period.	**Code**	**Integration Time**
				1	$2^1 \times T_S$
				2	$2^2 \times T_S$
				3	$2^3 \times T_S$
				.	.
				.	.
				30	$2^{30} \times T_S$
				31	$2^{31} \times T_S$
					T_S = sample period
	2: Bypass	1	Fine DCC bypass.	**Code**	**Result**
				0	Update DCC estimate
				1	Keep old estimate
	1: Interpolate	1	Fine DCC interpolator reduces discontinuity between the current dc estimate and the new estimate.	0	Disabled
				1	Enabled
	0: Freeze	1	Fine DCC freeze is used to hold the current dc estimate.	0	Disabled
				1	Enabled
C	AGC Control 0	4	AGC Control Settings.		
	3: Force VGA Gain	1	Force the VGA gain to a specific value. This control line overrides the slow loop, fast decay loop, and fast attack loop when enabled.	**Code**	**Result**
				0	Disabled
				1	Enable forced gain mode
	2: FD_Enable	1	Fast decay loop enable.	0	Disabled
				1	Enable fast decay loop
	1: FA_Enable	1	Fast attack loop enable.	**Code**	**Result**
				0	Disabled
				1	Enable fast attack loop
	0: Reserved	1	Reserved.	N/A	

Reg. (Hex)	Mnemonic	Bit Width	Description	Additional Information	
D	AGC Control 1	9	VGA gain (dB) = (0.094) × VGA gain word.		
	8 to 0: VGA Gain		This drives the VGA directly when force VGA gain = 1.	**Code**	**Gain (dB)**
				0	0 dB
				1	0.094 dB
				2	0.188 dB
				.	.
				.	.
				382	35.9 dB
				383	36.002 dB
E	AGC Control 2	16	AGC hysteresis and requested level.		
	15 to 8: Hysteresis	8	Upper hysteresis threshold = requested level + hysteresis. Lower hysteresis threshold = requested level − hysteresis. The gain word does not change if the peak measurement falls between the upper and lower hysteresis threshold.	**Code**	**Hysteresis (dB)**
				0	0
				1	±.094 dB
				2	±.188 dB
				.	.
				.	.
				254	±23.876 dB
				255	±23.97 dB
	7 to 0: Requested Level	8	The requested level for the slow loop. The full-scale input into the AD6650 is 2 V p-p = 4 dBm.	**Code**	**Requested Level (dBm)**
				0	+4 dBm
				1	+3.906 dBm
				2	+3.812 dBm
				.	.
				.	.
				254	−19.8 dBm
				255	−19.97 dBm
F	AGC Control 3	11	Loop gain = (mantissa/256) × $\frac{1}{2}^{exponent}$.		
	10 to 8: Loop Gain Exponent	3	Loop gain exponent (slow loop).	**Code**	**Loop Gain Exp**
				0	2^0
				1	2^1
				.	.
				.	.
				6	2^6
				7	2^7
	7 to 6: Reserved	2	Reserved.	N/A	
	5 to 0: Loop Gain Mantissa	6	Loop gain mantissa (slow loop).	**Code**	**Mantissa**
				0	0
				1	1
				2	2
				.	.
				.	.
				62	62
				63	63

Reg. (Hex)	Mnemonic	Bit Width	Description	Additional Information	
10	AGC Control 4	13	Fast attack and fast decay loop parameters.		
	12 to 10: FD_Step	3	Fast decay step size.	**Code**	**Step size (dB)**
				0	0 dB
				1	0.094 dB
				2	0.188 dB
				.	.
				.	.
				6	0.564 dB
				7	0.658 dB
	9 to 8: FA_Thresh	2	Fast attack threshold measured at the antialiasing filters.	**Code**	**Threshold**
				0	−6.02 dBFS
				1	−3.1 dBFS
				2	−0.915 dBFS
				3	0 dBFS
	7 to 4: FA_Count	4	Fast attack count. The fast attack loop steps the gain down by FA_Step for FA_Count number of clock cycles.	**Code**	**Count**
				0	1
				1	2
				2	3
				.	.
				.	.
				14	14
				15	15
	3 to 0: FA_Step	4	Fast attack step size.	**Code**	**Step size (dB)**
				0	0 dB
				1	0.094 dB
				2	0.188 dB
				.	.
				.	.
				14	1.316 dB
				15	1.41 dB
11	AGC Control 5	16	Slow loop peak detector period.		
	15 to 8: SPB Peak Detector Period	8	Signal plus blocker peak detector period for the slow loop; f_S = 26 MHz; f_{SYM} =270.833 kHz; SPB peak period = ¼ × (f_{SAMP}/f_{SYM}).	**Code**	**Samples (f_S clock cycles)**
				0	0
				1	1
				2	2
				.	.
				.	.
				254	254
				255	255
	7 to 0: Reserved	8	Reserved.	Must be written 8′b00000000	
12	Reserved	7	Reserved.	Must be written 7′b0000000	
13	AGC Control 7			**Code**	**Threshold**
	8 to 0: FD SPB Threshold		Fast decay signal plus blocker threshold.	0	0 dBFS
				1	−0.094 dBFS
				2	−0.188 dBFS
				.	.
				.	.
				510	−47.94 dBFS
				511	−48.034 dBFS

Reg. (Hex)	Mnemonic	Bit Width	Description	Additional Information	
				Code	**Count**
14	Start Holdoff Counter	16	The power-up sequence is initiated with a Soft_SYNC or Pin_SYNC and then the start holdoff counter counts down to 1, and the chip power-up sequence starts. 0 is an invalid value.	1	1
				2	2
				.	.
				.	.
				65,534	65,534
				65,535	65,535
				Code	**Decimation**
15	CIC4 Decimation ($M_{CIC4} - 1$)	5	Should be ≥12 because CIC and IIR have maximum rates of 26 MHz/12.	7	8
				8	9
				9	10
				.	.
				.	.
				30	31
				31	32
				Code	**Scale Factor**
16	CIC4 Scale (Scale − 12)	4	Controls the attenuation of the data into the CIC4 stage in 6 dB increments. This register has a range of 12 to 20, which supports decimations from 8 to 32 according to Equation 4.	0	12
				1	13
				2	14
				.	.
				.	.
				7	19
				8	20
				Code	**Results**
17	IIR Control	1	Sync mask.	0	Disabled
				1	Enabled
				Code	**Decimation**
18	RCF Decimation Register ($M_{RCF} - 1$)	3	Decimation of 1 to 8.	0	1
				1	2
				2	3
				.	.
				.	.
				6	7
				7	8
				Code	**Phase**
19	RCF Decimation Phase (P_{RCF})	3	Phase from 0 to $M_{RCF} - 1$.	0	0
				1	1
				.	.
				.	.
				6	6
				7	7
				Code	**Offset**
1A	RCF Coefficient Offset (CO_{RCF})	6	Range is 0 to 48 taps.	0	0
				1	1
				2	2
				.	.
				.	.
				46	46
				47	47

Reg. (Hex)	Mnemonic	Bit Width	Description	Additional Information	
				Code	**Taps**
1B	RCF Taps (N_{Taps} − 1)	6	1 to 48.	0	1
				1	2
				.	.
				.	.
				46	47
				47	48
				Code	**Scale Factor**
1C	RCF Scale	2	0, −6 dB, −12 dB, and −18 dB gain adjust to prevent coefficients from clipping the MAC.	0	−18 dB
				1	−12 dB
				2	−6 dB
				3	0 dB
1D	BIST for A-I	24	16-bit data available, I/DATA_I.		
1E	BIST for A-Q	24	16-bit data available, Q/DATA_Q.		
1F	BIST for B-I	24	16-bit data available, I/DATA_I.		
20	BIST for B-Q	24	16-bit data available, Q/DATA_Q.		
21	Serial Control	9	Power-up value is 9'bxxxxx0xxx for Bit 3 to make it a serial slave.		
	8: Fine DCC Data to BIST	1	Data is available through the I/Q BIST registers when Bit 8 is high.		
				Code	**Results**
	7: B Data Serial Ouput Select	1	Port B data serial output select.	0	Use SDO0 for B data
				1	Use SDO1 for B data
	6 to 5: I_SDFS Control	2	Serial port control functions.	0	AI pulse
				1	AI, BI pulses
				2	AI, AQ, BI, BQ pulses
				3	High for SDO0 valid
	4: SOWL	1	Serial output word length.	0	16-bit words
				1	24-bit words
	3: SBM	1	Serial bus master.	0	Serial slave
				1	Serial bus master
	2 to 0: SDIV [2:0]	3	Serial divider.	0	Divide-by-1
				.	.
				.	.
				7	Divide-by-8
22	AutoCalibration Control	4	New calibration sequence control registers. Power-up value is 4'b0000.		
	3: Reserved	1	Reserved.	Must be written 0	
	2: Reserved	1	Reserved.	Must be written 1	
				Code	**Results**
	1: DAC Power-Down Disable	1	Power down VGA DACs during the power-up sequence to calibrate the dc offset.	0	Power down DACs
				1	DACs on
	0: Enable	1	Autocalibration enable.	0	Disabled
				1	Enabled
23 to 3F	Reserved				
40 to 6F	Coefficient Memory		Common coefficients for Channel A and Channel B.	48 × 20 bit RAM	
70 to FF	Reserved				

REGISTER DETAILS

Table 19. PLL Register 0: Control Latch

CH Address	Register	Description	Comment
DB21 to DB0	RSVD	Reserved	Must be written 00 0000 0111 1100 0100 0000 (MSB ... LSB).

Table 20. PLL Register 1: R Counter Latch

CH Address	Register	Description	Comment
DB21 to DB14	RSVD	Reserved	Must be written 0001 0100 (DB21 ... DB14).
DB13 to DB0	R1 to R14	14-bit reference counter, R	

Table 21. PLL Register 2: N Counter Latch

CH Address	Register	Description	Comment
DB21 to DB19	RSVD	Reserved	Must be written 000.
DB18 to DB6	B13 to B1	13-bit B counter	B13 to B1 programs the 13-bit B counter.
DB5	RSVD	Reserved	Must be written 0.
DB4 to DB0	A5-A1	5-bit A counter	A5 to A1 programs the 5-bit counter. The divide range is 0 (00000) to 31 (11111).

Table 22. PLL Register 3—Reserved

CH Address	Register	Bit Definitions	Comment
DB21 to DB0	RSVD	Reserved	Must be written 11 0001 1000 0000 0000 0000 (MSB ... LSB).

0x00: Clock Divider Control [1]

The clock divider control bit sets the internal clock rate for the AD6650. If this bit is set low and the clock rate is ≤52 MSPS, the internal divide-by-2 is bypassed. If a faster clock rate is desired, the clock divider control bit should be set high. By setting this bit high, the internal divide-by-2 is used.

0x01: PLL Control Register 0 [21:0]

This register is reserved and must be written 00 0000 0111 1100 0100 0000 (MSB ... LSB).

0x02: PLL Control Register 1 [21:0]

DB13 to DB0: These bits are used to set the R-counter for the PLL.

DB21 to DB14: These bits are reserved and must be written 0001 0100.

0x03: PLL Control Register 2 [21:0]

DB4 to DB0: This 5-bit register is used to set the value for the A counter in the PLL.

DB5: This bit is reserved and must be written to 0.

DB18 to DB6: This 13-bit register is used to set the value for the B-counter in the PLL.

DB21 to DB19: These bits are reserved and must be written 000.

0x04: PLL Control Register 3 [21:0]

This register is reserved and must be written 11 0001 1000 0000 0000 0000 (MSB ... LSB).

0x05: Clamp Control [5:0]

This register either enables or disables the clamps on the output of the mixers. These clamps should be enabled.

0x06: Reserved [8:0]

This register is reserved and must be written 00000000.

0x07: Reserved [8:0]

This register is reserved and must be written 00000000.

0x08: Reserved [8:0]

This register is reserved and must be written 00010001.

0x09: Reserved [1:0]

This register is reserved and should be written low.

0x0A: Coarse DC Correction Control Register [3:0]

Address 0xA is the coarse dc correction control register. It is used to enable the coarse correction with Bit 0 and to initiate calibrations on Channel A and/or Channel B. Bit 3 and Bit 2 of this register can be used to initiate coarse calibrations when the device is running and can be used in conjunction with an external switch if desired. Bit 1 is used to activate the internal pseudorandom noise generator, which is useful for looking at the digital filter response and performing the built-in self-test.

Table 23. Coarse DC Correction Control Functions

Bit No.	Description
3	Calibrate B
2	Calibrate A
1	PN_EN
0	CDCC enable

0xB: Fine DC Correction Filter [19:0]

The fine dc correction block is used to provide a good dc correction for small signals that are under the range of the AGC loop. Address 0xB has four parameters.

Table 24. Fine DC Correction Filter Functions

Bits	Description
19 to 13	Upper threshold
12 to 8	Lower threshold
7 to 3	Minimum period
2	Bypass
1	Interpolator enable
0	Freeze

Bit 19 to Bit 13

The upper threshold disables the fine dc correction algorithm for large input signals that could potentially contain significant dc content from the modulated data. This should be set below the range of the AGC loop, which is equal to the requested level of −36 dB. It should also be set above the uncorrected dc level so that the fine DCC is guaranteed to range.

The upper threshold should be set low enough so that the dc content is not estimated while the loop is ranging because the changing gain distorts the estimate. Setting the upper threshold lower also decreases effects from dc content in the signal such as dc offset from modulated data with high correlations or mobiles with LO feedthrough.

It is equally important not to set the upper threshold too low. If the upper threshold is set so low that the desired signal is consistently higher than this threshold, a new dc estimate, which is necessary to compensate for power supply or temperature drifts, will not occur. Therefore, a thorough understanding of the signal statistics for the application is required.

As a guideline, the upper threshold should be set between −40 dBFS and −70 dBFS. If it is set below −72 dBFS, the uncorrected dc offset from the analog front end and coarse correction can increase the effective minimum period because the peak detectors in the fine dc correction block ranges off the dc content as well as the signal of interest.

Bit 12 to Bit 8

The lower threshold determines where the minimum integration period is used. When the peak of the input to the fine dc correction block is lower than this level, the accumulators average 2^{Min_period} samples at the output rate (1 or 2 samples/symbol). When the peak of the signal increases above this, the integration periods increase by a factor of 4 for every 6 dB that the signal power increases.

It should be noted that any dc content left after the coarse correction can be seen by the fine dc correction peak detector and causes the integration period to change. For example, if the lower threshold is −96 dBFS and the dc content is −78 dBFS, the signal is at least 18 dB larger; therefore, the integration period is at least 64× (that is, $4^{(18/6)}$) the minimum period.

The lower threshold can be set near the upper threshold to provide a constant integration period of 2^{Min_period} if desired.

Bit 7 to Bit 3

This interval is equal to 2^{Min_period}. The minimum period determines the integration period when the peak signal power into the fine dc correction block is less than the lower threshold. This can be used in combination with the lower threshold to make sure there is enough integration to estimate the dc for small signals.

If Min_period is 12, the period of integration for a signal with power less than or equal to −96.32 dBFS is 4096 samples. For each 6.02 dBFS increase in the signal power, the integration period quadruples. The Min_period register can be programmed from 1 to 31; 0 is not a valid value for this register.

Bit 2

This is the bypass bit that effectively shuts down the fine dc correction block. When this bit is 1, no correction is performed.

Bit 1

This bit enables an interpolator that can smooth out the updated estimate transition by a fixed interpolation by 256. This is a linear interpolator that allows the correction block to gradually shift between the old estimate and the new estimate to avoid transients if there has been significant dc shift. If disabled, the shift in correction values happens instantaneously, causing a discontinuity in the signal; however, if the interpolator is enabled, this shift occurs over 256 samples, preventing any large discontinuities. The interpolator should not be enabled if Min_period is set to less than 8 (a period of 256 samples). Use of the interpolator is not recommended at this time, and this bit should be set to 0.

Bit 0

When set to 1, this bit freezes the estimate of the dc correction and resets the peak detector to the smallest possible signal state (−138 dB peak signal). This way, the dc can be estimated once

and constantly corrected. This is useful for debugging and for use when the dc estimate can be performed at discrete predefined times.

Even though the upper threshold register can vary between 0 and 15 and the Min_period register can vary between 1 and 31, only certain combinations of the two are valid. This is because the growth is restricted to 34 bits. Equation 23 can be used to determine if a combination of values is valid. If C < 0, the combination is invalid; otherwise, the combination is valid.

$$C = 34 - (2 \times (16 - \textit{Upper Threshold}) + \textit{Min_period}) \quad (23)$$

0x0C: AGC Control 0 [3:0]

Bit 3

The force VGA gain control register allows the user to force the VGA gain to a specific value. This control line overrides the slow loop, fast decay loop, and fast attack loop when enabled. By setting this bit low, the force VGA gain control is disabled. By setting this bit high, the force VGA gain control is enabled. For normal operation, this bit should be disabled.

Bit 2

By setting this bit high, the fast decay loop is enabled; by setting this bit low, the fast decay loop is disabled. It is recommended that the fast decay loop be enabled for normal operation. For a description of the fast decay functionality, see the AGC Loop/Relinearization section.

Bit 1

By setting this bit high, the fast attack loop is enabled; by setting this bit low, the fast attack loop is disabled. It is recommended that the fast decay loop be enabled for normal operation. For a description of the fast attack functionality, see the AGC Loop/Relinearization section.

Bit 0

This bit is reserved and should be written low.

0x0D: AGC Control 1 [8:0]

If the force VGA bit is enabled in AGC Control Register 0 (Bit 3 = 1), this register controls the gain setting for the VGA. The gain is controlled in 0.094 dB steps with a maximum gain of 36 dB. Code 0 corresponds to 0 dB gain or minimum gain, whereas Code 383 corresponds to 36 dB gain or maximum gain.

0x0E: AGC Control 2 [15:0]

The AGC Control 2 register is a 16-bit register that sets the amount of hysteresis used in the AGC loop and sets the requested level for the AGC loop.

Bit 15 to Bit 8

These upper bits set the hysteresis level in 0.094 dB steps. Code 0 corresponds to 0 dB of hysteresis, and Code 255 corresponds to ±23.97 dB of hysteresis.

Bit 7 to Bit 0

These lower eight bits set the requested level for the AGC slow loop. Setting the code to 0 sets the requested level to +4 dBm, which corresponds to the full-scale input of the AD6650. Setting the code to 255 sets the requested level to −19.97 dBm.

0x0F: AGC Control 3 [10:0]

Bit 10 to Bit 8

This 3-bit register sets the loop gain exponent for the slow loop of the AD6650 AGC. The values can range from 0 to 7. The equation for the loop gain is noted in the AGC Loop/Relinearization section.

Bit 7 to Bit 6

These two bits are reserved and should be written low.

Bit 5 to Bit 0

This 6-bit register represents the loop gain mantissa for the slow loop of the AD6650 AGC. The values for this register range from 0 to 63. The equation for the loop gain is noted in the AGC Loop/Relinearization section.

0x10: AGC Control 4 [12:0]

Bit 12 to Bit 10

This 3-bit register is used to set the fast decay step size. The gain continues to increase until it has reached the fast decay threshold or until the maximum gain has been reached.

Bit 9 to Bit 8

This 2-bit register sets the threshold for the fast attack AGC loop. When the desired signal reaches this threshold, the gain is reduced by the FA_Step for FA_Count number of clock cycles.

Bit 7 to Bit 4

The fast attack loop steps the gain down by FA_Step for FA_Count number of clock cycles.

Bit 3 to Bit 0

The FA_Step register determines how large a step to take once the fast attack threshold has been reached. This value is expressed in decibels.

0x11: AGC Control 5 [15:0]

Bit 15 to Bit 8

This 8-bit register sets the signal plus blocker peak detector period for the AGC slow loop. It can be set from 0 to 255 samples.

Bit 7 to Bit 0

Reserved and must be written 00000000.

0x12: Reserved [6:0]

This register is reserved and must be written 0000000.

0x13: AGC Control 7 [8:0]

This 9-bit register is used to set the threshold for the fast decay signal plus blocker. Values can range from 0 dBFS to −48 dBFS.

The peak detector for this threshold monitors the desired signal and blocker peaks at the ADC output.

0x14: Start Holdoff Counter [15:0]

The start holdoff counter is loaded with the value written to this address when a sync is initiated. It can be initiated by either a Soft_SYNC or Pin_SYNC. The counter begins decrementing, and when it reaches a value of 1, the channel exits sleep mode and begins processing data. If this register is written 1, the start occurs immediately when the SYNC comes into the channel. If it is written 0, no SYNC occurs.

0x15: CIC4 Decimation Minus One (M_{CIC4} – 1) [4:0]

This register is used to set the decimation in the CIC4 filter. The value written to this register is the decimation minus one. The value of this register should be 12 or greater because the CIC and IIR have maximum rates of 26 MHz/12. Although this is a 5-bit register, the decimation is usually limited to between 12 and 32. Decimations higher than 32 require more scaling than the CIC4's capability.

0x16: CIC4 Scale [3:0]

The CIC4 scale factor is used to compensate for the growth of the CIC4 filter. See the Fourth-Order Cascaded Integrator Comb Filter (CIC4) section for details.

0x17: IIR Control Register [1]

Address 0x17 is the IIR control register. When this bit is set to 0, the sync mask is disabled. In this mode, after a SYNC is issued to the AD6650, the IIR data path is not cleared. If the sync mask is enabled, the bit is set to 1, and the data path is cleared of its contents and starts accumulating new data on the first valid clock after a Soft_SYNC or Pin_SYNC is issued.

0x18: RCF Decimation Register Minus One (M_{RCF} – 1) [2:0]

This register is used to set the decimation of the RCF stage. The value written is the decimation minus one. This is a 3-bit register that allows decimations up to 8.

0x19: RCF Decimation Phase (P_{RCF}) [2:0]

This register allows any one of the MRCF phases of the filter to be used and can be adjusted dynamically. Each time a filter is started, this phase is updated. When a channel is synchronized, it retains the phase setting selected. This can be used as part of a timing recovery loop with an external processor or can allow multiple RCFs to work together while using a single RCF pair. See the RAM Coefficient Filter section for more details.

0x1A: RCF Coefficient Offset (CO_{RCF}) [5:0]

This register is used to specify which section of the 256-word coefficient memory is used for a filter. It can be used to select among multiple filters that are loaded into memory and referenced by this pointer. This register is shadowed and the filter pointer is updated every time a new filter is started. This allows the coefficient offset to be written even while a filter is being computed without disturbing operation. The next sample that comes out of the RCF will be with the new filter.

0x1B: RCF Taps Minus One (N_{TAPS} – 1) [5:0]

The number of taps for the RCF filter minus one is written to this register.

0x1C: RCF Scale Register [1:0]

This 2-bit register represents the output scale factor of the RCF. This register is used to scale the output data between 0 dB and −18 dB in 6 dB steps.

0x1D to 0x20: BIST Register [23:0]

These four registers allow the complete digital functionality of the I and Q data path in the A and B channels to be tested in the system. See the User-Configurable Built-In Self-Test (BIST) section for more details.

0x21: Serial Control Register [8:0]

This register controls the serial port of the AD6650 and determines the output format.

Bit 8

Fine DCC data to BIST.

Bit 7

If this bit is enabled (set high), Channel B data is output on Serial Data Output 1 (SDO1).

Bit 6 to Bit 5

Choose the serial data frame sync (SDFS) mode. See the Serial Data Frame Sync section for a full description of each mode. The following bits select the corresponding mode.

Table 25. Serial Port Control Functions

Bits	Description
11	High for SDO0 valid
10	AI, AQ, BI, BQ pulses
01	AI, BI pulses
00	AI pulse

Bit 4

By setting this bit low, the output data stream is 16-bit I and 16-bit Q data-words for both the A and B channels. By setting this bit high, the output data stream is 24-bit I and 24-bit Q data words for both the A and B chan nels. To fully realize the dynamic range of the AD6650, it is recommended that the 24-bit mode be used.

Bit 3

By setting this bit high, the AD6650 becomes the serial bus master. It is recommended that this bit be enabled (set high).

Bit 2 to Bit 0

This 3-bit register controls the divider on the serial clock (SCLK) on the output of the AD6650. It is possible to divide the SCLK by 8, allowing a flexible interface to a DSP or FPGA.

0x22: Autocalibration Register [3:0]

Address 0x22 is the autocalibration register and controls the automatic coarse dc autocalibration at start-up.

Bit 3

Reserved. This bit should be set to 0.

Bit 2

Reserved. This bit should be set to 1.

Bit 1

Determines whether to power down the VGA and mixer on a coarse calibration. This should be set to 0 to allow the state machine to power down the VGA and mixer. If it is known that there is no dc input into the part, this can be set to 1 to improve the correction performance, which allows more flexibility in setting the lower threshold.

Bit 0

Enables the autocalibration. This should be set to 1 for the calibration to run automatically. Then the AD6650 waits approximately 20.63 ms after a Soft_SYNC or Pin_SYNC enables the part and then runs a coarse dc calibration. This allows some warm-up time for the analog path to thermally stabilize.

0x23 to 0x3F: Reserved

These registers must not be written.

0x40 to 0x6F: Coefficient Memory

This memory is utilized to store up to forty-eight 20-bit RCF coefficients shared by Channel A and Channel B.

0x70 to 0xFF: Reserved

These registers must not be written.

OUTLINE DIMENSIONS

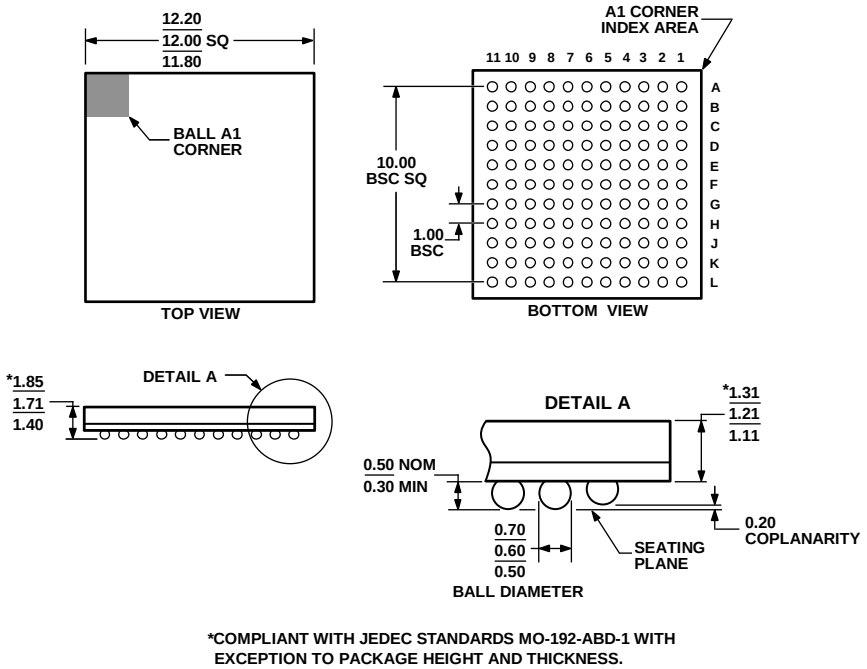


Figure 42. 121-Lead Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-121)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range[1]	Package Description	Package Option
AD6650ABC	−25°C to +85°C	121-Lead Chip Scale Package Ball Grid Array [CSP_BGA]	BC-121
AD6650ABCZ[2]	−25°C to +85°C	121-Lead Chip Scale Package Ball Grid Array [CSP_BGA]	BC-121
AD6650BBC	−25°C to +85°C	121-Lead Chip Scale Package Ball Grid Array [CSP_BGA]	BC-121
AD6650BBCZ[2]	−25°C to +85°C	121-Lead Chip Scale Package Ball Grid Array [CSP_BGA]	BC-121
AD6650/PCB		Evaluation Board with AD6650 and Software	

[1] The AD6650 is guaranteed fully functional from −40°C to +85°C. All ac minimum specifications are guaranteed from −25°C to +85°C, but degrade slightly from −25°C to −40°C.
[2] Z = Pb-free part.

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D03683-0-1/07(A)