4-Channel, 104 MSPS Digital Transmit Signal Processor (TSP)

AD6623

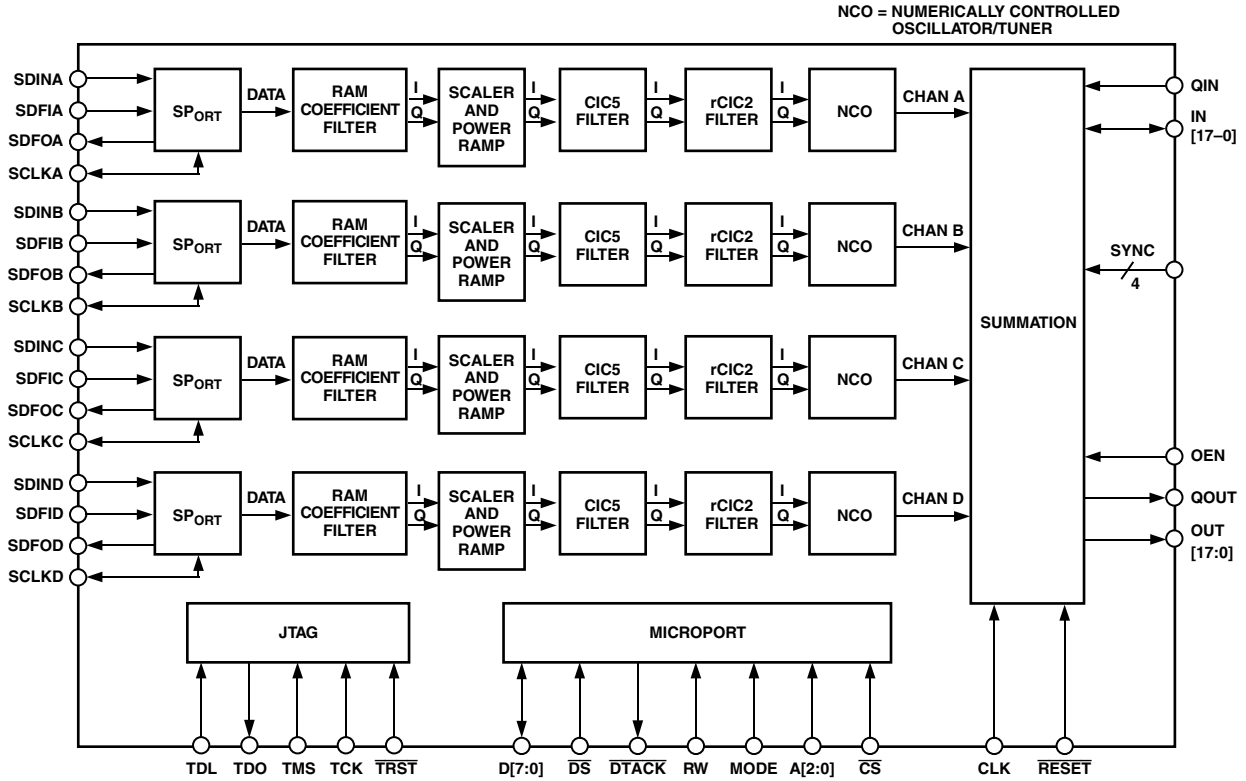
FEATURES

- Pin Compatible to the AD6622
- 18-Bit Parallel Digital IF Output
  - Real or Interleaved Complex
- 18-Bit Bidirectional Parallel Digital IF Input/Output
  - Allows Cascade of Chips for Additional Channels
  - Clipped or Wrapped Over Range
  - Two's Complement or Offset Binary Output
- Four Independent Digital Transmitters in Single Package
- RAM Coefficient Filter (RCF)
  - Programmable IF and Modulation for Each Channel
  - Programmable Interpolating RAM Coefficient Filter
  - $\pi/4$-DQPSK Differential Phase Encoder
  - $3\pi/8$-PSK Linear Encoder
  - 8-PSK Linear Encoder
  - Programmable GMSK Look-Up Table
  - Programmable QPSK Look-Up Table
  - All-Pass Phase Equalizer
  - Programmable Fine Scaler
  - Programmable Power Ramp Unit
- High Speed CIC Interpolating Filter
- Digital Resampling for Noninteger Interpolation Rates
- NCO Frequency Translation
  - Carrier Output from DC to 52 MHz
  - Spurious Performance Better than –100 dBc
- Separate 3-Wire Serial Data Input for Each Channel
  - Bidirectional Serial Clocks and Frames
- Microprocessor Control
- 2.5 V CMOS Core, 3.3 V Outputs, 5 V Inputs
- JTAG Boundary Scan

APPLICATIONS

- Cellular/PCS Base Stations
- Micro/Pico Cell Base Stations
- Wireless Local Loop Base Stations
- Multicarrier, Multimode Digital Transmit
  - GSM, EDGE, IS136, PHS, IS95, TDS CDMA, UMTS, CDMA2000
- Phased Array Beam Forming Antennas
- Software Defined Radio
  - Tuning Resolution Better than 0.025 Hz
  - Real or Complex Outputs

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT DESCRIPTION

The AD6623 is a 4-channel Transmit Signal Processor (TSP) that creates high bandwidth data for Transmit Digital-to-Analog Converters (TxDACs) from baseband data provided by a Digital Signal Processor (DSP). Modern TxDACs have achieved sufficiently high sampling rates, analog bandwidth, and dynamic range to create the first Intermediate Frequency (IF) directly. The AD6623 synthesizes multicarrier and multistandard digital signals to drive these TxDACs. The RAM-based architecture allows easy reconfiguration for multimode applications. Modulation, pulse-shaping and anti-imaging filters, static equalization, and tuning functions are combined in a single, cost-effective device. Digital IF signal processing provides repeatable manufacturing, higher accuracy, and more flexibility than comparable high dynamic range analog designs.

The AD6623 has four identical digital TSPs complete with synchronization circuitry and cascadable wideband channel summation. AD6623 is pin compatible to AD6622 and can operate in AD6622-compatible control register mode.
The AD6623 utilizes a 3.3 V I/O power supply and a 2.5 V core power supply. All I/O pins are 5 V tolerant. All control registers and coefficient values are programmed through a generic microprocessor interface. Intel and Motorola microprocessor bus modes are supported. All inputs and outputs are LVCMOS compatible.

FUNCTIONAL OVERVIEW

Each TSP has five cascaded signal processing elements: a programmable interpolating RAM Coefficient Filter (RCF), a programmable Scale and Power Ramp, a programmable fifth order Cascaded Integrator Comb (CIC5) interpolating filter, a flexible second order Resampling Cascaded Integrator Comb filter (rCIC2), and a Numerically Controlled Oscillator/Tuner (NCO).

The outputs of the four TSPs are summed and scaled on-chip. In multicarrier wideband transmitters, a bidirectional bus allows the Parallel (wideband) IF Input/Output to drive a second DAC. In this operational mode two AD6623 channels drive one DAC and the other two AD6623 channels drive a second DAC. Multiple AD6623s may be combined by driving the INOUT[17:0] of the succeeding with the OUT[17:0] of the preceding chip. The INOUT[17:0] can alternatively be masked off by software to allow preceding AD6623's outputs to be ignored.

Each channel accepts input data from independent serial ports that may be connected directly to the serial port of Digital Signal Processor (DSP) chips.

The RCF implements any one of the following functions: Interpolating Finite Impulse Response (FIR) filter, $\pi/4$-DQPSK modulator, 8-PSK modulator, or $3\pi/8$-8-PSK modulator, GMSK modulator, and QPSK modulator. Each AD6623 channel can be dynamically switched between the GMSK modulation mode and the $3\pi/8$-8-PSK modulation mode in order to support the GSM/EDGE standard. The RCF also implements an Allpass Phase Equalizer (APE) which meets the requirements of IS-95-A/B standard (CDMA transmission).

The programmable Scale and Power Ramp block allows power ramping on a time-slot basis as specified for some air-interface standards (e.g., GSM, EDGE). A fine scaling unit at the programmable FIR filter output allows an easy signal amplitude level adjustment on time slot basis.

The CIC5 provides integer rate interpolation from 1 to 32 and coarse anti-image filtering. The rCIC2 provides fractional rate interpolation from 1 to 4096 in steps of 1/512. The wide range of interpolation factors in each CIC filter stage and a highly flexible resampler incorporated into rCIC2 makes the AD6623 useful for creating both narrowband and wideband carriers in a high-speed sample stream.

The high resolution 32-bit NCO allows flexibility in frequency planning and supports both digital and analog air interface standards. The high speed NCO tunes the interpolated complex signal from the rCIC2 to an IF channel. The result may be real or complex. Multicarrier phase synchronization pins and phase offset registers allow intelligent management of the relative phase of independent RF channels. This capability supports the requirements for phased array antenna architectures and management of the wideband peak/power ratio to minimize clipping at the DAC.

The wideband Output Ports can deliver real or complex data. Complex words are interleaved into real (I) and imaginary (Q) parts at half the master clock rate.

AD6623–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	Test Level	AD6623 Min	AD6623 Typ	AD6623 Max	Unit
VDD	IV	2.25	2.5	2.75	V
VDDIO	IV	3.0	3.3	3.6	V
$T_{AMBIENT}$	IV	–40	+25	+85	°C

ELECTRICAL CHARACTERISTICS

Parameter (Conditions)	Temp	Test Level	Min	Typ	Max	Unit
LOGIC INPUTS (5 V TOLERANT)						
Logic Compatibility	Full			3.3 V CMOS		
Logic "1" Voltage	Full	IV	2.0		5.0	V
Logic "0" Voltage	Full	IV	–0.3		+0.8	V
Logic "1" Current	Full	IV		1	10	µA
Logic "0" Current	Full	IV		0	10	µA
Input Capacitance	25°C	V		4		pF
LOGIC OUTPUTS						
Logic Compatibility	Full			3.3 V CMOS/TTL		
Logic "1" Voltage (I_{OH} = 0.25 mA)	Full	IV	2.0	VDD – 0.2		V
Logic "0" Voltage (I_{OL} = 0.25 mA)	Full	IV		0.2	0.4	V
IDD SUPPLY CURRENT						
GSM Example: CORE		V		232		mA
I/O				56		mA
IS-136 Example: CORE		V		207		mA
I/O				55		mA
WBCDMA Example		V		TBD		mA
Sleep Mode	Full	IV		TBD		mA
POWER DISSIPATION						
GSM Example		V		740		mW
IS-136 Example		V		700		mW
WBCDMA Example		V		TBD		mW
Sleep Mode	Full	IV		TBD		mW

See the Thermal Management section of the data sheet for further details.

GENERAL TIMING CHARACTERISTICS[1, 2]

Parameter (Conditions)		Temp	Test Level	AD6623AS Min	Typ	Max	Unit
CLK Timing Requirements:							
t_{CLK}	CLK Period	Full	I	9.6			ns
t_{CLKL}	CLK Width Low	Full	IV	3			ns
t_{CLKH}	CLK Width High	Full	IV	3	$0.5 \times t_{CLK}$		ns
$\overline{RESET}$ Timing Requirement:							
t_{RESL}	$\overline{RESET}$ Width Low	Full	I	30.0			ns
Input Data Timing Requirements:							
t_{SI}	INOUT[17:0], QIN to ↑CLK Setup Time	Full	IV	1			ns
t_{HI}	INOUT[17:0], QIN to ↑CLK Hold Time	Full	IV	2			ns
Output Data Timing Characteristics:							
t_{DO}	↑CLK to OUT[17:0], INOUT[17:0], QOUT Output Delay Time	Full	IV	2		6	ns
t_{DZO}	OEN HIGH to OUT[17:0] Active	Full	IV	3		7.5	ns
SYNC Timing Requirements:							
t_{SS}	SYNC(0, 1, 2, 3) to ↑CLK Setup Time	Full	IV	1			ns
t_{HS}	SYNC(0, 1, 2, 3) to ↑CLK Hold Time	Full	IV	2			ns
Master Mode Serial Port Timing Requirements (SCS = 0): Switching Characteristics[3]							
t_{DSCLK1}	↑CLK to ↑SCLK Delay (divide by 1)	Full	IV	4		10.5	ns
t_{DSCLKH}	↑CLK to ↑SCLK Delay (for any other divisor)	Full	IV	5		13	ns
t_{DSCLKL}	↑CLK to ↓SCLK Delay (divide by 2 or even number)	Full	IV	3.5		9	ns
$t_{DSCLKLL}$	↓CLK to ↓SCLK Delay (divide by 3 or odd number)	Full	IV	4		10	ns
	Channel is Self-Framing						
t_{SSDI0}	SDIN to ↑SCLK Setup Time	Full	IV	1.7			ns
t_{HSDI0}	SDIN to ↑SCLK Hold Time	Full	IV	0			ns
t_{DSFO0A}	↑SCLK to SDFO Delay	Full	IV	0.5		3.5	ns
	Channel is External-Framing						
t_{SSFI0}	SDFI to ↑SCLK Setup Time	Full	IV	2			ns
t_{HSFI0}	SDFI to ↑SCLK Hold Time	Full	IV	0			ns
t_{SSDI0}	SDIN to ↑SCLK Setup Time	Full	IV	2			ns
t_{HSDI0}	SDIN to ↑SCLK Hold Time	Full	IV	0			ns
t_{DSFO0B}	↑SCLK to SDFO Delay	Full	IV	0.5		3	ns
Slave Mode Serial Port Timing Requirements (SCS = 1): Switching Characteristics[3]							
t_{SCLK}	SCLK Period	Full	IV		$2 \times t_{CLK}$		ns
t_{SCLKL}	SCLK Low Time	Full	IV	3.5			ns
t_{SCLKH}	SCLK High Time	Full	IV	3.5			ns
	Channel is Self-Framing						
t_{SSDH}	SDIN to ↑SCLK Setup Time	Full	IV	1			ns
t_{HSDH}	SDIN to ↑SCLK Hold Time	Full	IV	2.5			ns
t_{DSFO1}	↑SCLK to SDFO Delay	Full	IV	4		10	ns
	Channel is External-Framing						
t_{SSFI1}	SDFI to ↑SCLK Setup Time	Full	IV	2			ns
t_{HSFI1}	SDFI to ↑SCLK Hold Time	Full	IV	1			ns
t_{SSDI1}	SDIN to ↑SCLK Setup Time	Full	IV	1			ns
t_{HSDI1}	SDIN to ↑SCLK Hold Time	Full	IV	2.5			ns
t_{DSFO1}	↓SCLK to SDFO Delay	Full	IV	10			ns

NOTES

[1]All Timing Specifications valid over VDD range of 2.375 V to 2.675 V and VDDIO range of 3.0 V to 3.6 V.

[2]C_{LOAD} = 40 pF on all outputs (unless otherwise specified).

[3]The timing parameters for SCLK, SDIN, SDFI, SDFO, and SYNC apply to all four channels (A, B, C, and D).

Specifications subject to change without notice.

MICROPROCESSOR PORT TIMING CHARACTERISTICS[1, 2]

Parameter (Conditions)		Temp	Test Level	AD6623AS Min	Typ	Max	Unit
MICROPROCESSOR PORT, MODE INM (MODE = 0)							
MODE INM Write Timing:							
t_{SC}	Control[3] to ↑CLK Setup Time	Full	IV	4.5			ns
t_{HC}	Control[3] to ↑CLK Hold Time	Full	IV	2.0			ns
t_{HWR}	$\overline{WR}$(RW) to RDY($\overline{DTACK}$) Hold Time	Full	IV	8.0			ns
t_{SAM}	Address/Data to $\overline{WR}$(RW) Setup Time	Full	IV	3.0			ns
t_{HAM}	Address/Data to RDY($\overline{DTACK}$) Hold Time	Full	IV	2.0			ns
t_{DRDY}	$\overline{WR}$(RW) to RDY($\overline{DTACK}$) Delay	Full	IV	4.0			ns
t_{ACC}	$\overline{WR}$(RW) to RDY($\overline{DTACK}$) High Delay	Full	IV	$4 \times t_{CLK}$	$5 \times t_{CLK}$	$9 \times t_{CLK}$	ns
MODE INM Read Timing:							
t_{SC}	Control[3] to ↑CLK Setup Time	Full	IV	4.5			ns
t_{HC}	Control[3] to ↑CLK Hold Time	Full	IV	2.0			ns
t_{SAM}	Address to $\overline{RD}$($\overline{DS}$) Setup Time	Full	IV	3.0			ns
t_{HAM}	Address to Data Hold Time	Full	IV	2.0			ns
t_{ZOZ}	Data Three-State Delay	Full	IV				ns
t_{DD}	RDY($\overline{DTACK}$) to Data Delay	Full	IV				ns
t_{DRDY}	$\overline{RD}$($\overline{DS}$) to RDY($\overline{DTACK}$) Delay	Full	IV	4.0			ns
t_{ACC}	$\overline{RD}$($\overline{DS}$) to RDY($\overline{DTACK}$) High Delay	Full	IV	$8 \times t_{CLK}$	$10 \times t_{CLK}$	$13 \times t_{CLK}$	ns
MICROPROCESSOR PORT, MOTOROLA (MODE = 1)							
MODE MNM Write Timing:							
t_{SC}	Control[3] to ↑CLK Setup Time	Full	IV	4.5			ns
t_{HC}	Control[3] to ↑CLK Hold Time	Full	IV	2.0			ns
t_{HDS}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Hold Time	Full	IV	8.0			ns
t_{HRW}	RW($\overline{WR}$) to $\overline{DTACK}$(RDY) Hold Time	Full	IV	8.0			ns
t_{SAM}	Address/Data to RW($\overline{WR}$) Setup Time	Full	IV	3.0			ns
t_{HAM}	Address/Data to RW($\overline{WR}$) Hold Time	Full	IV	2.0			ns
t_{DDTACK}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Delay						ns
t_{ACC}	RW($\overline{WR}$) to $\overline{DTACK}$(RDY) Low Delay	Full	IV	$4 \times t_{CLK}$	$5 \times t_{CLK}$	$9 \times t_{CLK}$	ns
MODE MNM Read Timing:							
t_{SC}	Control[3] to ↑CLK Setup Time	Full	IV	4.0			ns
t_{HC}	Control[3] to ↑CLK Hold Time	Full	IV	2.0			ns
t_{HDS}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Hold Time	Full	IV	8.0			ns
t_{SAM}	Address to $\overline{DS}$($\overline{RD}$) Setup Time	Full	IV	3.0			ns
t_{HAM}	Address to Data Hold Time	Full	IV	2.0			ns
t_{ZD}	Data Three-State Delay	Full	IV				ns
t_{DD}	$\overline{DTACK}$(RDY) to Data Delay	Full	IV				ns
t_{DDTACK}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Delay	Full	IV				ns
t_{ACC}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Low Delay	Full	IV	$8 \times t_{CLK}$	$10 \times t_{CLK}$	$13 \times t_{CLK}$	ns

NOTES
[1]All Timing Specifications valid over VDD range of 2.375 V to 2.675 V and VDDIO range of 3.0 V to 3.6 V.
[2]C_{LOAD} = 40 pF on all outputs (unless otherwise specified).
[3]Specification pertains to control signals: RW, ($\overline{WR}$), $\overline{DS}$, ($\overline{RD}$), $\overline{CS}$.

Specifications subject to change without notice.

TIMING DIAGRAMS

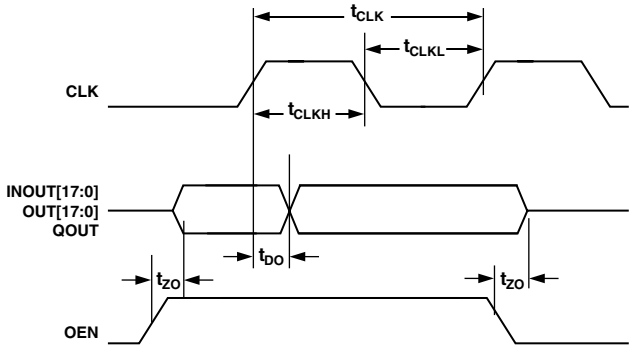


Figure 1. Parallel Output Switching Characteristics



Figure 4. $\overline{RESET}$ Timing Requirements

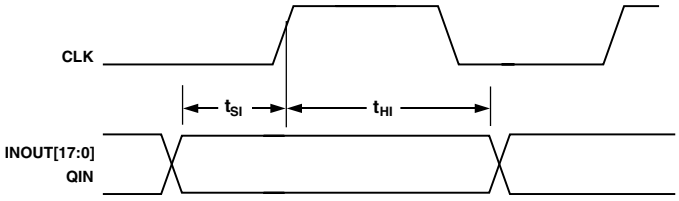


Figure 2. Wideband Input Timing

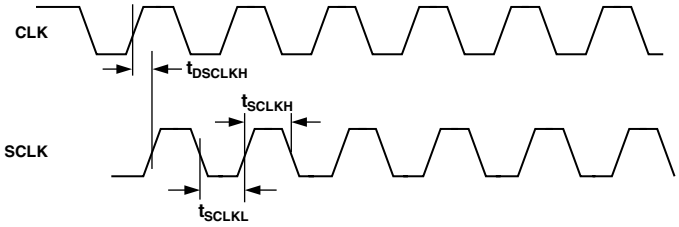


Figure 5. SCLK Switching Characteristics (Divide by 1)

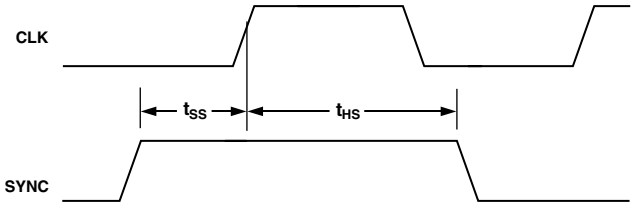


Figure 3. SYNC Timing Inputs

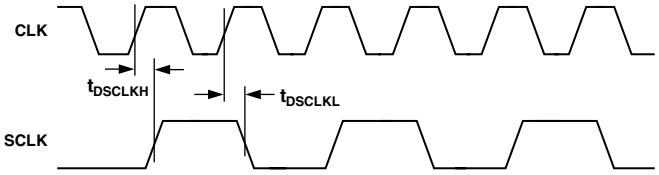


Figure 6. SCLK Switching Characteristic (Divide by 2 or EVEN Integer)

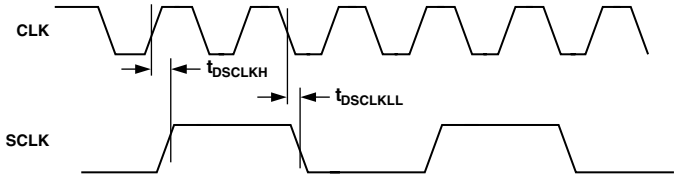


Figure 7. SCLK Switching Characteristic (Divide by 3 or ODD Integer)

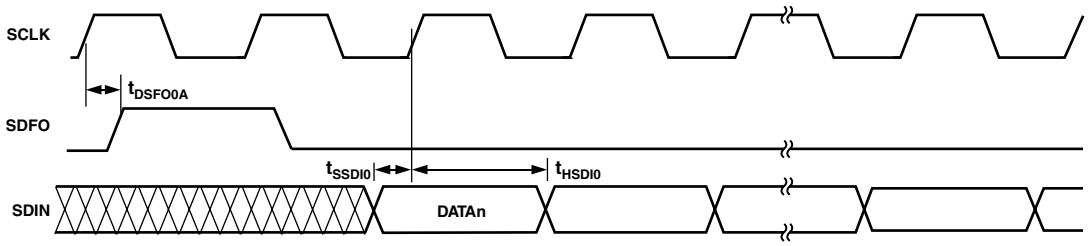


Figure 8. Serial Port Timing, Master Mode (SCS = 0), Channel is Self-Framing

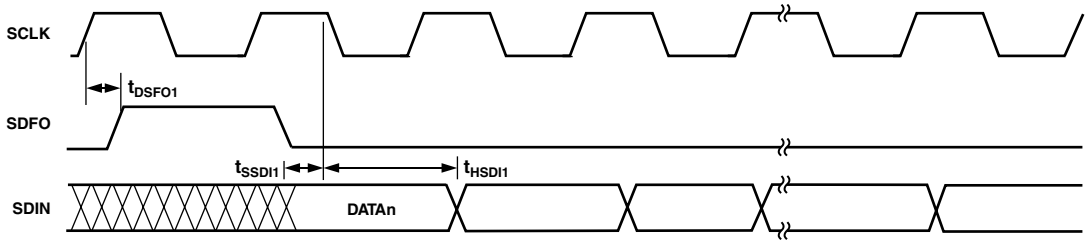


Figure 9. Serial Port Timing, Slave Mode (SCS = 1), Channel is Self-Framing

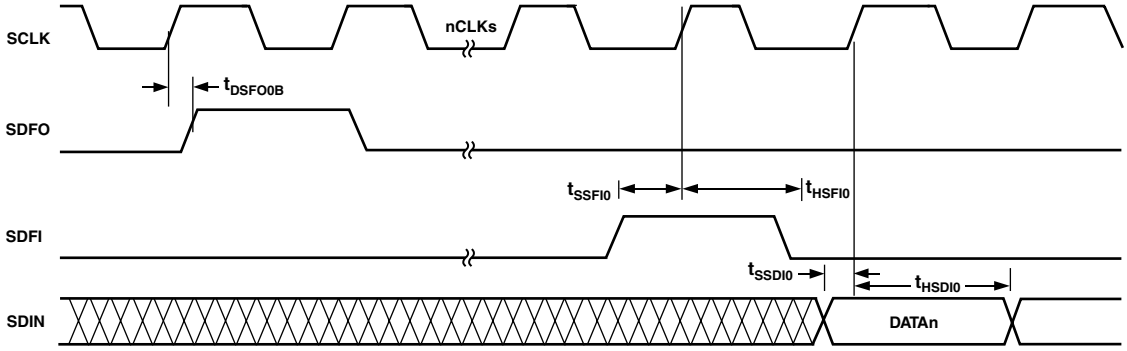


Figure 10. Serial Port Timing, Master Mode (SCS = 0), Channel is External-Framing

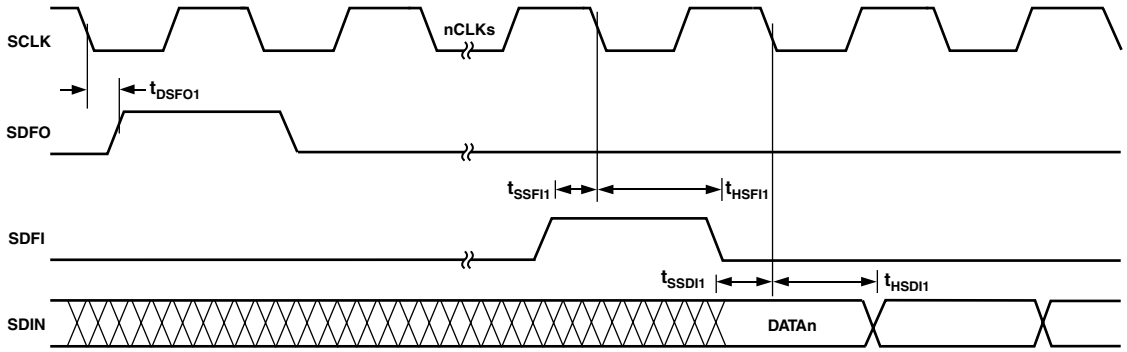
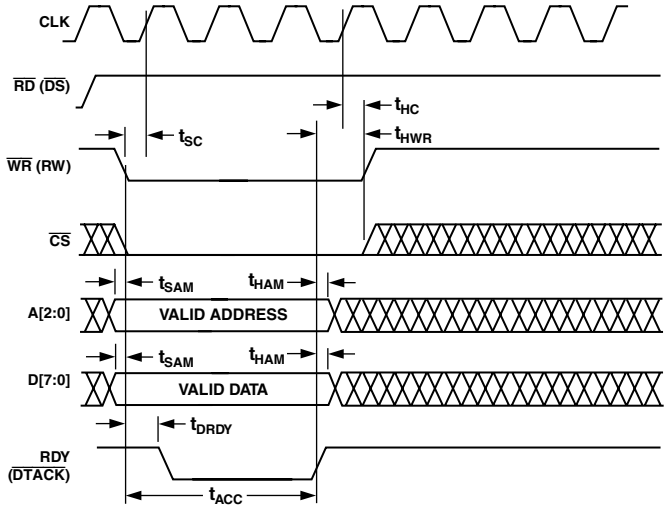


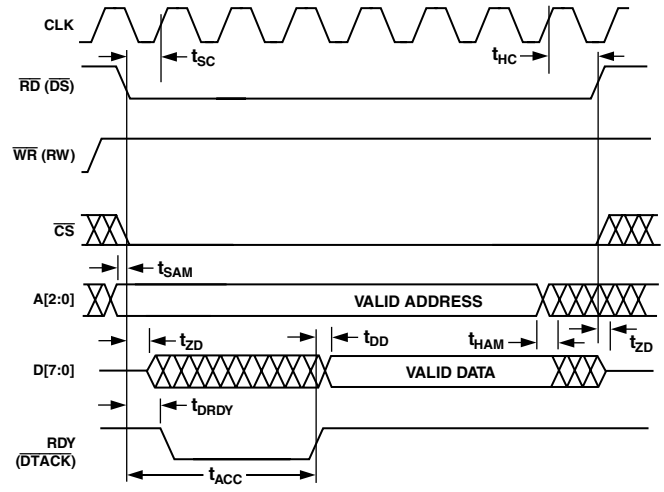
Figure 11. Serial Port Timing, Slave Mode (SCS = 1), Channel is External-Framing

TIMING DIAGRAMS—INM MICROPORT MODE



NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FE OF $\overline{WR}$ TO THE RE OF RDY.
2. t_{ACC} REQUIRES A MAXIMUM 9 CLK PERIODS.

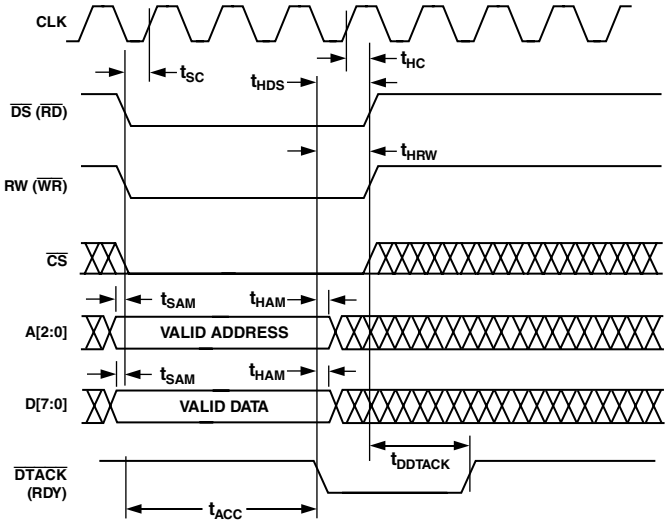
Figure 12. INM Microport Write Timing Requirements



NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FE OF $\overline{WR}$ TO THE RE OF RDY.
2. t_{ACC} REQUIRES A MAXIMUM OF 13 CLK PERIODS AND APPLIES TO A[2:0] = 7, 6, 5, 3, 2, 1

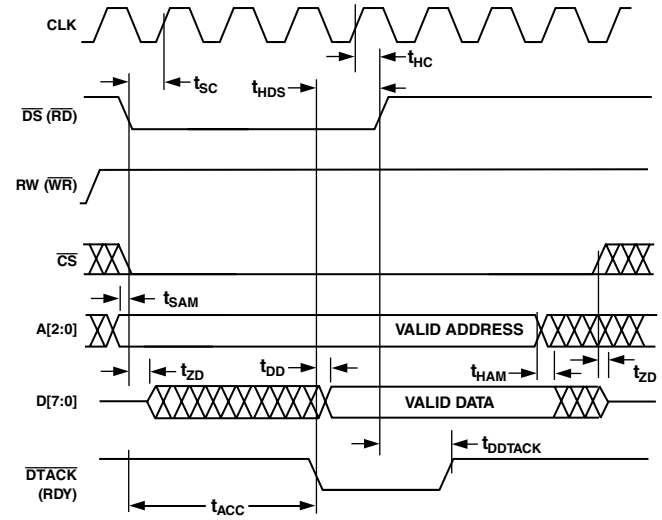
Figure 13. INM Microport Read Timing Requirements

TIMING DIAGRAMS—MNM MICROPORT MODE



NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FE OF $\overline{DS}$ TO THE FE OF $\overline{DTACK}$.
2. t_{ACC} REQUIRES A MAXIMUM 9 CLK PERIODS.

Figure 14. MNM Microport Write Timing Requirements



NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FE OF $\overline{DS}$ TO THE FE OF $\overline{DTACK}$.
2. t_{ACC} REQUIRES A MAXIMUM 13 CLK PERIODS.

Figure 15. MNM Microport Read Timing Requirements

ABSOLUTE MAXIMUM RATINGS*

VDDIO . . . . . –0.3 V to +3.6 V
VDD . . . . . –0.3 V to +2.75 V
Input Voltage . . . . . –0.3 V to +5 V (5 V Tolerant)
Output Voltage Swing . . . . . –0.3 V to VDDIO + 0.3 V
Load Capacitance . . . . . 200 pF
Junction Temperature Under Bias . . . . . 125°C
Operating Temperature . . . . . –40°C to +85°C (Ambient)
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 sec) . . . . . 280°C

*Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the devices at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

128-Lead MQFP with Internal Heat Spreader:
θ_{JA} = 28.1°C/W, no airflow
θ_{JA} = 22.6°C/W, 200 lfpm airflow
θ_{JA} = 20.5°C/W, 400 lfpm airflow

196-Lead BGA:
θ_{JA} = 26.3°C/W, no airflow
θ_{JA} = 22°C/W, 200 lfpm airflow

Thermal measurements made in the horizontal position on a 4-layer board.

EXPLANATION OF TEST LEVELS

I. 100% Production Tested
II. 100% Production Tested at 25°C, and Sample Tested at Specified Temperatures
III. Sample Tested Only
IV. Parameter Guaranteed by Design and Analysis
V. Parameter is Typical Value Only

ORDERING GUIDE

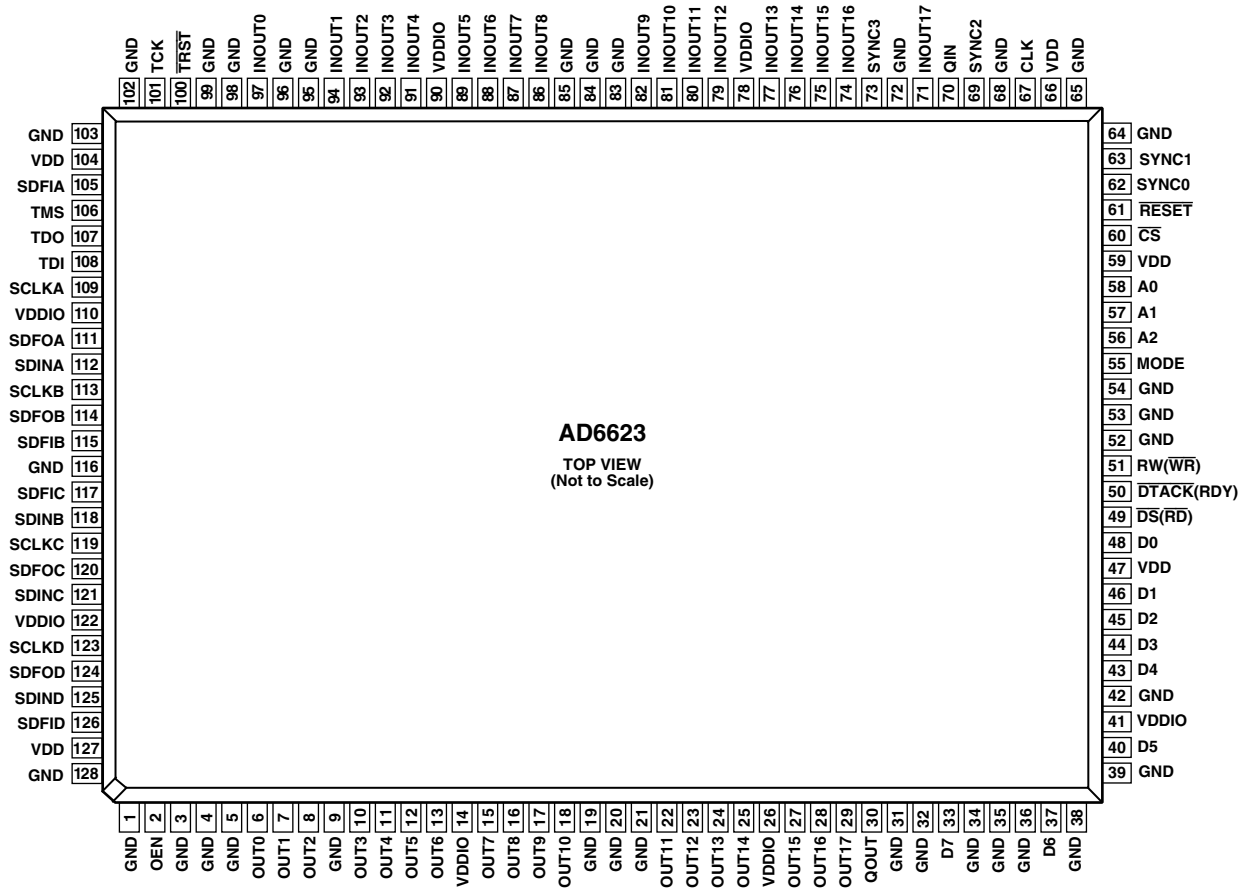
Model	Temperature Range	Package Description	Package Option
AD6623AS	–40°C to +85°C (Ambient)	128-Lead MQFP (Plastic Quad Flatpack)	S-128
AD6623ABC	–40°C to +85°C (Ambient)	196-Lead CSPBGA (Chip Scale Package Ball Grid Array)	BC-196
AD6623S/PCB		MQFP Evaluation Board with AD6623 and Software	
AD6623BC/PCB		CSPBGA Evaluation Board with AD6623 and Software	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6623 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION
128-Lead MQFP

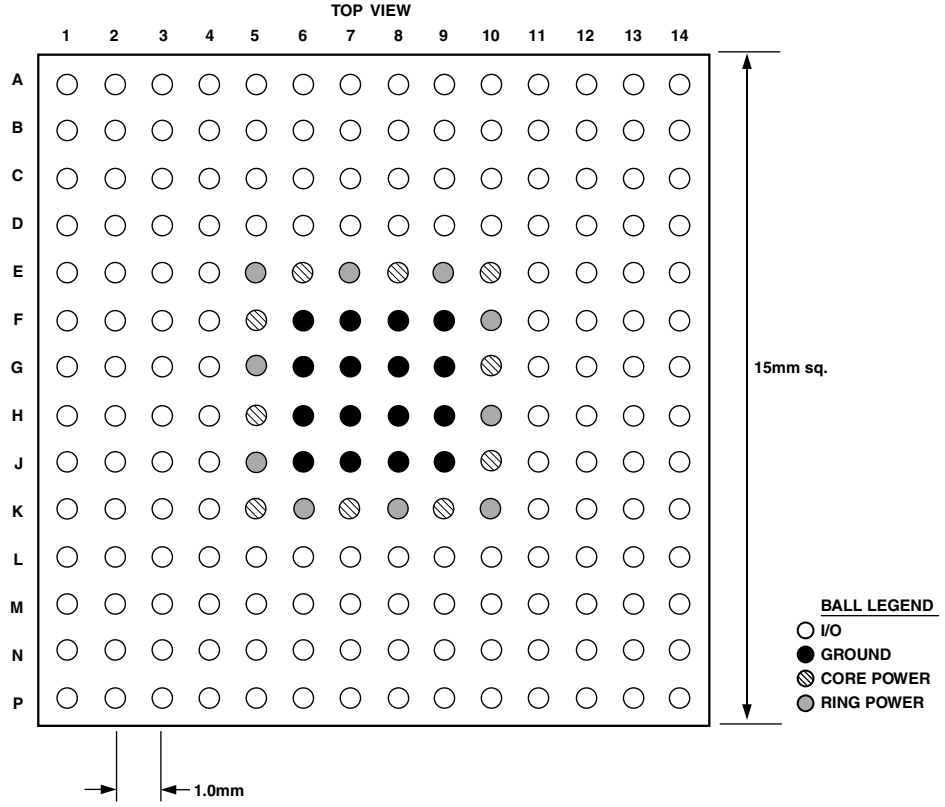


128-LEAD FUNCTION DESCRIPTIONS

Pin Number	Mnemonic	Type	Description
1, 3–5, 9, 19–21, 31, 32, 34–36, 38, 39, 42, 52–54, 64–65, 68, 72, 83–85, 95, 96, 98, 99, 102, 103, 116, 128	GND	P	Ground Connection
2	OEN[1]	I	Active High Output Enable Pin
29, 28, 27, 25, 24, 23, 22, 18, 17, 16, 15, 13, 12, 11, 10, 8, 7, 6	OUT[17:0]	O/T	Parallel Output Data
47, 59, 66, 104, 127	VDD	P	2.5 V Supply
14, 26, 41, 78, 90, 110, 122	VDDIO	P	3.3 V Supply
30	QOUT	O/T	When HIGH indicates Q Output Data (Complex Output Mode)
33, 37, 40, 43, 44, 45, 46, 48	D[7:0]	I/O/T	Bidirectional Microport Data
49	$\overline{\text{DS}}$ ($\overline{\text{RD}}$)	I	INM Mode: Read Signal, MNM Mode: Data Strobe Signal
50	$\overline{\text{DTACK}}$ (RDY)	O	Acknowledgment of a Completed Transaction (Signals when µP Port Is Ready for an Access) Open Drain, Must Be Pulled Up Externally
51	RW ($\overline{\text{WR}}$)	I	Active HIGH Read, Active Low Write
55	MODE	I	Sets Microport Mode: MODE = 1, MNM Mode; MODE = 0, INM Mode
56, 57, 58	A[2:0]	I	Microport Address Bus
60	$\overline{\text{CS}}$	I	Chip Select, Active low enable for µP Access
61	$\overline{\text{RESET}}$[2]	I	Active Low Reset Pin
62	SYNC0[1]	I	SYNC Signal for Synchronizing Multiple AD6623s
63	SYNC1[1]	I	SYNC Signal for Synchronizing Multiple AD6623s
67	CLK[1]	I	Input Clock
69	SYNC2[1]	I	SYNC Signal for Synchronizing Multiple AD6623s
70	QIN[1]	I	When HIGH indicates Q input data (Complex Input Mode)
71, 74–77, 79–82, 86–89, 91–94, 97	INOUT[17:0][1]	I/O	Wideband Input/Output Data (Allows Cascade of Multiple AD6623 Chips In a System)
73	SYNC3[1]	I	SYNC Signal for Synchronizing Multiple AD6623s
100	$\overline{\text{TRST}}$[2]	I	Test Reset Pin
101	TCK[1]	I	Test Clock Input
105	SDFIA	I	Serial Data Frame Input—Channel A
106	TMS[2]	I	Test Mode Select
107	TDO	O	Test Data Output
108	TDI[1]	I	Test Data Input
109	SCLKA	I/O	Bidirectional Serial Clock—Channel A
111	SDFOA	O	Serial Data Frame Sync Output—Channel A
112	SDINA[1]	I	Serial Data Input—Channel A
113	SCLKB	I/O	Bidirectional Serial Clock—Channel B
114	SDFOB	O	Serial Data Frame Sync Output—Channel B
115	SDFIB	I	Serial Data Frame Input —Channel B
117	SDFIC	I	Serial Data Frame Input—Channel C
118	SDINB[1]	I	Serial Data Input—Channel B
119	SCLKC	I/O	Bidirectional Serial Clock—Channel C
120	SDFOC	O	Serial Data Frame Sync Output—Channel C
121	SDINC[1]	I	Serial Data Input—Channel C
123	SCLKD	I/O	Bidirectional Serial Clock—Channel D
124	SDFOD	O	Serial Data Frame Sync Output—Channel D
125	SDIND[1]	I	Serial Data Input—Channel D
126	SDFID	I	Serial Data Frame Input—Channel D

NOTES
[1]Pins with a Pull-Down resistor of nominal 70 kΩ.
[2]Pins with a Pull-Up resistor of nominal 70 kΩ.

PIN CONFIGURATION
196-Lead CSPBGA



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC			SDFID	SDINC	SDINB	SDFOB	SCLKB	SCLKA	TDO	SDFIA	TCK		NC
B				OEN	SDIND	SDFOC	SDFIC	SDINA	TDI		$\overline{\text{TRST}}$			
C				SDFOD		SCLKD	SCLKC	SDFIB	SDFOA	TMS				IN0
D	OUT2		OUT0									IN2		IN1
E		OUT1	OUT3		VDDIO	VDD	VDDIO	VDD	VDDIO	VDD				IN4
F	OUT5	OUT4	OUT6		VDD	GND	GND	GND	GND	VDDIO		IN3	IN5	IN7
G	OUT8	OUT7			VDDIO	GND	GND	GND	GND	VDD		IN6	IN8	IN9
H	OUT9	OUT10	OUT12		VDD	GND	GND	GND	GND	VDDIO			IN11	IN10
J	OUT11	OUT13			VDDIO	GND	GND	GND	GND	VDD		IN12	IN14	IN13
K	OUT14		OUT17		VDD	VDDIO	VDD	VDDIO	VDD	VDDIO		IN16	IN17	IN15
L	OUT16		OUT15									QIN		SYNC3
M	QOUT		D7	D4	D1	$\overline{\text{DTACK}}$ (RDY)	MODE (ALE)	A1	$\overline{\text{RESET}}$					SYNC2
N				D5	D3	D0	RW($\overline{\text{WR}}$)		A0	SYNC0				
P	NC	D6		D2		$\overline{\text{DS}}$($\overline{\text{RD}}$)			A2	$\overline{\text{CS}}$	SYNC1		CLK	NC

NC = NO CONNECT

196-LEAD FUNCTION DESCRIPTIONS

Mnemonic	Type	Function
POWER SUPPLY		
VDD	P	2.5 V Supply
VDDIO	P	3.3 V IO Supply
GND	G	Ground
INPUTS		
INOUT[17:0][1]	I/O	A Input Data (Mantissa)
QIN[1]	I	When HIGH Indicates Q Input Data (Complex Input Mode)
$\overline{\text{RESET}}$[2]	I	Active LOW Reset Pin
CLK[1]	I	Input Clock
SYNC0[1]	I	All Sync Pins Go to All Four Output Channels
SYNC1[1]	I	All Sync Pins Go to All Four Output Channels
SYNC2[1]	I	All Sync Pins Go to All Four Output Channels
SYNC3[1]	I	All Sync Pins Go to All Four Output Channels
SDINA[1]	I	Serial Data Input—Channel A
SDINB[1]	I	Serial Data Input—Channel B
SDINC[1]	I	Serial Data Input—Channel C
SDIND[1]	I	Serial Data Input—Channel D
$\overline{\text{CS}}$	I	Active LOW Chip Select
CONTROL		
SCLKA	I/O	Bidirectional Serial Clock—Channel A
SCLKB	I/O	Bidirectional Serial Clock—Channel B
SCLKC	I/O	Bidirectional Serial Clock—Channel C
SCLKD	I/O	Bidirectional Serial Clock—Channel D
SDFOA	O	Serial Data Frame Sync Output—Channel A
SDFOB	O	Serial Data Frame Sync Output—Channel B
SDFOC	O	Serial Data Frame Sync Output—Channel C
SDFOD	O	Serial Data Frame Sync Output—Channel D
SDFIA	I	Serial Data Frame Input—Channel A
SDFIB	I	Serial Data Frame Input—Channel B
SDFIC	I	Serial Data Frame Input—Channel C
SDFID	I	Serial Data Frame Input—Channel D
OEN[1]	I	Active High Output Enable Pin
MICROPORT CONTROL		
D[7:0]	I/O/T	Bidirectional Microport Data
A[2:0]	I	Microport Address Bus
$\overline{\text{DS}}$ ($\overline{\text{RD}}$)	I	Active Low Data Strobe (Active Low Read)
$\overline{\text{DTACK}}$ (RDY)[2]	O/T	Active Low Data Acknowledge (Microport Status Bit)
RW ($\overline{\text{WR}}$)	I	Read Write (Active Low Write)
MODE	I	Intel or Motorola Mode Select
OUTPUTS		
OUT[17:0]	O	Wideband Output Data
QOUT	O	When HIGH Indicates Q Output Data (Complex Output Mode)
JTAG AND BIST		
$\overline{\text{TRST}}$[2]	I	Test Reset Pin (Active Low)
TCK[1]	I	Test Clock Input
TMS[2]	I	Test Mode Select Input
TDO	O/T	Test Data Output
TDI[1]	I	Test Data Input

NOTES
[1]Pins with a Pull-Down resistor of nominal 70 kΩ.
[2]Pins with a Pull-Up resistors of nominal 70 kΩ.

CONTROL REGISTER ADDRESS NOTATION

Register address notation and bit assignment referred to throughout this data sheet are as follows: There are eight, one-digit "External" register addresses in decimal format. "Internal" address notation (read from left to right) begins with "0x", meaning the address that follows is hexadecimal. The next three characters represent the address. The first number or character is the MSB of the address. If an "n" is present, its value can be 1, 2, 3, or 4 and it depends upon the channel that is being addressed (A, B, C, or D). The remaining two digits preceding the colon (if present) are the LSBs of the address. If a colon follows the address, then the succeeding digits tell the user what bit number(s) is/are involved in decimal format. For example, 0xn24:7-0.

SERIAL DATA PORT

The AD6623 has four independent Serial Ports (A, B, C, and D), and each accepts data to its own channel (A, B, C, or D) of the device. Each Serial Port has four pins: SCLK (Serial CLocK), SDFO (Serial Data Frame Out), SDFI (Serial Data Frame In), and SDIN (Serial Data INput). SDFI and SDIN are inputs, SDFO is an output, and SCLK is either input or output depending on the state of SCS (Serial Clock Slave: 0xn16, Bit 4). Each channel can be operated either as a Master or Slave channel depending upon SCS. The Serial Port can be self-framing or accept external framing from the SFDI pin or from the previous adjacent channel (0xn16, Bits 7 and 6).

Serial Master Mode (SCS = 0)

In master mode, SCLK is created by a programmable internal counter that divides CLK. When the channel is "sleeping," SCLK is held low. SCLK becomes active on the first rising edge of CLK after Channel sleep is removed (D0 through D3 of external address 4). Once active, the SCLK frequency is determined by the CLK frequency and the SCLK divider, according to the equations below.

AD6623 mode:

$$f_{SCLK} = \frac{f_{CLK}}{SCLKdivider + 1} \quad (1)$$

AD6622 mode:

$$f_{SCLK} = \frac{f_{CLK}}{2 \times (SCLKdivider + 1)} \quad (2)$$

The SCLK divider is a 5-bit unsigned value located at Internal Channel Address 0xn0D (Bits 4–0), where "n" is 1, 2, 3, or 4 for the chosen channel A, B, C, or D, respectively. The user must select the SCLK divider to insure that SCLK is fast enough to accept full input sample words at the input sample rate. See the design example at the end of this section. The maximum SCLK frequency is equal to the CLK when operating in AD6623 mode serial clock master. When operating in AD6622 compatible mode, the maximum SCLK frequency is one-half the CLK. The minimum SCLK frequency is 1/32 of the CLK frequency in AD6623 mode or 1/64 of the CLK frequency when in AD6622 mode. SDFO changes on the positive edge of SCLK when in master mode. SDIN is captured on positive edge when SCLK is in master mode.

Serial Slave Mode (SCS = 1)

Any of the AD6623 serial ports may be operated in the serial slave mode. In this mode, the selected AD6623 channel requires that an external device such as a DSP to supply the SCLK. This is done to synchronize the serial port to meet an external timing requirement. SDIN is captured on negative edge of SCLK when in slave mode.

Serial Data Framing

The SDIN input pin of each transmit channel of the AD6623 receives data from an external DSP to be digitally filtered, interpolated, and then modulated by the NCO-generated carrier. Serial data from the DSP to the AD6623 is sent as a series of blocks or frames. The length of each block is a function of the desired output format that is supported by the AD6623. Block length may range from 1 bit (MSK) to 32 bits of I and Q data.

The flow of data to the SDIN input is regulated either by the AD6623 (in Self-Framing Mode) or by the external DSP (using AD6623 External Framing Mode). This is accomplished by generating a pulse, SDFO or SDFI, to indicate that the next frame or serial data block is ready to be input or sent to the AD6623. Functions of the two pins, SDFO and SDFI, are fully described in the framing modes that follow.

Self-Framing Mode

In this mode Bit 7 of register 0xn16 is set low. The serial data frame output, SDFO, generates a self-framing data request and is pulsed high for one SCLK cycle at the input sample rate. In this mode, the SDFI pin is not used, and the SDFO signal would be programmed to be a serial data frame request (0xn16, Bit 5 = 0). SDFO is used to provide a sync signal to the host. The input sample rate is determined by the CLK divided by channel interpolation factor. If the SCLK rate is not an integer multiple of the input sample rate, then the SDFO will continually adjust the period by one SCLK cycle to keep the average SDFO rate equal to the input sample rate. When the channel is in sleep mode, SDFO is held low. The first SDFO is delayed by the channel reset latency after the Channel Reset is removed. The channel reset latency varies dependent on channel configuration.

External Framing Mode

In this mode Bit 7 of register 0xn16 is set high. The external framing can come from either the SDFI pin (0xn16, Bit 6 = 0) or the previous adjacent channel (0xn16, Bit 6 = 1). In the case of external framing from a previous channel, it uses the internal frame end signal for serial data frame synchronizing. When in master mode, SDFO and SDFI transition on the positive edge of SCLK, and SDIN is captured on the positive edge of SCLK. When in slave mode, SDFO and SDFI transition on the negative edge of SCLK, and SDIN is captured on the negative edge of SCLK.

Serial Port Cascade Configuration

In this case the SDFO signal from the last channel of the first chip would be programmed to be a serial data frame end (SFE:0xn16, Bit 5 = 1). This SDFO signal would then be fed as an input for the second cascaded chip's SDFI pin input. The second chip would be programmed to accept external framing from the SDFI pin (0xn16, Bit 7 = 1, Bit 6 = 0).

Serial Data Format

The format of data applied to the serial port is determined by the RCF mode selected in Control Register 0xn0C. Below is a table showing the RCF modes and input data format that it sets.

Table I. Serial Data Format

0xn0C Bit 6	0xn0C Bit 5	0xn0C Bit 4	Serial Data Word Length	RCF Mode
0	0	0	32	FIR
0	0	1		π/4-DQPSK
0	1	0		GMSK
0	1	1		MSK
1	0	0	24 (Bit 9 is high)	FIR,
			16 (Bit 9 is low)	compact
1	0	1		8-PSK
1	1	0		3π/8-8-PSK
1	1	1		QPSK

The serial data input, SDIN, accepts 32-bit words as channel input data. The 32-bit word is interpreted as two 16-bit two's complement quadrature words, I followed by Q, MSB first. This results in linear I and Q data being provided to the RCF. The first bit is shifted into the serial port starting on the next rising edge of SCLK after the SDFO pulse. Figure 16 shows a timing diagram for SCLK master (SCS = 0) and SDFO set for frame request (SFE = 0).

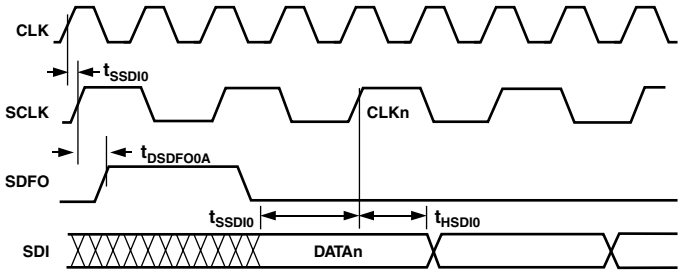


Figure 16. Serial Port Switching Characteristics

As an example of the Serial Port operation, consider a CLK frequency of 62.208 MHz and a channel interpolation of 2560. In that case, the input sample rate is 24.3 kSPS (62.208 MHz/2560), which is also the SDFO rate. Substituting, $f_{SCLK} \geq 32\ 3\ f_{SDFO}$ into the equation and solving for SCLKdivider, we find the minimum value for SCLKdivider according to the equation below.

$$SCLKdivider \leq \frac{f_{CLK}}{32 \times f_{SDFO}} \quad (3)$$

Evaluating this equation for our example, SCLKdivider must be less than or equal to 79. Since the SCLKdivider channel register is a 5-bit unsigned number it can only range from 0 to 31. Any value in that range will be valid for this example, but if it is important that the SDFO period is constant, then there is another restriction. For regular frames, the ratio f_{SCLK}/f_{SDFO} must be equal to an integer of 32 or larger. For this example, constant SDFO periods can only be achieved with an SCLK divider of 31 or less.

See Table II for usable SCLK divider values and the corresponding SCLK and f_{SCLK}/f_{SDFO} ratio for the example of L = 2560.

In conclusion, SDFO rate is determined by the AD6623 CLK rate and the interpolation rate of the channel. The SDFO rate is equal to the channel input rate. The channel interpolation is equal to RCF interpolation times CIC5 interpolation, times CIC2 interpolation:

$$\left(L = L_{RCF} \times L_{CIC5} \times \frac{L_{CRIC2}}{M_{CRIC2}} \right) \quad (4)$$

The SCLK divide ratio is determined by SCLKdivider as shown in equation 3. The SCLK must be fast enough to input 32 bits of data prior to the next SDFO. Extra SCLKs are ignored by the serial port.

Table II. Example of Usable SCLK Divider Values and f_{SCLK}/f_{SDFO} Ratios for L = 2560

SCLKdivider	f_{SCLK}/f_{SDFO}
0	2560
1	1280
3	640
4	512
7	320
9	256
15	160
19	128
31	80

PROGRAMMABLE RAM COEFFICIENT FILTER (RCF)

Each channel has a fully independent RAM Coefficient Filter (RCF). The RCF accepts data from the Serial Port, processes it, and passes the resultant I and Q data to the CIC filter. A variety of processing options may be selected individually or in combination, including PSK and MSK modulation, FIR filtering, all-pass phase equalization, and scaling with arbitrary ramping. See Table III.

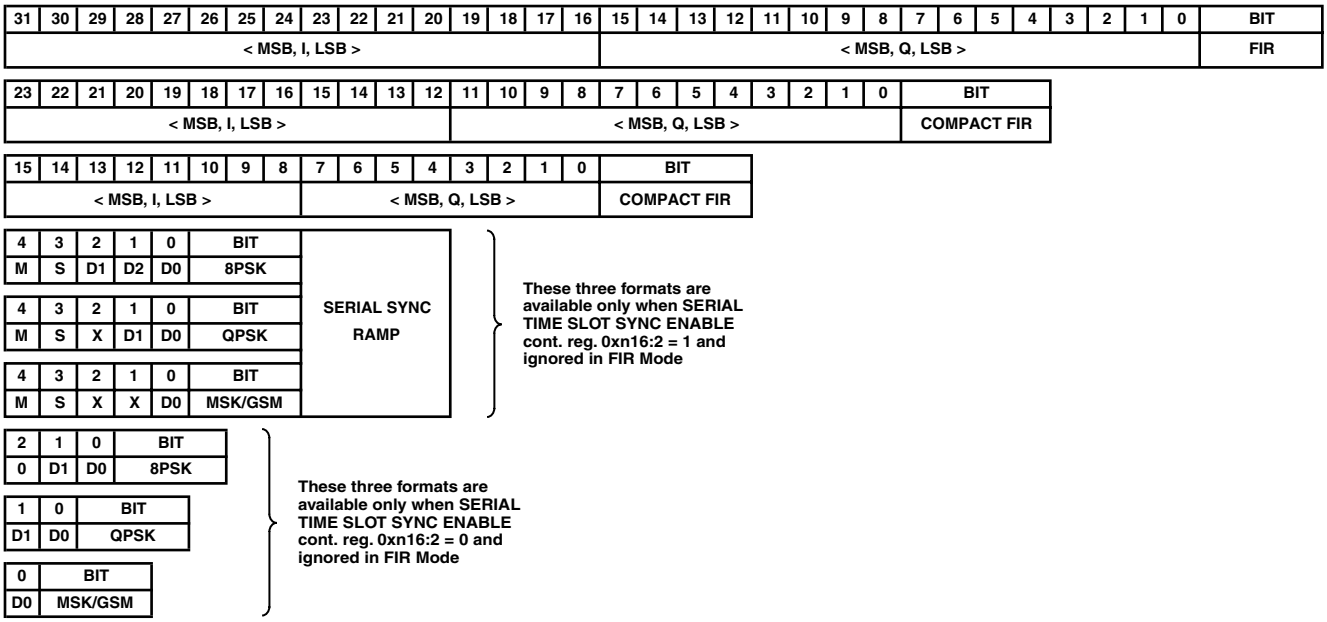
Table III. Data Format Processing Options

Processing Block	Input Data	Output Data
Interpolating FIR Filter	I and Q	I and Q
PSK Modulator	2 or 3 bits per symbol	Unfiltered I and Q: π/4-QPSK, 8-PSK, or 3π/8-8-PSK
MSK Modulator	1 bit per symbol	Filtered MSK or GSM I and Q
QPSK	2 bits per symbol	Filtered QPSK I and Q
All-pass Phase Equalizer	I and Q	I and Q
Scale and Ramp	I and Q	I and Q

OVERVIEW OF THE RCF BLOCKS

The Serial Port passes data to the RCF with the appropriate format and bit precision for each RCF configuration, see Figure 17. The data may be modulated vectors or unmodulated bits. I and Q vectors are sent directly to the Interpolating Fir Filter. Unmodulated bits may be sent to the PSK Modulator, the Interpolating MSK Modulator, or the Interpolating QPSK Modulator. The PSK Modulator produces unfiltered I and Q vectors at the symbol rate which are then passed through the Interpolating FIR Filter. The Interpolating MSK Modulator and the Interpolating QPSK Modulator produce oversampled, pulse-shaped vectors directly without employing the Interpolating FIR Filter. When possible, the MSK and QPSK modulators are recommended for increased throughput and decreased power consumption compared to Interpolating FIR Filter. In addition, the Interpolating MSK Modulator can realize filters with nonlinear inter-symbol interference, achieving excellent accuracy for GMSK applications.

After interpolation, an optional Allpass Phase Equalizer (APE) can be inserted into the signal path. The APE can realize any real, stable, two-pole, two-zero all-pass filter at the RCF's interpolated rate. This is especially useful to precompensate for nonlinear phase responses of receive filters in terminals, as specified by IS-95. When active, the APE utilizes shared hardware with the interpolating modulators and filter, which may reduce the allowed RCF throughput, inter-symbol interference, or both. See Figure 18.



M = mode bit. If M = 0, then the MSB of 3-bit mode select word at 0xn0C:6 is set to 0 (this is also called MODE 0). If M = 1, then the MSB is set to 1 and this is MODE 1. Mode allows quick format changes via the serial port, for example, 010 = GMSK and 110 = 3pi/8PSK. The value m should be held for the duration of the time slot since the value of m will only be updated after the RCF Scale Holdoff Counter reaches a value of 1 (see below).

S = serial time slot sync bit. If S = 0, then no sync is generated. If S = 1, a "Serial Time Slot Sync" occurs that loads the RCF Scale Hold-off Counter with a user programmed value and commences a backwards count of CLK cycles. When the counter reaches one, an automatic sequence occurs as follows: Power Ramp Down occurs, m (above) is updated, serial input is suspended for a REST or QUIET time and any control register with a 2 superscript is updated. After REST, the serial input becomes active and the power level is ramped up to the Fine Scale multiplier value or any lesser power level. Ramp enable bit, 0xn16:0, must be set to logic 1 for the ramp functions to occur. See the RCF Power Ramping and Time Slot Synchronization sections for more detail.

X = don't care

D = payload data bit

Important notes: The sync pulse, s, should be held at Logic 1 for only one serial frame since every frame with Logic 1 in the s position will cause the RCF Scale Hold-off Counter to reload its beginning count and begin counting again. The RCF Scale Hold-off Counter counts master CLK cycles. The REST time period is a programmable 5-bit value that counts interpolated RCF output samples before resuming serial input to the channel. The succeeding actions of any hold-off counter in the AD6623 can be defeated by setting its count value to 0.

Figure 17. Data Formats Supported by the AD6623 when SCLK Master (SCS = 0), and SFDO Set for Frame Request (SFE = 0)

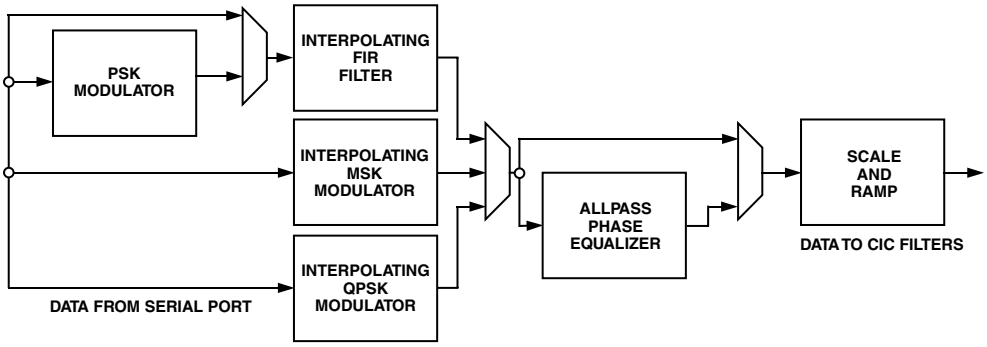


Figure 18. RCF Block Diagram

Table IV. FIR Filter Internal Precision

Signal	x × y Notation	Minimum		Maximum	
		Decimal	Hexadecimal (h)	Decimal	Hexadecimal (h)
I and Q Inputs	1.15	–1.00000	+1.00000	0.999969	0.FFFE
Coefficients	1.15	–1.00000	+1.00000	0.999969	0.FFFE
Product	2.18	–0.99969	+3.00020	1.000000	1.00000
Sum	4.18	–7.00000	+8.00000	7.999996	7.FFFFC
FIR Output	1.17	–1.00000	+1.00000	0.999992	0.FFFF8

The Scale and Ramp block adjusts the final magnitude of the modulated RCF output. A synchronization pulse from the SYNC0–3 pins or serial words can be used to command this block to ramp down, pause, and ramp up to a new scale factor. The shape of the ramp is stored in RAM, allowing complete sample by sample control at the RCF interpolated rate. This is particularly useful for time division multiplexed standards such as GSM/EDGE. Modulator configurations can be updated while the ramp is quiet, allowing for GSM and EDGE timeslots to be multiplexed together without resetting or reconfiguring the channel. Each of the RCF processing blocks is discussed in greater detail in the following sections.

INTERPOLATING FIR FILTER

The Interpolating FIR Filter realizes a real, sum-of-products filter on I and Q inputs using a single interleaved Multiply-Accumulator (MAC) running at the CLK rate. The input signal is interpolated by integer factors to produce arbitrary impulse responses up to 256 output samples long.

Each bus in the data path carries bipolar two's complement values. For the purpose of discussion, we will arbitrarily consider the radix point positioned so that the input data ranges from –1 to just below 1. In Figure 19, the data buses are marked x × y to denote finite precision limitations. A bus marked x × y has x bits above the radix and y bits below the radix, which implies a range from -2^{x-1} to $2^{x-1} - 2^{-y}$ in 2^{-y} steps. The range limits are tabulated in Table IV for each bus. The hexadecimal values are bit-exact and each MSB has negative weight. Note that the Product bus range is limited by result of the multiplication and the two most significant bits are the same except in one case.

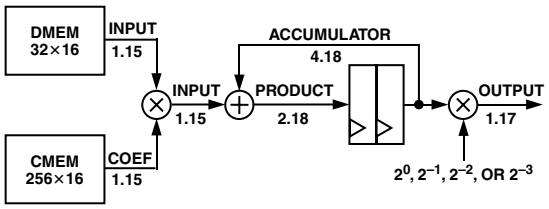


Figure 19. Interpolating FIR Filter Block Diagram

The RCF realizes a FIR filter with optional interpolation. The FIR filter can produce impulse responses up to 256 output samples long. The FIR response may be interpolated up to a factor of 256, although the best filter performance is usually achieved when the RCF interpolation factor (L_{RCF}) is confined to eight or below. The 256 × 16 coefficient memory (CMEM) can be divided among an arbitrary number of filters, one of which is selected by the Coefficient Offset Pointer (channel address 0x0B). The polyphase implementation is an efficient equivalent to an integer up-sampler followed FIR filter running at the interpolated rate.

The AD6623 RCF realizes a sum-of-products filter using a polyphase implementation. This mode is equivalent to an interpolator followed by a FIR filter running at the interpolated rate. In the functional diagram below, the interpolating block increases the rate by the RCF interpolation factor (L_{RCF}) by inserting L_{RCF}–1 zero valued samples between every input sample. The next block is a filter with a finite impulse response length (N_{RCF}) and an impulse response of h[n], where n is an integer from 0 to N_{RCF}–1.

The difference equation for Figure 20 is written below, where h[n] is the RCF impulse response, b[n] is the interpolated input sample sequence at point 'b' in the diagram above, and c[n] is the output sample sequence at point 'c' in Figure 20.

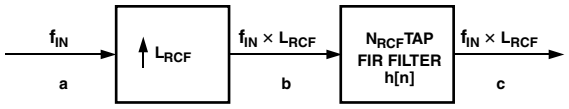


Figure 20. RCF Interpolation

$$c[n] = \sum_{k=0}^{N_{RCF}-1} h[n] \times b[n-k] \quad (5)$$

This difference equation can be described by the transfer function from point 'b' to 'c' as:

$$H_{bc}(z) = \sum_{k=0}^{N_{RCF}-1} h[n] \times z^{-1} \quad (6)$$

The actual implementation of this filter uses a polyphase decomposition to skip the multiply-accumulates when b[n–k] is zero. Compared to the diagram above, this implementation has the benefits of reducing by a factor of L_{RCF} both the time needed to calculate an output and the required data memory (DMEM). The price of these benefits is that the user must place the coefficients into the coefficient memory (CMEM) indexed by the interpolation phase. The process of selecting the coefficients and placing them into the CMEM is broken into three steps shown below.

The FIR accepts two's complement I and Q samples from the serial port with a fixed-point resolution of 16 bits each. When the serial port provides data with less precision, the LSBs are padded with zeroes.

The Data-Mem stores the most recent 16 I and Q pairs for a total of 32 words. The size of the Data-Mem limits the RCF impulse response to 16 × L_{RCF} output samples. When the data words from the Serial Port have fewer than 16 bits, the LSBs are padded with zeroes. The Data-Mem can be accessed through the Microport from 0x20 to 0x5F above the processing channel's base internal address, while the channel's Prog bit is set (external address 4). In order to avoid start-up transients, the Data-Mem should be cleared before operation. The Prog bit must then be reset to enable normal operation.

The Coef-Mem stores up to 256 16-bit filter coefficients. The Coef-Mem can be accessed through the Microport from 0x800 to 0x8FF above the processing channel's base internal address, while the channel's Prog bit is set (external address 4). For AD6622 compatibility, the lower 128 words are also mirrored from 0x080 to 0x0FF above the processing channel's base internal address, while the Prog bit is set.

There is a single Multiply-Accumulator (MAC) on which both the I and Q operations must be interleaved. Two CLK cycles are required for the MAC to multiply each coefficient by an I and Q pair. The MAC is also used for four additional CLK cycles if the All-pass Phase Equalizer is active.

The size of the Data-Mem and Coef-Mem combined with the speed of the MAC determine the total number of the taps per phase (T_{RCF}) that may be calculated. T_{RCF} is the number of RCF input samples that influence each RCF output sample. The maximum available T_{RCF} is calculated by the equation below.

$$T_{RCF} \le least\ of\left(16, floor\left(\frac{256}{L_{RCF}}\right), floor\left(\frac{f_{CLK}}{2 \times f_{SDFO}} - 2 \times APE\right)\right) \quad (7)$$

Where APE = 1 (allpass phase equalizer enabled) or 0 (allpass phase equalizer disabled) and f_{SDFO} = [Output Data Rate/Total Interpolation Rate] in Hz. "*floor()*" indicates that the value within the parenthesis should be reduced to the lowest integer, e.g., floor(9.9999) = 9.

The impulse response length at the output of the RCF is determined by the product of the number of interfering input samples (T_{RCF}) and the RCF interpolation factor (L_{RCF}), as shown by equation (8) below. The values of N_{RCF} and T_{RCF} are programmed into control registers. L_{RCF} is not a control register, but N_{RCF} and T_{RCF} must be set so that L_{RCF} is an integer. If the integer interpolation by the RCF results in an inconvenient sample rate at the output of the RCF, the desired output rate can usually be achieved by selecting non-integer interpolation in the resampling CIC^2 filter.

$$N_{RCF} = T_{RCF} \times L_{RCF} \quad (8)$$

Table V. Channel A RCF Control Registers

Channel Address	Bit Width	Description
0x10A	16	15–8: N_{RCF} –1 B; 7–0: N_{RCF} –1 A
0x10B	8	7–0: O_{RCF}
0x10C	10	9: Ch. A Compact FIR Input Word Length 0: 16 bits–8 I followed by 8 Q 1: 24 bits–12 I followed by 12 Q 8: Ch. A RCF PRBS Enable 7: Ch A RCF PRBS Length 0: 15 1: 8,388,607 6–4: Ch. A RCF Mode Select 000 = FIR 001 = π/4-DQPSK Modulator 010 = GMSK Look-Up Table 011 = MSK Look-Up Table 100 = FIR compact mode 101 = 8-PSK 110 = 3π/8-8PSK Modulator 111 = QPSK Look-Up Table 3–0: Ch. A RCF Taps per Phase
0x10D	8	7–6: RCF Coarse Scale (g): 00 = 0 dB 01 = –6 dB 10 = –12 dB 11 = –18 dB 5: Ch. A Allpass Ph. Eq. Enable 4–0: Serial Clock Divider (1, ..., 32)
0x10E	16	15–2: Ch. A Unsigned Scale Factor 1–0: Reserved
0x10F	18	17–16: Ch. A Time Slot Sync Select 00: Sync0 (See 0x001 Time Slot) 01: Sync1 10: Sync2 11: Sync3 15–0: Ch. A RCF Scale Hold-Off Counter 1) Ramp Down (if Ramp is enabled) 2) Update Scale and Mode 3) Ramp Up (if Ramp is enabled)
0x110	16	15–0: Ch. A RCF Phase EQ Coef1
0x111	16	15–0: Ch. A RCF Phase EQ Coef2
0x112	16	15–0: Ch. A RCF MPSK Magnitude 0
0x113	16	15–0: Ch. A RCF MPSK Magnitude 1
0x114	16	15–0: Ch. A RCF MPSK Magnitude 2
0x115	16	15–0: Ch. A RCF MPSK Magnitude 3
0x116	8	7: Reserved 6: Ch. A Serial Data Frame Select 0: Serial Data Frame Request 1: Serial Data Frame End 5: Ch. A External SDFI Select 0: Internal SDFI 1: External SDFI 4: Ch. A SCLK Slave Select 0: Master 1: Slave 3: Ch. A Serial Fine Scale Enable 2: Ch. A Serial Time Slot Sync Enable (ignored in FIR mode) 1: Ch. A Ramp Interpolation Enable 0: Ch. A Ramp Enable
0x117	6	5–0: Ch. A Mode 0 Ramp Length, R0–1
0x118	6	5–0: Ch. A Mode 1 Ramp Length, R1–1
0x119	5	4–0: Ch. A Ramp Rest Time, Q
0x11A–0x11F		Reserved
0x120–0x13F	16	15–0: Ch. A Data Memory
0x140–0x17F	16	15–14: Reserved 13–0: Ch. A Power Ramp Memory
0x180–0x1FF	16	15–0: Ch. A Coefficient Memory This address is mirrored at 0x900–0x97F and contiguously extended at 0x980–0x9FF

PSK MODULATOR

The PSK Modulator is an AD6623 extension feature that is only available when the control register bit 0x000:7 is high. The PSK Modulator creates 32-bit complex inputs to the Interpolating FIR Filter from two or three data bits captured by the serial port. The FIR Filter operates exactly as if the 32-bit word came directly from the serial port. There are three PSK modulation options to choose from: π/4-DQPSK, 8-PSK, and 3π/8-8-PSK. Every symbol of any of these modulations can be represented by one of the 16 phases shown in Figure 21.

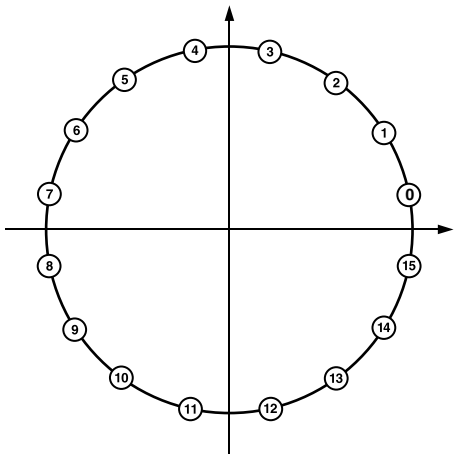


Figure 21. 16-Phase Modulations

All of these phase locations are represented in rectangular coordinates by only four unique magnitudes in the positive and negative directions. These four values are read from four channel registers that are programmed according to the following table, which gives the generic formulas and a specific example. The example is notable because it is only 0.046 dB below full-scale and the 16-bit quantization is so benign at that magnitude, that the rms error is better than –122 dBc. It is also worth noting that because none of the phases are aligned with the axes, magnitudes slightly beyond 0.16 dB above full-scale are achievable.

Table VI. Program Registers

Channel Register	Magnitude M	Magnitude E 0x7F53
0x12	M 3 cos(π/16)	0x7CE1
0x13	M 3 cos(3π/16)	0x69DE
0x14	M 3 cos(5π/16)	0x46BD
0x15	M 3 cos(7π/16)	0x18D7

Using the four channel registers from the preceding table, the PSK Modulator assembles the 16 phases according to Table VII.

Table VII. PSK Modulator Phase

Phase	I Value	Q Value
0	0x12	0x15
1	0x13	0x14
2	0x14	0x13
3	0x15	0x12
4	–0x15	+0x12
5	–0x14	+0x13
6	–0x13	+0x14
7	–0x12	+0x15
8	–0x12	–0x15
9	–0x13	–0x14
10	–0x14	–0x13
11	–0x15	–0x12
12	+0x15	–0x12
13	+0x14	–0x13
14	+0x13	–0x14
15	+0x12	–0x15

The following three sections show how the phase values are created for each PSK modulation mode.

π/4-DQPSK Modulation

IS-136 compliant π/4-DQPSK modulation is selected by setting the channel register 0xn0C: 6–4 to 001b. The phase word is calculated according to the following diagram. The two LSBs of the serial input word update the payload bits once per symbol. The QPSK Mapper creates a data dependent static phase word (Sph) which is added to a time dependent rotating phase word (Rph). The Rph starts at zero when the RCF is reset or switches modes via a sync pulse. Otherwise, the Rph increments by two on every symbol.

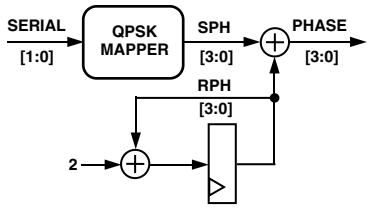


Figure 22. QPSK Mapper

The Sph word is calculated by the QPSK Mapper according to the following truth table.

Table VIII. QPSK Mapper Truth Table

Serial [1:0]	Sph [3:0]
00b	0
01b	4
11b	8
10b	12

8-PSK Modulation

IS-136+ compliant 8-PSK modulation is selected by setting the channel register 0xn0C: 6–4 to 101b. The Phase word is calculated according to the following diagram. The three LSBs of the serial input word update the payload bits once per symbol.



Figure 23. 8-PSK Mapper

The Phase word is calculated by the 8-PSK Mapper according to the following truth table:

Table IX. 8-PSK Mapper Truth Table

Serial [2:0]	Sph [3:0]
111b	0
011b	2
010b	4
000b	6
001b	8
101b	10
100b	12
110b	14

3π/8-8-PSK Modulation

EDGE compliant 3π/8-8-PSK modulation is selected by setting the channel register 0xn0C: 6–4 to 110b. The phase word is calculated according to the following diagram. The three LSBs of the serial input word update the payload bits once per symbol. The 8-PSK Mapper creates a data-dependent static phase word (Sph) which is added to a time-dependent rotating phase word (Rph). The 8-PSK Mapper operates exactly as described in the preceding 8-PSK Modulation section. The Rph starts at zero when the RCF is reset or switches modes via a sync pulse. Otherwise, the Rph increments by three on every symbol.

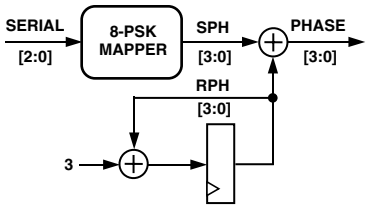


Figure 24. 3 π/8-8-PSK Mapper

MSK Look-Up Table
The MSK Look-Up Table mode for the RCF is selected in Control Register 0xn0C. In the MSK Mode, the RCF performs arbitrary pulse-shaping based on four symbols of impulse response. For the MSK Mode, the serial input format is 1 bit of data.

GMSK Look-Up Table
The GMSK Look-Up Table mode for the RCF is selected in Control Register 0xn0C. In the GMSK Mode, the RCF performs arbitrary pulse-shaping based on four symbols of impulse response. For the GMSK Mode, the serial input format is 1 Bit of data.

QPSK Look-Up Table
The QPSK Filter mode for the RCF is selected in Control Register 0xn0C. In the QPSK Mode, the RCF performs baseband linear pulse-shaping based on filter impulse response up to 12 symbols. For the QPSK Mode, the serial input format is 1 Bit I followed by 1 Bit Q.

PHASE EQUALIZER
The IS-95 Standard includes a phase equalizer after matched filtering at the baseband transmit side of a base station. This filter pre-distorts the transmitted signal at the base station in order to compensate for the distortion introduced to the received signal by the analog baseband filtering in a handset. The AD6623 includes this functionality in the form of an Infinite Impulse Response (IIR) all-pass filter in the RCF. This Phase Equalizer pre-distort filter has the following transfer function:

$$H(z) = \frac{Y(z)}{X(z)} = \frac{1 + b1z + b2z^2}{z^2 + b1z + b2} \quad (9)$$

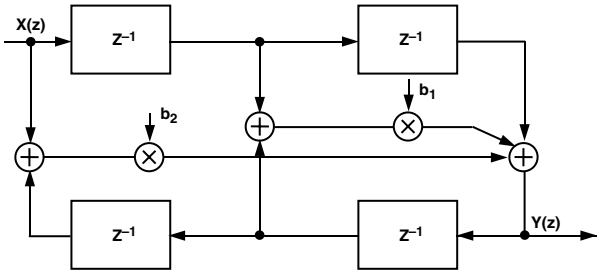


Figure 25. Second Order All-Pass IIR Filter

The Allpass Phase Equalizer (APE) is enabled (logic 1) or disabled (logic 0) in Control Register 0xn0D:5. The value of Bit 5 then becomes the value of the APE term in Equation 7. The coefficients b_1 and b_2 are located in Control Registers 0xn10 and 0xn11 respectively.

The format for b_1 and b_2 is two's complement fractional binary with a range of [–2, 2). With one bit for sign at most significant bit position there are 15 bits for magnitude. The value of one bit is $(2^{-15}) \times 2$, or 0.00006103515625. The register values, in hexadecimal, and the corresponding coefficient weight from positive full-scale through zero to negative full-scale is illustrated in Table X.

Table X. Coefficient Weights

Register Value	Coefficient Weight
0x7FFF	+1.999938964844
..	
0x0001	+0.00006103515625
0x0000	0
0xFFFF	–0.00006103515625
..	
0x8001	–1.999938964844
0x8000	–2

Table XI shows the recommended b_1 and b_2 coefficients for the respective oversampling rate.

Table XI. b_1 and b_2 Coefficients

Over-sampling	b_0	b_1	b_2
1	1	–0.25421 (0.efbbh)	+0.11188 (0.0729h)
2	1	–0.96075 (0.c283h)	+0.33447 (0.1568h)
3	1	–1.28210 (0.adf2h)	+0.48181 (0.1ed6h)
4	1	–1.45514 (0.a2dfh)	+0.57831 (0.2503h)
5	1	–1.56195 (0.9c09h)	+0.64526 (0.294ch)
6	1	–1.63409 (0.976bh)	+0.69415 (0.2c6dh)
7	1	–1.68604 (0.9418h)	+0.73132 (0.2eceh)
8	1	–1.72516 (0.9197h)	+0.76050 (0.30ach)

FINE SCALE AND POWER RAMP
Fine Scale multiplier factors in the range [0, 2) with a step resolution of 2^{-16}. Power Ramp multiplier factors in the range [0, 1) with a step resolution of 2^{-14}.

FINE SCALING
Fine Scale multiplier factors range from [0, 2) with a step resolution of 2^{-15} in the AD6622 emulation mode and 2^{-16} in the AD6623 emulation mode. Scaling values for each channel are programmed at register 0xn0E in the AD6623 internal memory using the Microport interface.

RCF POWER RAMPING
When the output of the AD6623 is programmed to be a rapid series of on/off bursts of data, the DAC used to produce an analog output signal will produce undesirable spectral components that should (or must) be suppressed. Shaping or "ramping" the transition from no power to full power, and vice versa, reduces the amplitude of these spurious signals. To program the ramp function a user must provide, through the Microport, the ramp memory (RMEM) coefficient values (up to 64), number of RMEM coefficients to "construct" the ramp (1 to 64) and selection of a synchronizing signal source as discussed below. The programmable power ramp up/down unit allows power ramping on time-slot basis as specified for some wireless transmission technologies (e.g. TDMA).

The shape of the ramp is stored in RAM. The RAM coefficients (RMEM) allow complete sample-by-sample control at the RCF interpolated rate. This is particularly useful for time division multiplexed standards such as GSM/EDGE. A time slot or "burst" is ramped-up and down by multiplying the Fine Scaled output of the RCF by a series of up to 64 ramp coefficients. If more ramp resolution is required, up to 64 interpolated coefficients can be added if the Ramp Interpolation bit, 0xn16:1, is set to

Logic 1. This extends the maximum ramp length to 128 coefficients. Although the ramp is limited in length, its time duration is a function of the output sample rate of the RCF multiplied by the ramp length. Ramp duration is twice as long with Ramp Interpolation enabled than when it is not enabled.

The channel's Ramp Enable bit at control register address 0xn16: bit 0, must be set to Logic 1 or else the ramp function will be bypassed and the RCF output data is passed unaltered to the CIC interpolation stages. When in use, the maximum signal gain is dependent on what value is stored in the last valid RMEM (ramp memory) location. RMEM words are 14-bits with a range of [0-1).

When the ramp is triggered, the following sequence occurs (see Figures 26 and 27): RAMP-DOWN beginning at the last coefficient of the specified ramp length and proceeding, sample-by-sample, to the first coefficient. Next, a REST or quiet period (from 0 to 32 RCF output samples duration) occurs. During this time, the Mode bit (as shown in Figure 17, AD6623 Data Format and Bit Definition chart) is updated, input sampling is halted and any control register with a superscript 2 is updated. Modulator configurations can be updated while the ramp is "quiet" allowing for GSM and EDGE timeslots to be multiplexed without resetting or reconfiguring the channel. Lastly, RAMP-UP occurs beginning at the first coefficient and ending at the last coefficient of the specified length. The final output level from the ramp stage is equal to the RCF Fine Scale output level multiplied by the last ramp coefficient.

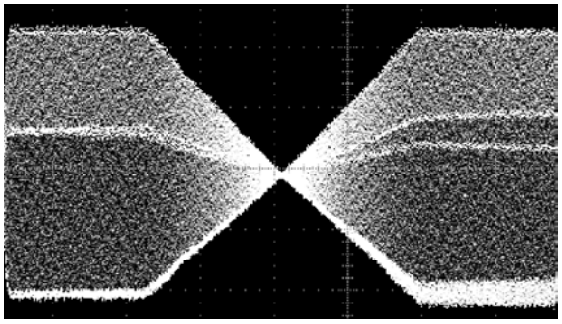


Figure 26. View of an unmodulated carrier with linear ramp-down and ramp-up and rest time between ramps set to 0.

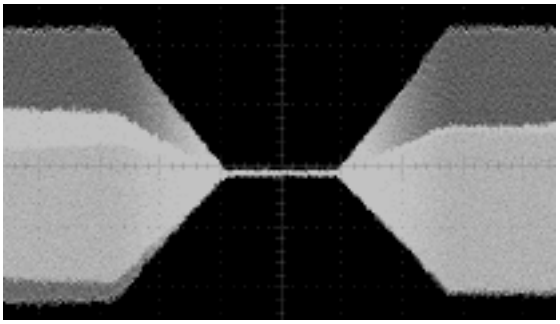


Figure 27. View of an unmodulated carrier with linear ramp-down and ramp-up and rest time between ramps set to 30 (RCF output sample time periods)

Ramp Triggering

The ramp sequence is triggered by the Fine Scale Hold-Off counter. The counter is loaded with a 16-bit user-specified value (>1 and $<2^{16}$) upon receipt of a sync pulse. The counter then counts-down (master CLK cycles) to 1, triggers the Ramp sequence and updates the Fine Scale factor. The counter will then stop at a count of zero. If the counter is initially loaded with 0, then the scale hold-off counter is bypassed and will not trigger any succeeding events. There are three ways to provide the sync pulse that loads the hold-off counter that ultimately triggers the ramp:

1. Serial Input sync. This method is selected when "Serial Time Slot Sync Enable", 0xn16:2, is set to Logic 1 and appropriate serial word input bits are set as described in Figure 17 (AD6623 Data Format and Bit Definition chart). This allows a channel's Fine Scale Hold-Off Counter to be loaded and a power ramp sequence to be triggered by a data word without resorting to hardware or software generated sync pulses. This sync signal is routed to the OR gate following the Time Slot Sync multiplexer shown in the Sync Control block diagram, Figure 37.
2. Hardware Sync. Sync Pins 0, 1, 2, and 3 provide a means to load the fine scale hold-off counter using the channel's "Time Slot Sync" multiplexer. The multiplexer allows selection of the desired hard or "pin"-sync signal using two software controlled select lines at register addresses 0xn0F:17 and 0xn0F:16. Pin-Sync is the most precise method of synchronization. This block shares 2 signals with the Beam Sync block. They are Software Beam Sync and Sync0. This means that whenever a Sync0 or soft beam sync is sent to the Beam Sync block, the same signals are also sent to the Time Slot Sync block.
3. Software Sync. This function allows the user to load Start, Hop, Beam and Fine Scale holdoff counters via software commands through the AD6623 Microport. Sync signals generated in this manner are the least precise means of synchronization. All software sync bits are located at address 5 of the external register (see Table XXI External Registers). The Time Slot soft-sync is derived from the shared Beam Sync soft sync. Setting D6, "Beam", high will generate a soft sync signal that loads the Fine Scale hold-off counter as well as the Beam Sync phase hold-off counter. User must select which channel(s) will receive the soft sync signal(s) using bits D0 through D3 at external address 5 and select what type of sync signal(s) is to be generated (using bits D4, 5 and 6 at address 5). As an example, to generate a Time Slot soft sync for channel C, a user would set bits D2 and D6 high. D6 is the actual sync signal and D2 routes the sync signal only to channel C.

Special Handling Required for SYNC0 Pin-Sync

Proper routing of Sync0 (a hardware sync pulse) for Time Slot Sync may require bits in several registers to be set depending upon the number of active channels. These control bits are located in the Internal "Common Function" Registers (address 0x001) and the Internal "Channel Function" Registers (address 0xn00, 0xn03, 0xn05, 0xn0F). Address 0x001 contains 8 bits that will mask the distribution of pin-sync pulses from Sync0 to all channels and enable which sync multiplexers (start, hop, and beam) receive Sync0 pulses. Furthermore, the MSB at 0x001 is a "First Sync Only" flag that, when high, allows only one Sync0 pulse to be routed to the selected sync block(s). Following this, all 8-bits of register 0x001 are cleared to completely mask off subsequent pulses.

Sync pulses from Sync1, 2, and 3 pins are not masked in any fashion and directly connect to all Sync multiplexers of all channels. The Sync Control Block Diagram, Figure 37, in the Synchronization section of this data sheet provides an overview of all sync signal routing for one channel.

CASCADED INTEGRATOR COMB (CIC) INTERPOLATING FILTERS

The I and Q outputs of the RCF stage are interpolated by two cascaded integrator comb (CIC) filters. The CIC section is separated into three discrete blocks: a fifth order filter (CIC5), a second order resampling filter (rCIC2), and a scaling block (CIC Scaling). The CIC5 and rCIC2 blocks each exhibit a gain that changes with respect to their rate change factors, L_{rCIC2}, M_{rCIC2}, and L_{CIC5}. The product of these gains must be compensated for in a shared CIC Scaling block and can be done to within 6 dB. The remaining compensation can come from the RCF (in the form of coefficient scaling) or the fine scaling unit.

CIC Scaling

The scale factor S_{CIC} is a programmable unsigned integer between 4 and 32. This is a combined scaler for the CIC5 and rCIC2 stages. The overall gain of the CIC section is given by the equation below

$$CIC_Gain = L_{CIC5}{}^{4} \times L_{rCIC2} \times 2^{-S_{CIC}} \quad (10)$$

CIC5

The first CIC filter stage, the CIC5, is a fifth order interpolating cascaded integrator comb whose impulse response is completely defined by its interpolation factor, L_{CIC5}. The value L_{CIC5}–1 can be independently programmed for each channel at location 0xn09.

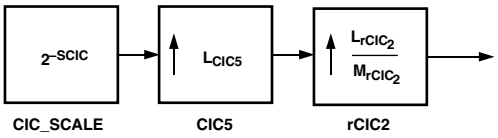


Figure 28. CIC5

While this control register is 8 bits wide, L_{CIC5} should be confined to the range from 1 to 32 to avoid the possibility of internal overflow for full scale inputs. The output rate of this stage is given by the equation below.

$$f_{CIC2} = f_{CIC5} \times L_{CIC5} \quad (11)$$

The transfer function of the CIC5 is given by the following equations with respect to the CIC5 output sample rate, f_{SAMP5}.

$$CIC5(z) = \left(\frac{1 - z^{-L_{CIC5}}}{1 - z^{-1}} \right)^5 \quad (12)$$

The SCIC value can be independently programmed for each channel at Control Register 0xn06. S_{CIC} may be safely calculated according to equation (13) below to ensure the net gain through the CIC stages.

SCIC serves to frame which bits of the CIC output are transferred to the NCO stage. This results in controlling the data out of the CIC stages in 6 dB increments. For the best dynamic range, S_{CIC} should be set to the smallest value possible (lowest attenuation) without creating an overflow condition. This can be safely accomplished using the equation below. To ensure the CIC output data is in range, Equation 13 must always be met. The maximum total interpolation rate may be limited by the amount of scaling available.

$$S_{CIC} \geq ceil\left(4 \times \log_2\left(L_{CIC5}\right) + \log_2\left(L_{CIC2}\right)\right) \quad (13)$$

$$0 \leq S_{CIC} \leq 58 \quad (14)$$

This polynomial fraction can be completely reduced as follows demonstrating a finite impulse response with perfect phase linearity for all values of L_{CIC5}.

$$CIC5(z) = \left(\sum_{k=0}^{L_{CIC5}-1} z^{-k} \right)^5 = \sum_{k=1}^{L_{CIC5}-1} \left(z^{-1} - e^{j2\pi \frac{k}{L_{CIC5}}} \right)^5 \quad (15)$$

The frequency response of the CIC5 can be expressed as follows. The initial $1/L_{CIC5}$ factor normalizes for the increased rate, which is appropriate when the samples are destined for a DAC with a zero order hold output. The maximum gain is $L_{CIC5}{}^{4}$ at baseband, but internal registers peak in response to various dynamic inputs. As long as L_{CIC5} is confined to 32 or less, there is no possibility of overflow at any register.

$$CIC5(f) = \frac{1}{L_{CIC5}} \left(\frac{sin\left(\pi \frac{L_{CIC5} \times f}{f_{CIC5}} \right)}{sin\left(\pi \frac{f}{f_{CIC5}} \right)} \right)^5 \quad (16)$$

The pass band droop of CIC5 should be calculated using this equation and can be compensated for in the RCF stage. The gain should be calculated from the CIC scaling section above.

As an example, consider an input from the RCF whose bandwidth is 0.141 of the RCF output rate, centered at baseband. Interpolation by a factor of five reveals five images, as shown below.

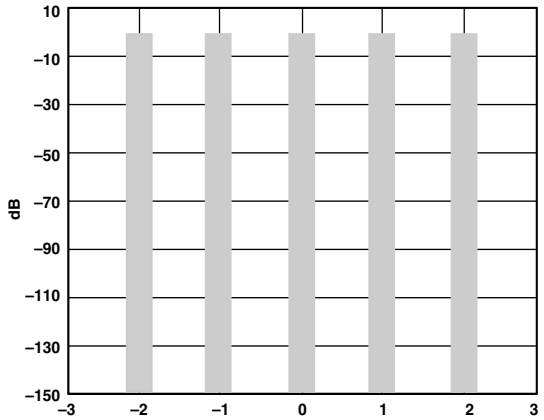


Figure 29. Unfiltered CIC5 Images

The CIC5 rejects each of the undesired images while passing the image at baseband. The images of a pure tone at channel center (DC) are nulled perfectly, but as the bandwidth increases the rejection is diminished. The lower band edge of the first image always has the least rejection. In this example, the CIC5 is interpolating by a factor of five and the input signal has a bandwidth of 0.141 of the RCF output sample rate. The plot below shows –110 dBc rejection of the lower band edge of the first image. All other image frequencies have better rejection.

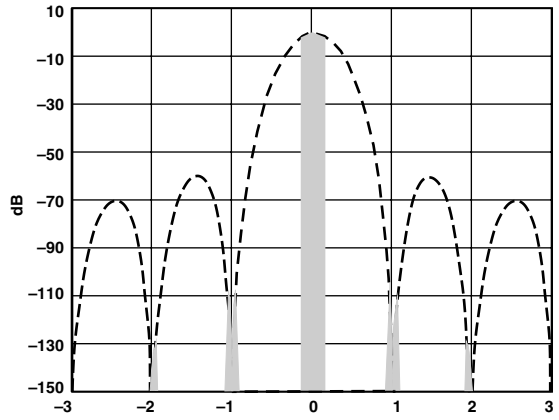


Figure 30. Filtered CIC5 Images

Table XII lists maximum bandwidth that will be rejected to various levels for CIC5 interpolation factors from 1 to 32. The example above corresponds to the listing in the –110 dB column and the L_{CIC5} = 5 row. It is worth noting here that the rejection of the CIC5 improves as the interpolation factor increases.

Table XII. Max Bandwidth of Rejection for L_{CIC5} Values

L_{CIC5}	–110 dB	–100 dB	–90 dB	–80 dB	–70 dB
1	Full	Full	Full	Full	Full
2	0.101	0.127	0.160	0.203	0.256
3	0.126	0.159	0.198	0.246	0.307
4	0.136	0.170	0.211	0.262	0.325
5	0.136	0.175	0.217	0.269	0.333
6	0.143	0.178	0.220	0.282	0.337
7	0.144	0.179	0.222	0.275	0.340
8	0.145	0.180	0.224	0.276	0.341
9	0.146	0.181	0.224	0.277	0.342
10	0.146	0.182	0.225	0.278	0.343
11	0.147	0.182	0.226	0.278	0.344
12	0.147	0.182	0.226	0.279	0.344
13	0.147	0.183	0.226	0.279	0.345
14	0.147	0.183	0.226	0.279	0.345
15	0.148	0.183	0.227	0.280	0.345
16	0.148	0.183	0.227	0.280	0.345
17	0.148	0.183	0.227	0.280	0.346
18	0.148	0.183	0.227	0.280	0.346
19	0.148	0.183	0.227	0.280	0.346
20	0.148	0.184	0.227	0.280	0.346
21	0.148	0.184	0.227	0.280	0.346
22	0.148	0.184	0.227	0.280	0.346
23	0.148	0.184	0.227	0.280	0.346
24	0.148	0.184	0.227	0.280	0.346
25	0.148	0.184	0.227	0.281	0.346
26	0.148	0.184	0.227	0.281	0.346
27	0.148	0.184	0.227	0.281	0.346
28	0.148	0.184	0.227	0.281	0.346
29	0.148	0.184	0.227	0.281	0.346
30	0.148	0.184	0.227	0.281	0.346
31	0.148	0.184	0.227	0.281	0.346
32	0.148	0.184	0.228	0.281	0.346

THE rCIC2 RESAMPLING INTERPOLATION FILTER

The rCIC2 filter is a second order re-sampling Cascaded Integrator Comb filter whose impulse response is defined by its rate-change factors, L_{rCIC2} and M_{rCIC2}. The r_{CIC2} filter is implemented using a technique that does not require a faster clock than the output rate thus simplifying design and saving power while maintaining jitter-free operation. The rCIC2 stage allows for noninteger relationships between the input data rate and the master clock. This allows easier implementation of systems that are either multimode or require a clock that is not a multiple of the input data rate. The overall effect is referred to as "rate-change". A specific rate-change is accomplished by choosing appropriate interpolation and decimation values for equation (17) below. For example, if an interpolation ratio of 2.69 is needed, then set L_{rCIC2} = 269 and M_{rCIC2} = 100.

Permissible Values of L_{rCIC2} and M_{rCIC2}

The two parameters that determine the rate-change of the rCIC2 filter are:

1. The interpolation factor, L_{rCIC2}, ranging from 1 to 4096 (12 bits)
2. The decimation factor, M_{rCIC2}, ranging from 1 to 512 (9 bits)

The range of L_{rCIC2} is limited by L_{CIC5} according to Table XIII.

Table XIII. Maximum Permissible L_{rCIC2} Values

Chosen L_{CIC5} Value	Maximum Allowed L_{rCIC2} Value
1 to 22	4095
23	3836
24	3236
25	2748
26	2349
27	2020
28	1746
29	1518
30	1325
31	1162
32	1024

M_{rCIC2} is restricted by equations (17) and (18) below.

$$M_{rCIC2} \le \frac{L_{rCIC2}}{1+COMPLEX} \quad (17)$$

Where: L_{rCIC2} = Interpolation of rCIC2
COMPLEX = Complex Output Mode (off = 0, on = 1),

$$(2\times TPP)+(4\times APE)+6 \ne (1+COMPLEX)\times ceil\left(L_{CIC5}\times\frac{L_{rCIC2}}{M_{rCIC2}}\right) \quad (18)$$

Where:
TPP = Taps Per Phase (of RAM Coefficient Filter)
APE = Allpass Phase Equalizer (off = 0, on = 1)
COMPLEX = Complex Output Mode (off = 0, on = 1)
ceil = when a value within the parenthesis is not an integer, then round-up to the next integer (e.g., 9.001 = 10)
L_{CIC5} = Interpolation rate of CIC5
L_{rCIC2} = Interpolation of rCIC2
M_{rCIC2} = Decimation of rCIC2

Resampling is implemented by apparently increasing the input sample rate by the factor L, using zero stuffing for the new data samples. Following the resampler is a second order cascaded integrator comb filter. Filter characteristics are determined only by the fractional rate change (L/M).

The filter can produce output signals at the full CLK rate of the AD6623. The output rate of this stage is given by the equation below.

$$f_{OUT} = \frac{L_{rCIC2}}{M_{rCIC2}} f_{rCIC2} \quad (19)$$

Both L_{rCIC2} and M_{rCIC2} are unsigned integers. The interpolation rate (L_{rCIC2}) may be from 1 to 4096 and the decimation (M_{rCIC2}) may be between 1 and 512. The stage can be bypassed by setting the L and M to 1.

The transfer function of the rCIC2 is given by the following equations with respect to the rCIC2 output sample rate, f_{OUT}.

$$rCIC2(z) = \left(\frac{1 - z^{-L_{rCIC2}}}{1 - z^{-1}} \right)^2 \quad (20)$$

Frequency Response of rCIC2

The frequency response of the rCIC2 can be expressed as follows. The maximum gain is L_{rCIC2} at baseband. The initial M_{rCIC2}/L_{rCIC2} factor normalizes for the increased rate, which is appropriate when the samples are destined for a DAC with a zero order hold output.

$$rCIC2(f) = \frac{M_{rCIC2}}{L_{rCIC2}} \left(\frac{\sin\left(\pi \frac{L_{rCIC2} \times f}{f_{out}} \right)}{\sin\left(\pi \frac{f}{f_{out}} \right)} \right)^2 \quad (21)$$

The pass-band droop of CIC5 should be calculated using this equation and can be compensated for in the RCF stage. The gain should be calculated from the CIC scaling section above.

Programming Guidelines for AD6623 CIC Filters

The values $M_{rCIC2}–1$, $L_{rCIC2}–1$ can be independently programmed for each channel at locations 0xn07, 0xn08. While these control registers are nine bits and 12 bits wide respectively, $M_{rCIC2}–1$ and $L_{rCIC2}–1$ should be confined to the ranges shown by Table XIII according to the interpolation factor of the CIC5. Exceeding the recommended guidelines may result in overflow for input sequences at or near full scale. While relatively large ratios of L_{rCIC2}/M_{rCIC2} allow for the larger overall interpolations with minimal power consumption, L_{rCIC2}/M_{rCIC2} should be minimized to achieve the best overall image rejection.

As an example, consider an input from the CIC5 whose bandwidth is 0.0033 of the CIC5 rate, centered at baseband. Interpolation by a factor of five reveals five images, as shown below.

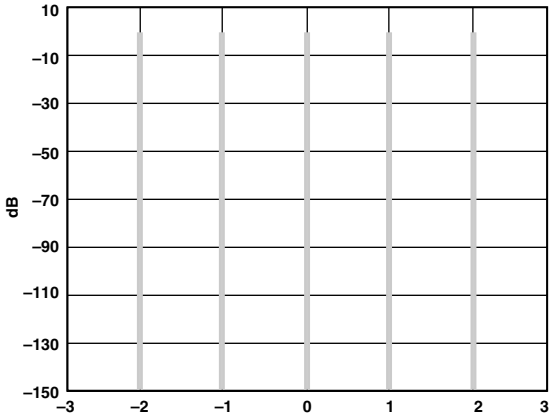


Figure 31. Unfiltered rCIC2 Images

The rCIC2 rejects each of the undesired images while passing the image at baseband. The images of a pure tone at channel center (DC) are nulled perfectly, but as the bandwidth increases the rejection is diminished. The lower band edge of the first image always has the least rejection. In this example, the rCIC2 is interpolating by a factor of five and the input signal has a bandwidth of 0.0033 of the CIC5 output sample rate. Figure 32 shows –110 dBc rejection of the lower band edge of the first image. All other image frequencies have better rejection.

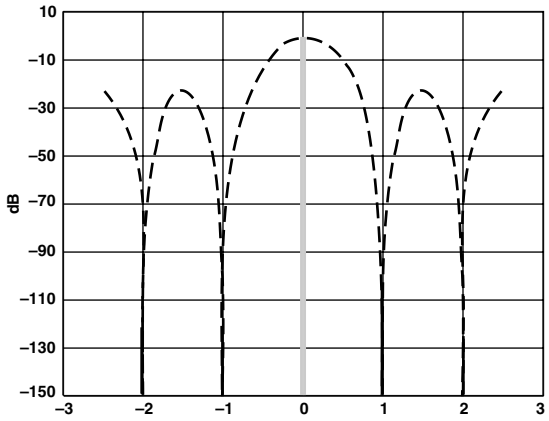


Figure 32. Filtered rCIC2 Images

Table XIV lists maximum bandwidth that will be rejected to various levels for CIC2 interpolation factors from 1 to 32. The example above corresponds to the listing in the –110 dB column and the L_{rCIC2} = 5 row. The rejection of the CIC2 improves as the interpolation factor increases.

Table XIV. Maximum Bandwidth of Rejection for L_{rCIC2} Values

L_{rCIC2}	–110 dB	–100 dB	–90 dB	–80 dB	–70 dB
1	Full	Full	Full	Full	Full
2	0.0023	0.0040	0.0072	0.0127	0.0226
3	0.0029	0.0052	0.0093	0.0165	0.0292
4	0.0032	0.0057	0.0101	0.0179	0.0316
5	0.0033	0.0059	0.0105	0.0186	0.0328
6	0.0034	0.0060	0.0107	0.0189	0.0334
7	0.0034	0.0061	0.0108	0.0192	0.0338
8	0.0035	0.0062	0.0109	0.0193	0.0341
9	0.0035	0.0062	0.0110	0.0194	0.0343
10	0.0035	0.0062	0.0110	0.0195	0.0344
11	0.0035	0.0062	0.0110	0.0195	0.0345
12	0.0035	0.0062	0.0111	0.0196	0.0346
13	0.0035	0.0062	0.0111	0.0196	0.0346
14	0.0035	0.0063	0.0111	0.0196	0.0346
15	0.0035	0.0063	0.0111	0.0197	0.0347
16	0.0035	0.0063	0.0111	0.0197	0.0347
17	0.0035	0.0063	0.0111	0.0197	0.0347
18	0.0035	0.0063	0.0111	0.0197	0.0348
19	0.0035	0.0063	0.0111	0.0197	0.0348
20	0.0035	0.0063	0.0111	0.0197	0.0348
21	0.0035	0.0063	0.0111	0.0197	0.0348
22	0.0035	0.0063	0.0111	0.0197	0.0348
23	0.0035	0.0063	0.0111	0.0197	0.0348
24	0.0035	0.0063	0.0112	0.0197	0.0348
25	0.0035	0.0063	0.0112	0.0198	0.0348
26	0.0035	0.0063	0.0112	0.0198	0.0349
27	0.0035	0.0063	0.0112	0.0198	0.0349
28	0.0035	0.0063	0.0112	0.0198	0.0349
29	0.0035	0.0063	0.0112	0.0198	0.0349
30	0.0035	0.0063	0.0112	0.0198	0.0349
31	0.0035	0.0063	0.0112	0.0198	0.0349
32	0.0035	0.0063	0.0112	0.0198	0.0349

NUMERICALLY CONTROLLED OSCILLATOR/TUNER (NCO)

Each channel has a fully independent tuner. The tuner accepts data from the CIC filter, tunes it to a digital Intermediate Frequency (IF), and passes the result to a shared summation block. The tuner consists of a 32-bit quadrature NCO and a Quadrature Amplitude Mixer (QAM). The NCO serves as a local oscillator and the QAM translates the interpolated channel data from baseband to the NCO frequency. The worst case spurious signal from the NCO is better than –100 dBc for all output frequencies. The tuner can produce real or complex outputs as requested by the shared summation block.

In the complex mode, the NCO serves as a quadrature local oscillator running at $f_{CLK}/2$ capable of producing any frequency step between $-f_{CLK}/4$ and $+f_{CLK}/4$ with a resolution of $f_{CLK}/2^{33}$ (0.0121 Hz for f_{CLK} = 104 MHz).

In the real mode, the NCO serves as a quadrature local oscillator running at f_{CLK} capable of producing any frequency step between $-f_{CLK}/2$ and $+f_{CLK}/2$ with a resolution of $f_{CLK}/2^{32}$ (0.0242 Hz for f_{CLK} = 104 MHz). The quadrature portion of the output is discarded. Negative frequencies are distinguished from positive frequencies solely by spectral inversion. The digital IF is calculated using the equation:

$$f_{IF} = f_{NCO} \times \frac{NCO_frequency}{2^{32}} \quad (22)$$

where:

NCO_frequency is the decimal equivalent of the 32-bit binary value written to 0xn02,

f_{IF} is the desired intermediate frequency (in Hz), and

f_{NCO} is $f_{CLK}/2$ (in Hz) for complex outputs and f_{CLK} (in Hz) for real outputs.

Phase Dither

The AD6623 provides a phase dither option for improving the spurious performance of the NCO. Phase dither is enabled by writing a "1" to Bit 3 of Channel Register 0xn01. When phase dither is enabled, spurs due to phase truncation in the NCO are randomized. The choice of whether phase dither is used in a system will ultimately be decided by the system goals and the choice of IF frequency. The 18 most significant bits of the phase accumulator are used by the angle to Cartesian conversion. If the NCO frequency has all zeroes below the 18th bit, then phase dither has no effect. If the fraction below the 18th bit is near a 1/2 or 1/3 of the 18th bit, then spurs will accumulate separated from the IF by 1/2 or 1/3 of the CLK frequency. The smaller the denominator of this residual fraction, the larger the spurs due to phase truncation will be. If the phase truncation spurs are unacceptably high for a given frequency, then the phase dither can reduce these at the penalty of a slight elevation in total error energy. If the phase truncation spurs are small, then phase dither will not be effective in reducing them further, but a slight elevation in total error energy will occur.

Amplitude Dither

Amplitude dither can also be used to improve spurious performance of the NCO. Amplitude dither is enabled by writing a "1" to Bit 4 of Channel Register at 0xn01. When enabled, amplitude dither can reduce spurs due to truncation at the input to the QAM. If the entire frequency word is close to a fraction that has a small

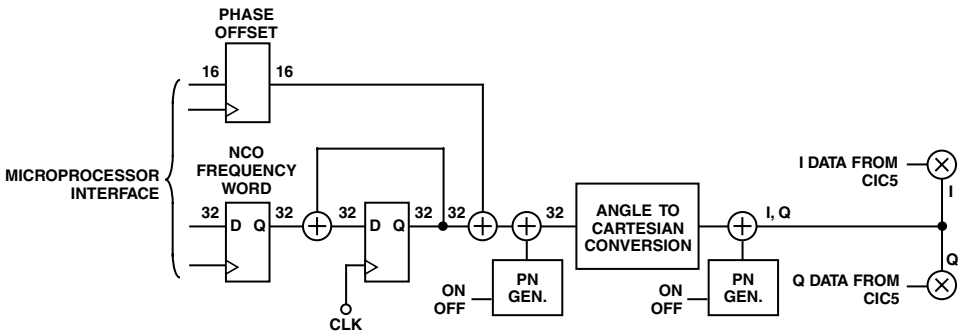


Figure 33. Numerically Controlled Oscillator and QAM Mixer

denominator, the spurs due to amplitude truncation will be large and amplitude dither will spread these spurs effectively. Amplitude dither also will increase the total error energy by approximately 3 dB. For this reason amplitude dither should be used judiciously.

Phase Offset
The phase offset (Channel Register 0xn04) adds an offset to the phase accumulator of the NCO. This is a 16-bit register that is interpreted as a 16-bit unsigned integer. Phase offset ranges from 0 to nearly 2π radians with a resolution of π/32768 radians. This register allows multiple NCOs to be synchronized to produce sine waves with a known phase relationship.

NCO Frequency Update and Phase Offset Update Hold-Off Counters
The update of both the NCO frequency and phase offset can be synchronized with internal Hold-Off counters. Both of these counters are 16-bit unsigned integers and are clocked at the master CLK rate. These Hold-Off counters used in conjunction with the frequency or phase offset registers, allow beam forming and frequency hopping. See the Synchronization section of the data sheet for additional details. The NCO phase can also be cleared on Sync (set to 0x0000) by setting Bit 2 of Channel Register 0xn01 high.

NCO Control Scale
The output of the NCO can be scaled in four steps of 6 dB each via Channel Register 0xn01, Bits 1–0. Table XV show a breakdown of the NCO Control Scale. The NCO always has loss to accommodate the possibility that both the I and Q inputs may reach full-scale simultaneously, resulting in a 3 dB input magnitude.

Table XV. NCO Control Scale

0xn01 Bit 1	0xn01 Bit 0	NCO Output Level
0	0	–6 dB (no attenuation)
0	1	–12 dB attenuation
1	0	–18 dB attenuation
1	1	–24 dB attenuation

SUMMATION BLOCK
The Summation Block of the AD6623 serves to combine the outputs of each channel to create a composite multicarrier signal. The four channels are summed together and the result is then added with the 18-bit Wideband Input Bus (IN[17:0]). The final summation is then driven on the 18-bit Wideband Output Bus (OUT[17:0]) on the rising edge of the high speed clock. If the OEN input is low then this output bus is three-stated. If the OEN input is high then this bus will be driven by the summed data. The OEN is active high to allow the Wideband Output Bus to be connected to other busses without using extra logic. Most other busses (like 374 type registers) require a low output enable, which is opposite of the AD6623 OEN, thus eliminating extra circuitry.

Dual 18-Bit Output Configuration
The wideband parallel input IN[17:0] is defined as bidirectional, to support dual parallel outputs. Each parallel output produces the sum of two of the four internal TSPs and AD6623 that can drive two DACs. Channels are added in pairs (A + B), (C + D) as shown in Figure 34.

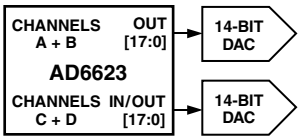


Figure 34. AD6623 Driving Two DACs

Output Data Format
The Wideband Output Bus may be interpreted as a two's complement number or as an offset binary number as defined by Bit 1 of the Summation Mode Control Register at address 0x000. When this bit is high, then the Wideband Output is in two's complement mode and when it is low it is configured for offset binary output data. Offset binary data format is used when driving an offset binary DAC or test equipment, etc., that can accept offset binary. The two's complement mode should be used in the following circumstances:

- When driving a DAC that accepts two's complement data
- When driving another AD6623 in cascade mode
- When driving test equipment, FIFO memory, etc. that can accept two's complement data format

Output Clip Detection
The MSB (Bit 17) of the Wideband Output Bus is typically used as a guard bit for the purpose of clipping the wideband output bus when Bit 0 of the Summation Mode Control Register at address 0x000 is high. If clip detection is enabled then Bit 17 of the output bus is not used as a data bit. Instead, Bit 16 will become the MSB and is connected to the MSB of the DAC. Configuring the DAC in this manner gives the summation block a gain of 0 dB. When clip detection is not enabled and Bit 17 is used as a data bit then the summation block will have a gain of –6.02 dB.

There are two data output modes. The first is offset binary. This mode is used only when driving offset binary DACs. Two's complement mode may be used in one of two circumstances. The first is when driving a DAC that accepts two's complement data. The second is when driving another AD6623 in cascade mode.

When clipping is enabled, the two's complement mode output bus will clip to 0x2FFFF for output signals more positive than the output can express and it will clip to 0x3000 for signals more negative than the output can express. In offset binary mode the output bus will clip to 0x3FFFF for output signals more positive than the output can express and it will clip to 0x2000 for signals more negative than the output can express.

Cascading Multiple AD6623s
The Wideband Input is always interpreted as an 18-bit two's complement number and is typically connected to the Wideband Output Bus of another AD6623 in order to send more than four carriers to a single DAC. The Output Bus of the preceding AD6623 should be configured in two's complement mode and clip detection disabled. The 18-bit resolution insures that the noise and spur performance of the wideband data stream does not become the limiting factor as large numbers of carriers are summed.

There is a two-clock cycle latency from the Wideband Input Bus to the Wideband Output Bus. This latency may be calibrated out of the system by use of the Start Hold-Off counter. The preceding AD6623 in a cascaded chain can be started two CLK cycles before the following AD6623 is started and the data from each AD6623 will arrive at the DAC on the same clock cycle. In systems where the individual signals are not correlated, this is usually not necessary.

Selection of Real and Complex Output Data Types
The AD6623 is capable of outputting both real and complex data. When in Real mode the QIN input is tied low signaling that all inputs on the Wideband Input Bus are real and that all outputs on the Wideband Output Bus are real. The Wideband Input Bus will be pulled low and no data will be added to the composite signal if this port is unused (not connected).

If complex data is desired there are two ways this can be obtained. The first method is to simply set the QIN input of the AD6623 high and to set the Wideband Input Bus low. This allows the AD6623 to output complex data on the Wideband Output Bus. The I data samples would be identified when QOUT is low and the Q data samples would be identified when QOUT is high. The second method of obtaining complex data is to provide a QIN signal that toggles on every rising edge of the CLK. This could be obtained by connecting the QOUT of another AD6623 to QIN as shown in Figure 35. In a cascaded system the QIN of the first AD6623 in the chain would typically be tied high and the QOUT of the first AD6623 would be connected to the QIN of the following part. All AD6623s will synchronize themselves to the QIN input so that the proper samples are always paired and the Wideband Output bus represents valid complex data samples. Table XVI shows different parallel input and output data bus formats as a function of QIN and QOUT.

Table XVI. Valid Output Bus Data Modes

QIN	Wideband Input IN[17:0]	Output Data Type OUT[17:0], QOUT
Low	Real	Real
High	Zero	Complex
Pulsed	Complex	Complex

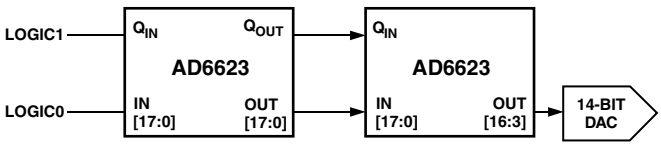


Figure 35. Cascade Operation of Two AD6623s

SYNCHRONIZATION
Three types of synchronization can be achieved with the AD6623. These are Start, Hop, and Beam. Each is described in detail below. The synchronization is accomplished with the use of a shadow register and a Hold-Off counter. See Figure 36 for a simplistic schematic of the NCO shadow register and NCO Frequency Hold-Off counter to understand basic operation. Enabling the clock (AD6623 CLK) for the Hold-Off counter can occur with either a Soft_Sync (via the Microport), or a Pin Sync. The functions that include shadow registers to allow synchronization include:
1. Start
2. Hop (NCO Frequency)
3. Beam (NCO Phase Offset)

Hold-Off Counters and Shadow Registers
Hold-Off Counters are used with the five synchronized AD6623 functions:

- Start of Channel(s)
- RCF Fine Scale output level update
- Power Ramping of Time Slot transmissions
- Frequency Hopping
- Phase Shifting for Beam ControlStart

These are 16-bit counters that are preloaded with a programmable value upon receipt of a synchronizing pulse. The counter then counts down to zero and stops. The counters are re-triggerable during countdown. If the counter is re-triggered, it re-loads its count value and starts again and may preclude the triggering of the event as intended. When the count reaches one, a trigger signal is emitted which causes the desired event (Start, Ramp, Hop, Beam, Scale) to commence. The counters are clocked with the AD6623 CLK that determines the time resolution of the each count. With a 104 MHz CLK, the resolution is approximately 10 ns and the delay range is from approximately 20 ns to 0.6 ms. If a Hold-Off Counter is loaded with 0, it will not respond to synchronizing pulses and the event will not be triggered by the hold-off counter.

The AD6623 can "trigger" all of the aforementioned events except Ramping without a soft-sync, pin-sync, or data-sync. This is through the use of the Sleep bit for each channel at External Address 5. Whenever a channel is brought out of sleep mode (sleep bit = ↓ low) an automatic pulse updates all active and shadow registers. This feature allows a channel to be reprogrammed while it is sleeping and then activated with immediate implementation of the changes.

Shadow Register are provided for three functions, Frequency Hop, Fine Scale, and Phase Offset. A shadow register precedes an active register. It holds the next number to be used by the active register whenever that function's hold-off counter causes the active register to be updated with the new value. Active registers are also updated with the contents of a shadow register any time the channel is brought out of the sleep mode.

A shadow register is updated during normal programming of the registers through the Microport. Active registers for frequency, fine scale and phase offset words can only receive their update data from a shadow register. When software reads-back a channel's programmed values, it is reading back the shadow registers of the fine scale and phase offset functions but reads the active frequency register as shown in Figure 36.

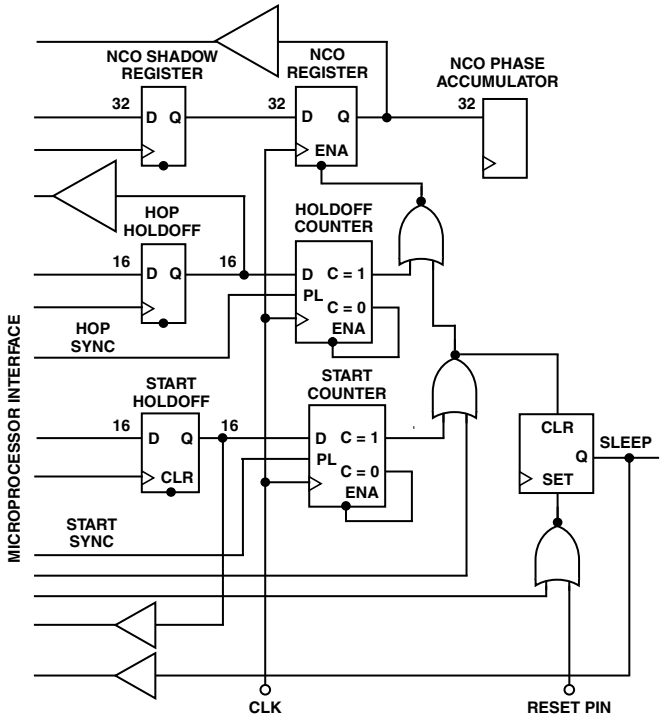


Figure 36. NCO Shadow Register and Hold-Off Counter

Start
Refers to the start-up of an individual channel, chip, or multiple chips. If a channel is not used, it should be put in the Sleep Mode to reduce power dissipation. Following a hard reset (low pulse on the AD6623 RESET pin), all channels are placed in the Sleep Mode.

Start With No Sync
If no synchronization is needed to start multiple channels or multiple AD6623s, the following method should be used to initialize the device.

1. To program a channel, it must first be set to the Program Mode (bit high) and Sleep Mode (bit high) (Ext Address 4). The Program Mode allows programming of data memory and coefficient memory (all other registers are programmable whether in Program Mode or not). Since no synchronization is used, all Sync bits are set low (External Address 5). All appropriate control and memory registers (filter) are then loaded. The Start Update Hold-Off Counter (0xn00) should be set to 0.
2. Set the appropriate program and sleep bits low (Ext Address 4). This enables the channel. The channel must have Program and Sleep Mode low to activate a channel.

Start with SoftSync
The AD6623 includes the ability to synchronize channels or chips under microprocessor control. One action to synchronize is the start of channels or chips. The Start Update Hold-Off Counter (0xn00) in conjunction with the Start bit and Sync bit (Ext Address 5) allow this synchronization. Basically the Start Update Hold-Off Counter delays the Start of a channel(s) by its value (number of AD6623 CLKs). The following method is used to synchronize the start of multiple channels via microprocessor control.

1. Set the appropriate channels to sleep mode (a hard reset to the AD6623 Reset pin brings all four channels up in Sleep Mode).
2. Write the Start Update Hold-Off Counter(s) (0xn00) to the appropriate value (greater than 1 and less than 2^{16}–1). If the chip(s) is not initialized, all other registers should be loaded at this step.
3. Write the Start bit and the Syncx(s) bit high (Ext Address 5).
4. This starts the Start Update Hold-Off Counter counting down. The counter is clocked with the AD6623 CLK signal. When it reaches a count of one the sleep bit of the appropriate channel(s) is set low to activate the channel(s).

Start with Pin Sync
Four hardware sync pins are available on the AD6623 to provide the most accurate synchronization, especially between multiple AD6623s. Synchronization of start with an external signal is accomplished with the following method.

1. Set the appropriate channels to sleep mode (a hard reset to the AD6623 Reset pin brings all four channels up in sleep mode).
2. Write the Start Update Hold-Off Counter(s) (0xn00) to the appropriate value (greater than 1 and less than 2^{16}–1). If the chip(s) is not initialized, all other registers should be loaded at this step.
3. Set the Start on Pin Sync bit and the appropriate Sync Pin Enable high (0xn01).
4. When the Sync pin is sampled high by the AD6623 CLK this enables the count down of the Start Update Hold-Off Counter. The counter is clocked with the AD6623 CLK signal. When it reaches a count of one the sleep bit of the appropriate channel(s) is set low to activate the channel(s).

Hop
A jump from one NCO frequency to a new NCO frequency. This change in frequency can be synchronized via microprocessor control or an external Sync signal as described below.

To set the NCO frequency without synchronization the following method should be used.

Set Frequency No Hop

1. Set the NCO Frequency Hold-Off Counter to 0.
2. Load the appropriate NCO frequency. The new frequency will be immediately loaded to the NCO.

Hop with SoftSync
The AD6623 includes the ability to synchronize a change in NCO frequency of multiple channels or chips under microprocessor control. The NCO Frequency Hold-Off Counter (0xn03) in conjunction with the Hop bit and the Sync bit (Ext Address 5) allow this synchronization. Basically the NCO Frequency Hold-Off counter delays the new frequency from being loaded into the NCO by its value (number of AD6623 CLKs). The following method is used to synchronize a hop in frequency of multiple channels via microprocessor control.

1. Write the NCO Frequency Hold-Off (0xn03) counter to the appropriate value (> 1 and < 2^{16}–1).
2. Write the NCO Frequency register(s) to the new desired frequency.
3. Write the Hop bit and the Sync(s) bit high (Ext Address 5).
4. This starts the NCO Frequency Hold-Off counter counting down. The counter is clocked with the AD6623 CLK signal. When it reaches a count of one the new frequency is loaded into the NCO.

Hop with Pin Sync
Four hardware Sync pins are available on the AD6623 to provide the most accurate synchronization, especially between multiple AD6623s. Synchronization of hopping to a new NCO frequency with an external signal is accomplished with the following method.

1. Write the NCO Frequency Hold-Off Counter(s) (0xn03) to the appropriate value (greater than 1 and less than 2^{16}–1).
2. Write the NCO Frequency register(s) to the new desired frequency.
3. Set the Hop on Pin Sync bit and the appropriate Sync pin Enable high (0xn01).
4. When the Sync pin is sampled high by the AD6623 CLK this enables the count down of the NCO Frequency Hold-Off Counter. The counter is clocked with the AD6623 CLK signal. When it reaches a count of one the new frequency is loaded into the NCO.

Beam
A change in phase for a particular channel and can be synchronized with respect to other channels or AD6623s. This change in phase can be synchronized via microprocessor control or an external Sync signal.

To set the amplitude without synchronization the following method should be used.

Set Phase No Beam
1. Set the NCO Phase Offset Update Hold-Off Counter (0xn05) to 0.
2. Load the appropriate NCO Phase Offset (0xn04). The NCO Phase Offset will be immediately loaded.

Beam with SoftSync
The AD6623 includes the ability to synchronize a change in NCO phase of multiple channels or chips under microprocessor control. The NCO Phase Offset Update Hold-Off Counter in conjunction with the Beam bit and the Sync bit (Ext Address 5) allow this synchronization. Basically the NCO Phase Offset Update Hold-Off Counter delays the new phase from being loaded into the NCO/RCF by its value (number of AD6623 CLKs). The following method is used to synchronize a beam in phase of multiple channels via microprocessor control.
1. Write the NCO Phase Offset Update Hold-Off Counter (0xn05) to the appropriate value (greater than 1 and less then 2^{16}–1).
2. Write the NCO Phase Offset register(s) to the new desired phase and amplitude.
3. Write the Beam bit and the Sync(s) bit high (Ext Address 5).
4. This starts the NCO Phase Offset Update Hold-Off Counter counting down. The counter is clocked with the AD6623 CLK signal. When it reaches a count of one the new phase is loaded into the NCO.

Beam with Pin Sync
Four hardware sync pins are available on the AD6623 to provide the most accurate synchronization, especially between multiple AD6623s. Synchronization of beaming to a new NCO Phase Offset with an external signal is accomplished using the following method.
1. Write the NCO Phase Offset Hold-Off (0xn05) Counter(s) to the appropriate value (greater than 1 and less than 2^{16}–1).
2. Write the NCO Phase Offset register(s) to the new desired phase and amplitude.
3. Set the Beam on Pin Sync bit and the appropriate Sync Pin Enable high (0xn01).
4. When the Sync pin is sampled high by the AD6623 CLK this enables the count down of the NCO Phase Offset Hold-Off counter. The counter is clocked with the AD6623 CLK signal. When it reaches a count of one the new phase is loaded into the NCO registers.

Time Slot (Ramp)
This enables power ramping and allows input data format changes during the "quiet" period after ramp-down. It must be synchronized using the Microport (soft sync), input data or a hardware sync pin. A Time Slot normally takes the form of: ramp-down to minimum power, "rest" period and ramp-up to maximum output power. See the "RCF POWER RAMPING" section of this data sheet for related information.

*The "Beam" soft sync signal is also routed to the Time Slot function. This is a "shared" bit and it provides soft sync pulses to both the Phase Hold-Off and Fine Scale Hold-Off counters simultaneously.

The PROG Mode bits located at External Address 4:7-4, referred to below, must be set HIGH whenever RMEM (ramp memory), CMEM (coefficient memory) or DMEM (data memory) are to be programmed. However, when programming is completed, the PROG bit for the channel(s) must be returned LOW for proper channel functioning.

Set Output Power, No Ramp
The steps below assume that the user has established a data flow from input to output of the AD6623.
1. Place the channel(s) in SLEEP Mode (external address 4:3-0, write bit(s) high).
2. Set bit 0 of Internal Address 0xn16 (the channel's Ramp Enable bit) to Logic 0. This defeats the ramp function.
3. Set the fine scaling and coarse scaling control register values associated with the RCF (0xn0D:7-6 and 0xn0E:15-2), CIC (0xn06:4-0), NCO (0xn01:1-0) and SUMMATION stages to the desired levels according to the SCALING section of this data sheet.
4. Finally, re-establish an output data flow to a DAC by bringing the appropriate SLEEP bits low and verify desired signal amplitude. Note: a START sync pulse is automatically generated when the channel is brought out of SLEEP Mode. The START pulse loads the updated control register data to the appropriate active counters and shadow registers.

Time Slot (Ramp) with SoftSync
Time Slot or ramping functions for each channel can be engaged with software synchronizing words received through the Microport. The RCF Fine Scale Hold-Off Counter in conjunction with the Beam bit* (which is the sync signal) and SyncA, B, C, and/or D (the channel to be sync'ed) in External Register address 5 allow this synchronization. The RCF Fine Scale Hold-Off Counter delays the beginning of the Time Slot function as well as updating the Fine Scale amplitude value (if applicable). The amount of time delay is set by the value (number of AD6623 CLK periods) written to the register at 0xn0F:15-0. Since the Time Slot event is of short duration, the user should consider a digital scope set for Normal or One-Shot triggering to capture the event and verify functionality. The following steps are used to synchronize a Time Slot or Ramp event with a software word received through the Microport; they assume that the user has established a data flow from input to output of the AD6623.
1. Place the channel(s) in SLEEP Mode (external address 4:3-0, write bit(s) high) and in the PROG Mode (external address 4:7-4, write the bit(s) high).
2. Write the Fine Scale Hold-Off Counter (0xn0F:15-0) to the appropriate value (>1 and <2^{16}–1).
3. Set the Ramp Enable bit (0xn16:0) high.
4. Load RMEM (ramp memory) with up to 64 coefficients (0xn40-17F) with the desired values ranging from 0 to 2^{14}–1 that represent the "shape" of the ramp transition. Where 0 is zero gain and 2^{14}–1 is unity gain.
5. Load the channel's ramp length minus 1, up to 63 at 0xn17
6. Load the channel's ramp rest time minus 1, up to 31, at 0xn19.
7. Re-establish an output data flow to the DAC by bringing the channel(s) SLEEP bits low and PROG bits LOW.
8. Write the Beam bit* high and desired Sync(A, B, C, and/or D) bit(s) high at Ext. Address 5. Return Beam bit to Logic 0.

9. This starts the Fine Scale Hold-Off Counter counting down. The counter is clocked with the AD6623 CLK signal. When it reaches a count of one, the ramp will commence from the last coefficient until it reaches the first coefficient of the specified ramp length. If a Rest has been programmed, Rest will commence for the programmed length and then the ramp will begin again at the first coefficient and ending at the last coefficient in the RMEM (ramp memory).

Time Slot with Pin Sync

The procedure for using the hardware synchronizing pins (SYNC0, 1, 2, and 3) to engage the Time Slot function is very similar to the Soft Sync. So for this case, only the differences between the two methods will be noted. It will be helpful to examine the Hardware and Software Sync Control Block Diagram, Figure 37, in order to visualize the process.

Hardware sync pins, (SYNC0, 1, 2, and 3), are all capable of loading the Fine Scale Hold-Off Counters that trigger the ramp function of any channel. The SYNC pin labels do not signify attachment to specific channels, but conversely, each SYNC pin is routed directly or indirectly to every channel. The task that the user faces is to see that the sync signal is properly routed and selected. The Time Slot Sync multiplexer seen in Figure 37 is used to select a hardware pin sync signal. SYNC1, 2, and 3 are directly routed to the multiplexer, whereas SYNC0 is routed through two AND gates before it reaches the multiplexer. The AND gates duplicate the AD6622 single sync pin function to allow pin compatibility.

*SYNC0 is routed in parallel to both the Beam and Time Slot multiplexers and it is a "shared" signal after is has been enabled at 0x001:6.

To use SYNC1, 2, or 3, simply set the select "lines" according to the Channel Register address (0xn0F:16-17) for the desired sync signal. Attach a sync signal source to the package pin. When it is time to sync, assert a Logic high (minimum 1 CLK period +2 ns duration) and return to Logic 0. This loads the Fine Scale Hold-Off Counter and a countdown commences. Holding a logic high at the chosen sync input pin longer than needed will result in additional delay as the Scale Hold-Off Counter is continually loaded with the same beginning count. From the Block Diagram, Figure 37, it can be seen (note the OR gates at the output of each multiplexer) that a software sync can also be used in conjunction with a hardware sync without any modification to the hardware setup.

SYNC0 is selected at the Time Slot multiplexer using the same select "lines" at 0xn0F:16-17 as for SYNC 1, 2, and 3; however, two additional "masking" registers must be dealt with to get SYNC0 routed to the Time Slot Sync multiplexer. First, SYNC0 must be enabled to enter the desired channel(s) using Common Function Register address 0x001:3-0 (Logic High = selected). Secondly, once the channel(s) is/are selected, then the Beam* multiplexer must be selected as the destination for Sync0 by setting 0x001:6 to Logic High.

Once the pin sync signals have been connected, routed and selected, the procedure for triggering a Time Slot or Ramp sequence is nearly identical as outlined for a soft sync except for Step 8. The user should substitute the pin-sync procedure in place of the soft sync method.

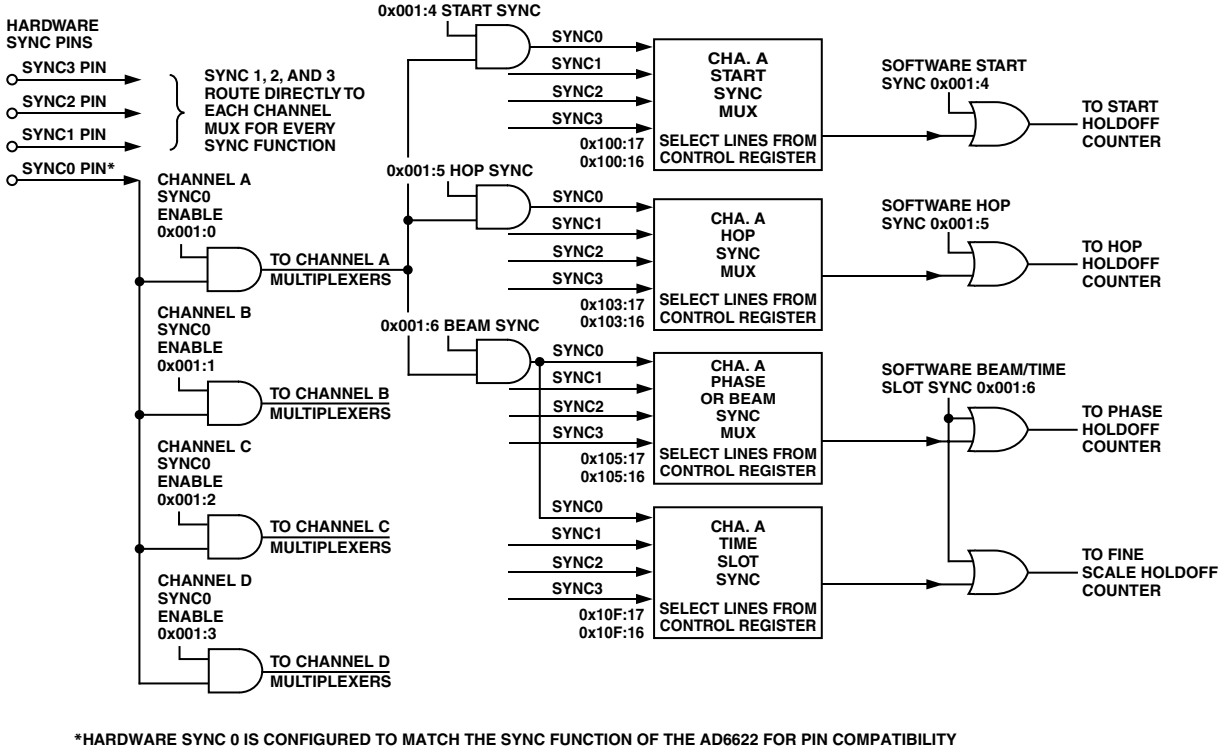


Figure 37. Block Diagram of Hardware and Software Sync Control for One AD6623 Sync Channel

JTAG INTERFACE

The AD6623 supports a subset of IEEE Standard 1149.1 specification. For additional details of the standard, please see *IEEE Standard Test Access Port and Boundary-Scan Architecture*, IEEE-1149 publication from IEEE.

The AD6623 has five pins associated with the JTAG interface. These pins are used to access the on-chip Test Access Port and are listed in Table XVII.

Table XVII. Test Access Port Pins

Name	Pin Number	Description
$\overline{\text{TRST}}$	100	Test Access Port Reset
TCK	101	Test Clock
TMS	106	Test Access Port Mode Select
TDI	108	Test Data Input
TDO	107	Test Data Output

Note that TCK and TDI are internally pulled down which is opposite of IEEE Standard 1149.1. These pins may be connected to external pull-up resistors, with the associated additional current draw through the pull-ups, or left unconnected.

The AD6623 supports four op codes are shown in Table XVIII. These instructions set the mode of the JTAG interface.

Table XVIII. Op Codes

Instruction	Op Code
IDCODE	10
BYPASS	11
SAMPLE/PRELOAD	01
EXTEST	00

The Vendor Identification Code (Table XIX) can be accessed through the IDCODE instruction and has the following format.

Table XIX. Vendor Identification Code

MSB Version	Part Number	Manufacturer ID Number	LSB Mandatory
0000	0010 0111 1000 0000	000 1110 0101	1

A BSDL file for this device is available from Analog Devices, Inc. Contact Analog Devices for more information.

SCALING

Proper scaling of the wideband output is critical to maximize the spurious and noise performance of the AD6623. A relatively small overflow anywhere in the data path can cause the spurious free dynamic range to drop precipitously. Scaling down the output levels also reduces dynamic range relative to an approximately constant noise floor. A well-balanced scaling plan at each point in the signal path will be rewarded with optimum performance. The scaling plan can be separated into two parts: multicarrier scaling and single-carrier scaling.

Multicarrier Scaling

An arbitrary number of AD6623s can be cascaded to create a composite digital IF with many carriers. As the number of carriers increases, the peak to rms ratio of the composite digital IF will increase as well. It is possible and beneficial to limit the peak to rms ratio through careful frequency planning and controlled phase offsets. Nevertheless, in most cases with a large number of carriers, the worst-case peak is an unlikely event.

The AD6623 immediately preceding the DAC can be programmed to clip rather than wrap around (see the Summation Block description). For a large number of carriers, a rare but finite chance of clipping at the AD6623 wideband output will result in superior dynamic range compared to lowering each carrier level until clipping is impossible. This will also be the case for most DACs. Through analysis or experimentation, an optimal output level of individual carriers can be determined for any particular DAC.

Single-Carrier Scaling

Once the optimal power level is determined for each carrier, one must determine the best way to achieve that level. The maximum SNR can be achieved by maximizing the intermediate power level at each processing stage. This can be done by assuming the proper level at the output and working along the following path: Summation, NCO, CIC, Ramp, RCF, and finally, Fine Scaler Unit.

The Summation Block is intended to combine multiple carriers with each carrier at least 6 dB below full scale. For this configuration, the AD6623 driving the DAC should have clip detection enabled. OUT17 becomes a clip indicator that reports clipping in both polarities. If the DAC requires offset binary outputs, then the internal offset binary conversion should be enabled as well. Any preceding cascaded AD6623s should disable clip detection and offset binary conversion. The IN17–IN0 of the first AD6623 in the cascade should be grounded. See the Summation Block section for details. In this configuration, intermediate OUT17s will serve as guard bits that allow intermediate sums to exceed full scale. As long as the final output does not exceed 6 dB over full scale, the clip detector will perform correctly.

If a single carrier needs to exceed –6 dB full scale, hardwired scaling can be accomplished according to Table XX. This is most useful when the AD6623 is processing a Single Wideband Carrier such as UMTS or CDMA 2000.

Table XX. Hardwired Scaling

Max. Single Carrier Level	Connect to DAC MSB	Clip Detect	Offset Binary Compensation
–12.04 dB	OUT17	N/A	Internal
–6.02 dB	OUT16	±	Internal
0 dB	OUT15	+ only	0x08000
+6.02 dB	OUT14	+ only	0x0C000

The NCO/Tuner is equipped with an output scaler that ranges from –6.02 dB to –24.08 dB below full scale, in +6.02 dB steps. See the NCO/Tuner section for details. The best SNR will be achieved by maximizing the input level to the NCO and using the largest possible NCO attenuation. For example, to achieve an output level –20 dB below full scale, one should set the CIC output level to –1.94 dB below full scale and attenuate by –18.06 dB in the NCO.

The CIC is equipped with an output scaler that ranges from 0 dB to –186.64 dB below full scale in +6.02 dB steps. This large attenuation is necessary to compensate for the potentially large gains associated with CIC interpolation. See the CIC section for details. For example to achieve an output level of –1.94 dB below full scale, with a CIC5 interpolation of 27 (+114.51 dB gain) and a CIC2 interpolation of 3 (+9.54 dB gain), one should set the CIC_Scale to 20 and the Fine Scale Unit output level to –5.59 dB below full scale.

$$-1.94 - 9.54 - 114.51 + 20 \times 6.02 = -5.59 \quad (23)$$

The ramp unit when bypassed will have exactly 0 dB of gain and can be ignored. When in use, the gain is dependant on what value is stored in the last valid RMEM location. RMEM words are 14 bits [0–1), so when the value is positive full scale, the gain is about –0.0005 dB; probably neglectable.

The RCF coefficients should be normalized to positive full scale. This will yield the greatest dynamic range. The RCF is equipped with an output scaler that ranges from 0 dB to –18.06 dB below full scale in +6.02 dB steps. This attenuation can be used to partially compensate for filter gain in the RCF. For example, if the maximum gain of the RCF coefficients is +11.26 dB, the RCF coarse scale should be set to 2 (+12.04 dB). This yields an RCF output level and fine scale input level of –0.78 dB

$$11.26 - 12.04 = -0.78 \quad (24)$$

The fine scale unit is left to turn a –0.78 dB level into a –5.59 dB level. This requires a gain of –4.81 dB, which corresponds to a 14-bit [0–2] scale value of 1264h. All subsequent rescalings during chip operation should be relative to this maximum.

$$-5.59 - 0.78 = -4.81 \quad (25)$$

$$floor\left(10^{\frac{-4.81}{20}} \times 2^{13}\right) = 1264h \quad (26)$$

Finally, as described in the RCF section, there may be a worst-case peak of a phase that is larger than the channel center gain. In the preceding example, if the worst case to channel center ratio is larger than 4.59 dB (potentially overflowing the RCF), then the RCF_Coarse_Scale should be reduced by one and the CIC_Scale should be increased by one. In the preceding example, if the worst case to channel center ratio is larger than 5.59 dB (potentially overflowing the RCF and CIC), then the RCF_Coarse_Scale should be reduced by one and the NCO_Output_Scale should be increased by one.

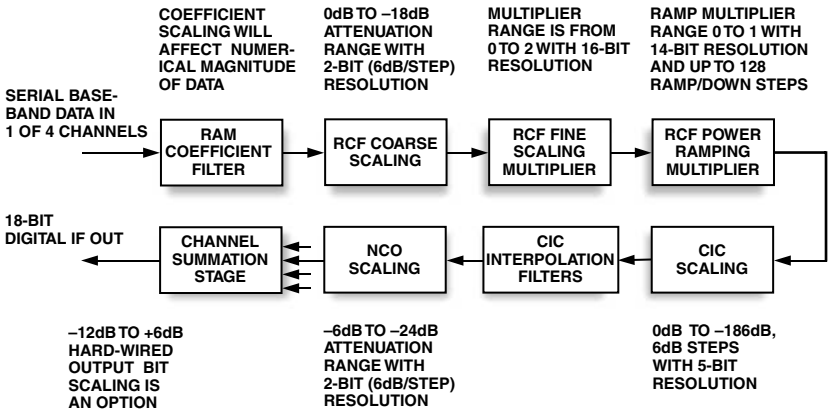


Figure 38. AD6623 Stage-by-Stage Summary of Available Scaling and Power Ramping Functions

MICROPORT INTERFACE

The Microport interface is the communications port between the AD6623 and the host controller. There are two modes of bus operation: Intel nonmultiplexed mode (INM), and Motorola nonmultiplexed mode (MNM) that is set by hard-wiring the MODE pin to either ground or supply. The mode is selected based on the use of the Microport control lines (DS or RD, DTACK or RDY, RW, or WR) and the capabilities of the host processor. See the timing diagrams for details on the operation of both modes.

The External Memory Map provides data and address registers to read and write the extensive control registers in the Internal Memory Map. The control registers access global chip functions and multiple control functions for each independent channel.

Microport Control

All accesses to the internal registers and memory of the AD6623 are accomplished indirectly through the use of the microprocessor port external registers shown in Table XXI. Accesses to the External Registers are accomplished through the 3 bit address bus (A[2:0]) and the 8-bit data bus (D[7:0]) of the AD6623 (Microport). External Address [3:0] provides access to data read from or written to the internal memory (up to 32 bits). External Address [0] is the least significant byte and External Address [3] is the most significant byte. External Address [4] controls the Sleep Mode of each channel. External Address [5] controls the sync status of each channel. External Address [7:6] determines the Internal Address selected and whether this address is incremented after subsequent reads and/or writes to the internal registers.

EXTERNAL MEMORY MAP

The External Memory Map is used to gain access to the Internal Memory Map described below. External Address [7:6] sets the Internal Address to which subsequent reads or writes will be performed. The top two bits of External Address [7] allow the user to set the address to auto increment after reads, writes, or both. All internal data words have widths that are less than or equal to 32 bits. Accesses to External Address [0] also triggers access to the AD6623's internal memory map. Thus during writes to the Internal Registers, External Address [0] must be written last to insure all data is transferred. Reads are the opposite in that External Address [0] must be the first data register read (after setting the appropriate internal address) to initiate an internal access.

External Address [5:4] reads and writes are transferred immediately to Internal Control Registers. External Address [4] is the sleep register. The sleep bits can be set collectively by the address. The sleep bits can be cleared by operation of start syncs as shown in Table XXI.

Table XXI. External Registers

External Address	External Data							
	D7	D6	D5	D4	D3	D2	D1	D0
7:UAR	Wrinc	Rdinc	–	–	IAII	IAIO	IA9	IA8
6:LAR	IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0
5:SoftSync	–	Beam	Hop	Start	Sync D	Sync C	Sync B	Sync A
4:Sleep	Prog D	Prog C	Prog B	Prog A	Sleep D	Sleep C	Sleep B	Sleep A
3:Byte3	ID31	ID30	ID29	ID28	ID27	ID26	ID25	ID24
2:Byte2	ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16
1:Byte1	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
0:Byte0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

External Address [5] is the Sync register. These bits are write only. There are three types of Syncs: Start, Hop, and Beam. Each of these can be sent to any or all of the four channels. For example, a write of X0010100 would issue a start sync to Channel C only. A write of X1101111 would issue a Beam Sync and a Hop Sync to all channels.

The internal address bus is 12 bits wide and the internal data bus is 32 bits wide. External address 7 is the UAR (Upper Address Register) and stores the upper four bits of the address space in UAR[3:0]. UAR[7:6] define the auto-increment feature. If Bit 6 is high, the internal address is incremented after an internal read. If Bit 7 is high, the internal address is incremented after an internal write. If both bits are high, the internal address in incremented after either a write or a read. This feature is designed for sequential access to internal locations. External address 6 is the LAR (Lower Address Register) and stores the lower 8 bits of the internal address. External addresses 3 through 0 store the 32 bits of the internal data. All internal accesses are two clock cycles long.

Writing to an internal location with a data width of 16 bits is achieved by first writing the upper four bits of the address to Bits 3 through 0 of the UAR (Bits 7 and 6 of the UAR are written to determine whether or not the auto increment feature is enabled). The LAR is then written with the lower eight bits of the internal address (it doesn't matter if the LAR is written before the UAR as long as both are written before the internal access). Since the data width of the internal address is 16 bits, only Data Register 1 and Data Register 0 are needed. Data Register 1 must be written first because the write to Data Register 0 triggers the internal access. Data Register 0 must always be the last register written to initiate the internal write.

Reading from the Microport is accomplished in a similar manner. The internal address is first written. A read from Data Register 0 activates the internal read, thus Register 0 must always be read first to initiate an internal read. This provides the 8 LSBs of the internal read through the Microport (D[7:0]). Additional bytes are then read by changing the external address (A[2:0]) and performing additional reads. If Data Register 3 (or any other) is read before Data Register 0, incorrect data will be read. Data Register 0 must be read first in order to transfer data from the Core Memory to the External Memory locations. Once the data register is read, the remaining locations may be examined in any order.

Access to the external registers of Table XXI is accomplished in one of two modes using the $\overline{CS}$, $\overline{DS}$($\overline{RD}$), RW($\overline{WR}$), and $\overline{DTACK}$(RDY) inputs. The access modes are Intel Nonmultiplexed mode and Motorola Nonmultiplexed mode. These modes are controlled by the MODE input (MODE = 0 for INM, MODE = 1 for MNM).

Intel Nonmultiplexed Mode (INM)
MODE must be tied low to operate the AD6623 Microport in INM mode. The access type is controlled by the user with the chip select ($\overline{CS}$), read ($\overline{RD}$), and write ($\overline{WR}$) inputs. The ready (RDY) signal is produced by the Microport to communicate to the user the Microport is ready for an access. RDY goes low at the start of the access and is released when the internal cycle is complete. See the timing diagrams for both the read and write modes in the Specifications.

Motorola Nonmultiplexed Mode (MNM)
MODE must be tied high to operate the AD6623 Microport in MNM mode. The access type is controlled by the user with the chip select ($\overline{CS}$), data strobe ($\overline{DS}$), and read/write (RW) inputs. The data acknowledge ($\overline{DTACK}$) signal is produced by the Microport to acknowledge the completion of an access to the user. $\overline{DTACK}$ goes low when an internal access is complete and then will return high after $\overline{DS}$ is deasserted. See the timing diagrams for both the read and write modes in the Specifications.

The $\overline{DTACK}$(RDY) pin is configured as an open drain so that multiple devices may be tied together at the microprocessor/ microcontroller without contention.

The Microport of the AD6623 allows for multiple accesses while $\overline{CS}$ is held low ($\overline{CS}$ can be tied permanently low if the Microport is not shared with additional devices). The user can access multiple locations by pulsing the RW($\overline{WR}$) or $\overline{DS}$($\overline{RD}$) lines and changing the contents of the external three bit address bus (A[2:0]).

External Address 7 Upper Address Register (UAR)
Sets the four most significant bits of the internal address, effectively selecting channels 1, 2, 3, or 4 (D2:D0). The autoincrement of read and write are also set (D7:D6).

External Address 6 Lower Address Register (LAR)
Sets the internal address 8 LSBs (D7:D0).

External Address 5, SoftSync
This register is write only. Bits in this address control the software synchronization or "softsync" of the AD6623 channels. If the user intends to bring up channels with no synchronization requirements or opts for "Pin Sync" control, then all bits of this register should be written low. Two types of sync signals are available with the AD6623. The first is Soft Sync. Soft Sync is software synchronization enabled through the Microport. The second synchronization method is Pin Sync. Pin Sync is enabled by a signal applied to the Sync 0-3 Pins. See the Synchronization section for detailed explanations of the different modes.

External Address 4 Sleep
Bits in this register determine how the chip is programmed and enables the channels. The program bits (D7:D4) must be set high to allow programming of CMEM and DMEM for each channel. Sleep bits (D3:D0) are used to activate or sleep channels. These can be used manually by the user to bring up a channel by simply writing the required channel high. These bits can also be used in conjunction with the Start and Sync signals available in External Address 5 to synchronize the channels. See the Synchronization section for a detailed explanation of different modes.

External Address 3:0 (Data Bytes)
These registers return or accept the data to be accessed for a read or write to internal addresses.

INTERNAL COUNTER REGISTERS AND ON-CHIP RAM

AD6623 and AD6622 Compatibility
The AD6623 functions and programmability significantly exceed those of the AD6622 while maintaining AD6622 pin compatibility and functionality when desired. AD6622 compatibility is selected when Bit 7 of Internal Control Register 0x000 is low. In this state, all AD6623 extended control registers are cleared. While in the AD6622 mode the unused AD6623 pins are three-stated.

Listed below is the mapping of internal AD6623 registers. AD6622 compatibility is selected by setting 0x000:7 low. In this state, all AD6623 extended control registers are cleared. Registers marked as "Reserved" must be written low.

Common Function Registers (not associated with a particular channel)

Internal Address	Bit	AD6622 Compatible Description	AD6623 Extensions Description
0x000	7	AD6623 Extension = 0[1]	AD6623 Extension = 1[1]
	6–5	Reserved	No Change
	4	Reserved	Wideband Input Disable[1]
	3	Reserved	Dual Output Enable[1]
	2	Reserved	No Change
	1	Offset Binary Outputs[1]	No Change
	0	Clip Wideband I/O[1]	No Change
0x001	7	First Sync Only[2]	No Change
	6	Beam on Pin Sync[2]	No Change
	5	Hop on Pin Sync[2]	No Change
	4	Start on Pin Sync[2]	No Change
	3	Ch. D Sync0 Pin Enable[2]	No Change
	2	Ch. C Sync0 Pin Enable[2]	No Change
	1	Ch. B Sync0 Pin Enable[2]	No Change
	0	Ch. A Sync0 Pin Enable[2]	No Change
0x002	23–0	Unused	BIST Counter[1, 2]
0x003	15–0	Unused	BIST Value (read only)

Channel Function Registers (0x1xx = Ch. A, 0x2xx = Ch. B, 0x3xx = Ch. C, 0x4xx = Ch. D)

Internal Address	Bit	AD6622 Compatible Description	AD6623 Extensions Description
0x100	17–16	Unused	Ch. A Start Sync Select[2] 00: Sync0 (See 0x001) 01: Sync1 10: Sync2 11: Sync3
	15–0	Ch. A Start Hold-Off Counter[2]	No Change
0x101	7–5	Reserved	No Change
	4	Ch. A NCO Amplitude Dither Enable	No Change
	3	Ch. A NCO Phase Dither Enable	No Change
	2	Ch. A NCO Clear Phase Accumulator on Sync	No Change
	1–0	Ch. A NCO Scale	No Change
		00: –6 dB	No Change
		01: –12 dB	No Change
		10: –18 dB	No Change
		11: –24 dB	No Change
0x102	31–0	Ch. A NCO Frequency Value[2]	No Change
0x103	17–16	Unused	Ch. A Hop Sync Select[2] 00: Sync0 (See 0x001 Hop) 01: Sync1 10: Sync2 11: Sync3
	15–0	Ch. A NCO Frequency Update Hold–Off Counter[2]	No Change
0x104	15–0	Ch. A NCO Phase Offset[3]	No Change[3]

Channel Function Registers (continued)

Internal Address	Bit	AD6622 Compatible Description	AD6623 Extensions Description
0x105	17–16	Reserved	Ch. A Phase Sync Select[2] 00: Sync0 (See 0x001 Beam) 01: Sync1 10: Sync2 11: Sync3
	15–0	Ch. A NCO Phase Offset Update Hold–off Counter[2]	No Change
0x106	7–5	Reserved	No Change
	4–0	Ch. A CIC Scale, S_{CIC}	No Change
0x107	8–0	Reserved	Ch. A CIC2 Decimation, M_2 –1
0x108	11–8	Reserved	Ch. A CCI2 Interpolation, L_2 –1, extended
	7–0	Ch. A C1C2 Interpolation, L_2 –1	No Change
0x109	7–0	Ch. A C1C5 Interpolation, L_5 –1	No Change
0x10A	15–8	Reserved	Ch. A RCF TapsB, N_{RCF} – 1 (8 bits)[2]
	7	Reserved	Ch. A RCF TapsA, N_{RCF} – 1 (new MSB)[3]
	6–0	Ch. A RCF TapsA, N_{RCF} – 1 (7 bits)[2]	No Change[3]
0x10B	7	Reserved	Ch. A RCF Coef Offset, O_{RCF} (new MSB)[3]
	6–0	Ch. A RCF Coefficient Offset, O_{RCF} (7 bits)[2]	No Change[3]
0x10C	15–10	Unused	Reserved
	9	Unused	Ch. A Compact FIR Input Word Length 0: 16 bits—8 I followed by 8 Q 1: 24 bits—12 I followed by 12 Q
	8	Unused	Ch. A RCF PRBS Enable
	7	Ch. A PRBS Length[2] 0: 15 1: 8,388,607	Ch. A RCF PRBS Length[2] 0: 15 1: 8,388,607
	6	Ch. A RCF PRBS Enable	Ch. A RCF Mode Select (1 of 3)[3]
	5	Ch. A RCF Mode Select (1 of 2)[2]	Ch. A RCF Mode Select (2 of 3)[3]
	4	Ch. A RCF Mode Select (2 of 2)[2] 00: FIR 01: FIR 10: QPSK 11: MSK	Ch. A RCF Mode Select (3 of 3)[3] 000: FIR 001: π/4–DQPSK 010: GMSK 011: MSK 100: FIR, Compact Input Resolution 101: 8–PSK 110: 3π/8–8PSK 111: QPSK
	3–0	Ch. A RCF (Taps per Phase) –1[2]	No Change[3]
0x10D	7–6	Ch. A RCF Coarse Scale (a) 00: 0 dB 01: –6 dB 10: –12 dB 11: –18 dB	No Change[3]
	5	Ch. A RCF Phase EQ Enable	No Change
	4–0	Ch. A Serial Clock Divisor (2, 4, …64)	Ch. A Serial Clock Divisor (1, 2,…32)
0x10E	15	Ch. A Serial Fine Scale Factor Enable	Ch. A Unsigned Scale Factor[3] This is extended to allow values in the range (0–2).
	14–2	Ch. A RCF Unsigned Scale Factor [3]	No Change[3]
	1–0	Reserved	Reserved
0x10F	17–16	Unused	Ch. A Time Slot Sync Select 00: Sync0 (See 0x001 Beam) 01: Sync1 10: Sync2 11: Sync3
	15–0	Ch. A RCF Scale Hold–Off Counter[2]	The counter is unchanged, but instead of just scale update, when the counter hits one, the following sequence is initiated: 1. Ramp Down (if Ramp is enabled) 2. Update RCF Mode Select registers marked with "2". 3. Ramp Up (if Ramp is enabled)

Channel Function Registers (continued)

Internal Address	Bit	AD6622 Compatible Description	AD6623 Extensions Description
0x110	15–0	Ch. A RCF Phase EQ Coef1	No Change
0x111	15–0	Ch. A RCF Phase EQ Coef2	No Change
0x112	15–0	Unused	Ch. A RCF FIR–PSK Magnitude 0
0x113	15–0	Unused	Ch. A RCF FIR–PSK Magnitude 1
0x114	15–0	Unused	Ch. A RCF FIR–PSK Magnitude 2
0x115	15–0	Unused	Ch. A RCF FIR–PSK Magnitude 3
0x116	7–6	Unused	Ch. A Serial Data Frame Input Select 0x: Internal Frame Request 10: External SDFI Pad 11: Previous Channel's Frame End
	5	Unused	Ch. A Serial Data Frame Output Select 0: Serial Data Frame Request 1: Serial Data Frame End
	4	Unused	Ch. A Serial Clock Slave (SCS) SCS = 0: Master Mode (SCLK is an output) SCS = 1: Slave Mode (SCLK is an input)
	3	Unused	Reserved
	2	Unused	Ch. A Serial Time Slot Sync Enable (ignored in FIR mode)
	1	Unused	Ch. A Ramp Interpolation Enable
	0	Unused	Ch. A Ramp Enable
0x117	5–0	Unused	Ch. A Mode 0 Ramp Length, R0–1
0x118	4–0	Unused	Ch. A Mode 1 Ramp Length, R1–1
0x119	4–0	Unused	Ch. A Ramp Rest Time, Q (No inputs requested during rest time.)
0x11A–11F		Unused	No Change
0x120–13F	15–0	Ch. A Data RAM	No Change
0x140–17F	15–14	Unused	No Change
	13–0	Unused	Ch. A Ramp RAM
0x180–1FF	15–0	Ch. A Coefficient RAM	No Change This address is mirrored at 0x900–0x97F and contiguously extended at 0x980–0x9FF

NOTES
[1]Clear on $\overline{\text{RESET}}$.
[2]Allows dynamic updates.
[3]These bits update after a Start or a Beam Sync. See CR 0x10F

(0x000) Summation Mode Control

Controls features in the summation block of the AD6623.

Bits 5–6: Reserved.
Bit 4: Low: Wideband Input Enabled.
High: Wideband Input Disabled.
Bit 3: Low: Dual Output Disabled.
High: Dual Output Enabled.
Bit 2: Reserved.
Bit 1: Low: Output data will be in two's complement.
High: Output data will be in offset binary.
Bit 0: Low: Over-range will wrap.
High: Over-range will clip to full scale.

(0x001) Sync Mode Control

Bit 7: Ignores all but the first Sync0 pulse. Following this, all 8 bits are cleared to completely mask off subsequent pulses.
Bit 6: Beam on pin Sync0.
Bit 5: Hop on pin Sync0.
Bit 4: High enables the count down of the Start Hold-Off Counter. The counter is clocked with the AD6623 CLK signal. When it reaches a count of one the Sleep bit of the appropriate channel(s) is set low to activate the channel(s).
Bits 3–0: High enables synchronization of these channels. See the Synchronization section of the data sheet for detailed explanation.

(0x002) BIST Counter

Sets the length, in CLK cycles, of the built-in self test.

(0x003) BIST Result

A read-only register containing the result after a self test. Must be compared to a known good result for a given setup to determine pass/fail.

(0xn00) Start Update Hold-Off Counter
See the Synchronization section for detailed explanation. If no synchronization is required, this register should be set to 0.

Bits 17–16: The Start Sync Select bits are used to set which sync pin will initiate a start sequence.

Bits 15–0: The Start Update Hold-Off Counter is used to synchronize start–up of AD6623 channels and can be used to synchronize multiple chips. The Start Update Hold-Off Counter is clocked by the AD6623 CLK (master clock).

(0xn01) NCO Control
Bit 1:0 Set the NCO scaling per Table XXII.

Table XXII. NCO Control (0xn01)

Bit 1	Bit 0	NCO Output Level
0	0	–6 dB (no attenuation)
0	1	–12 dB attenuation
1	0	–18 dB attenuation
1	1	–24 dB attenuation

Bit 2: High clears the NCO phase accumulator to 0 on either a Soft Sync or Pin Sync (see Synchronization for details).

Bit 3: High enables NCO phase dither.

Bit 4: High enables NCO amplitude dither.

Bits 7–5: Reserved and should be written low.

(0xn02) NCO Frequency
This register is a 32-bit unsigned integer that sets the NCO Frequency. The NCO Frequency contains a shadow register for synchronization purposes. The NCO frequency. can be read back directly; however, the shadow register cannot.

$$NCO_{FREQUENCY} = 2^{32} \times \left(\frac{f_{CHANNEL}}{CLK} \right) \quad (27)$$

NCO output frequency should not exceed approximately 45% of the CLK.This makes allowance for the image filtering after D/A conversion.

(0xn03) NCO Frequency Update Hold-Off Counter
See the Synchronization section for detailed explanation. If no synchronization is required, this register should be set to 0.

Bits 17–16: The Hop Sync Select bits are used to set which sync pin will initiate a hop sequence.

Bits 15–0: The Hold-Off Counter is used to synchronize the change of NCO frequencies.

(0xn04) NCO Phase Offset
This register is a 16-bit unsigned integer that is added to the phase accumulator of the NCO. This allows phase synchronization of multiple channels of the AD6623(s). The NCO Phase Offset contains a shadow register for synchronization purposes. The shadow can be read back directly, the NCO Phase Offset cannot. See the Synchronization section for details.

(0xn05) NCO Phase Offset Update Hold-Off Counter
See the Synchronization section for a detailed explanation. If no synchronization is required, this register should be set to 0.

Bits 17–16: The Phase Sync Select bits are used to set which sync pin will initiate a phase sync sequence.

Bits 15–0: The Hold-Off Counter is used to synchronize the change of NCO phases.

(0xn06) CIC Scale
Bits 4–0: Sets the CIC scaling per the equation below.

$$CIC_Scale = ceil \times \left(\log_2 \left(L_{CIC5}^4 \times L_{CIC2} \right) \right) \quad (28)$$

See the CIC section for details.

(0xn07) CIC2 Decimation – 1 (M_{CIC2} – 1)
This register is used to set the decimation in the CIC2 filter. The value written to this register is the decimation minus one. The CIC2 decimation can range from 1 to 512 depending upon the interpolation of the CIC2. There is no timing error associated with this decimation. See the CIC2 section for further details.

(0xn08) CIC2 Interpolation – 1 (L_{CIC2} – 1)
This register is used to set the interpolation in the CIC2 filter. The value written to this register is the interpolation minus one. The CIC2 interpolation can range from 1 to 4096. L_{rCIC2} must be chosen equal to or larger than M_{rCIC2} and both must be chosen such that a suitable CIC2 Scalar can be chosen. For more details the CIC2 section should be consulted.

(0xn09) CIC5 Interpolation – 1
This register sets the interpolation rate for the CIC5 filter stage (unsigned integer). The programmed value is the CIC5 Interpolation – 1. Maximum interpolation is limited by the CIC scaling available (See the CIC section).

(0xn0A) Number of RCF Coefficients – 1
This register sets the number of RCF Coefficients and is limited to a maximum of 256. The programmed value is the number of RCF Coefficients – 1. There is an A register and a B register at this memory location. Value A is used when the RCF is operating in mode 0 and value B is used when in mode 1. The RCF mode bit of interest here is bit 6 of address 0xn0C.

(0xn0B) RCF Coefficient Offset
This register sets the offset for RCF Coefficients and is normally set to 0. It can be viewed as a pointer which selects the portion of the CMEM used when computing the RCF filter. This allows multiple filters to be stored in the Coefficient memory space, selecting the appropriate filter by setting the offset.

(0xn0C) Channel Mode Control 1
Bit 9: High, selecting compact FIR mode results in 24-bit serial word length (12 I followed by 12 Q). When low, selecting compact FIR mode results in 16-bit serial word length (8 I followed by 8 Q).

Bit 8: High enables RCF Pseudo-Random Input Select.

Bit 7: High selects a Pseudo-Random sequence length of 8,388,607. Low selects a Pseudo-Random Sequence length of 15.

Bits 6–4: Sets the channel input format as shown in Table XXIII.

Table XXIII. Channel Inputs

Bit 6	Bit 5	Bit 4	Input Mode
0	0	0	FIR
0	0	1	π/4-DQPSK
0	1	0	GSM
0	1	1	MSK
1	0	0	Compact FIR
1	0	1	8PSK
1	1	0	3π/8-8PSK
1	1	1	QPSK

Bit 6 Can be set through the serial port (see section on serial word formats).

Bits 3–0: Sets (N_{RCF}/L_{RCF}) –1

(0xn0D) Channel Mode Control 2

Bits 7–6: Sets the RCF Coarse Scale as shown in Table XXIV.

Table XXIV. RCF Coarse Scale

Bit 7	Bit 6	RCF Coarse Scale (dB)
0	0	0
0	1	–6
1	0	–12
1	1	–18

Bit 5: High enables the RCF phase equalizer.

Bits 4–0: Sets the serial clock divider (SDIV) that determines the serial clock frequency based on the following equation.

$$f_{SCLK} = \frac{CLK}{SDIV + 1} \quad (29)$$

(0xn0E) Fine Scale Factor

Bits 15–2: Sets the RCF Fine Scale Factor as an unsigned number representing the values (0,2). This register is shadowed for synchronization purposes. The shadow can be read back directly, the Fine Scale Factor can not.

Bits 1–0: Reserved.

(0xn0F) RCF Time Slot Sync

Bits 17–16: The Time Slot Sync Select bits are used to set which sync pin will initiate a time slot sync sequence.

Bits 15–0: The **Fine Scale** Hold-Off Counter is used to synchronize the change of RCF Fine Scale. See the Synchronization section for a detailed explanation. If no synchronization is required, this register should be set to 0.

(0xn10–0xn11) RCF Phase Equalizer Coefficients

See the RCF section for details.

(0xn12–0xn15) FIR-PSK Magnitudes

See the RCF section for details.

(0xn16) Serial Port Setup

Bits 7–6: Serial Data Frame Start Select

Table XXV. Serial Port Setup

Bit 7	Bit 6	Serial Data Frame Start
0	X	Internal Frame Request
1	0	External SDFI Pad
1	1	Previous Channel's Frame End

Bit 5: High means SDFO is a frame end, low means SDFO is a frame request.

Bit 4: High selects serial slave mode. SCLK is an input in serial slave mode.

Bit 3: Reserved

Bit 2: High enables Serial Time Slot Syncs (not available in FIR Mode).

Bit 1: High enables Power Ramp coefficient interpolation.

Bit 0: High enables the Power Ramp.

(0xn17) Power Ramp Length 0

This is the length of the ramp for Mode 0, minus one.

(0xn18) Power Ramp Length 1

This is the length of the ramp for Mode 1, minus one. Setting this to zero disables dual ramps.

(0xn19) Power Ramp Rest Time

This is the number of RCF output samples to rest for between a ramp down and a ramp up.

(0xn1A–0xn1F) Unused

(0xn20–0xn3F) Data Memory

This group of registers contain the RCF Filter Data. See the RCF section for additional details.

(0xn40–0xn7F) Power Ramp Coefficient Memory

This group of registers contain the Power Ramp Coefficients. See the Power Ramp section for additional details.

(0xn80–0xnFF) Coefficient Memory

This group of registers contain the RCF Filter Coefficients. See the RCF section for additional details.

PSEUDOCODE

Write Pseudocode

```
Void Write_Micro(ext_address, int data);

Main()
{

/* This code shows the programming of the
NCO frequency register using the Write_Micro
function defined above. The variable
address is the External Address A[2:0] and
data is the value to be placed in the
external interface register.

Internal Address = 0x102, channel 1
*/

/*Holding registers for NCO byte wide
access data*/
int d3, d2, d1, d0;
/*NCO frequency word (32 bits wide)*/
NCO_FREQ=0x1BEFEFFF;
/*write Chan */
Write_Micro(7, 0x01);
/*write Addr */
Write_Micro(6,0x02);
/*write Byte 3*/
d3=(NCO_FREQ & 0xFF02Y∞00)>>24;
Write_Micro(3,d3);
/*write Byte 2*/
d2=(NCO_FREQ & 0xFF0000)>>16;
Write_Micro(2,d2);
/*write Byte 1*/
d1=(NCO_FREQ & 0xFF00)>>8;
Write_Micro(1,d1);
/*write Byte 0, Byte 0 is written last and
causes an internal write to occur*/
d0=NCO_FREQ & 0xFF;
Write_Micro(0,d0);
}
```

Read Pseudocode

```
Void Read_Micro(ext_address);
Main()
{
/* This code shows the reading of the NCO
frequency register using the Read_Micro
function defined above. The variable
address is the External Address A[2:0]

Internal Address = 0x102, channel 1
*/

/*Holding registers for NCO byte wide
access data*/
int d3, d2, d1, d0;
/*NCO frequency word (32 bits wide)*/
/*write Chan */
Write_Micro(7, 0x01);
/*write Addr*/
Write_Micro(6,0x02);
/*read Byte 0, all data is moved from the
Internal Registers to the interface
registers on this access, thus Byte 0 must
be accessed first for the other Bytes to be
valid*/
d0=Read_Micro(0) & 0xFF;
/*read Byte 1*/
d1=Read_Micro(1) & 0xFF;
/*read Byte 2*/
d2=Read_Micro(2) & 0xFF;
/*read Byte 0 */
d3=Read_Micro(3) & 0xFF;
}
```

AD6623 EVALUATION PCB AND SOFTWARE

Analog Devices offers a fully populated printed circuit board and necessary software to evaluate the AD6623 performance. The software loads the AD6623 program registers, loads RCF (RAM Coefficient Filter) coefficients and programs the onboard FPGA and microcontroller. Designers should contact their local Analog Devices product distributor for ordering information.

The PCB and software have been designed for maximum flexibility to accommodate many different applications with minimum need of external devices. Please refer to the AD6623 Evaluation Board Manual for detailed information.

FIR filter design is an extremely important consideration in UMTS (Universal Mobile Telecommunications System), wideband CDMA and other sophisticated data transmission schemes. Transmitted signals must comply with channel specifications to assure non-interference with neighboring signal channels as well as minimizing inter-symbol interference. The AD6623 FIR filter software was designed to fulfill these goals. The latest AD6623 evaluation board and FIR filter software are both available from the Analog Devices web site at http://www.analog.com/techSupport/DesignTools/evaluationBoards/Ad6623.html

Additional features of the AD6623 PCB kit:

- Onboard 14-bit, 175 MSPS Interpolating TxDAC (AD9772A) for analog reconstruction of digital outputs. (Appropriate external anti-alias filter may be required.)
- On board voltage regulation requires only a single 9 V, 1 Amp external power supply to power all devices with 2.5 V, 3.3 V and 5 V.
- Digital outputs can be cascaded to a second AD6623 PCB for up to 8 output channels from a single DAC.
- Onboard "can type" crystal clock or BNC for external single-ended clock oscillator. CLK buffers are provided for every driven device
- AD6623 software utilizes the serial port of a Personal Computer for board programming—supports Windows™ 95, 98, NT and 2000.
- High quality, multi-layer PCB
- Comprehensive instruction manual complete with schematics, parts layout diagrams, illustrations.

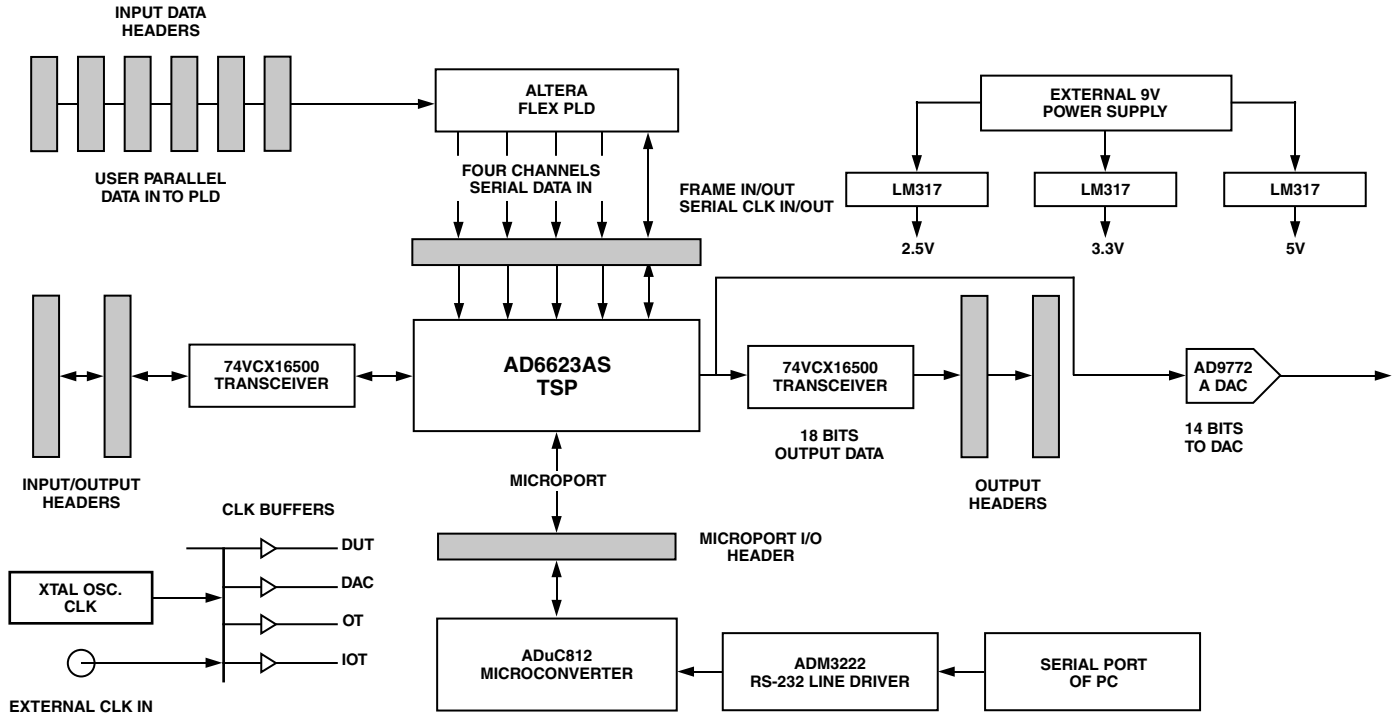


Figure 39. AD6623AS Evaluation Board

APPLICATIONS

The AD6623 provides considerable flexibility for the control of the synchronization, relative phasing, and scaling of the individual channel inputs. Implementation of a multichannel transmitter invariably begins with an analysis of the output spectrum that must be generated.

Using the AD6623 to Process UMTS Carriers

The AD6623 may be used to process two UMTS carriers, each with an output oversampling rate of 24× (i.e., 92.16 MSPS). The AD6623 configuration used to accomplish this consists of using two processing channels in parallel to process each UMTS carrier. Please refer to the Using the AD6623 to Process Two UMTS Carriers with 24× Oversampling, section.

Digital to Analog Converter (DAC) Selection

The selection of a high performance DAC depends on a number of factors. The dynamic range of the DAC must be considered from a noise and spectral purity perspective. The 14-bit AD9772A is the best choice for overall bandwidth, noise, and spectral purity.

In order to minimize the complexity of the analog interpolation filter which must follow the DAC, the sample rate of the master clock is generally set to at least three times the maximum analog frequency of interest.

In the case where a 15 MHz band of interest is to be up-converted to RF, the lowest frequency might be 5 MHz and the upper band edge at 20 MHz (offset from dc to afford the best image reject filter after the first digital IF). The minimum sample rate would be set to 65 MSPS.

Consideration must also be given to data rate of the incoming data stream, interpolation factors, and the clock rate of the DSP.

Multiple TSP Operation

Each of the four Transmit Signal Processors (TSPs) of the AD6623 can adequately reject the interpolation images of narrow bandwidth carriers such as AMPS, IS-136, GSM, EDGE, and PHS. Wider bandwidth carriers such as IS-95 and IMT2000 require a coordinated effort of multiple processing channels.

This section demonstrates how to coordinate multiple TSPs to create wider bandwidth channels without sacrificing image rejection. As an example, a UMTS carrier is modulated using four TSP channels (an entire AD6623). The same principles can be applied to different designs using more or fewer TSPs. This section does not explore techniques for using multiple TSPs to solve problems other than Serial Port or RCF throughput.

Designing filter coefficients and control settings for de-interleaved TSPs is no harder than designing a filter for a single TSP. For example, if four TSPs are to be used, simply divide the input data rate by four and generate the filter as normal. For any design, a better filter can always be realized by incrementing the number of TSPs to be used. When it is time to program the TSPs, only two small differences must be programmed. First, each channel is configured with exactly the same filter, scalers, modes and NCO frequency. Since each channel receives data at one-quarter the data rate and in a staggered fashion, the Start Hold-Off Counters must also be staggered (see "Programming Multiple TSPs" section). Second, the phase offset of each NCO must be set to match the demultiplexed ratio (in this example). Thus the phase offset should be set to 90 degrees (16384 which is one-quarter of a 16-bit register).

Determining the Number of TSPs to Use

There are three limitations of a single TSP that can be overcome by deinterleaving an input stream into multiple TSPs: Serial Port bandwidth, the time restriction to the RCF impulse response length (NRCF), and the DMEM restriction to NRCF.

If the input sample rate is faster than the Serial Port can accept data, the data can be de-interleaved into multiple Serial Ports. Recalling from the Serial Port description, the SCLK frequency (f_{SCLK}) is determined by the equation below. To minimize the number of processing channels, SCLKdivider should be set as low as possible to get the highest f_{SCLK}- that the serial data source can accept.

$$f_{SCLK} = \frac{f_{CLK}}{SCLKdivider + 1} \tag{30}$$

A minimum of 32 SCLK cycles are required to accept an input sample, so the minimum number of TSPs (NTSP) due to limited Serial Port bandwidth is a function of the input sample rate (f_{IN}), as shown in the equation below.

$$N_{TSP} \geq ceil\left(\frac{32 \times f_{IN}}{f_{SCLK}}\right) \tag{31}$$

For example for a UMTS system, we will assume f_{CLK} = 76.8 MHz, and the serial data source can drive data at 38.4 Mbps (SCLKdivider = 0). To achieve f_{IN} = 3.84 MHz, the minimum N_{TSP} is 3 with a Serial Clock f_{SCLK} = 52 MHz which is a limitation of the Serial Port (This is TSP channels, not TSP ICs).

Multiple TSPs are also required if the RCF does not have enough time or DMEM space to calculate the required RCF filter. Recalling the maximum N_{TAPS}– equation from the RCF description, are three restrictions to the RCF impulse response length, N_{RCF}.

Time Restriction CMEM Restriction

$$N_{RCF} \leq \min\left(\frac{1}{2}, 16 \times L_{RCF}\ 256\right) \tag{32}$$

DMEM Restriction

where:

$$L = L_{RCF} \times L_{CIC5} \times \frac{L_{CIC2}}{M_{CIC2}} = \frac{N_{TSP} \times f_{CLK}}{f_{IN}} \tag{33}$$

De-interleaving the input data into multiple TSPs extends the time restriction and may possibly extend the DMEM restriction, but will not extend the CMEM restriction. De-interleaving the input stream to multiple TSPs divides the input sample rate to each TSP by the number of TSPs used (N_{TSP}). To keep the output rate fixed, L must be increased by a factor of N_{CH}, which extends the time restriction. This increase in L may be achieved by increasing any one or more of L_{RCF}, L_{CIC5}, or L_{CIC2} within their normal limits. Achieving a larger L by increasing L_{RCF} instead of L_{CIC5} or L_{CIC2} will relieves the DMEM restriction as well.

In a UMTS example, N_{TSP} = 4, f_{CLK} = 76.8 MHz, and f_{IN} = 3.84 MHz, resulting in L = 80. Factoring L into L_{RCF} = 10, L_{CIC} = 8, and L_{CIC2} = 1 results in a maximum N_{RCF} = 40 due to the time restriction. Figure 42 shows an example RCF impulse response which has a frequency response as shown in Figure 43

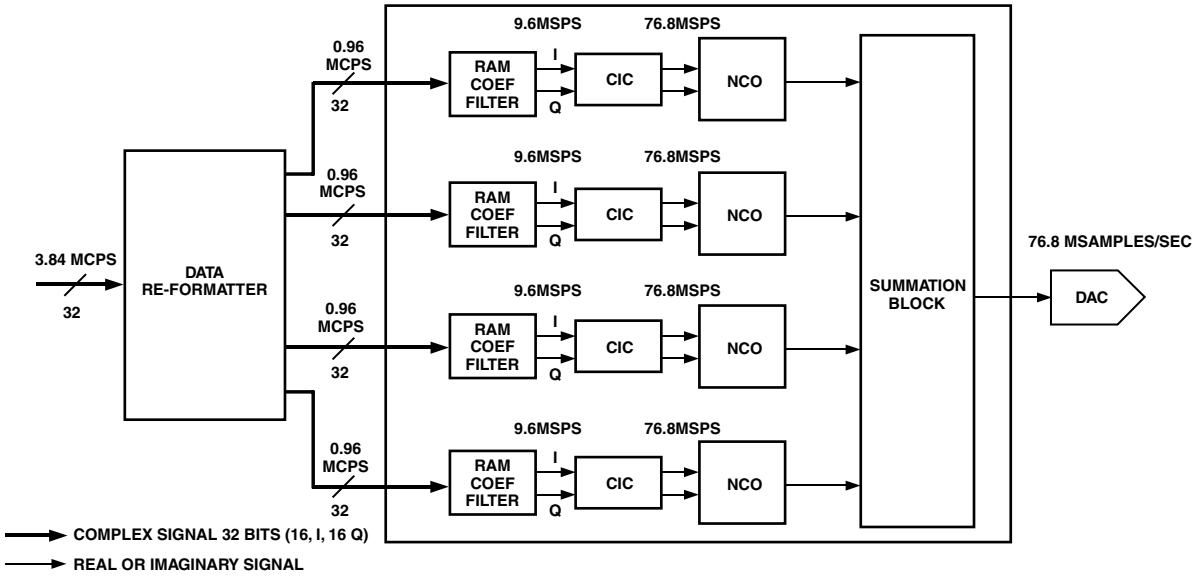


Figure 40. Driving Multiple TSP Serial Ports

from 0 Hz to 7.68 MHz ($f_{IN} \times L_{RCF}/N_{TSP}$). The composite RCF and CIC frequency response is shown in Figure 44, on the same frequency scale. This figure demonstrates a good approximation to a root-raised-cosine with a roll-off factor of 0.22, a passband ripple of 0.1 dB, and a stopband ripple better than –70 dB until the lobe of the first image which peaks at –60 dB about 7.68 MHz from the carrier center. This lobe could be reduced by shifting more of the interpolation towards the RCF, but that would sacrifice near in performance. As shown, the first image can be easily rejected by an analog filter further up the signal path.

Scaling must be considered as normal with an interpolation factor of L, to guarantee no overflow in the RCF, CIC, or NCOs. The output level at the summation port should be calculated using an interpolation factor of L/N_{TSP}.

Programming Multiple TSPs

Configuring the TSPs for de-interleaved operation is straight forward. All the Channel Registers and the CMEM of each TSP are programmed identically, except the Start Hold-Off Counters and NCO Phase Offset.

In order to separate the input timing to each TSP, the Hold-Off Counters must be used to start each TSP successively in response to a common Start SYNC. The Start SYNC may originate from the SYNC pin or the Microport. Each subsequent TSP must have a Hold-Off Counter value L/N_{TSP} larger than its predecessor's. If the TSPs are located on cascaded AD6623s, the Hold-Off Counters of the upstream device should be incremented by an additional one.

In the UMTS example, L = 80 and N_{TSP} = 4, so to respond as quickly as possible to a Start SYNC, the Hold-Off Counter values should be 1, 21, 41, and 61.

Driving Multiple TSP Serial Ports

When configured properly, the AD6623 will drive each SDFO out of phase. Each new piece of data should be driven only into the TSP that pulses its SDFO pin at that time.

In the UMTS example in Figure 41, L = 80 and N_{TSP} = 4, so each serial port need only accept every fourth input sample. Each serial port is shifting at peak capacity, so sample 1, 2, and 3 begin shifting into Serial Ports B, C, and D before sample 0 is completed into Serial Port A.

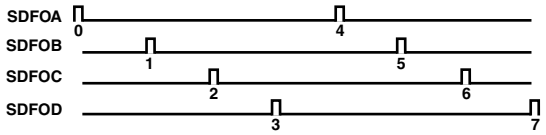


Figure 41. UMTS Example

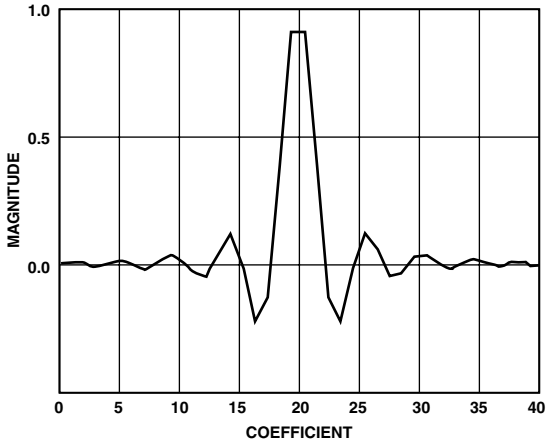


Figure 42. Typical Impulse Response for WBCDMA (Wide-Band Code Division Multiple Access)

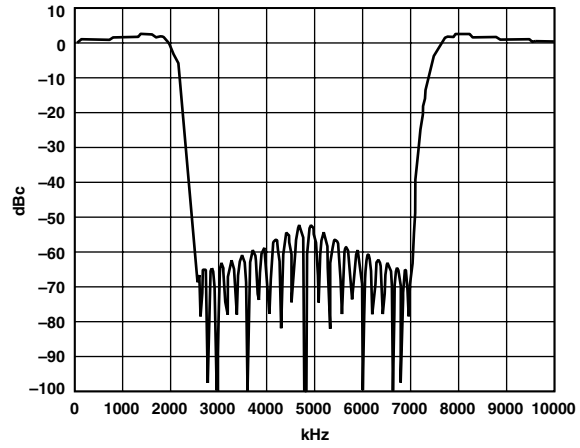


Figure 43. RAM Coefficient Filter, Frequency Response for WBCDMA

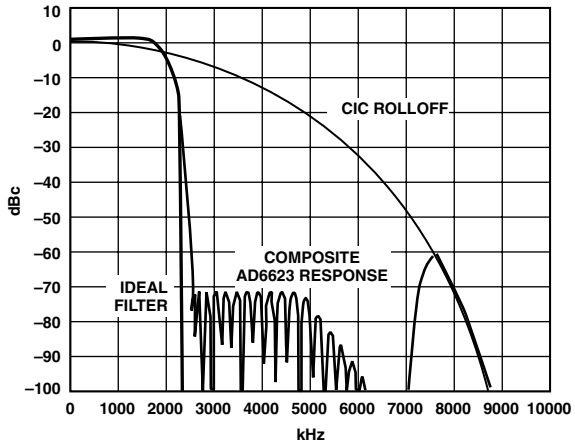


Figure 44. RCF and CIC, Frequency Response for WBCDMA

USING THE AD6623 TO PROCESS TWO UMTS CARRIERS WITH 24× OUTPUT RATE

Overview

The AD6623 may be used to process two UMTS carriers, each with an output rate of 24× (i.e., 92.16 MSPS). The AD6623 configuration used to accomplish this consists of using two processing channels in parallel to process each UMTS carrier. The ideology behind the parallel processing approach is that each channel operates on half of the input samples, processing every other sample. The reason is that the serial input data rate is limited to 3.25 MSPS for 16-bit I and 16-bit Q data (104 MSPS/32). The first channel of each pair begins processing the first input sample immediately. The second channel begins processing after a specific delay so that the two channels essentially will be operating 180 degrees out of phase with each other. Since each channel processes only half the input samples and thus receives input data at half the original rate, each channel has twice the original amount of time available for processing. This in turn makes available twice the original number of taps, resulting in much improved digital filtering capability. To maximize the number of available FIR filter taps, the highest possible input rate should be used. Therefore, this application note assumes an input sample rate of 3.84 MSPS and an output data rate of 24× (i.e., 92.16 MSPS), which in conjunction with the 1× input rate (assumes two channels used per carrier at 1.92 MSPS) results in a total decimation value of 24. Since two AD6623 channels will be used for each carrier, each channel will operate with a total interpolation of forty-eight, resulting in a total of 24 taps for the FIR filter. All channels must be configured with the same FIR filter coefficients, decimation and interpolation values, and scaling values.

Configuring the AD6623

The Serial Input Data ports need run at 1.92 MSPS by using f_{SCLK} = 92.16 MSPS, with SCLK divider = 0 (0x0D, Bits 4- 0 = 0). In order to properly process a UMTS channel across two channels the channels need to be synchronized. The channel starts will be delayed by precise input clock periods, and the NCO's will be independently phased to account for starting channels out of phase. The final output summation stage adds data from separate channels together.

It should be noted that all serial output ports must be configured for Serial Bus Master Mode, since SCLKs cannot be run at 92.16 MHz in slave mode.

When initiating carrier processing, care should be taken to ensure that both the primary and secondary processing channels are started with precise relative timing (preferably by a pulse on one of the SYNC pins). The device is configured with the following filtering parameters:

L_{RCF} = 6

N_{TAPS} = 24

L_{CIC5} = 8

L_{CIC2} = 1

M_{CIC2} = 1

SCLK = 92.16

AD6623 Register Configuration

To process two UMTS carriers with 24× output rate, the AD6623 must be properly configured. The following sections describe the required register settings for this configuration. Interpolation, decimation, and scaling values specified for the following registers were used to obtain the reference filter response shown in the Performance section of this data sheet. Other registers may be set as needed for any individual application.

For registers with bit fields, the following symbols are used:

0, 1: bit must be set to zero or one as indicated.

'u': bit is dependent on the user's application, but must be the same for both channels of a processing pair.

'x': bit can be set at user's discretion, regardless of the channel used.

Coefficient Memory (0x900–0x9FF, Bits 15:0)

Each pair of processing channels must be assigned the same FIR filter coefficients. Twenty-four taps must be used, typically loaded into addresses 0x900-0x9FF.

The FIR filter coefficients for the reference filter are:

–181
–101
24803
2420
–816
–4461
14446
1729
–1084
–5366
1588
–209
–209
1588
–5366
–1084
1729
14446
–4461
–816
2420
24803
–101
–181

Start Sync Control Register (0xn00, Bits 17:16)
The settings in this register must be the same for each pair of processing channels.

Start Holdoff Counter (0xn00, Bits 15:0)
The secondary channel of each processing pair needs to be configured such that it begins processing 180 degrees out of phase with the primary channel. The Start Holdoff Counter (SHC) of the secondary channel is set to the value of the primary channel plus LTOT/2, where LTOT is the overall channel interpolation.

$$SCC_{2ndChannel} = SCC_{1stChannel} + \frac{L_{TOT}}{2} \quad (34)$$

For example, in the case of LTOT = 48, the primary channel of each processing is set to two, while the secondary channel's Start Holdoff Counter is set to twenty-six.

NCO Frequency Registers (0xn02, Bits 31:0)
Each pair of processing channels must be assigned the same NCO Frequency Register values.

NCO Frequency Holdoff Counter (0xn03, Bits 15:0)
Each pair of processing channels must be assigned the same NCO Holdoff Counter value.

NCO Phase Offset Register (0xn04, Bits 15:0)
The NCO of the secondary channel must have its initial phase set such that, when it begins processing, its phase is equal to that of the primary channel's phase. The equation is given by:

$$NCOPhaseOffset = round\left[frac\left(\frac{L_{TOT}}{2} \cdot \frac{f_{NCO}}{f_{SAMP}} \right) \cdot 2^{16} \right] \quad (35)$$

where
round() returns the nearest integer of its argument,
frac() returns the fractional part of its argument,
f_{NCO} is the desired NCO frequency, and
f_{SAMP} is the desire output sample rate.

NCO Phase Offset Update Holdoff (0xn05, Bits 15:0)
Each pair of processing channels must be assigned the same NCO Phase Offset Update Holdoff value.

CIC Scale (0xn06, Bits 4:0)
Each pair of processing channels must use a value of seventeen for this register (S_{CIC} = 12).

rCIC2 Decimation-1 (0xn07, Bits 8:0)
Each pair of processing channels must use a value of zero for this register (rCIC2 decimation = 0).

rCIC2 Interpolation-1 (0xn08, Bits 7:0)
Each pair of processing channels must use a value of zero for this register (rCIC2 interpolation = 0).

CIC5 Interpolation-1 (0xn09, Bits 7:0)
Each pair of processing channels must use a value of seven for this register (CIC5 interpolation = 7).

RCF Number of Taps-1 (0xnA0, Bits 7:0)
Each pair of processing channels must use a value of twenty-three for this register (NRCF-1 = 23).

RCF Coefficient Offset (0xn0B, Bits 7:0)
Each processing channel must specify the offset of the address where its coefficients begin (typically zero).

RCF Mode (0xn0C, Bits 9:4)
Each pair of processing channels must set all these bits to zero.

RCF Mode (0xn0C, Bits 3:0)
Each pair of processing channels must be assigned the same number of taps per phase which in this case is four.

Serial Data Frame Input Select (0xn16, Bits 7:6)
The secondary channel of each processing pair needs to be configured such that it begins processing data after the primary channel's Frame end. This is done by setting the Serial Data Frame Input Select bits high (Bits 7:6 = 11).

Serial Data Frame Output Select (0xn16, Bits 5)
The primary channel of each processing pair needs to be configured such that it is configured for Serial Data Frame Request (Bit 5 = 0).

Serial Clock Slave (0xn16, Bits 4)
Each pair of processing channels must be configured in Master mode (Bit 4 = 0).

Performance
The filter performance of the AD6623's dual-channel processing approach is shown in Figure 45. This filter uses 24 taps, with RCF interpolation of 6, CIC5 interpolation of 8, and rCIC2 interpolation and decimation of 1 and 1, respectively. The near rejection at 5 MHz is 65 dBc, and rejection at 10 MHz is 80 dBc, with a passband ripple of 0.25 dB. The register settings implementing this filter are outlined in the AD6623 Register Configuration section of this technical note.

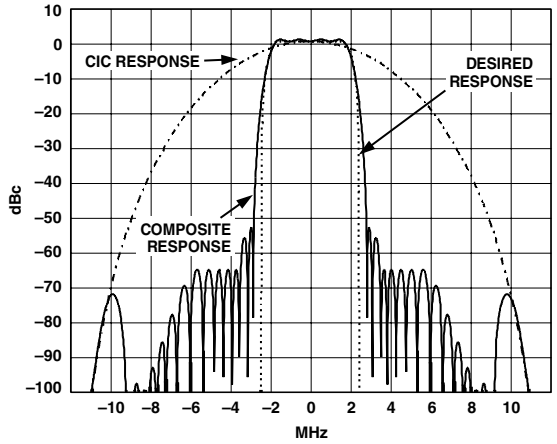


Figure 45. Composite Response to First CIC5 Null

THERMAL MANAGEMENT

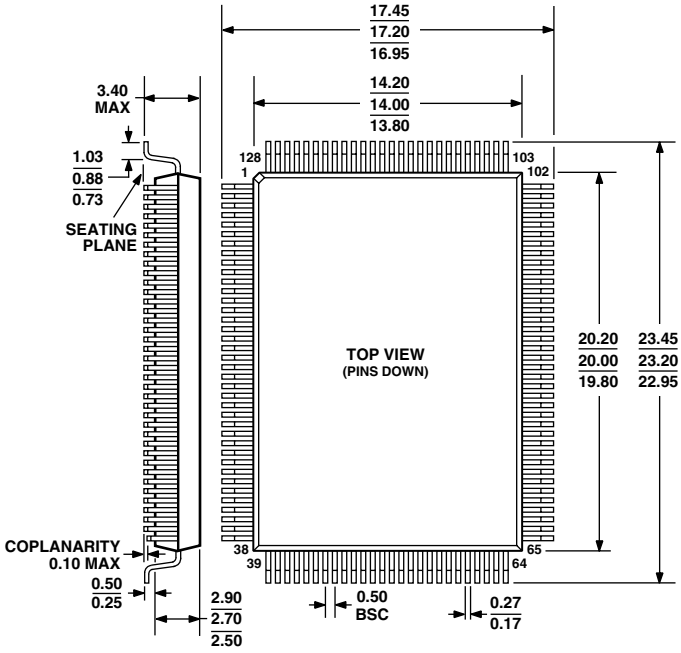
The power dissipation of the AD6623 is primarily determined by three factors: the clock rate, the number of channels active, and the distribution of interpolation rates. The faster the clock rate the more power dissipated by the CMOS structures of the AD6623 and the more channels active the higher the overall power of the chip. Low interpolation rates in the CIC stages (CIC5, CIC2) results in higher power dissipation. All these factors should be analyzed as each application has different thermal requirements.

The AD6623 128-Lead MQFP is specially designed to provide excellent thermal performance. To achieve the best performance the power and ground leads should be connected directly to planes on the PC board. This provides the best thermal transfer from the AD6623 to the PC board.

OUTLINE DIMENSIONS

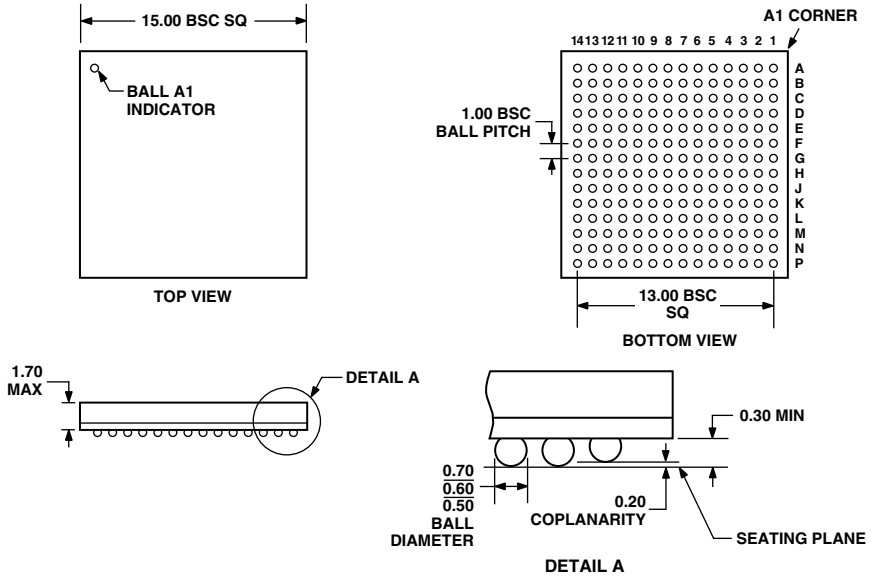
128-Lead Plastic Quad Flatpack [MQFP]
(S-128A)

Dimensions shown in millimeters



196-Lead Chip Scale Ball Grid Array [CSPBGA]
(BC-196)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-192AAE-1

NOTES

1. ACTUAL POSITION OF THE BALL GRID IS WITHIN 0.20 OF ITS IDEAL POSITION RELATIVE TO THE PACKAGE EDGES.
2. ACTUAL POSITION OF EACH BALL IS WITHIN 0.10 OF ITS IDEAL POSITION RELATIVE TO THE BALL GRID.
3. CENTER DIMENSIONS ARE NOMINAL.

AD6623
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C02768–0–9/02(A)

PRINTED IN U.S.A.