High Precision, Wideband RMS-to-DC Converter

Data Sheet **AD637**

FEATURES

High accuracy
- **0.02% maximum nonlinearity, 0 V to 2 V rms input**
- **0.1% additional error to crest factor of 3**

Wide bandwidth
- **8 MHz at 2 V rms input**
- **600 kHz at 100 mV rms**

Computes
- **True rms**
- **Square**
- **Mean square**
- **Absolute value**

dB output (60 dB range)

Chip select/power-down feature allows
- **Analog three-state operation**
- **Quiescent current reduction from 2.2 mA to 350 µA**

FUNCTIONAL BLOCK DIAGRAM

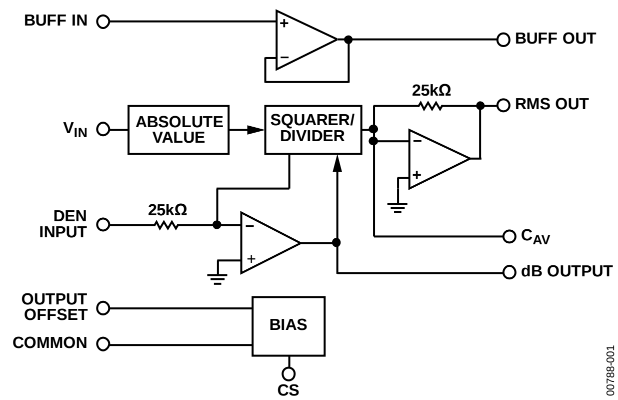

Figure 1.

GENERAL DESCRIPTION

The AD637 is a complete, high accuracy, rms-to-dc converter that computes the true rms value of any complex waveform. It offers performance that is unprecedented in integrated circuit rms-to-dc converters and comparable to discrete and modular techniques in accuracy, bandwidth, and dynamic range. The AD637 computes the true root mean square, mean square, or absolute value of any complex ac (or ac plus dc) input waveform and gives an equivalent dc output voltage. The true rms value of a waveform is more useful than an average rectified signal because it relates directly to the power of the signal. The rms value of a statistical signal relates to the standard deviation of the signal.

Superior crest factor compensation permits measurements of signals with crest factors of up to 10 with less than 1% additional error. The wide bandwidth of the AD637 permits the measurement of signals up to 600 kHz with inputs of 200 mV rms and up to 8 MHz when the input levels are above 1 V rms.

Direct dB value of the rms output with a range of 60 dB is available on a separate pin. An externally programmed reference current allows the user to select the 0 dB reference voltage to correspond to any level between 0.1 V and 2.0 V rms.

A chip select connection on the AD637 permits the user to decrease the supply current from 2.2 mA to 350 µA during periods when the rms function is not in use. This feature facilitates the addition of precision rms measurement to remote or handheld applications where minimum power consumption is critical. In addition, when the AD637 is powered down, the output goes to a high impedance state. This allows several AD637s to be tied together to form a wideband true rms multiplexer.

The input circuitry of the AD637 is protected from overload voltages in excess of the supply levels. The inputs are not damaged by input signals if the supply voltages are lost.

The AD637 is laser wafer trimmed to achieve rated performance without external trimming. The only external component required is a capacitor that sets the averaging period. The value of this capacitor also determines low frequency accuracy, ripple level, and settling time.

The on-chip buffer amplifier is used either as an input buffer or in an active filter configuration. The filter can be used to reduce the amount of ac ripple, thereby increasing accuracy.

The AD637 is available in accuracy Grade J and Grade K for commercial temperature range (0°C to 70°C) applications, accuracy Grade A and Grade B for industrial range (−40°C to +85°C) applications, and accuracy Grade S rated over the −55°C to +125°C temperature range. All versions are available in hermetically sealed, 14-lead SBDIP, 14-lead CERDIP, and 16-lead SOIC_W packages.

Rev. L Document Feedback

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REVISION HISTORY

SPECIFICATIONS

At 25°C, test frequency = 1 kHz, V_{IN} units are V_{RMS}, VS = ±15 V dc, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	AD637J/AD637A Min	Typ	Max	Unit
TRANSFER FUNCTION		$V_{OUT} = \sqrt{avg \times (V_{IN})^2}$			
CONVERSION ACCURACY					
Total Error, Internal Trim	See Figure 5			±1 ± 0.5	mV rms ±% of reading
T_{MIN} to T_{MAX}				±3.0 ± 0.6	mV ± % of reading
vs. Supply	V_{IN} = 300 mV		30	150	μV/V
	V_{IN} = −300 mV		100	300	μV/V
DC Reversal	−2 V < V_{IN} < +2 V			0.25	% of reading
Nonlinearity	2 V full scale			0.04	% of FSR
	7 V full scale			0.05	% of FSR
Total Error	External trim		±0.5 ± 0.1		mV ± % of reading
ERROR VS. CREST FACTOR (CF)	Additional, at 1 V rms				CF, %
	For CF = 1 to 2		Specified accuracy		
	For CF = 3		±0.1		% of reading
	For CF = 10		±1.0		% of reading
AVERAGING TIME CONSTANT			25		ms/μF C_{AV}
INPUT CHARACTERISTICS					
Signal Range	VS = ±15 V				
	Continuous		0 to 7		V rms
	Transient			±15	V p-p
	VS = ±5 V				
	Continuous		0 to 4		V rms
	Transient			±6	V p-p
Input Resistance		6.4	8	9.6	kΩ
Input Offset Voltage				±0.5	mV
FREQUENCY RESPONSE					
Bandwidth for 1% (0.09 dB) Additional Error	V_{IN} = 20 mV		11		kHz
	V_{IN} = 200 mV		66		kHz
	V_{IN} = 2 V		200		kHz
±3 dB					
	V_{IN} = 20 mV		150		kHz
	V_{IN} = 200 mV		1		MHz
	V_{IN} = 2 V		8		MHz
OUTPUT CHARACTERISTICS					
Offset Voltage				±1	mV
	vs. temperature		±0.05	±0.089	mV/°C
Voltage Swing, 2 kΩ load		0 to 12.0	13.5		V
	VS = ±3 V	0 to 2	2.2		V
Output Current		6			mA
Short-Circuit Current			20		mA
Resistance	CS high		0.5		Ω
Resistance	CS low		100		kΩ

Parameter	Test Conditions/Comments	AD637J/AD637A Min	Typ	Max	Unit
dB OUTPUT					
Error	V_{IN} = 7 mV to 7 V rms, 0 dBV		±0.5		dBV
Scale Factor			−3		mV/dB
Scale Factor Tempco			+0.33		% of reading/°C
			−0.033		dB/°C
I_{REF} for 0 dB = 1 V rms		5	20	80	µA
I_{REF} Range		1		100	µA
BUFFER AMPLIFIER					
Input Output Voltage Range			$-V_S$ to $(+V_S - 2.5)$		V
Input Offset Voltage			±0.8	±2	mV
Input Current			±2	±10	nA
Input Resistance			10^8		Ω
Output Current		−0.13		+5	mA
Short-Circuit Current			20		mA
Small Signal Bandwidth			1		MHz
Slew Rate	2 kΩ load, to $-V_S$		5		V/µs
DENOMINATOR INPUT					
Input Range			0 to 10		V
Input Resistance		20	25	30	kΩ
Offset Voltage			±0.2	±0.5	mV
CHIP SELECT (CS)					
RMS On Level			Open or $2.4 < V_C < +V_S$		V
RMS Off Level		$V_C < 0.2$		$V_C < 0.2$	V
I_{OUT} of Chip Select					
	CS low			10	µA
	CS high			0	µA
On Time Constant			10 + ((25 kΩ) × C_{AV})		µs
Off Time Constant			10 + ((25 kΩ) × C_{AV})		µs
POWER SUPPLY					
Operating Voltage Range		±3.0		±18	V
Quiescent Current			2.2	3	mA
Standby Current			350	450	µA

Table 2.

Parameter	Test Conditions/Comments	AD637K/AD637B Min	Typ	Max	Unit
TRANSFER FUNCTION		$V_{OUT} = \sqrt{avg \times (V_{IN})^2}$			
CONVERSION ACCURACY					
Total Error, Internal Trim	See Figure 5			±0.5 ± 0.2	mV rms ±% of reading
T_{MIN} to T_{MAX}				±2.0 ± 0.3	mV ± % of reading
vs. Supply	V_{IN} = 300 mV		30	150	µV/V
	V_{IN} = −300 mV		100	300	µV/V
DC Reversal	−2 V < V_{IN} < +2 V			0.1	% of reading
Nonlinearity	2 V full scale			0.02	% of FSR
	7 V full scale			0.05	% of FSR
Total Error	External trim		±0.25 ± 0.05		mV ± % of reading
ERROR VS. CREST FACTOR (CF)	Additional, at 1 V rms				CF, %
	For CF = 1 to 2		Specified accuracy		
	For CF = 3		±0.1		% of reading
	For CF = 10		±1.0		% of reading
AVERAGING TIME CONSTANT			25		ms/µF C_{AV}
INPUT CHARACTERISTICS					
Signal Range	VS = ±15 V				
	Continuous		0 to 7		V rms
	Transient			±15	V p-p
	VS = ±5 V				
	Continuous		0 to 4		V rms
	Transient			±6	V p-p
Input Resistance		6.4	8	9.6	kΩ
Input Offset Voltage				±0.2	mV
FREQUENCY RESPONSE					
Bandwidth for 1% (0.09 dB) Additional Error	V_{IN} = 20 mV		11		kHz
	V_{IN} = 200 mV		66		kHz
	V_{IN} = 2 V		200		kHz
±3 dB					
	V_{IN} = 20 mV		150		kHz
	V_{IN} = 200 mV		1		MHz
	V_{IN} = 2 V		8		MHz
OUTPUT CHARACTERISTICS					
Offset Voltage				±0.5	mV
	vs. temperature		±0.04	±0.056	mV/°C
Voltage Swing, 2 kΩ load		0 to 12.0	13.5		V
	VS = ±3 V	0 to 2	2.2		V
Output Current		6			mA
Short-Circuit Current			20		mA
Resistance	CS high		0.5		Ω
Resistance	CS low		100		kΩ
dB OUTPUT					
Error	V_{IN} = 7 mV to 7 V rms, 0 dBV		±0.3		dBV
Scale Factor			−3		mV/dB
Scale Factor Tempco			+0.33		% of reading/°C
			−0.033		dB/°C
I_{REF} for 0 dB = 1 V rms		5	20	80	µA
I_{REF} Range		1		100	µA

Parameter	Test Conditions/Comments	AD637K/AD637B Min	Typ	Max	Unit
BUFFER AMPLIFIER					
Input Output Voltage Range			$-V_S$ to $(+V_S - 2.5)$		V
Input Offset Voltage			±0.5	±1	mV
Input Current			±2	±5	nA
Input Resistance			10^8		Ω
Output Current		−0.13		+5	mA
Short-Circuit Current			20		mA
Small Signal Bandwidth			1		MHz
Slew Rate	2 kΩ load, to $-V_S$		5		V/µs
DENOMINATOR INPUT					
Input Range			0 to 10		V
Input Resistance		20	25	30	kΩ
Offset Voltage			±0.2	±0.5	mV
CHIP SELECT (CS)					
RMS On Level			Open or $2.4 < V_C < +V_S$		V
RMS Off Level			$V_C < 0.2$		V
I_{OUT} of Chip Select					
	CS low			10	µA
	CS high			0	µA
On Time Constant			$10 + ((25\ k\Omega) \times C_{AV})$		µs
Off Time Constant			$10 + ((25\ k\Omega) \times C_{AV})$		µs
POWER SUPPLY					
Operating Voltage Range		±3.0		±18	V
Quiescent Current			2.2	3	mA
Standby Current			350	450	µA

Table 3.

Parameter	Test Conditions/Comments	AD637S Min	Typ	Max	Unit
TRANSFER FUNCTION			$V_{OUT} = \sqrt{avg \times (V_{IN})^2}$		
CONVERSION ACCURACY					
Total Error, Internal Trim	See Figure 5			±1 ± 0.5	mV rms ±% of reading
T_{MIN} to T_{MAX}				±6 ± 0.7	mV ± % of reading
vs. Supply	V_{IN} = 300 mV		30	150	μV/V
	V_{IN} = −300 mV		100	300	μV/V
DC Reversal	−2 V < V_{IN} < +2 V			0.25	% of reading
Nonlinearity	2 V full scale			0.04	% of FSR
	7 V full scale			0.05	% of FSR
Total Error	External trim		±0.5 ± 0.1		mV ± % of reading
ERROR VS. CREST FACTOR (CF)	Additional, at 1 V rms				CF, %
	For CF = 1 to 2		Specified accuracy		
	For CF = 3		±0.1		% of reading
	For CF = 10		±1.0		% of reading
AVERAGING TIME CONSTANT			25		ms/μF C_{AV}
INPUT CHARACTERISTICS					
Signal Range	VS = ±15 V				
	Continuous		0 to 7		V rms
	Transient			±15	V p-p
	VS = ±5 V				
	Continuous		0 to 4		V rms
	Transient			±6	V p-p
Input Resistance		6.4	8	9.6	kΩ
Input Offset Voltage				±0.5	mV
FREQUENCY RESPONSE					
Bandwidth for 1% (0.09 dB) Additional Error	V_{IN} = 20 mV		11		kHz
	V_{IN} = 200 mV		66		kHz
	V_{IN} = 2 V		200		kHz
±3 dB					
	V_{IN} = 20 mV		150		kHz
	V_{IN} = 200 mV		1		MHz
	V_{IN} = 2 V		8		MHz
OUTPUT CHARACTERISTICS					
Offset Voltage				±1	mV
	vs. temperature		±0.04	±0.07	mV/°C
Voltage Swing, 2 kΩ load		0 to 12.0	13.5		V
	VS = ±3 V	0 to 2	2.2		V
Output Current		6			mA
Short-Circuit Current			20		mA
Resistance	CS high		0.5		Ω
Resistance	CS low		100		kΩ
dB OUTPUT					
Error	V_{IN} = 7 mV to 7 V rms, 0 dBV		±0.5		dBV
Scale Factor			−3		mV/dB
Scale Factor Tempco			+0.33		% of reading/°C
			−0.033		dB/°C
I_{REF} for 0 dB = 1 V rms		5	20	80	μA
I_{REF} Range		1		100	μA

Parameter	Test Conditions/Comments	AD637S Min	Typ	Max	Unit
BUFFER AMPLIFIER					
Input Output Voltage Range			$-V_S$ to $(+V_S - 2.5)$		V
Input Offset Voltage			±0.8	±2	mV
Input Current			±2	±10	nA
Input Resistance			10^8		Ω
Output Current		−0.13		+5	mA
Short-Circuit Current			20		mA
Small Signal Bandwidth			1		MHz
Slew Rate	2 kΩ load, to $-V_S$		5		V/µs
DENOMINATOR INPUT					
Input Range			0 to 10		V
Input Resistance		20	25	30	kΩ
Offset Voltage			±0.2	±0.5	mV
CHIP SELECT (CS)					
RMS On Level			Open or $2.4 < V_C < +V_S$		V
RMS Off Level					V
I_{OUT} of Chip Select					
	CS low			10	µA
	CS high			0	µA
On Time Constant			$10 + ((25\ k\Omega) \times C_{AV})$		µs
Off Time Constant			$10 + ((25\ k\Omega) \times C_{AV})$		µs
POWER SUPPLY					
Operating Voltage Range		±3.0		±18	V
Quiescent Current			2.2	3	mA
Standby Current			350	450	µA

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
ESD Rating	500 V
Supply Voltage	±18 V dc
Internal Quiescent Power Dissipation	108 mW
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10 sec)	300°C
Rated Operating Temperature Range	
AD637J, AD637K	0°C to 70°C
AD637A, AD637B	−40°C to +85°C
AD637S, 5962-8963701CA	−55°C to +125°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

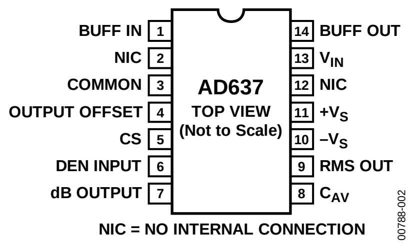


Figure 2. 14-Lead SBDIP/CERDIP Pin Configuration

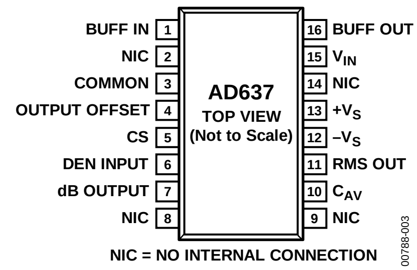


Figure 3. 16-Lead SOIC_W Pin Configuration

Table 5. 14-Lead SBDIP/CERDIP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	BUFF IN	Buffer Input
2, 12	NIC	No Internal Connection
3	COMMON	Analog Common
4	OUTPUT OFFSET	Output Offset
5	CS	Chip Select
6	DEN INPUT	Denominator Input
7	dB OUTPUT	dB Output
8	C_{AV}	Averaging Capacitor Connection
9	RMS OUT	RMS Output
10	$-V_S$	Negative Supply Rail
11	$+V_S$	Positive Supply Rail
13	V_{IN}	Signal Input
14	BUFF OUT	Buffer Output

Table 6. 16-Lead SOIC_W Pin Function Descriptions

Pin No.	Mnemonic	Description
1	BUFF IN	Buffer Input
2, 8, 9, 14	NIC	No Internal Connection
3	COMMON	Analog Common
4	OUTPUT OFFSET	Output Offset
5	CS	Chip Select
6	DEN INPUT	Denominator Input
7	dB OUTPUT	dB Output
10	C_{AV}	Averaging Capacitor Connection
11	RMS OUT	RMS Output
12	$-V_S$	Negative Supply Rail
13	$+V_S$	Positive Supply Rail
15	V_{IN}	Signal Input
16	BUFF OUT	Buffer Output

THEORY OF OPERATION

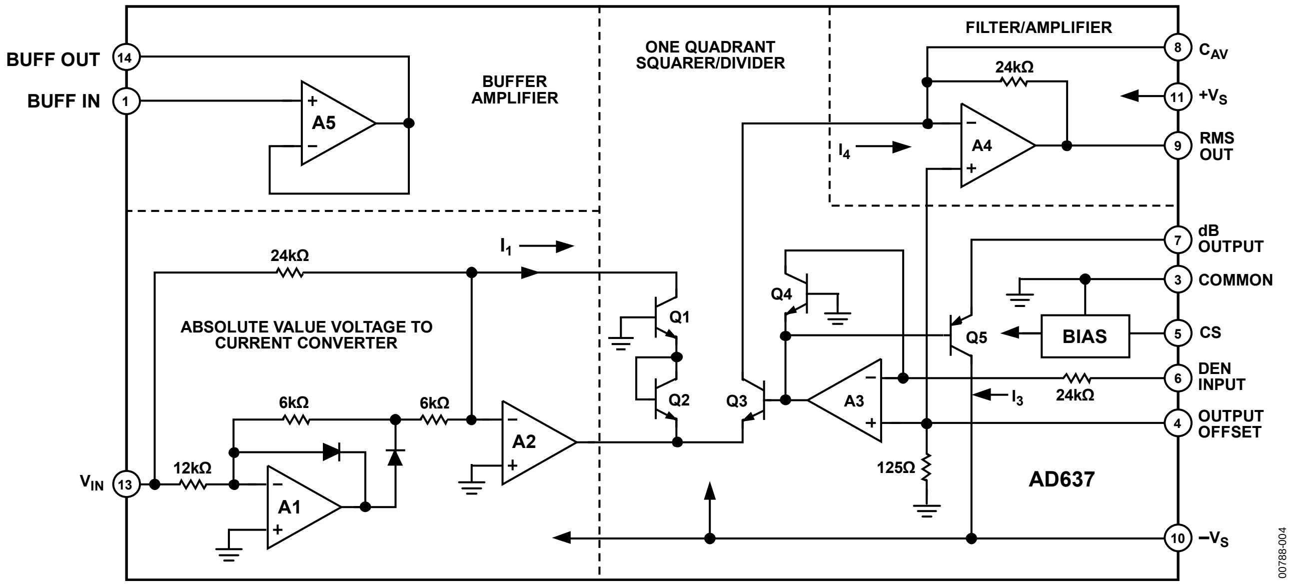


Figure 4. Simplified Schematic

The AD637 embodies an implicit solution of the rms equation that overcomes the inherent limitations of straightforward rms computation. The actual computation performed by the AD637 follows the equation:

$$V\ rms = Avg\left[\frac{V_{IN}^{\ 2}}{V\ rms}\right]$$

Figure 4 is a simplified schematic of the AD637, subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, filter circuit, and buffer amplifier. The input voltage (V_{IN}), which can be ac or dc, is converted to a unipolar current (I_1) by the A1 and A2 absolute value circuit. I_1 drives one input of the squarer/divider, which has the transfer function:

$$I_4 = \frac{I_1^{\ 2}}{I_3}$$

The output current of the squarer/divider, I_4, drives A4, forming a low-pass filter with the external averaging capacitor. If the RC time constant of the filter is much greater than the longest period of the input signal, then the A4 output is proportional to the average of I_4. The output of this filter amplifier is used by A3 to provide the denominator current I_3, which equals Avg I_4 and is returned to the squarer/divider to complete the implicit rms computation

$$I_4 = Avg\left[\frac{I_1^{\ 2}}{I_4}\right] = I_1\ rms$$

and

$$V_{OUT} = V_{IN}\ rms$$

To compute the absolute value of the input signal, the averaging capacitor is omitted. However, a small capacitance value at the averaging capacitor pin is recommended to maintain stability; 5 pF is sufficient for this purpose. The circuit operates identically to that of the rms configuration, except that I_3 is now equal to I_4, giving

$$I_4 = \frac{I_1^{\ 2}}{I_4}$$

$$I_4 = |I_1|$$

The denominator current can also be supplied externally by providing a reference voltage (V_{REF}) to Pin 6. The circuit operates identically to the rms case, except that I_3 is now proportional to V_{REF}. Therefore,

$$I_4 = Avg\ \frac{I_1^{\ 2}}{I_3}$$

and

$$V_{OUT} = \frac{V_{IN}^{\ 2}}{V_{DEN}}$$

This is the mean square of the input signal.

APPLICATIONS INFORMATION

STANDARD CONNECTION

The AD637 is simple to connect for a majority of rms measurements. In the standard rms connection shown in Figure 5, only a single external capacitor is required to set the averaging time constant. In this configuration, the AD637 computes the true rms of any input signal. An averaging error, the magnitude of which is dependent on the value of the averaging capacitor, is present at low frequencies. For example, if the filter capacitor, C_{AV}, is 4 µF, the error is 0.1% at 10 Hz and increases to 1% at 3 Hz. To measure ac signals, the AD637 can be ac-coupled by adding a nonpolar capacitor in series with the input, as shown in Figure 5.

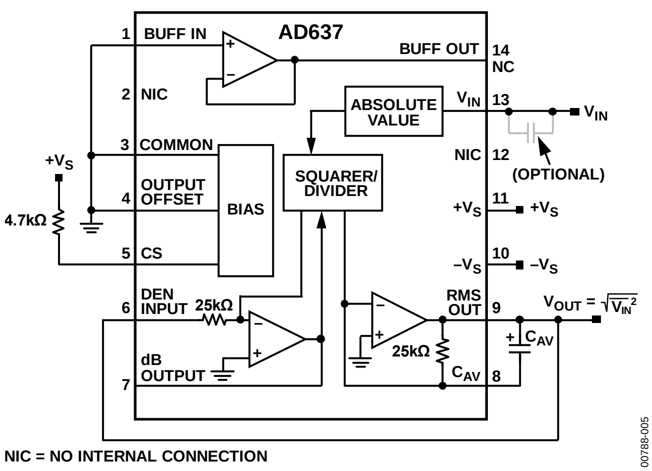


Figure 5. Standard RMS Connection

The performance of the AD637 is tolerant of minor variations in the power supply voltages; however, if the supplies used exhibit a considerable amount of high frequency ripple, it is advisable to bypass both supplies to ground through a 0.1 µF ceramic disc capacitor placed as close to the device as possible.

The output signal range of the AD637 is a function of the supply voltages, as shown in Figure 6. Use the output voltage buffered or nonbuffered, depending on the characteristics of the load. Connect the buffer input (Pin 1) to common if buffering is not required. The output of the AD637 is capable of driving 5 mA into a 2 kΩ load without degrading the accuracy of the device.

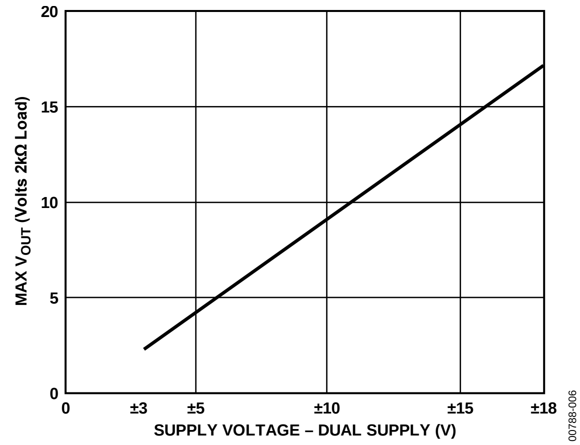


Figure 6. Maximum V_{OUT} vs. Supply Voltage

CHIP SELECT

The AD637 includes a chip select feature that allows the user to decrease the quiescent current of the device from 2.2 mA to 350 µA. This is done by driving CS, Pin 5, to below 0.2 V dc. Under these conditions, the output goes into a high impedance state. In addition to reducing the power consumption, the outputs of multiple devices can be connected in parallel to form a wide bandwidth rms multiplexer. Tie Pin 5 high to disable the chip select.

OPTIONAL TRIMS FOR HIGH ACCURACY

The AD637 includes provisions for trimming out output offset and scale factor errors resulting in significant reduction in the maximum total error, as shown in Figure 7. The residual error is due to a fixed input offset in the absolute value circuit and the residual nonlinearity of the device.

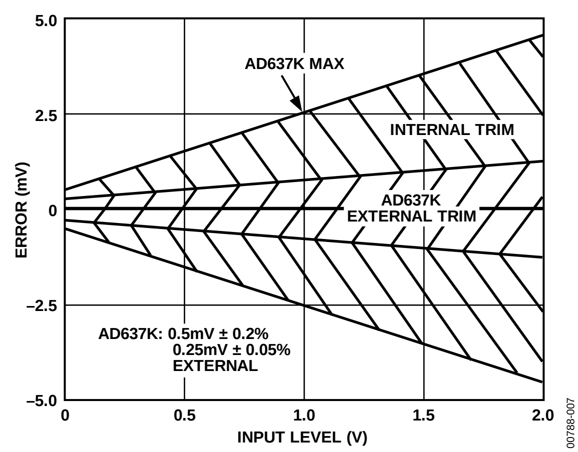


Figure 7. Maximum Total Error vs. Input Level AD637K Internal and External Trims

Referring to Figure 8 for optional external gain and offset trim schematic. The following sections describe trimming for greater accuracy in detail.

Offset Trim

Ground the input signal (V_{IN}) and adjust R1 until the output voltage at Pin 9 measures 0 V. Alternatively, apply the least expected value of V_{IN}.at the input V_{IN} and adjust R1 until the dc output voltage at Pin 9 measures the same value as the rms input.

Scale Factor Trim

Insert Resistor R4 in series with the input to decrease the range of the scale factor. Connect a precision source to Pin 13 and adjust the output for the desired full-scale input to V_{IN}, using either a calibrated dc or 1 kHz ac voltage, and adjust Resistor R3 to give the correct output at Pin 9 (that is, 1 V rms at the input results in a dc output voltage of 1.000 V dc). A 2 V p-p sine wave input yields 0.707 V dc at the output. Remaining errors are due to the nonlinearity.

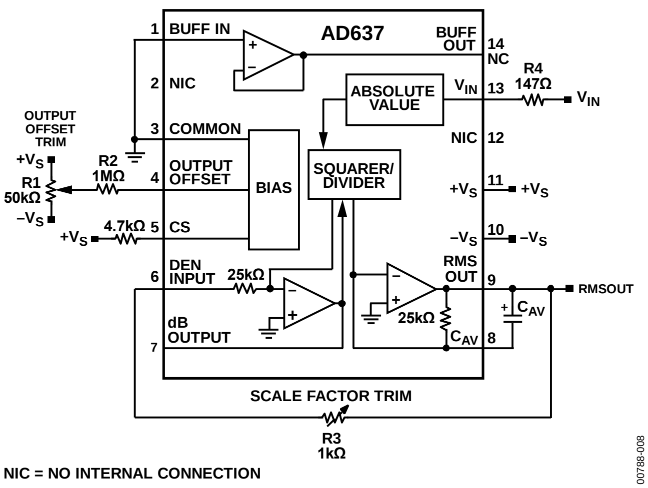


Figure 8. Optional External Gain and Offset Trims

CHOOSING THE AVERAGING TIME CONSTANT

The AD637 computes the true rms value of both dc and ac input signals. For dc inputs, the output tracks the absolute value of the input exactly. However, when the voltage is ac, the converted dc output voltage asymptotically approaches the theoretical rms value of the input. The deviation from the ideal rms value is due to the implicit denominator inherent to averaging over an infinite time span. Because the error diminishes as the averaging period increases, it quickly becomes negligible. The remaining error components are the ac ripple and dc offset voltage, if any. The ac and averaging error components are both functions of the input-frequency (*f*) and the averaging time constant τ (τ: 25 ms/µF of averaging capacitance). Figure 9 shows the output errors, which are enlarged for clarity. The frequency of the ac component (ripple) is twice the frequency of the input, the dc error is the RSS sum of the average rectified error and any fixed value dc offset.

The value of C_{AV} and the 25 kΩ feedback resistor establish the averaging time constant, and solely determines the magnitude of the rms-to-dc conversion error. Furthermore, any post-conversion filtering does not improve the dc component composite result.

Equation 1 defines the approximate peak value of the ac ripple component of the composite output.

$$\frac{50}{6.3\,\tau f}\ \text{in \% of reading where } (\tau > 1/f) \tag{1}$$

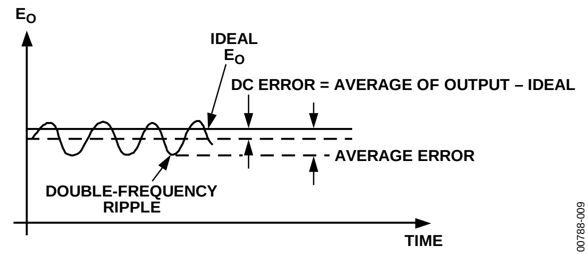


Figure 9. Enlarged Composite Conversion Result for a Sinusoidal Input

Increasing the value of the averaging capacitor or adding a post-rms filter network reduces the ripple error.

The dc error appears as a frequency dependent offset at the output of the AD637 and follows the relationship

$$\frac{1}{0.16 + 6.4\,\tau^2 f^2}\ \text{in \% of reading}$$

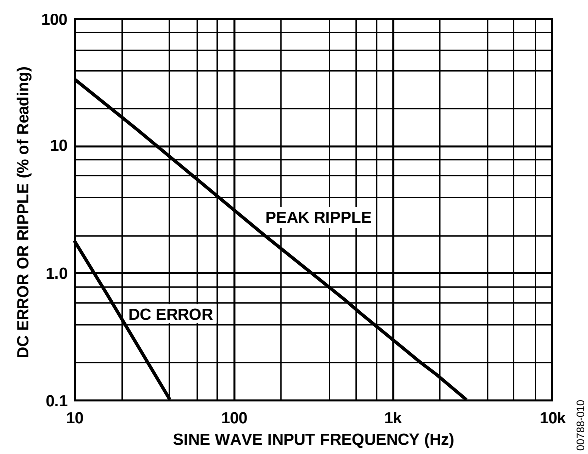


Figure 10. Comparison of Percent DC Error to the Percent Peak Ripple over Frequency Using the AD637 in the Standard RMS Connection with a 1 × µF C_{AV}

The ac ripple component of averaging error is greatly reduced by increasing the value of the averaging capacitor. However, the value of the averaging capacitor increases exponentially while the settling time increases directly proportion to the value of the averaging capacitor (T_S = 115 ms/µF of averaging capacitance).

A preferable ripple reduction method is to use a post conversion one or two-pole low-pass filter, as shown in Figure 11. Usually a single-pole filter gives the best overall compromise between ripple and settling time. Use the two-pole Sallen-Key for more ripple attenuation.

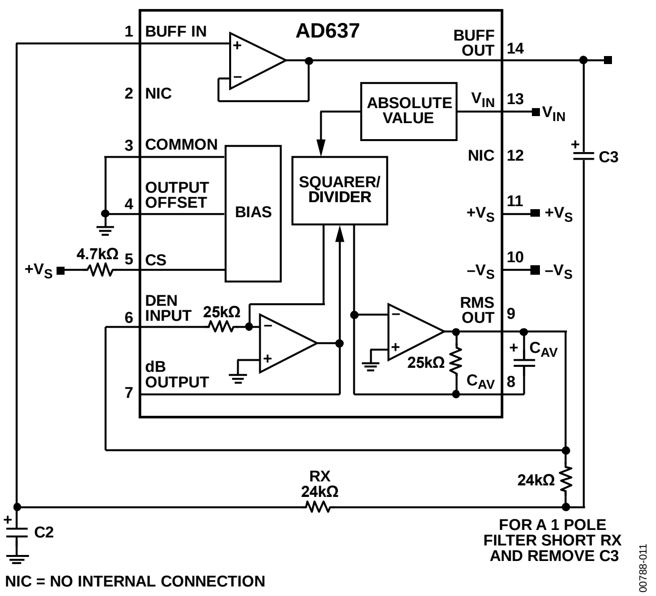


Figure 11. 2-Pole Sallen-Key Filter

Figure 12 shows values of C_{AV} and the corresponding averaging error as a function of sine wave frequency for the standard rms connection. The 1% settling time is shown on the right side of Figure 12.

Figure 13 shows the relationship between the averaging error, signal frequency settling time, and averaging capacitor value. Figure 13 is drawn for filter capacitor values of 3.3× the averaging capacitor value. This ratio sets the magnitude of the ac and dc errors equal at 50 Hz. As an example, by using a 1 μF averaging capacitor and a 3.3 μF filter capacitor, the ripple for a 60 Hz input signal is reduced from 5.3% of the reading using the averaging capacitor alone to 0.15% using the 1-pole filter. This gives a factor of 30 reduction in ripple, and yet the settling time only increases by a factor of 3. The values of Filter Capacitor C_{AV} and Filter Capacitor C2 can be calculated for the desired value of averaging error and settling time by using Figure 13.

The symmetry of the input signal also has an effect on the magnitude of the averaging error. Table 7 gives the practical component values for various types of 60 Hz input signals. These capacitor values can be directly scaled for frequencies other than 60 Hz—that is, for 30 Hz, these values are doubled, and for 120 Hz they are halved.

Use Figure 14 to determine the required value of C_{AV}, C2, and C3 for the desired level of ripple and settling time.

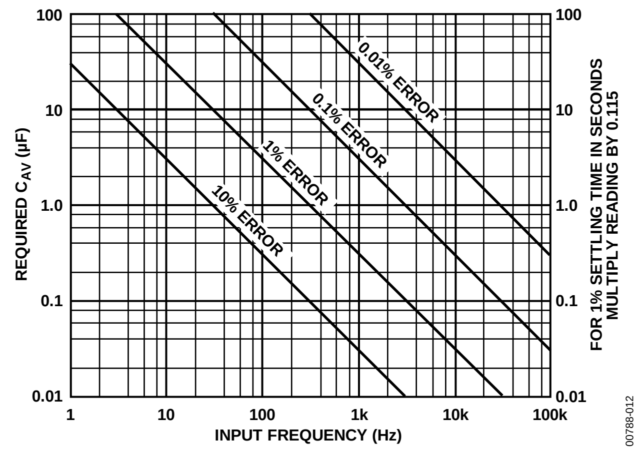


Figure 12. Values for C_{AV} and 1% Settling Time for Stated % of Reading; Averaging Error (% DC Error + % Ripple (Peak)); Accuracy Includes ±20% Component Tolerance

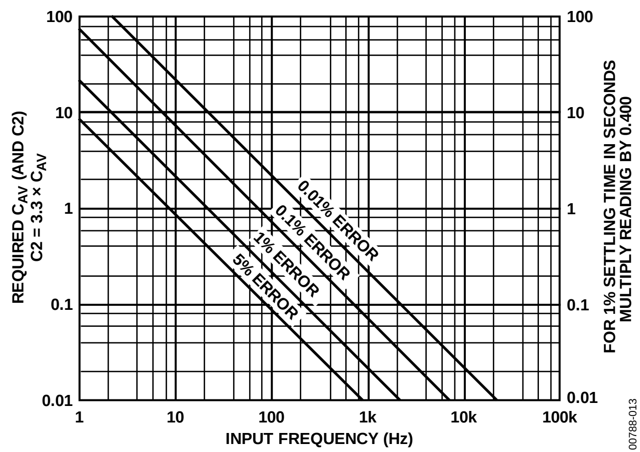


Figure 13. Values of C_{AV}, C2, and 1% Settling Time for Stated % of Reading for 1-Pole Post Filter; Averaging Error (% DC Error + % Ripple (Peak) Accuracy ±20% Due to Component Tolerance)

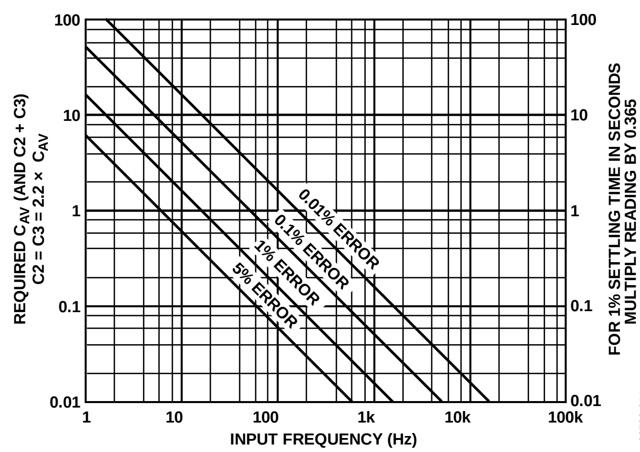
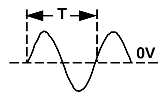
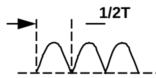
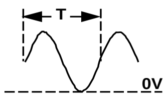
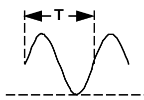
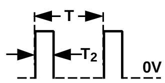
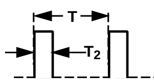
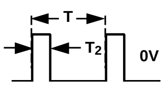
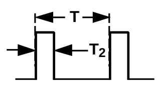


Figure 14. Values of C_{AV}, C2, and C3 and 1% Settling Time for Stated % of Reading for 2-Pole Sallen-Key Filter; Averaging Error (% DC Error + %Ripple (Peak) Accuracy ±20% Due to Component Tolerance)

Table 7. Practical Values of C_{AV} and C2 for Various Input Waveforms

Input Waveform and Period	Absolute Value Circuit Waveform and Period	Minimum R × C_{AV} Time Constant	Recommended Standard Values for C_{AV} and C2 for 1% Averaging Error @ 60 Hz with T = 16.6 ms		1% Settling Time
			C_{AV} (µF)	C2 (µF)	
A  Symmetrical Sine Wave		1/2T	0.47	1.5	181 ms
B  Sine Wave with dc Offset		T	0.82	2.7	325 ms
C  Pulse Train Waveform		10 (T – T_2)	6.8	22	2.67 sec
D 		10 (T – $2T_2$)	5.6	18	2.17 sec

FREQUENCY RESPONSE

The frequency response of the AD637 at various signal levels is shown in Figure 15. The dashed lines show the upper frequency limits for 1%, 10%, and ±3 dB of additional error. For example, note that for 1% additional error with a 2 V rms input, the highest frequency allowable is 200 kHz. A 200 mV signal can be measured with 1% error at signal frequencies up to 100 kHz.

To take full advantage of the wide bandwidth of the AD637, use care in the selection of the input buffer amplifier. To ensure that the input signal is accurately presented to the converter, the input buffer must have a −3 dB bandwidth that is wider than that of the AD637. Note the importance of slew rate in this application. For example, the minimum slew rate required for a 1 V rms, 5 MHz, sine wave input signal is 44 V/µs. The user is cautioned that this is the minimum rising or falling slew rate and that care must be exercised in the selection of the buffer amplifier, because some amplifiers exhibit a two-to-one difference between rising and falling slew rates. The AD845 is recommended as a precision input buffer.

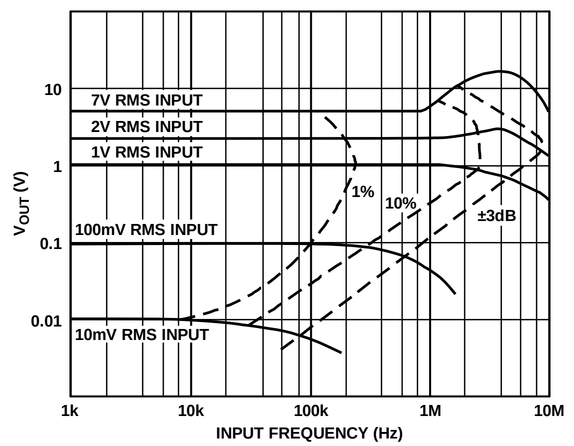


Figure 15. Frequency Response

AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the peak signal amplitude to the rms value of the signal (CF = V_P/V rms). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (≤2). Waveforms that resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 (CF = 1 $\sqrt{\eta}$).

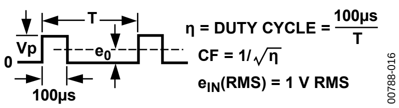


Figure 16. Duty Cycle Timing

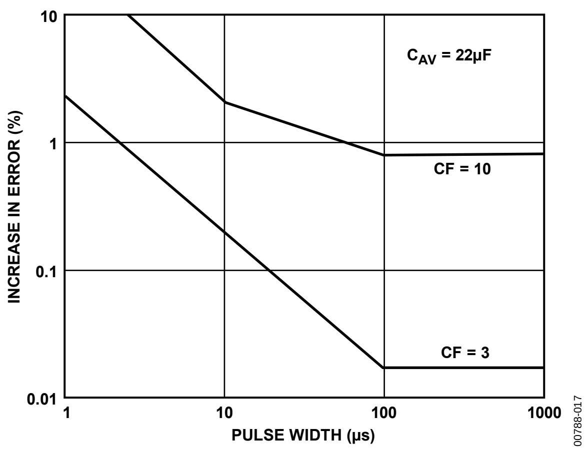


Figure 17. AD637 Error vs. Pulse Width Rectangular Pulse

Figure 18 is a curve of additional reading error for the AD637 for a 1 V rms input signal with crest factors from 1 to 11. A rectangular pulse train (pulse width 100 µs) is used for this test because it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from l to 10 while maintaining a constant 1 V rms input amplitude.

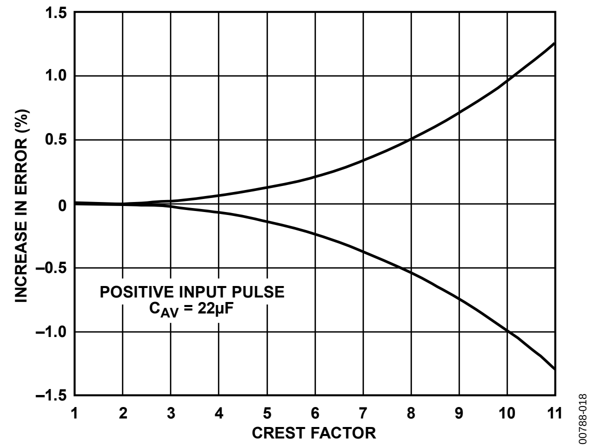


Figure 18. Additional Error vs. Crest Factor

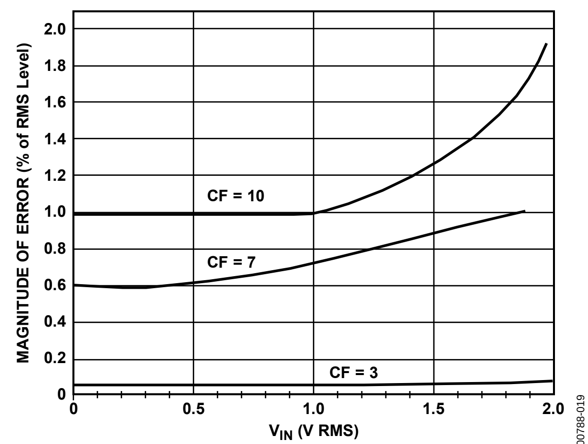


Figure 19. Error vs. RMS Input Level for Three Common Crest Factors

CONNECTION FOR dB OUTPUT

Another feature of the AD637 is the logarithmic, or decibel, output. The internal circuit that computes dB works well over a 60 dB range. Figure 20 shows the dB measurement connection. The user selects the 0 dB level by setting R1 for the proper 0 dB reference current, which is set to cancel the log output current from the squarer/divider circuit at the desired 0 dB point. The external op amp is used to provide a more convenient scale and to allow compensation of the 0.33%/°C temperature drift of the dB circuit. The temperature resistor, R3, as shown in Figure 20, is available from Precision Resistor Co., Inc., in Largo, Fla. (Model PT146).

dB CALIBRATION

Refer to Figure 20:

- Set V_{IN} = 1.00 V dc or 1.00 V rms
- Adjust R1 for 0 dB output = 0.00 V
- Set V_{IN} = 0.1 V dc or 0.10 V rms
- Adjust R2 for dB output = −2.00 V

Any other dB reference can be used by setting V_{IN} and R1 accordingly.

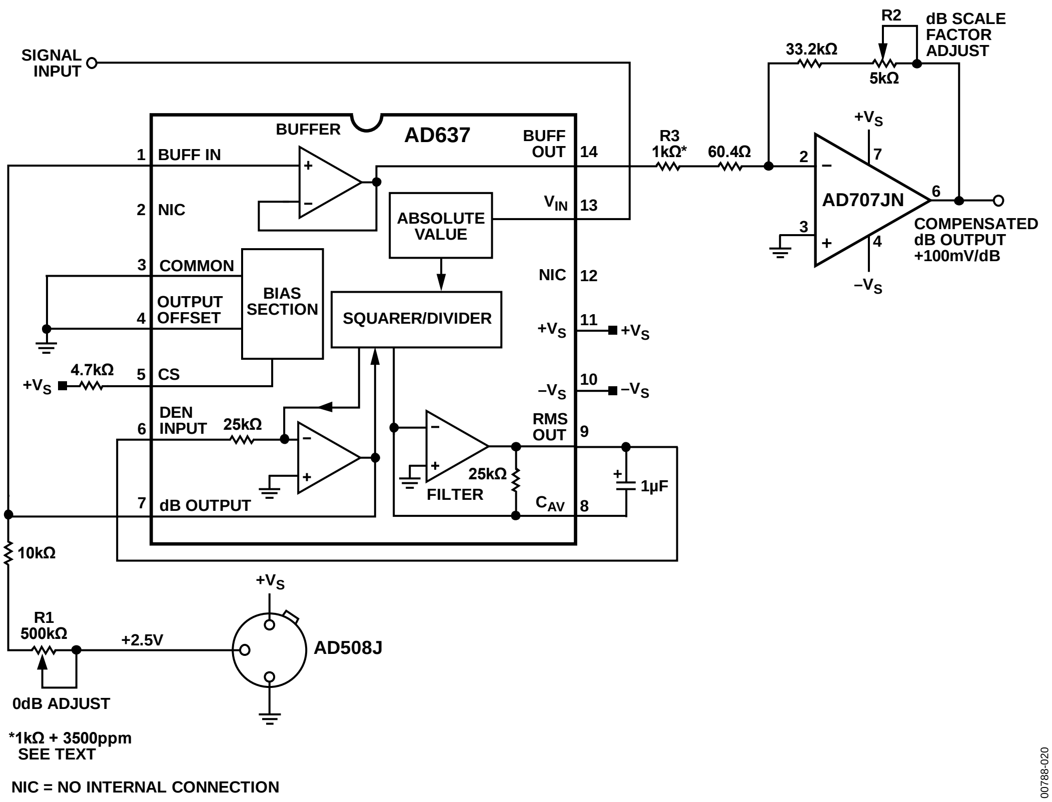


Figure 20. dB Connection

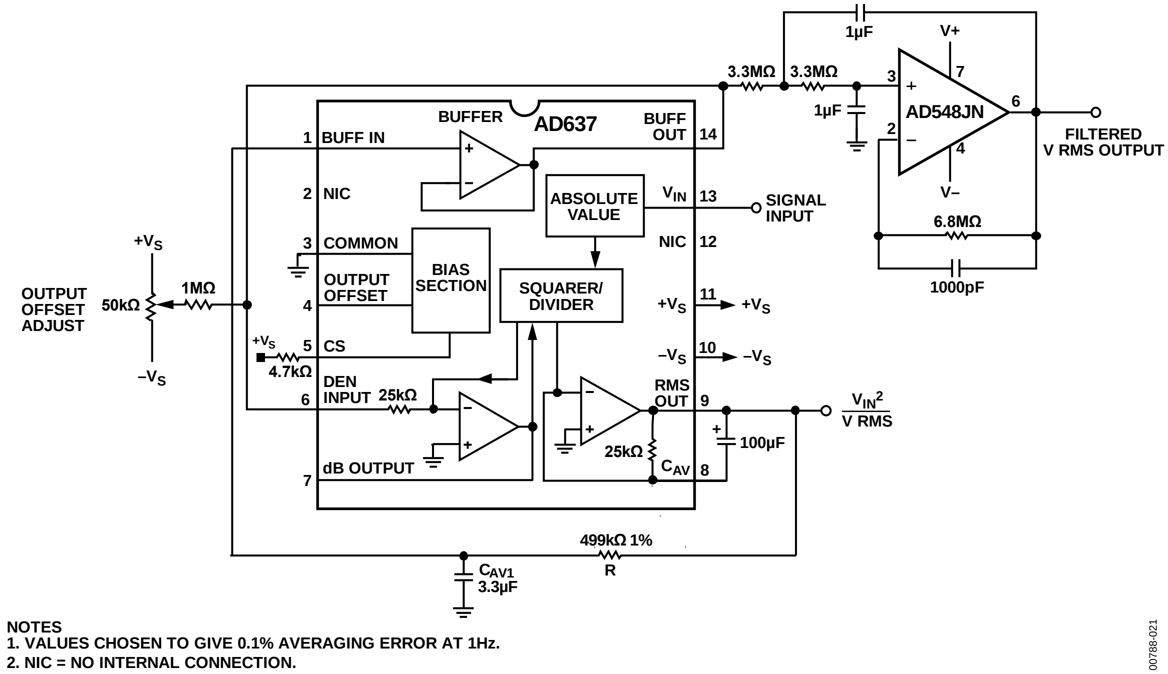


Figure 21. AD637 as a Low Frequency RMS Converter

LOW FREQUENCY MEASUREMENTS

If the frequencies of the signals to be measured are below 10 Hz, the value of the averaging capacitor required to deliver even 1% averaging error in the standard rms connection becomes extremely large. Figure 21 shows an alternative method of obtaining low frequency rms measurements. Determine the averaging time constant by the product of R and C_{AV1}, in this circuit, 0.5 sec/μF of C_{AV}. This circuit permits a 20:1 reduction in the value of the averaging capacitor, permitting the use of high quality tantalum capacitors. It is suggested that the 2-pole, Sallen-Key filter shown in Figure 21 be used to obtain a low ripple level and minimize the value of the averaging capacitor.

If the frequency of interest is below 1 Hz, or if the value of the averaging capacitor is still too large, increase the 20:1 ratio. This is accomplished by increasing the value of R. If this is done, it is suggested that a low input current, low offset voltage amplifier, such as the AD548, be used instead of the internal buffer amplifier. This is necessary to minimize the offset error introduced by the combination of amplifier input currents and the larger resistance.

VECTOR SUMMATION

Use two AD637s for vector summation as shown in Figure 22. Here, the averaging capacitors are omitted (nominal 100 pF capacitors are used to ensure stability of the filter amplifier), and the outputs are summed as shown. The output of the circuit is

$$V_{OUT} = \sqrt{V_X{}^2 + V_Y{}^2}$$

This concept can be expanded to include additional terms by feeding the signal from Pin 9 of each additional AD637 through a 10 kΩ resistor to the summing junction of the AD711 and tying all of the denominator inputs (Pin 6) together.

If C_{AV} is added to IC1 in this configuration, then the output is

$$\sqrt{\overline{V_X{}^2} + V_Y{}^2}$$

If the averaging capacitor is included on both IC1 and IC2, the output is

$$\sqrt{\overline{V_X{}^2} + \overline{V_Y{}^2}}$$

This circuit has a dynamic range of 10 V to 10 mV and is limited only by the 0.5 mV offset voltage of the AD637. The useful bandwidth is 100 kHz.

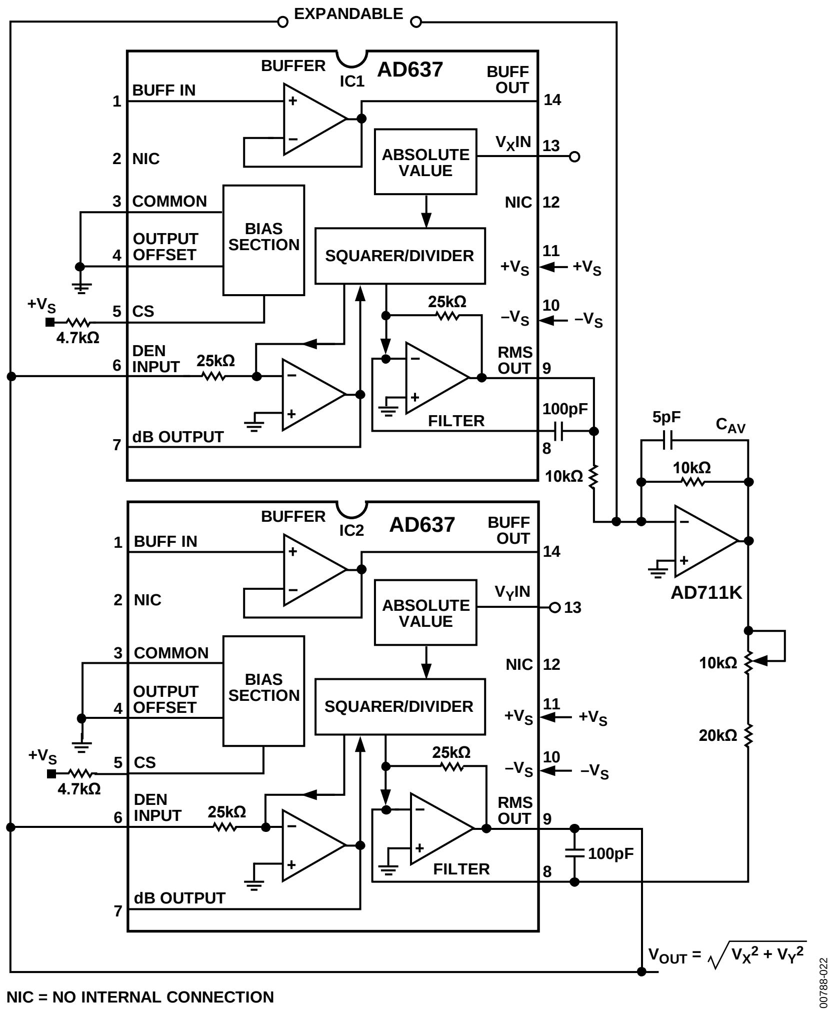


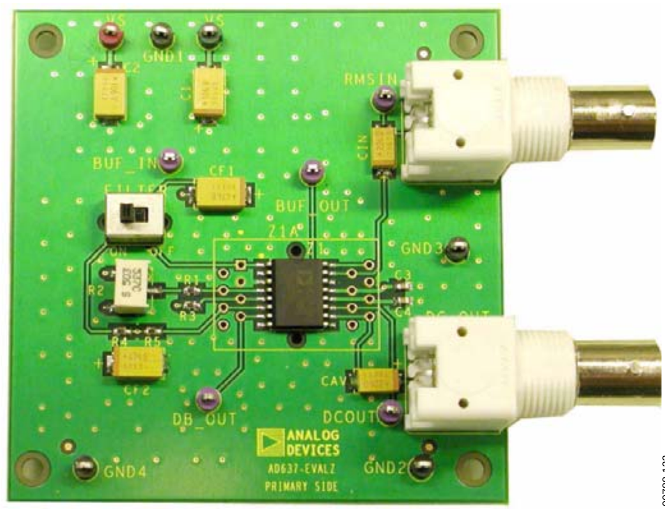
Figure 22. Vector Sum Configuration

EVALUATION BOARD

Figure 23 shows a digital image of the AD637-EVALZ, an evaluation board specially designed for the AD637. It is available at www.analog.com and is fully tested and ready for bench testing after connecting power and signal I/O. The circuit is configured for dual power supplies, and standard BNC connectors serve as the signal input and output ports.

Referring to the schematic in Figure 30, the input connector RMS_IN is capacitively coupled to Pin 15 (V_{IN} of SOIC package) of the AD637. The DC_OUT connector is connected to Pin 11, RMS OUT, with provisions for connections to the output buffer between Pin 1 and Pin 16. The buffer is an uncommitted op amp, and is configured on the AD637-EVALZ as a low-pass Sallen-Key filter whose f_C < 0.5 Hz. Users can connect to the buffer by moving the FILTER switch to the on position. DC_OUT is still the output of the AD637, and the test loop, BUF_OUT, is the output of the buffer. The R2 trimmer adjusts the output offset voltage.

The LPF frequency is changed by changing the component values of CF1, CF2, R4, and R5. See Figure 24 and Figure 30 to locate these components. Note that a wide range of capacitor and resistor values can be used with the AD637 buffer amplifier.



00788-123

Figure 23. AD637-EVALZ

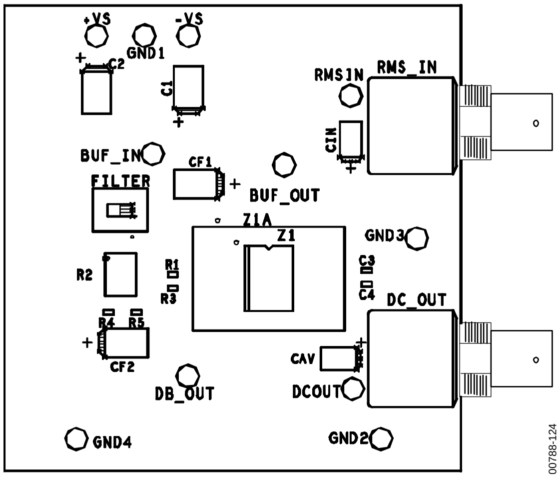


Figure 24. AD637-EVALZ Assembly

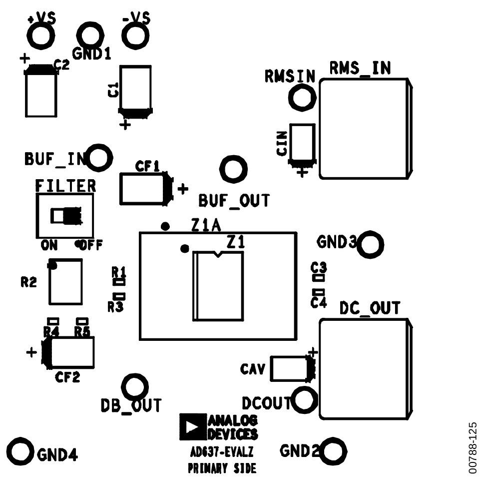


Figure 25. Component Side Silkscreen

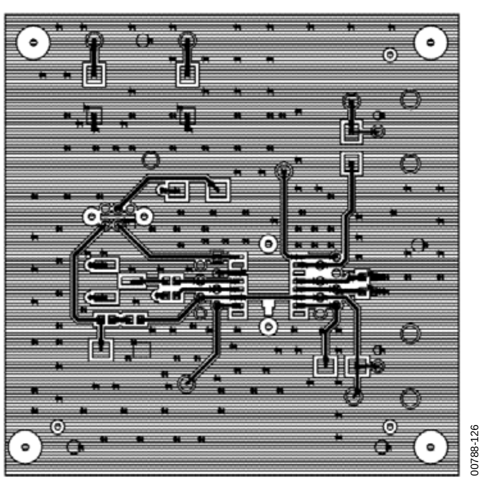


Figure 26. Evaluation Board—Component Side Copper

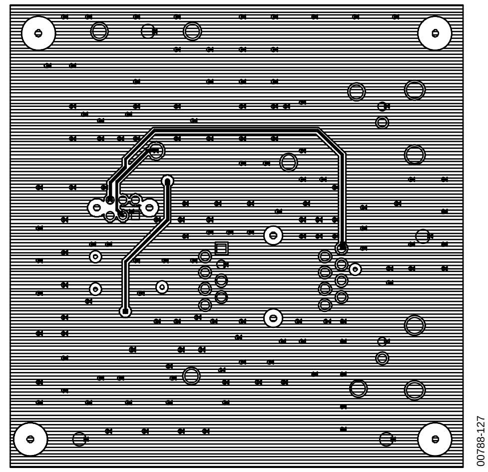


Figure 27. Evaluation Board—Secondary Side Copper

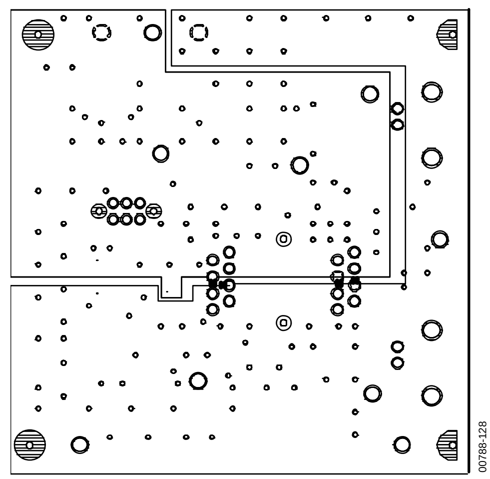


Figure 28. Evaluation Board—Internal Power Plane

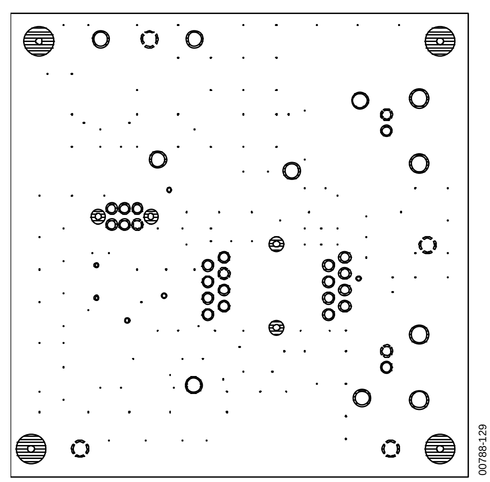


Figure 29. Evaluation Board—Internal Ground Plane

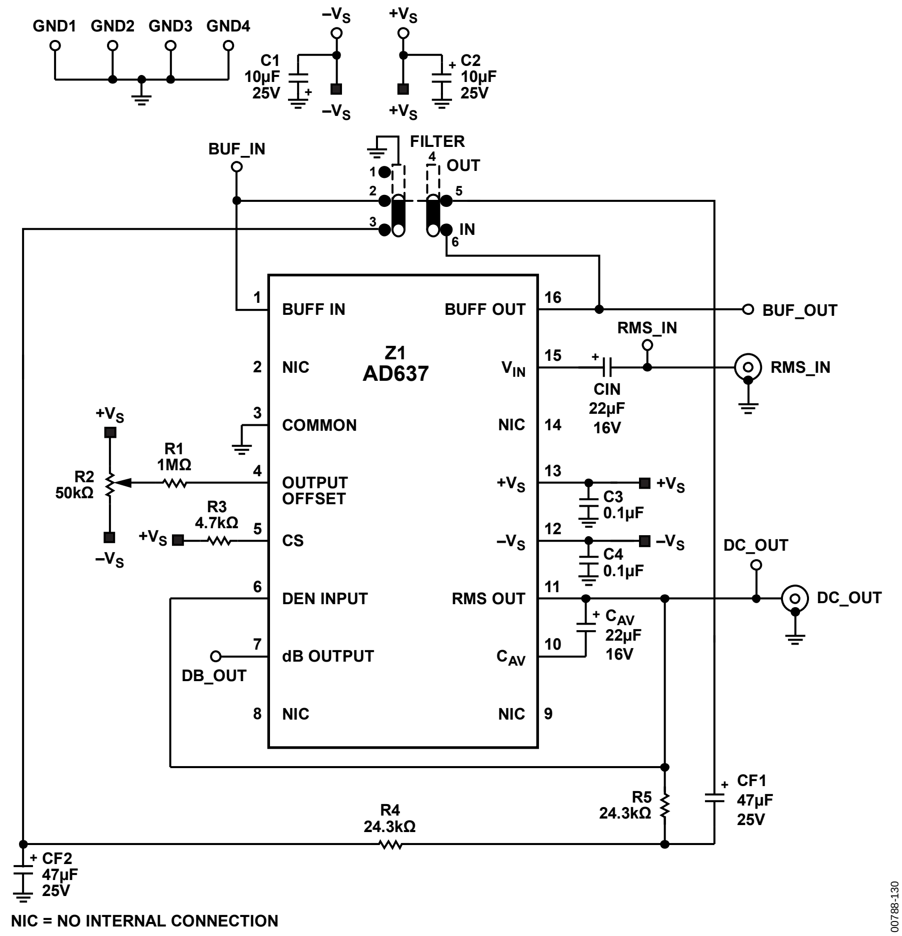


Figure 30. Evaluation Board Schematic

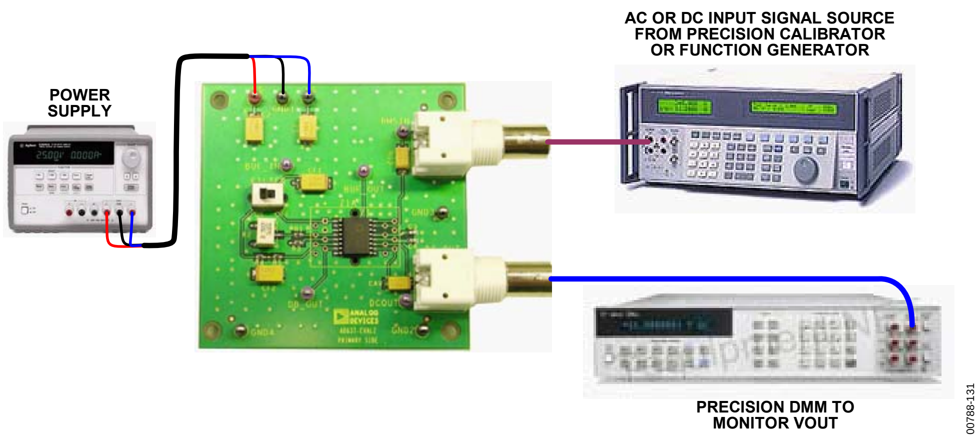


Figure 31. AD637-EVALZ Typical Bench Configuration

OUTLINE DIMENSIONS

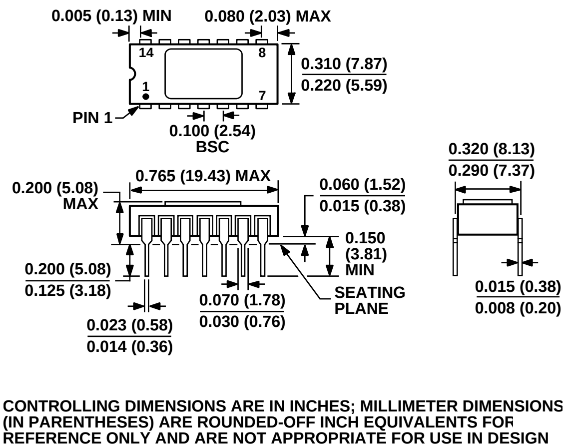


Figure 32. 14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP] (D-14)
Dimensions shown in inches and (millimeters)

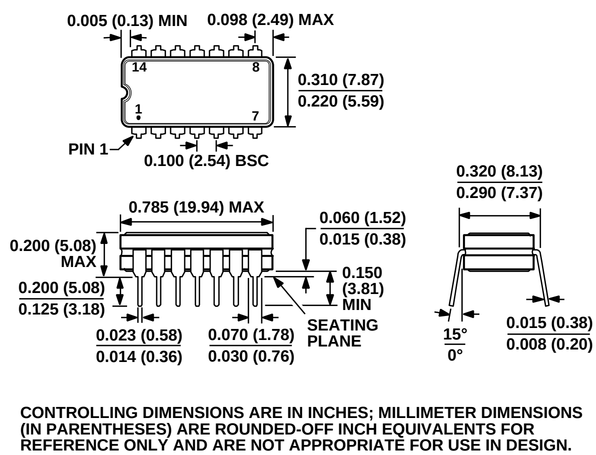


Figure 33. 14-Lead Ceramic Dual In-Line Package [CERDIP] (Q-14)
Dimensions shown in inches and (millimeters)

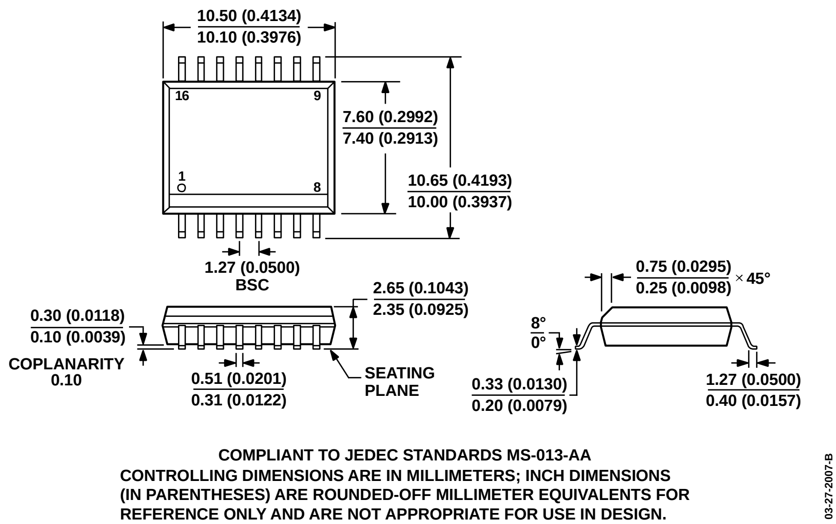


Figure 34. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Notes	Temperature Range	Package Description	Package Option
5962-8963701CA	2	−55°C to +125°C	14-Lead CERDIP	Q-14
AD637AQ		−40°C to +85°C	14-Lead CERDIP	Q-14
AD637ARZ		−40°C to +85°C	16-Lead SOIC_W	RW-16
AD637BRZ		−40°C to +85°C	16-Lead SOIC_W	RW-16
AD637JD		0°C to 70°C	14-Lead SBDIP	D-14
AD637JDZ		0°C to 70°C	14-Lead SBDIP	D-14
AD637JQ		0°C to 70°C	14-Lead CERDIP	Q-14
AD637JRZ		0°C to 70°C	16-Lead SOIC_W	RW-16
AD637JRZ-RL		0°C to 70°C	16-Lead SOIC_W	RW-16
AD637JRZ-R7		0°C to 70°C	16-Lead SOIC_W	RW-16
AD637KDZ		0°C to 70°C	14-Lead SBDIP	D-14
AD637KQ		0°C to 70°C	14-Lead CERDIP	Q-14
AD637KRZ		0°C to 70°C	16-Lead SOIC_W	RW-16
AD637SD		−55°C to +125°C	14-Lead SBDIP	D-14
AD637SD/883B		−55°C to +125°C	14-Lead SBDIP	D-14
AD637SQ/883B		−55°C to +125°C	14-Lead CERDIP	Q-14
AD637-EVALZ			Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] A standard microcircuit drawing is available.