Low Power Mixer
3 V Receiver IF Subsystem

AD607

FEATURES

Complete Receiver-on-a-Chip: Monoceiver® Mixer
- **–15 dBm 1 dB Compression Point**
- **–8 dBm Input Third Order Intercept**
- **500 MHz RF and LO Bandwidths**

Linear IF Amplifier
- **Linear-in-dB Gain Control**
- **Manual Gain Control**

Quadrature Demodulator
- **On-Board Phase-Locked Quadrature Oscillator**
- **Demodulates IFs from 400 kHz to 12 MHz**
- **Can Also Demodulate AM, CW, SSB**

Low Power
- **25 mW at 3 V**
- **CMOS Compatible Power-Down**

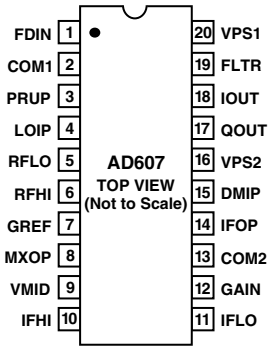
Interfaces to AD7013 and AD7015 Baseband Converters

APPLICATIONS

GSM, CDMA, TDMA, and TETRA Receivers
Satellite Terminals
Battery-Powered Communications Receivers

PIN CONFIGURATION

20-Lead SSOP
(RS Suffix)



GENERAL DESCRIPTION

The AD607 is a 3 V low power receiver IF subsystem for operation at input frequencies as high as 500 MHz and IFs from 400 kHz to 12 MHz. It consists of a mixer, IF amplifiers, I and Q demodulators, a phase-locked quadrature oscillator, and a biasing system with external power-down.

The AD607's low noise, high intercept mixer is a doubly balanced Gilbert cell type. It has a nominal –15 dBm input referred 1 dB compression point and a –8 dBm input referred third order intercept. The mixer section of the AD607 also includes a local oscillator (LO) preamplifier, which lowers the required LO drive to –16 dBm.

In MGC operation, the AD607 accepts an external gain-control voltage input from an external AGC detector or a DAC.

The I and Q demodulators provide in-phase and quadrature baseband outputs to interface with Analog Devices' AD7013 (IS54, TETRA, MSAT) and AD7015 (GSM) baseband converters. A quadrature VCO phase-locked to the IF drives the I and Q demodulators. The I and Q demodulators can also demodulate AM; when the AD607's quadrature VCO is phase-locked to the received signal, the in-phase demodulator becomes a synchronous product detector for AM. The VCO can also be phase-locked to an external beat-frequency oscillator (BFO), and the demodulator serves as a product detector for CW or SSB reception. Finally, the AD607 can be used to demodulate BPSK using an external Costas Loop for carrier recovery.

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REV. C

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AD607–SPECIFICATIONS (@ T_A = 25°C, Supply = 3.0 V, IF = 10.7 MHz, unless otherwise noted.)

Model	Conditions	AD607ARS Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
MIXER					
Maximum RF and LO Frequency Range	For Conversion Gain > 20 dB		500		MHz
Maximum Mixer Input Voltage	For Linear Operation; Between RFHI and RFLO		±54		mV
Input 1 dB Compression Point	RF Input Terminated in 50 Ω		–15		dBm
Input Third-Order Intercept	RF Input Terminated in 50 Ω		–5		dBm
Noise Figure	Matched Input, Max Gain, f = 83 MHz, IF = 10.7 MHz		14		dB
	Matched Input, Max Gain, f = 144 MHz, IF = 10.7 MHz		12		dB
Maximum Output Voltage at MXOP	Z_{IF} = 165 Ω, at Input Compression		±1.3		V
Mixer Output Bandwidth at MXOP	–3 dB, Z_{IF} = 165 Ω		45		MHz
LO Drive Level	Mixer LO Input Terminated in 50 Ω		–16		dBm
LO Input Impedance	LOIP to VMID		1		kΩ
Isolation, RF to IF	RF = 240 MHz, IF = 10.7 MHz, LO = 229.3 MHz		30		dB
Isolation, LO to IF	RF = 240 MHz, IF = 10.7 MHz, LO = 229.3 MHz		20		dB
Isolation, LO to RF	RF = 240 MHz, IF = 10.7 MHz, LO = 229.3 MHz		40		dB
Isolation, IF to RF	RF = 240 MHz, IF = 10.7 MHz, LO = 229.3 MHz		70		dB
IF AMPLIFIERS					
Noise Figure	Max Gain, f = 10.7 MHz		17		dB
Input 1 dB Compression Point	IF = 10.7 MHz		–15		dBm
Output Third-Order Intercept	IF = 10.7 MHz		18		dBm
Maximum IF Output Voltage at IFOP	Z_{IF} = 600 Ω		±560		mV
Output Resistance at IFOP	From IFOP to VMID		15		Ω
Bandwidth	–3 dB at IFOP, Max Gain		45		MHz
GAIN CONTROL	(See Figures 23 and 24)				
Gain Control Range	Mixer + IF Section, GREF to 1.5 V		90		dB
Gain Scaling	GREF to 1.5 V		20		mV/dB
	GREF to General Reference Voltage V_R		75/V_R		dB/V
Gain Scaling Accuracy	GREF to 1.5 V, 80 dB Span		±1		dB
Bias Current at GAIN			5		µA
Bias Current at GREF			1		µA
Input Resistance at GAIN, GREF			1		MΩ
I AND Q DEMODULATORS					
Required DC Bias at DMIP			VPOS/2		V dc
Input Resistance at DMIP	From DMIP to VMID		50		kΩ
Input Bias Current at DMIP			2		µA
Maximum Input Voltage	IF > 3 MHz		±150		mV
	IF ≤ 3 MHz		±75		mV
Amplitude Balance	IF = 10.7 MHz, Outputs at 600 mV p-p, F = 100 kHz		±0.2		dB
Quadrature Error	IF = 10.7 MHz, Outputs at 600 mV p-p, F = 100 kHz		–1.2		Degrees
Phase Noise in Degrees	IF = 10.7 MHz, F = 10 kHz		–100		dBc/Hz
Demodulation Gain	Sine Wave Input, Baseband Output		18		dB
Maximum Output Voltage	R_L ≥ 20 kΩ		±1.23		V
Output Offset Voltage	Measured from I_{OUT}, Q_{OUT} to VMID	–150	+10	+150	mV
Output Bandwidth	Sine Wave Input, Baseband Output		1.5		MHz
PLL					
Required DC Bias at FDIN			VPOS/2		V dc
Input Resistance at FDIN	From FDIN to VMID		50		kΩ
Input Bias Current at FDIN			200		nA
Frequency Range			0.4 to 12		MHz
Required Input Drive Level	Sine Wave Input at Pin 1		400		mV
Acquisition Time to ±3°	IF = 10.7 MHz		16.5		µs
POWER-DOWN INTERFACE					
Logical Threshold	For Power Up on Logical High		2		V dc
Input Current for Logical High			75		µA
Turn-On Response Time	To PLL Locked		16.5		µs
Standby Current			550		µA
POWER SUPPLY					
Supply Range		2.92		5.5	V
Supply Current	Midgain, IF = 10.7 MHz		8.5		mA
OPERATING TEMPERATURE					
T_{MIN} to T_{MAX}	Operation to 2.92 V Minimum Supply Voltage	–25		+85	°C
	Operation to 4.5 V Minimum Supply Voltage	–40		+85	°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage VPS1, VPS2 to COM1, COM2 . . . . . 5.5 V
Internal Power Dissipation[2] . . . . . 600 mW
2.92 V to 5.5 V Operating Temperature Range
. . . . . –25°C to +85°C
4.5 V to 5.5 V Operating Temperature Range
. . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

NOTES
[1] Stresses above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2] Thermal Characteristics: 20-lead SSOP Package: θ_{JA} = 126°C/W.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD607ARS	–25°C to +85°C for 2.92 V to 5.5 V Operation; –40°C to +85°C for 4.5 V to 5.5 V Operation	20-Lead Plastic SSOP	RS-20

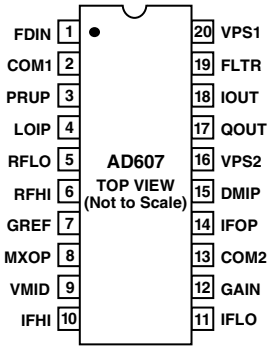
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD607 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Reads	Function
1	FDIN	Frequency Detector Input	PLL Input for I/Q Demodulator Quadrature Oscillator, ±400 mV Drive Required from External Oscillator. Must be biased at $V_P/2$.
2	COM1	Common #1	Supply Common for RF Front End and Main Bias
3	PRUP	Power-Up Input	3 V/5 V CMOS compatible power-up control; logical high = powered-up; max input level = VPS1 = VPS2.
4	LOIP	Local Oscillator Input	LO input, ac-coupled ±54 mV LO input is required (–16 dBm for 50 Ω input termination).
5	RFLO	RF "Low" Input	Usually Connected to AC Ground
6	RFHI	RF "High" Input	AC-Coupled, ±56 mV, Max RF Input for Linear Operation
7	GREF	Gain Reference Input	High Impedance Input, typically 1.5 V, sets gain scaling.
8	MXOP	Mixer Output	High Impedance, Single-Sided Current Output, ±1.3 V Max Voltage Output (±6 mA Max Current Output)
9	VMID	Midsupply Bias Voltage	Output of the Midsupply Bias Generator (VMID = VPOS/2)
10	IFHI	IF "High" Input	AC-Coupled IF Input, ±56 mV Max Input for Linear Operation
11	IFLO	IF "Low" Input	Reference Node for IF Input; Auto-Offset Null
12	GAIN	Gain Control Input	High Impedance Input, 0 V–2 V Using 3 V Supply, Max Gain at V = 0
13	COM2	Common #2	Supply Common for IF Stages and Demodulator
14	IFOP	IF Output	Low Impedance, Single-Sided Voltage Output, 5 dBm (±560 mV) Max
15	DMIP	Demodulator Input	Signal input to I and Q demodulators has a ±150 mV max input at IF > 3 MHz for linear operation; ±75 mV max input at IF < 3 MHz for linear operation. Must be biased at $V_P/2$.
16	VPS2	VPOS Supply #2	Supply to High Level IF, PLL, and Demodulators
17	QOUT	Quadrature Output	Low Impedance Q Baseband Output; ±1.23 V Full Scale in 20 kΩ Min Load; AC-Coupled
18	IOUT	In-Phase Output	Low Impedance I Baseband Output; ±1.23 V Full Scale in 20 kΩ Min Load; AC-Coupled
19	FLTR	PLL Loop Filter	Series RC PLL Loop Filter, Connected to Ground
20	VPS1	VPOS Supply #1	Supply to Mixer, Low Level IF, PLL, and Gain Control

PIN CONNECTION
20-Lead SSOP (RS-20)



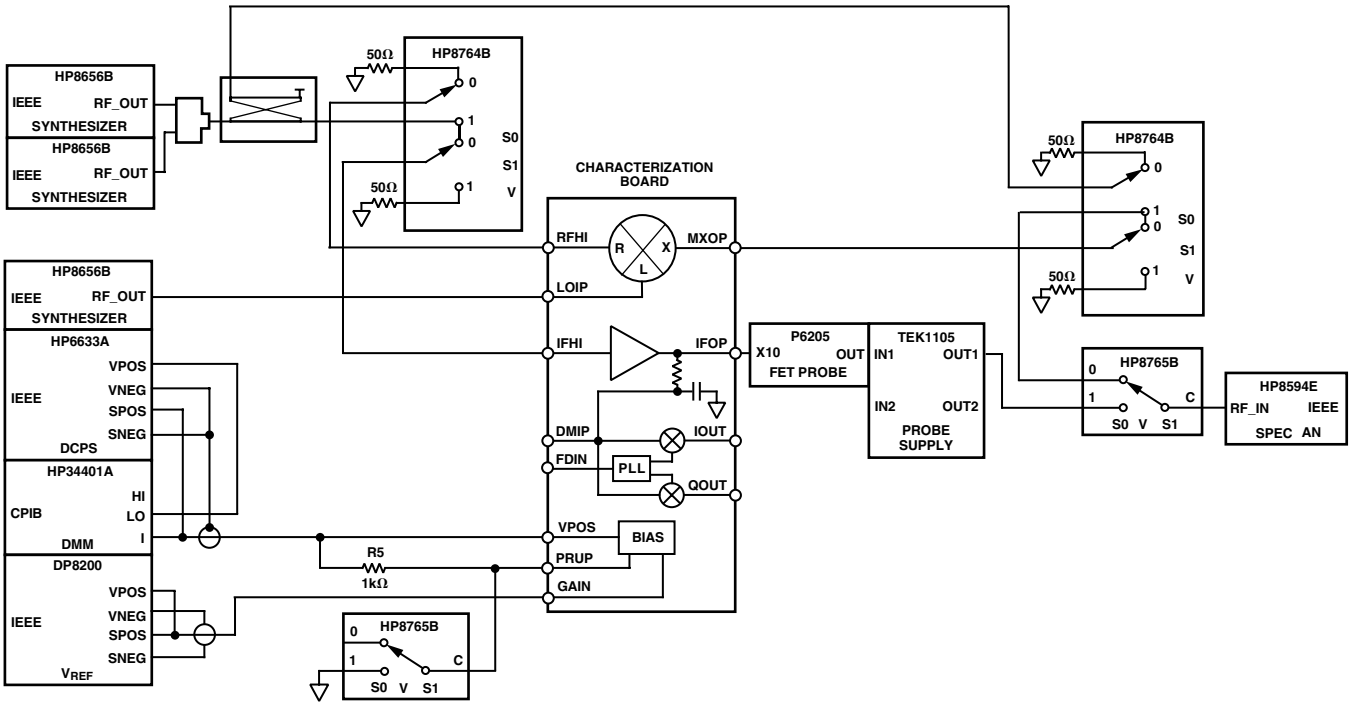


Figure 1. Mixer/Amplifier Test Set

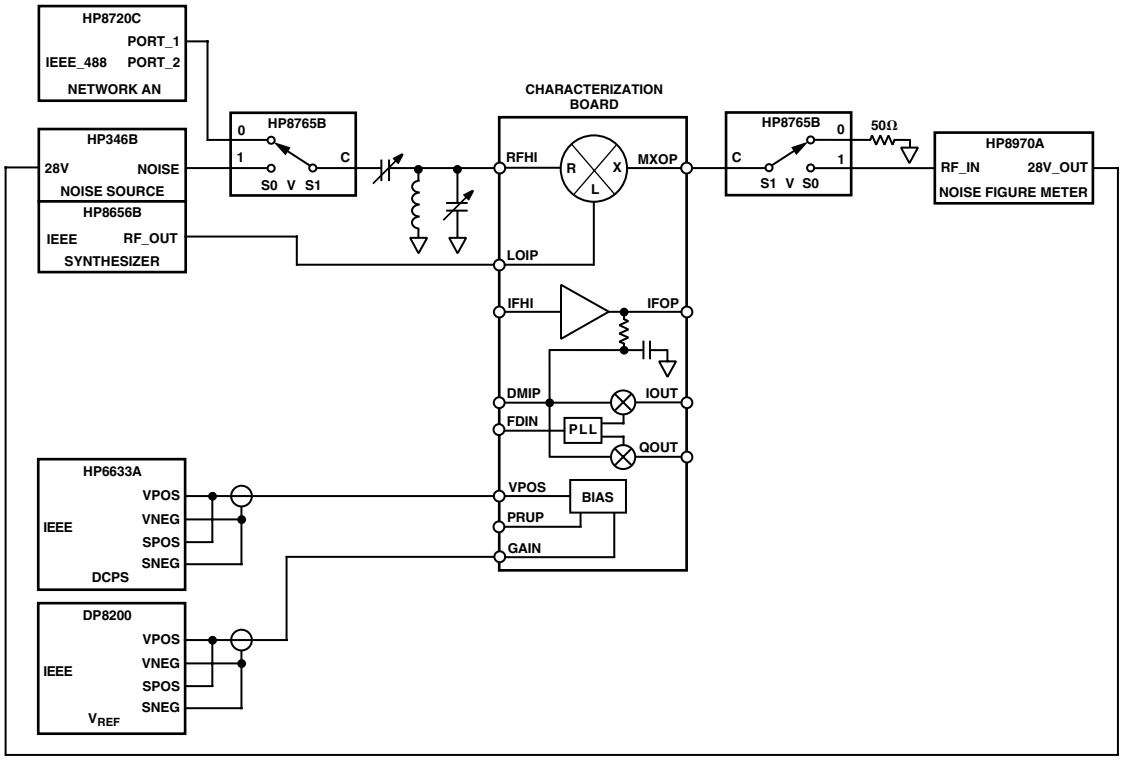


Figure 2. Mixer Noise Figure Test Set

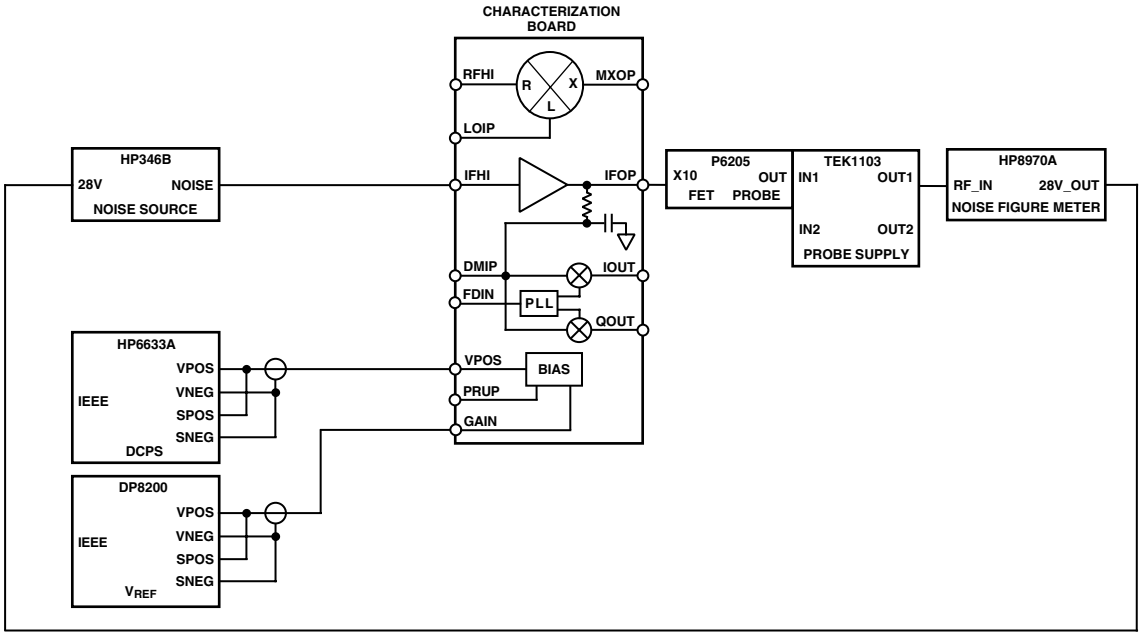


Figure 3. IF Amp Noise Figure Test Set

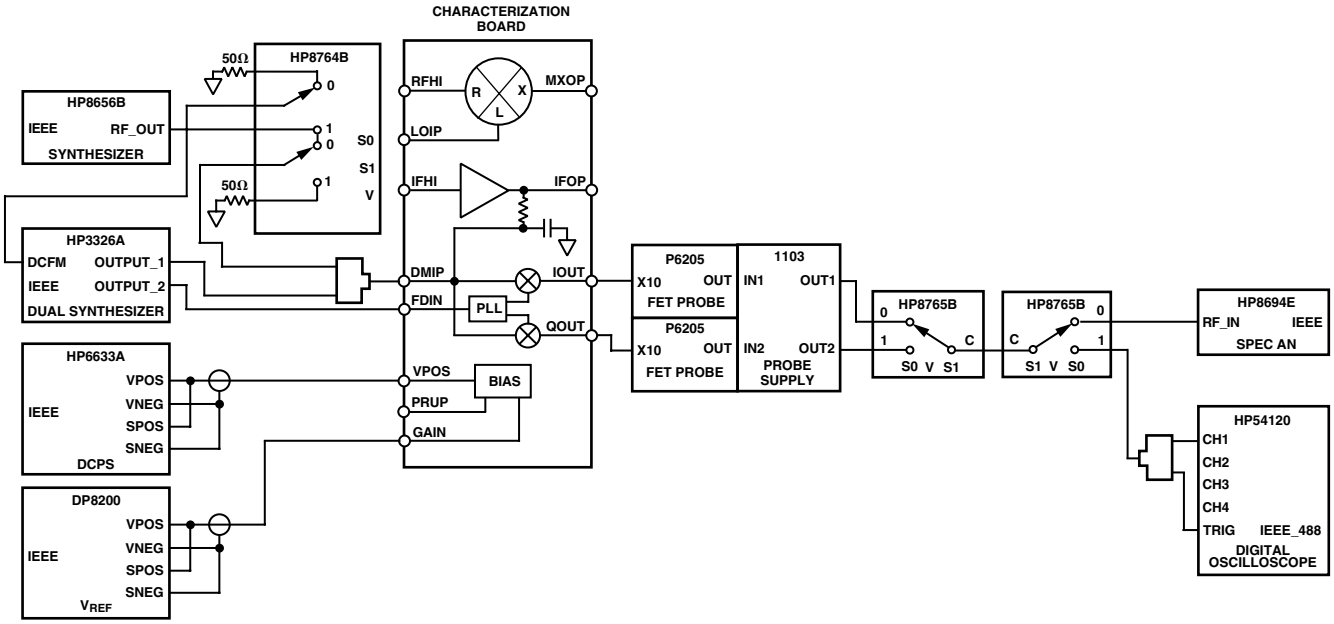


Figure 4. PLL/Demodulator Test Set

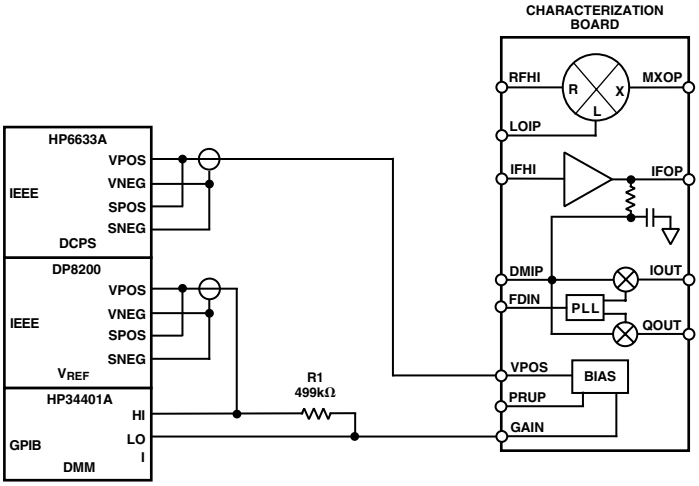


Figure 5. GAIN Pin Bias Test Set

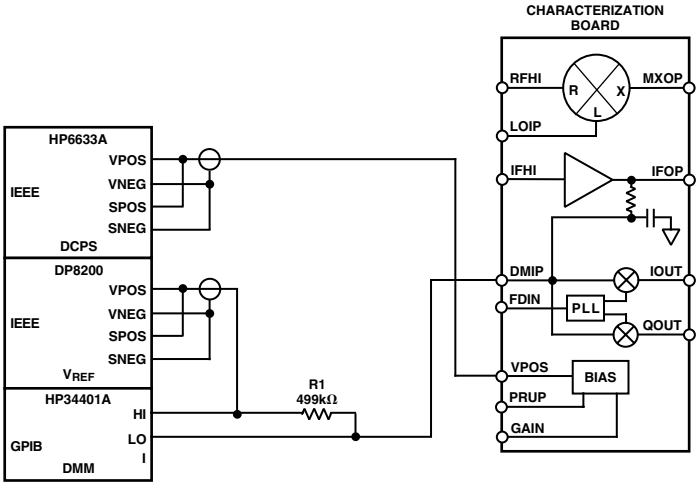


Figure 6. Demodulator Bias Test Set

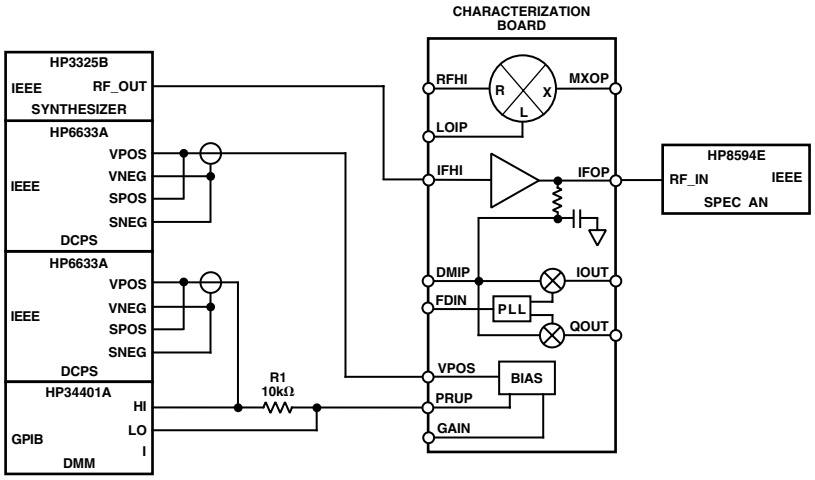


Figure 7. Power-Up Threshold Test Set

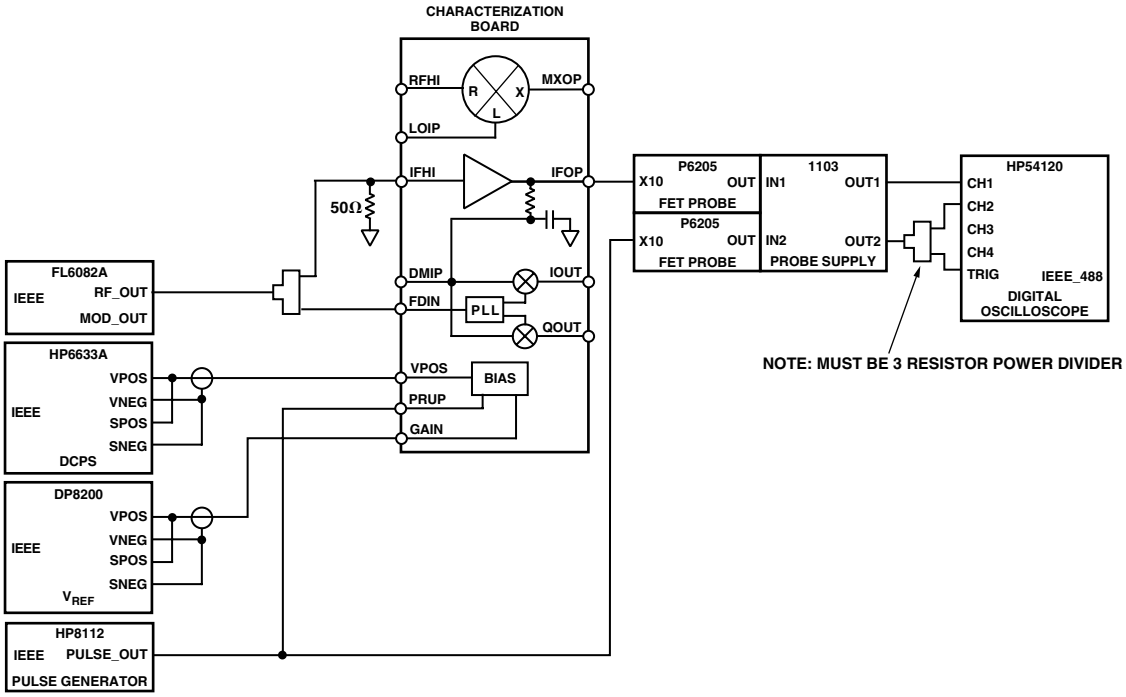


Figure 8. Power-Up Test Set

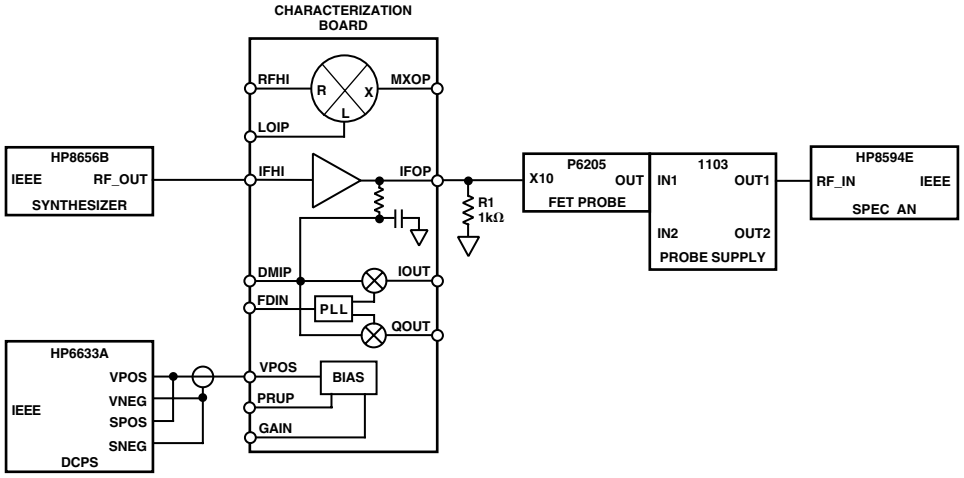


Figure 9. IF Output Impedance Test Set

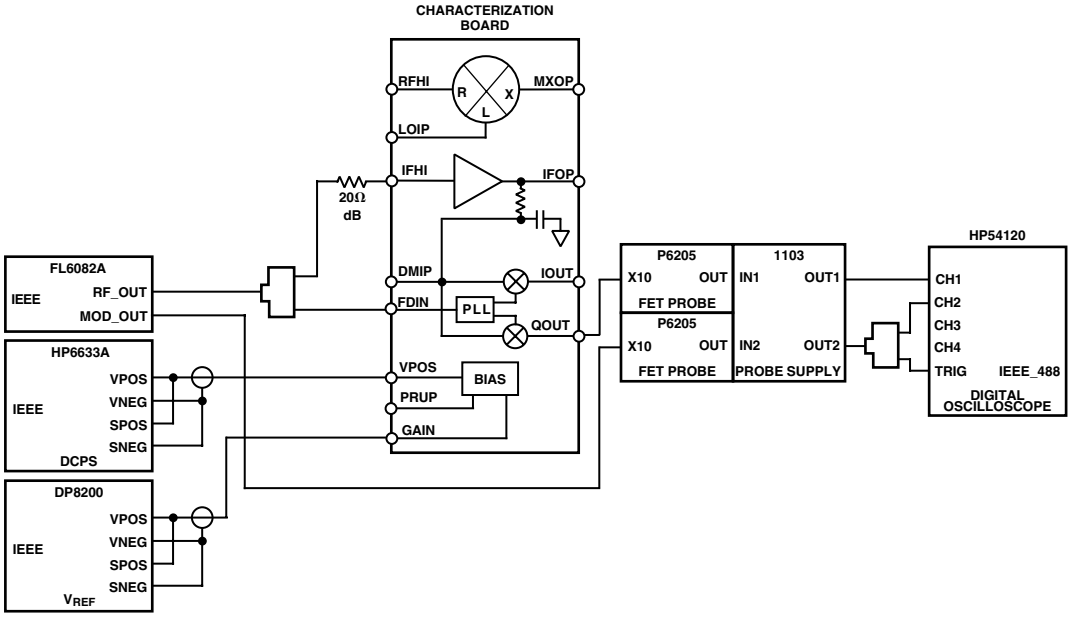


Figure 10. PLL Settling Time Test Set

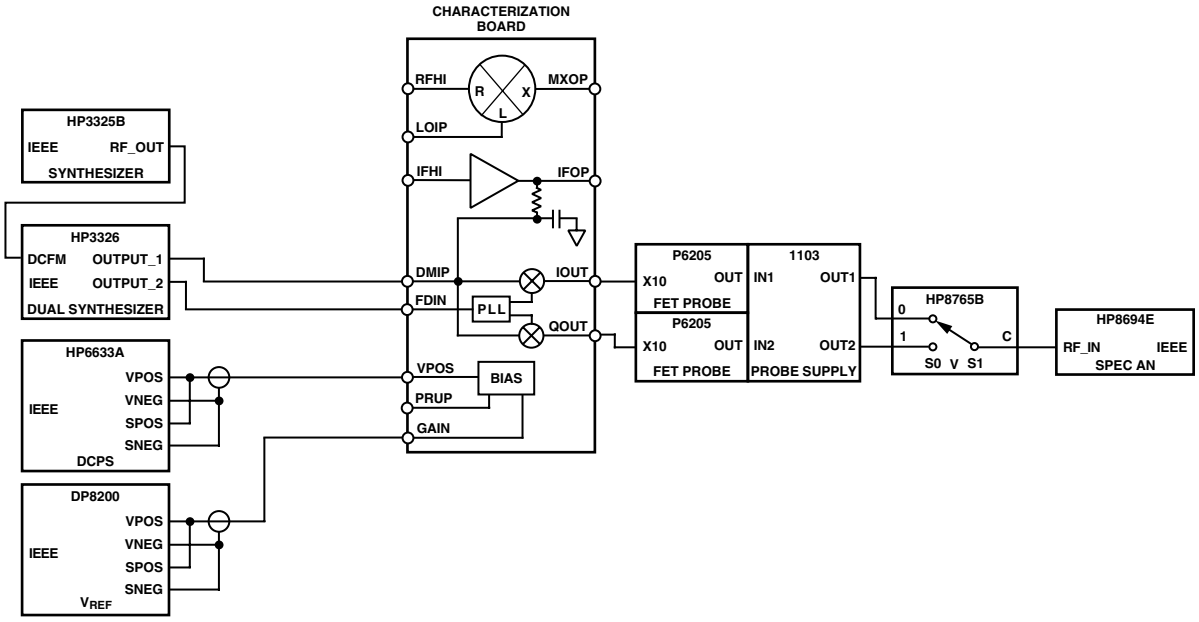


Figure 11. Quadrature Accuracy Test Set

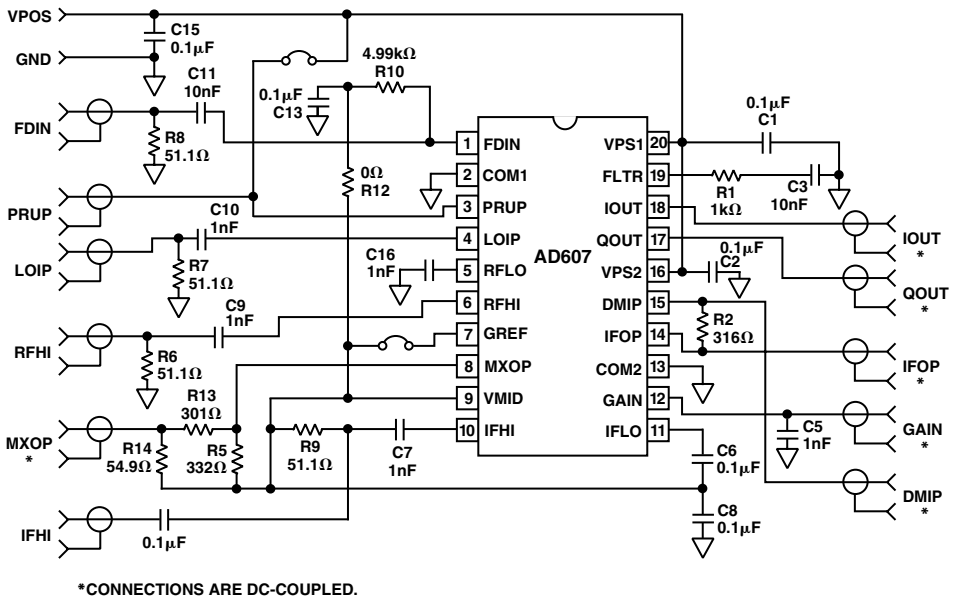
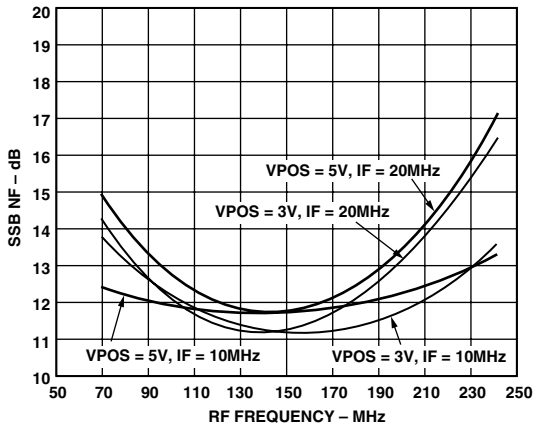
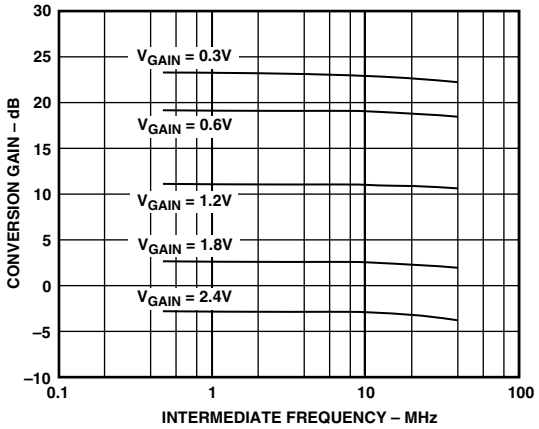


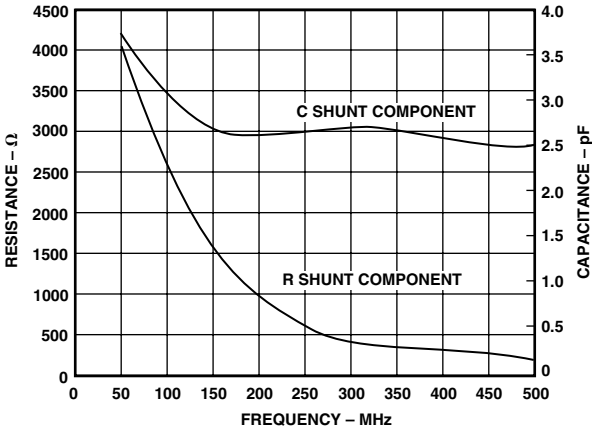
Figure 12. Characterization Board



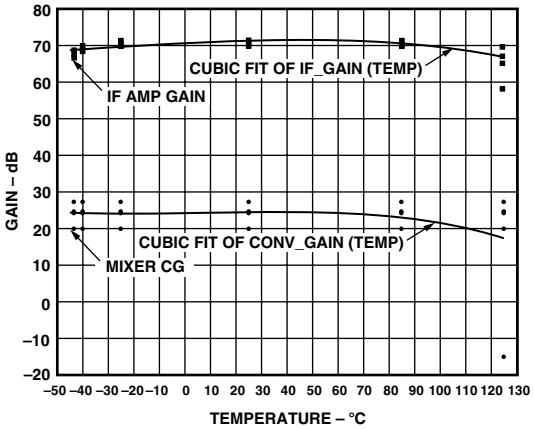
TPC 1. Mixer Noise Figure vs. Frequency



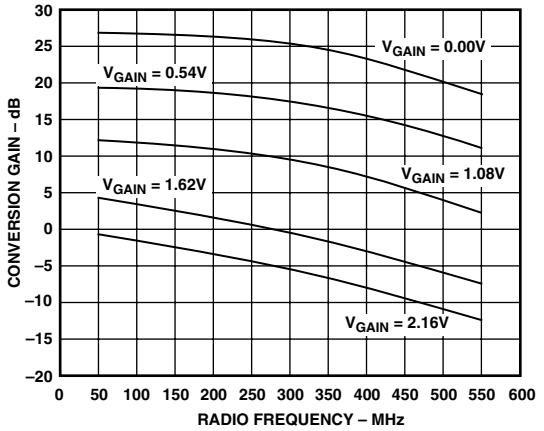
TPC 4. Mixer Conversion Gain vs. IF, T = 25°C, VPOS = 3 V, VREF = 1.5 V



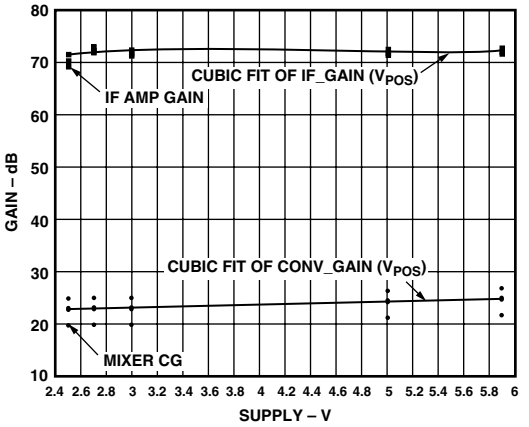
TPC 2. Mixer Input Impedance vs. Frequency, VPOS = 3 V, V GAIN = 0.8 V



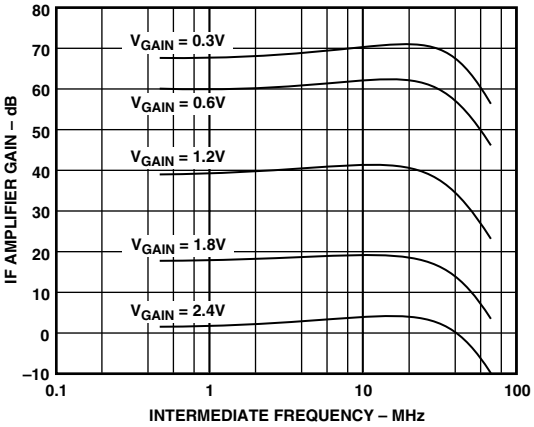
TPC 5. Mixer Conversion Gain and IF Amplifier Gain vs. Temperature, VPOS = 3 V, VGAIN = 0.3 V, VREF = 1.5 V, IF = 10.7 MHz, RF = 250 MHz



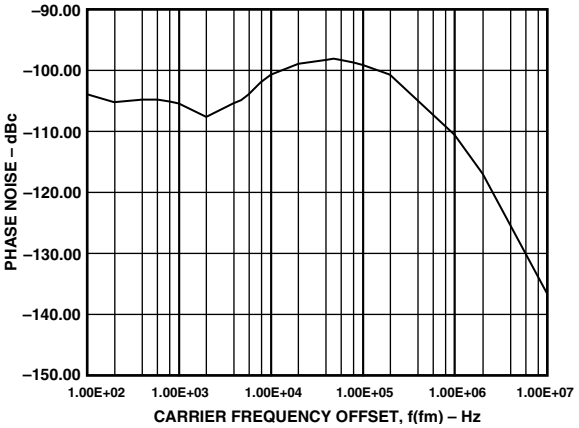
TPC 3. Mixer Conversion Gain vs. Frequency, T = 25°C, VPOS = 2.92 V, VREF = 1.35 V, IF = 10.7 MHz



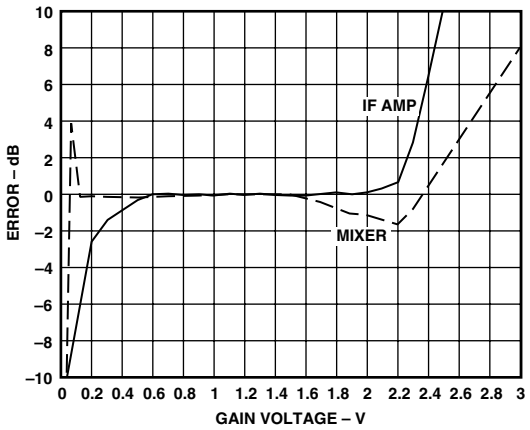
TPC 6. Mixer Conversion Gain and IF Amplifier Gain vs. Supply Voltage, T = 25°C, VGAIN = 0.3 V, VREF = 1.5 V, IF = 10.7 MHz, RF = 250 MHz



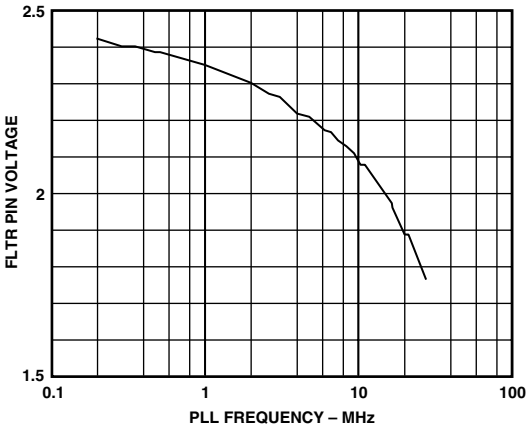
TPC 7. IF Amplifier Gain vs. Frequency, T = 25°C, VPOS = 3 V, VREF = 1.5 V



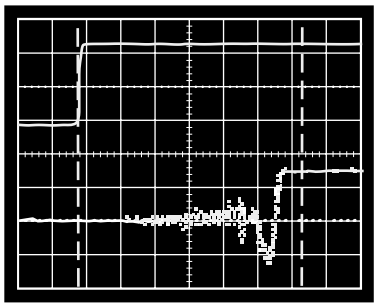
TPC 10. PLL Phase Noise L (F) vs. Frequency, VPOS = 3 V, C3 = 0.1 μF, IF = 10.7 MHz



TPC 8. Gain Error vs. Gain Control Voltage, Representative Part



TPC 11. PLL Loop Voltage at FLTR (K_{VCO}) vs. Frequency

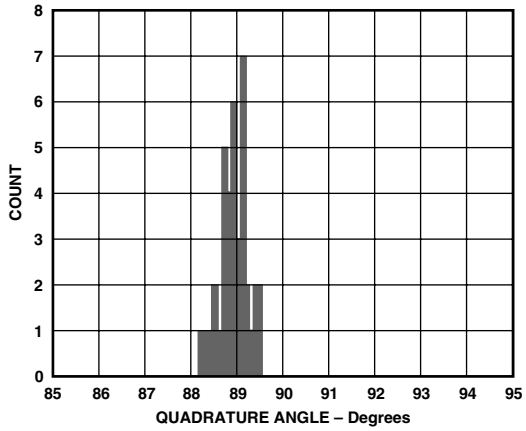


996.200μs 1.00870ms 1.02120ms

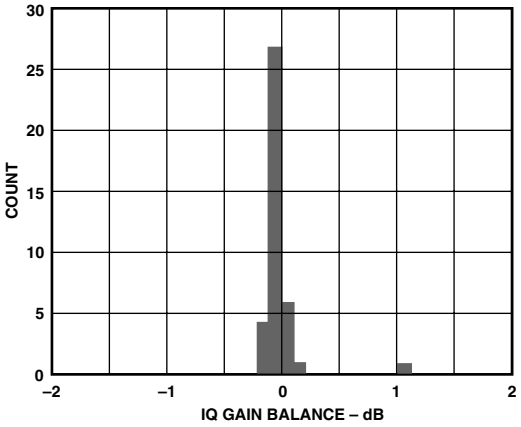
TIMEBASE	= 2.5μs/DIV	DELAY	= 1.00870ms
MEMORY 1	= 100.0mV/DIV	OFFSET	= 127.3mV
TIMEBASE	= 2.50μs/DIV	DELAY	= 1.00870ms
MEMORY 2	= 20.00mV/DIV	OFFSET	= 155.2mV
TIMEBASE	= 2.50μs/DIV	DELAY	= 1.00870ms
DELTA T	= 16.5199μs		
START	= 1.00048ms	STOP	= 1.01700ms

TRIGGER ON EXTERNAL AT POS. EDGE AT 134.0mV

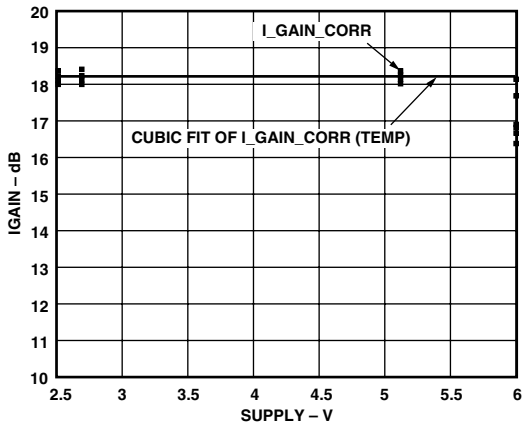
TPC 9. PLL Acquisition Time



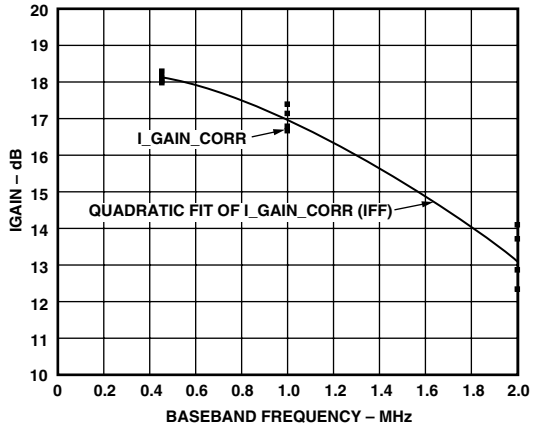
TPC 12. Demodulator Quadrature Angle, Histogram, T = 25°C, VPOS = 3 V, IF = 10.7 MHz



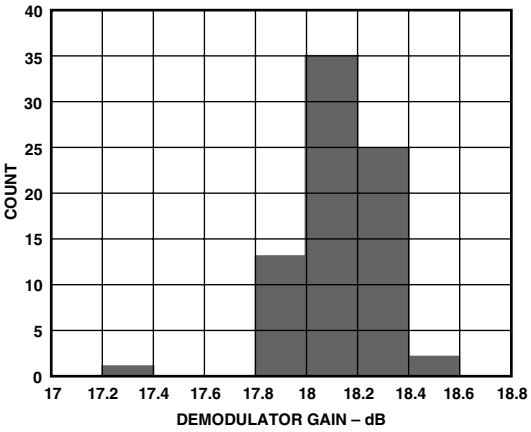
TPC 13. Demodulator Gain Balance, Histogram, T = 25°C, VPOS = 3 V, IF = 10.7 MHz



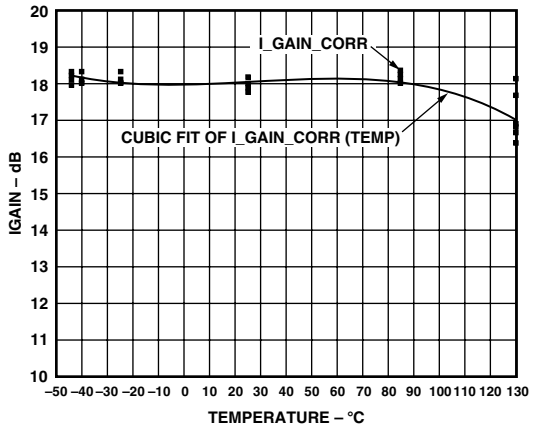
TPC 16. Demodulator Gain vs. Supply Voltage



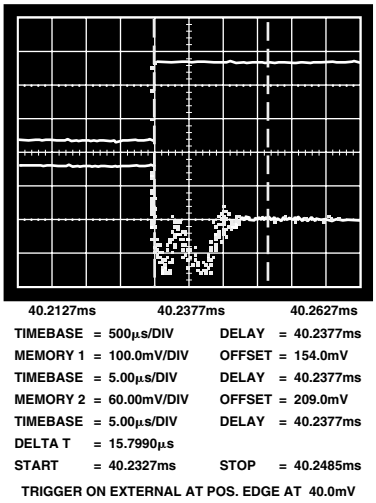
TPC 14. Demodulator Gain vs. Frequency



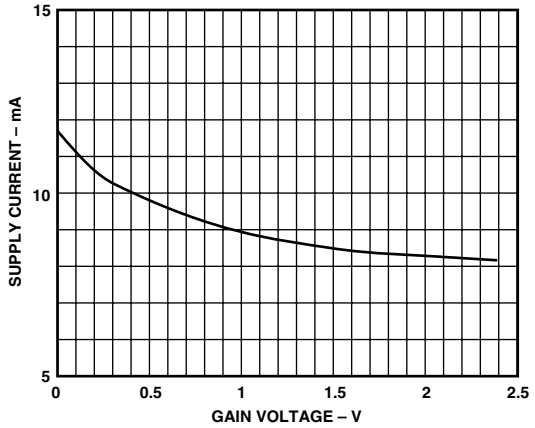
TPC 17. Demodulator Gain Histogram, T = 25°C, VPOS = 3 V, IF = 10.7 MHz



TPC 15. Demodulator Gain vs. Temperature



TPC 18. Power-Up Response Time to PLL Stable



TPC 19. Power Supply Current vs. Gain Control Voltage, GREF = 1.5 V

PRODUCT OVERVIEW

The AD607 provides most of the active circuitry required to realize a complete low power, single-conversion superheterodyne receiver, or most of a double-conversion receiver, at input frequencies up to 500 MHz, and an IF from 400 kHz to 12 MHz. The internal I/Q demodulators and their associated phase-locked loop, which can provide carrier recovery from the IF, support a wide variety of modulation modes, including n-PSK, n-QAM, and AM. A single positive supply voltage of 3 V is required (2.92 V minimum, 5.5 V maximum) at a typical supply current of 8.5 mA at midgain. In the following discussion, V_P will be used to denote the power supply voltage, which will be assumed to be 3 V.

Figure 13 shows the main sections of the AD607. It consists of a variable gain UHF mixer and linear four-stage IF strip, which together provide a voltage controlled gain range of more than 90 dB; dual demodulators, each comprising a multiplier followed by a two-pole, 2 MHz low-pass filter; and a phase-locked loop providing the inphase and quadrature clocks. A biasing system with CMOS compatible power-down completes the AD607.

Mixer

The UHF mixer is an improved Gilbert cell design, and can operate from low frequencies (it is internally dc-coupled) up to an RF input of 500 MHz. The dynamic range at the input of the mixer is determined at the upper end by the maximum input signal level of ±56 mV between RFHI and RFLO up to which the mixer remains linear, and at the lower end by the noise level. It is customary to define the linearity of a mixer in terms of the 1 dB gain-compression point and third order intercept, which for the AD607 are –15 dBm and –8 dBm, respectively, in a 50 Ω system.

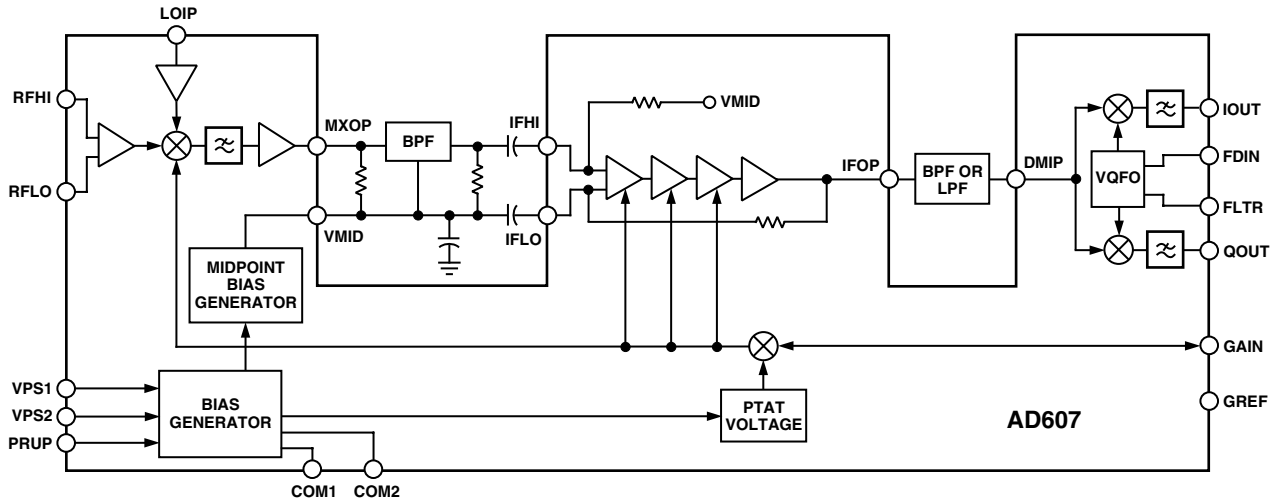


Figure 13. Functional Block Diagram

The mixer's RF input port is differential, that is, pin RFLO is functionally identical to RFHI, and these nodes are internally biased; we will generally assume that RFLO is decoupled to ac ground. The RF port can be modeled as a parallel RC circuit as shown in Figure 14.

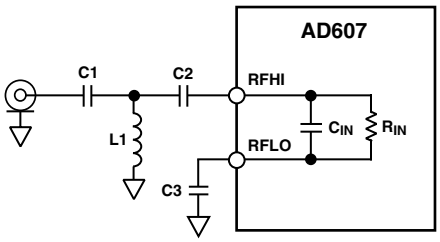


Figure 14. Mixer Port Modeled as a Parallel RC Network; an Optional Matching Network Is also Shown

The local oscillator (LO) input is internally biased at $V_P/2$ via a nominal 1000 Ω resistor internally connected from pin LOIP to VMID. The LO interface includes a preamplifier that minimizes the drive requirements, thus simplifying the oscillator design and reducing LO leakage from the RF port. Internally, this single-sided input is actually differential; the noninverting input is referenced to Pin VMID. The LO requires a single-sided drive of ±50 mV, or –16 dBm in a 50 Ω system.

The mixer's output passes through both a low-pass filter and a buffer, which provides an internal differential to single-ended signal conversion with a bandwidth of approximately 45 MHz. Its output at Pin MXOP is in the form of a single-ended current. This approach eliminates the 6 dB voltage loss of the usual series termination by replacing it with shunt terminations at both the input and the output of the filter. The nominal conversion gain is specified for operation into a total IF band-pass filter (BPF) load of 165 Ω, that is, a 330 Ω filter doubly-terminated as shown in Figure 14. Note that these loads are connected to bias point VMID, which is always at the midpoint of the supply (that is, $V_P/2$).

The conversion gain is measured between the mixer input and the input of this filter, and varies between 1.5 dB and 26.5 dB for a 165 Ω load impedance. Using filters of higher impedance, the conversion gain can always be maintained at its specified value or made even higher; for filters of lower impedance, of say Z_O, the conversion gain will be lowered by $10 \log_{10}(165/Z_O)$. Thus, the use of a 50 Ω filter will result in a conversion gain that is 5.2 dB lower. Figure 15 shows filter matching networks and Table I lists resistor values.

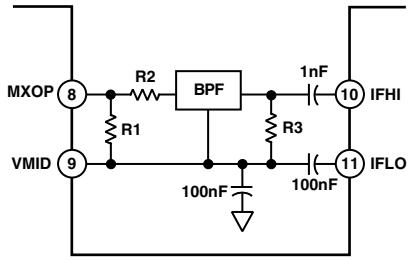


Figure 15. Suggested IF Filter Matching Network. The Values of R1 and R2 Are Selected to Keep the Impedance at Pin MXOP at 165 Ω

Table I. Filter Termination Resistor Values for Common IFs

IF	Filter Impedance	Filter Termination Resistor Values* for 24 dB of Mixer Gain		
		R1	R2	R3
450 kHz	1500 Ω	174 Ω	1330 Ω	1500 Ω
455 kHz	1500 Ω	174 Ω	1330 Ω	1500 Ω
6.5 MHz	1000 Ω	215 Ω	787 Ω	1000 Ω
10.7 MHz	330 Ω	330 Ω	0 Ω	330 Ω

*Resistor values were calculated such that R1+ R2 = Z_{FILTER} and R1‖ (R2 + Z_{FILTER}) = 165 Ω.

The maximum permissible signal level at MXOP is determined by both voltage and current limitations. Using a 3 V supply and VMID at 1.5 V, the maximum swing is about ±1.3 V. To attain a voltage swing of ±1 V in the standard IF filter load of 165 Ω requires a peak drive current of about ±6 mA, which is well within the linear capability of the mixer. However, these upper limits for voltage and current should not be confused with issues related to the mixer gain, already discussed. In an operational system, the AGC voltage will determine the mixer gain, and hence the signal level at the IF input Pin IFHI; it will always be less than ±56 mV (–15 dBm into 50 Ω), which is the limit of the IF amplifier's linear range.

IF Amplifier

Most of the gain in the AD607 arises in the IF amplifier strip, which comprises four stages. The first three are fully differential and each has a gain span of 25 dB for the nominal AGC voltage range. Thus, in conjunction with the mixer's variable gain, the total gain exceeds 90 dB. The final IF stage has a fixed gain of 20 dB, and it also provides differential to single-ended conversion.

The IF input is differential, at IFHI (noninverting relative to the output IFOP) and IFLO (inverting). Figure 16 shows a simplified schematic of the IF interface. The offset voltage of this stage would cause a large dc output error at high gain, so it is nulled by a low pass feedback path from the IF output, also shown in TPC 13. Unlike the mixer output, the signal at IFOP is a low-impedance single-sided voltage, centered at $V_P/2$ by the dc feedback loop. It may be loaded by a resistance as low as 50 Ω, which will normally be connected to VMID.

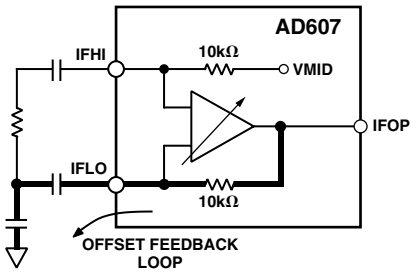
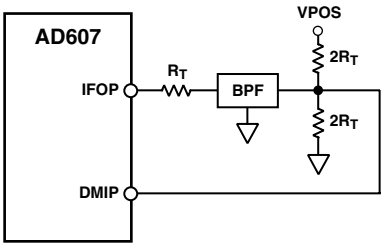


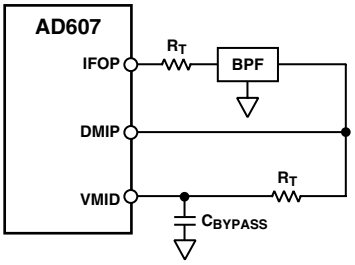
Figure 16. Simplified Schematic of the IF Interface

The IF's small-signal bandwidth is approximately 45 MHz from IFHI and IFLO through IFOP. The peak output at IFOP is ±560 mV at V_P = 3 V and ±400 mV at the minimum V_P of 2.92 V. This allows some headroom at the demodulator inputs (Pin DMIP), which accept a maximum input of ±150 mV for IFs > 3 MHz and ±75 mV for IFs ≤ 3 MHz (at IFs ≤ 3 MHz, the drive to the demodulators must be reduced to avoid saturating the output amplifiers with higher order mixing products that are no longer removed by the on-board low pass filters).

Since there is no band-limiting in the IF strip, the output-referred noise can be quite high; in a typical application and at a gain of 75 dB, it is about 100 mV rms, making post-IF filtering desirable. IFOP may be also used as an IF output for driving an A/D converter, external demodulator, or external AGC detector. Figure 17 shows methods of matching the optional second IF filter.



a. Biasing DMIP from Power Supply (Assumes BPF AC-Coupled Internally)



b. Biasing DMIP from VMID (Assumes BPF AC-Coupled Internally)

Figure 17. Input and Output Matching of the Optional Second IF Filter

Gain Scaling and RSSI

The AD607's overall gain, expressed in decibels, is linear-in-dB with respect to the AGC voltage V_G at Pin GAIN. The gain of all sections is maximum when V_G is zero, and reduces progressively up to V_G = 2.2 V (for V_P = 3 V; in general, up to a limit V_P – 0.8 V). The gain of all stages changes in parallel. The AD607 features temperature compensation of the gain scaling. The gain control scaling is proportional to the reference voltage applied to the Pin GREF. When this pin is tied to the midpoint of the supply (VMID), the scale is nominally 20 mV/dB (50 dB/V) for V_P = 3 V. Under these conditions, the lower 80 dB of gain range (mixer plus IF) corresponds to a control voltage of 0.4 V ≤ V_G ≤ 2.0 V. The final centering of this 1.6 V range depends on the insertion losses of the IF filters used. More generally, the gain scaling using these connections is V_P/150 (volts per dB), so scale becomes 33.3 mV/dB (30 dB/V) using a 5 V supply, with a proportional change in the AGC range, to 0.33 V ≤ V_G ≤ 3 V.

Table II lists gain control voltages and scale factors for power supply voltages from 2.92 V to 5.5 V

Alternatively, Pin GREF can be tied to an external voltage reference (V_R) from, for example, an AD1582 (2.5 V) or AD1580 (1.21 V) voltage reference, to provide supply-independent gain scaling of V_R/75 (volts per dB). When using the Analog Devices' AD7013 and AD7015 baseband converters, the external reference may also be provided by the reference output of the baseband converter (Figure 18). For example, the AD7015 baseband converter provides a V_R of 1.23 V; when connected to GREF, the gain scaling is 16.4 mV/dB (60 dB/V). An auxiliary DAC in the AD7015 can be used to generate the MGC voltage. Since it uses the same reference voltage, the numerical input to this DAC provides an accurate RSSI value in digital form, no longer requiring the reference voltage to have high absolute accuracy.

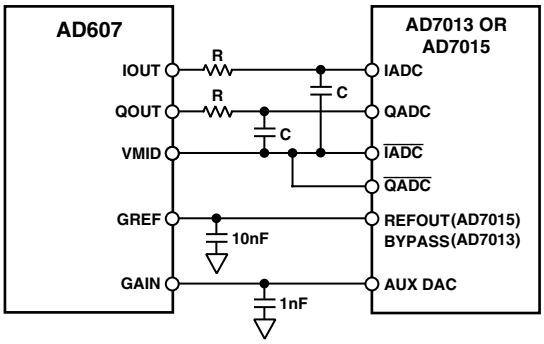
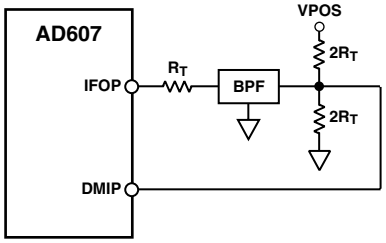


Figure 18. Interfacing the AD607 to the AD7013 or AD7015 Baseband Converters

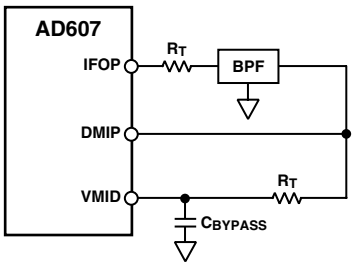
I/Q Demodulators

Both demodulators (I and Q) receive their inputs at Pin DMIP. Internally, this single-sided input is actually differential; the noninverting input is referenced to Pin VMID. Each demodulator comprises a full-wave synchronous detector followed by a 2 MHz, two-pole low-pass filter, producing single-sided outputs at pins IOUT and QOUT. Using the I and Q demodulators for IFs above 12 MHz is precluded by the 400 kHz to 12 MHz response of the PLL used in the demodulator section. Pin DMIP requires an external bias source at V_P/2; Figure 19 shows suggested methods.

Outputs IOUT and QOUT are centered at V_P/2 and can swing up to ±1.23 V even at the low supply voltage of 2.92 V. They can therefore directly drive the RX ADCs in the AD7015 baseband converter, which require an amplitude of 1.23 V to fully load them when driven by a single-sided signal. The conversion gain of the I and Q demodulators is 18 dB (X8), requiring a maximum input amplitude at DMIP of ±150 mV for IFs > 3 MHz.



a. Biasing DMIP from Power Supply (Assumes BPF AC-Coupled Internally)



b. Biasing DMIP from VMID (Assumes BPF AC-Coupled Internally)

Figure 19. Suggested Methods for Biasing Pin DMIP at $V_P/2$

For IFs < 3 MHz, the on-chip low-pass filters (2 MHz cutoff) do not attenuate the IF or feedthrough products. Thus, the maximum input voltage at DMIP must be limited to ±75 mV to allow sufficient headroom at the I and Q outputs for not only the desired baseband signal, but also the unattenuated higher-order demodulation products. These products can be removed by an external low-pass filter. In the case of IS54 applications using a 455 kHz IF and the AD7013 baseband converter, a simple one-pole RC filter with its corner above the modulation bandwidth is sufficient to attenuate undesired outputs.

Phase-Locked Loop

The demodulators are driven by quadrature signals that are provided by a variable frequency quadrature oscillator (VFQO), phase-locked to a reference signal applied to Pin FDIN. When this signal is at the IF, in-phase and quadrature baseband outputs are generated at IOUT and QOUT, respectively. The quadrature accuracy of this VFQO is typically –1.2°C at 10.7 MHz. The PLL uses a sequential-phase detector that comprises low power emitter-coupled logic and a charge pump (Figure 20).

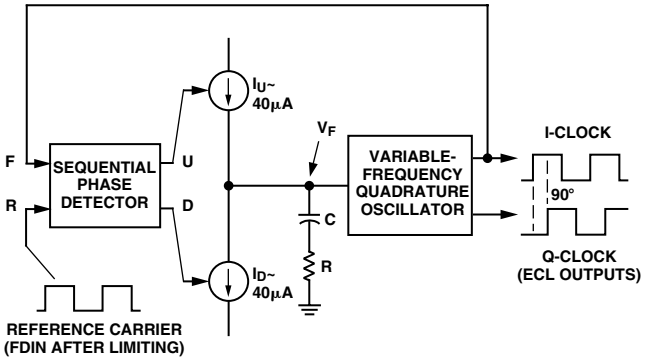


Figure 20. Simplified Schematic of the PLL and Quadrature VCO

The reference signal may be provided from an external source in the form of a high level clock, typically a low level signal (±400 mV) since there is an input amplifier between FDIN and the loop's phase detector. For example, the IF output itself can be used by connecting DMIP to FDIN, which will then provide automatic carrier recover for synchronous AM detection and take advantage of any post-IF filtering. Pin FDIN must be biased at $V_P/2$; Figure 22 shows suggested methods.

The VFQO operates from 400 kHz to 12 MHz and is controlled by the voltage between VPOS and FLTR. In normal operation, a series RC network forming the PLL loop filter is connected from FLTR to ground. The use of an integral sample-hold system ensures that the frequency-control voltage on Pin FLTR remains held during power-down, so reacquisition of the carrier typically occurs in 16.5 μs.

In practice, the probability of a phase mismatch at power-up is high, so the worst-case linear settling period to full lock needs to be considered in making filter choices. This is typically 16.5 μs at an IF of 10.7 MHz for a ±100 mV signal at DMIP and FDIN.

Table II. AD607 Gain and Manual Gain Control Voltage vs. Power Supply Voltage

Power Supply Voltage (V)	GREF (= VMID) (V)	Scale Factor (dB/V)	Scale Factor (mV/dB)	Gain Control Voltage Input Range (V)
3.0	1.5	50.00	20.00	0.400–2.000
3.5	1.75	42.86	23.33	0.467–2.333
4.0	2.0	37.50	26.67	0.533–2.667
4.5	2.25	33.33	30.00	0.600–3.000
5.0	2.5	30.00	33.33	0.667–3.333
5.5	2.75	27.27	36.67	0.733–3.667

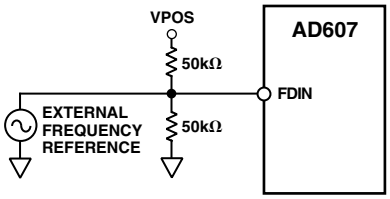
Maximum gain occurs for gain control voltage = 0 V.

Bias System

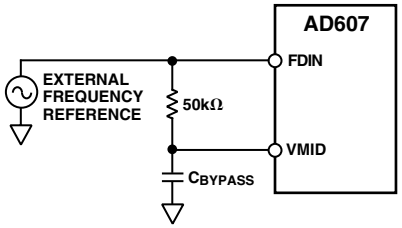
The AD607 operates from a single supply, V_P, usually of 3 V, at a typical supply current of 8.5 mA at midgain and T = 27°C, corresponding to a power consumption of 25 mW. Any voltage from 2.92 V to 5.5 V may be used.

The bias system includes a fast-acting active-high CMOS-compatible power-up switch, allowing the part to idle at 550 µA when disabled. Biasing is proportional-to-absolute temperature (PTAT) to ensure stable gain with temperature.

An independent regulator generates a voltage at the midpoint of the supply ($V_P/2$) that appears at the VMID pin at a low impedance. This voltage does not shut down, ensuring that the major signal interfaces (e.g., mixer-to-IF and IF-to-demodulators) remain biased at all times, thus minimizing transient disturbances at power-up and allowing the use of substantial decoupling capacitors on this node. The quiescent consumption of this regulator is included in the idling current.



a. Biasing FDIN from Supply when Using External Frequency Reference



b. Biasing FDIN from VMID when Using External Frequency Reference

Figure 21. Suggested Methods for Biasing Pin FDIN at $V_P/2$

USING THE AD607

In this section, we will focus on a few areas of special importance and include a few general application tips. As is true of any wideband high gain component, great care is needed in PC board layout. The location of the particular grounding points must be considered with due regard to the possibility of unwanted signal coupling, particularly from IFOP to RFHI or IFHI or both.

The high sensitivity of the AD607 leads to the possibility that unwanted local EM signals may have an effect on the performance. During system development, carefully-shielded test assemblies should be used. The best solution is to use a fully-enclosed box enclosing all components, with the minimum number of needed signal connectors (RF, LO, I, and Q outputs) in miniature coax form.

The I and Q output leads can include small series resistors (about 100 Ω) inside the shielded box without significant loss of performance, provided the external loading during testing is light (that is, a resistive load of more than 20 kΩ and capacitances of a few picofarads). These help to keep unwanted RF emanations out of the interior.

The power supply should be connected via a through-hole capacitor with a ferrite bead on both inside and outside leads. Close to the IC pins, two capacitors of different value should be used to decouple the main supply (V_P) and the midpoint supply pin, VMID. Guidance on these matters is also generally included in applications schematics.

Gain Distribution

As in all receivers, the most critical decisions in effectively using the AD607 relate to the partitioning of gain between the various subsections (Mixer, IF Amplifier, Demodulators) and the placement of filters so as to achieve the highest overall signal-to-noise ratio and lowest intermodulation distortion.

Figure 22 shows the main RF/IF signal path at maximum and minimum signal levels.

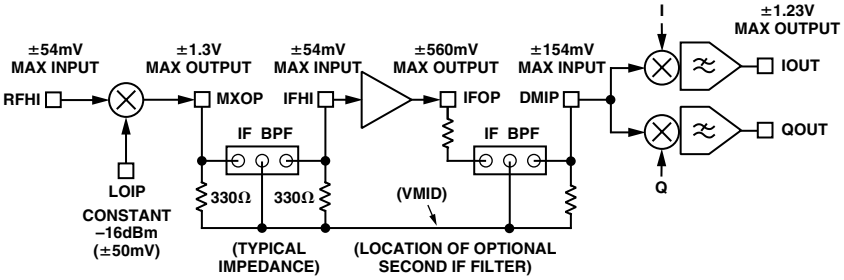


Figure 22. Signal Levels for Minimum and Maximum Gain

As noted earlier, the gain in dB is reduced linearly with the voltage V_G on the GAIN pin. Figure 23 shows how the mixer and IF strip gains vary with V_G when GREF is connected to VMID (1.5 V) and a supply voltage of 3 V is used. Figure 24 shows how these vary when GREF is connected to a 1.23 V reference.

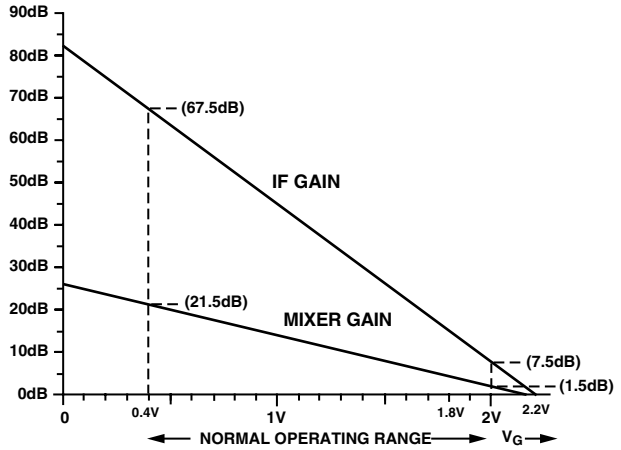


Figure 23. Gain Distribution for GREF = 1.5 V

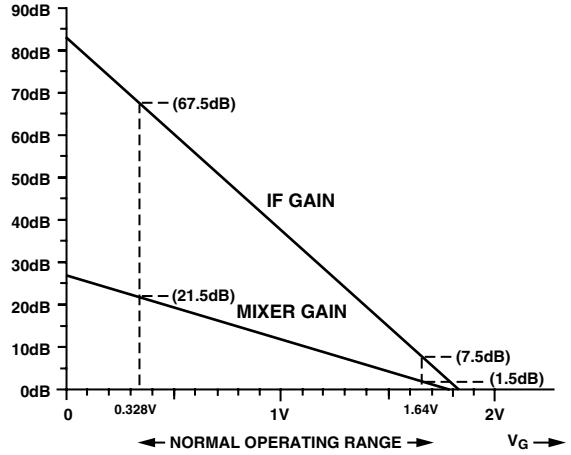


Figure 24. Gain Distribution for GREF = 1.23 V

Using the AD607 with a Fast PRUP Control Signal

If the AD607 is used in a system in which the PRUP signal (Pin 3) is applied with a rise time less than 35 µs, anomalous behavior occasionally occurs. The problem is intermittent, so it will not occur every time the part is powered up under these conditions. It does not occur for any other normal operating conditions when the PRUP signal has a rise time slower than 35 µs. Symptoms of operation with too fast a PRUP signal include low gain, oscillations at the I or Q outputs of the device, or no valid data occurring at the output of the AD607. The problem causes no permanent damage to the AD607, so it will often operate normally when reset.

Fortunately, there is a very simple solution to the fast PRUP problem. If the PRUP signal (Pin 3) is slowed down so that the rise time of the signal edge is greater than 35 µs, the anomalous behavior will not occur. This can be realized by a simple RC circuit connected to the PRUP pin, where R = 4.7 kΩ and C = 1.5 nF. This circuit is shown in Figure 25.

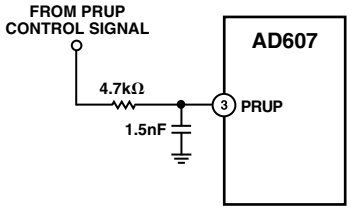


Figure 25. Proper Configuration of AD607 PRUP Signal

All designs incorporating the AD607 should include this circuitry.

Note that connecting the PRUP pin to the supply voltage will not eliminate the problem, since the supply voltage may have a rise time faster than 35 µs. With this configuration, the 4.7 kΩ series R and 1.5 nF shunt C should be placed between the supply and the PRUP pin as shown in Figure 25.

AD607 EVALUATION BOARD

The AD607 evaluation board (Figures 26 and 27) consists of an AD607, ground plane, I/O connectors, and a 10.7 MHz bandpass filter. The RF and LO ports are terminated in 50 Ω to provide a broadband match to external signal generators to allow a choice of RF and LO input frequencies. The IF filter is at 10.7 MHz and has 330 Ω input and output terminations; the board is laid out to allow the user to substitute other filters for other IFs.

The board provides SMA connectors for the RF and LO port inputs, the demodulated I and Q outputs, the manual gain control (MGC) input, the PLL input, and the power-up input. In addition, the IF output is also available at an SMA connector; this may be connected to the PLL input for carrier recovery to realize synchronous AM and FM detection via the I and Q demodulators, respectively. Table III lists the AD607 Evaluation Board's I/O Connectors and their functions.

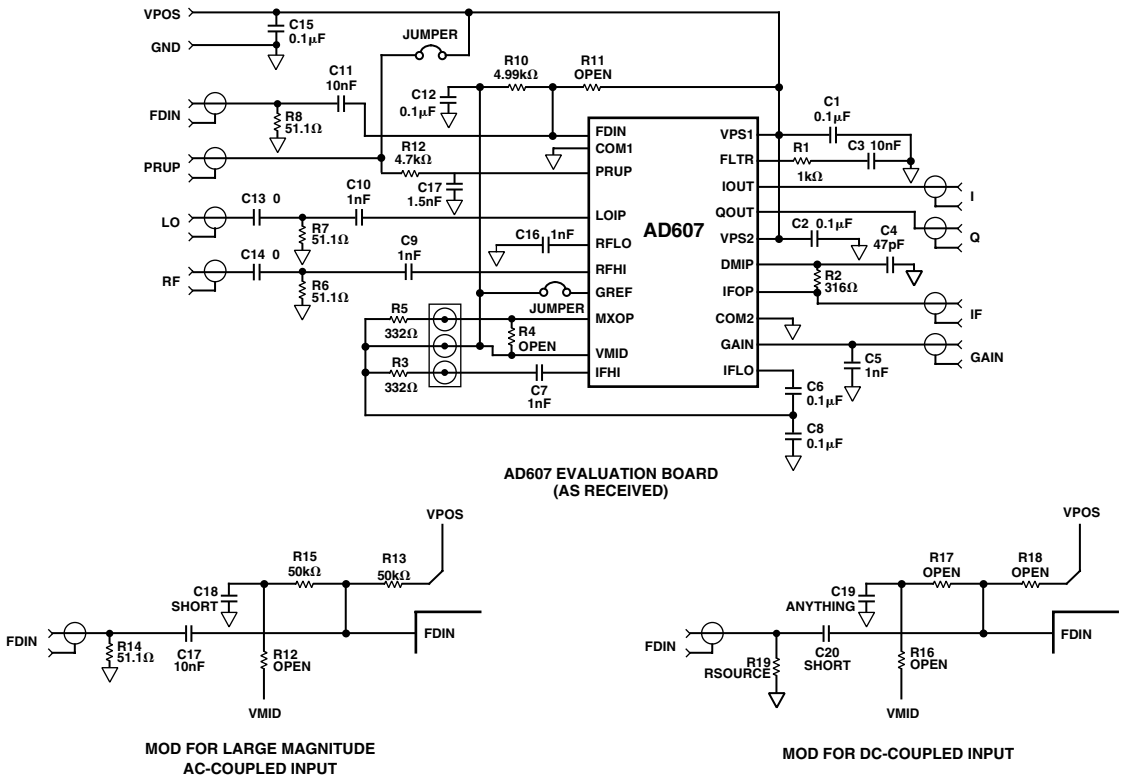


Figure 26. Evaluation Board

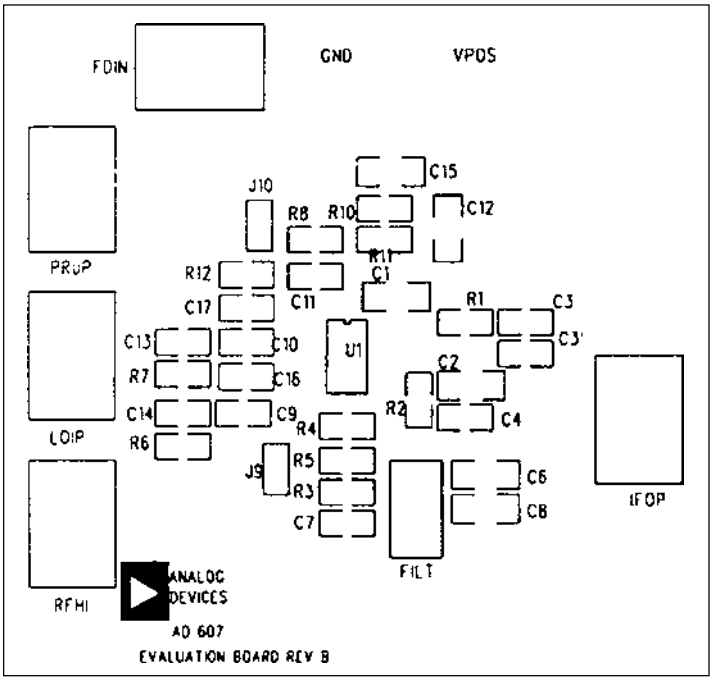


Figure 27a. Evaluation Board Layout, Topside

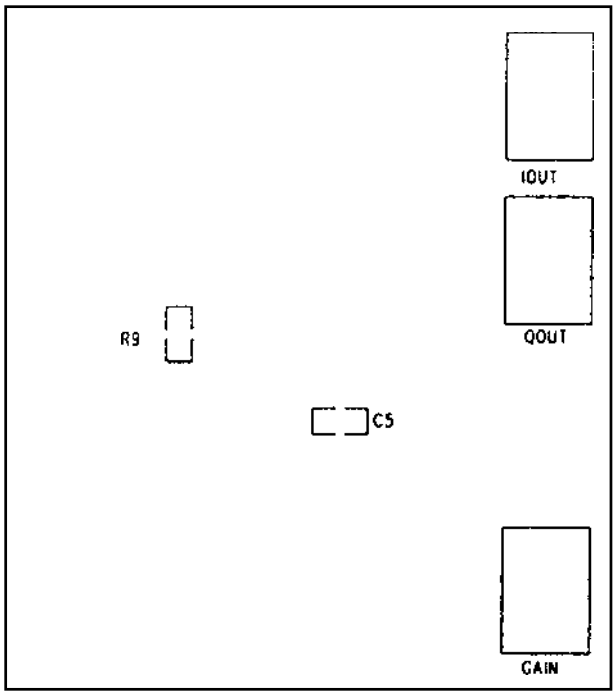


Figure 27b. Evaluation Board Layout, Bottom Side

Table III. AD607 Evaluation Board Input and Output Connections

Reference Designation	Connector Type	Description	Coupling	Approximate Signal Level	Comments
J1	SMA	Frequency Detector Input	DC	±400 mV	This pin needs to be biased at VMID and ac-coupled when driven by an external signal generator.
J2	SMA	Power-Up	DC	CMOS Logic Level Input	Tied to Positive Supply by Jumper J10
J3	SMA	LO Input	AC	–16 dBm (±50 mV)	Input is terminated in 50 Ω.
J4	SMA	RF Input	AC	–15 dBm max (±54 mV)	Input is terminated in 50 Ω.
J5	SMA	MGC Input	DC	0.4 V to 2.0 V (3 V Supply) (GREF = VMID)	Jumper is set for manual gain control input; see Table I for control voltage values.
J6	SMA	IF Output	AC	NA	This signal level depends on the AD607's gain setting.
J7	SMA	Q Output	AC	NA	This signal level depends on the AD607's gain setting.
J8	SMA	I Output	AC	NA	This signal level depends on the AD607's gain setting.
J9	Jumper	Ties GREF to VMID	NA	NA	Sets gain-control scale factor (SF); SF = 75/VMID in dB/V, where VMID = VPOS/2.
J10	Jumper	Ties Power-Up to Positive Supply	NA	NA	Remove to test power-up/-down.
T1	Terminal Pin	Power Supply Positive Input (VPS1, VPS2)	DC	DC	2.92 V to 5.5 V Draws 8.5 mA at midgain connection.
T2	Terminal Pin	Power Supply Return (GND)	DC	0 V	

In operation (Figure 28), the AD607 evaluation board draws about 8.5 mA at midgain (59 dB). Use high impedance probes to monitor signals from the demodulated I and Q outputs and the IF output. The MGC voltage should be set such that the signal level at DMIP does not exceed ±150 mV; signal levels above this will overload the I and Q demodulators. The insertion loss between IFOP and DMIP is typically 3 dB if a simple low-pass filter (R8 and C2) is used, and higher if a reverse-terminated band-pass filter is used.

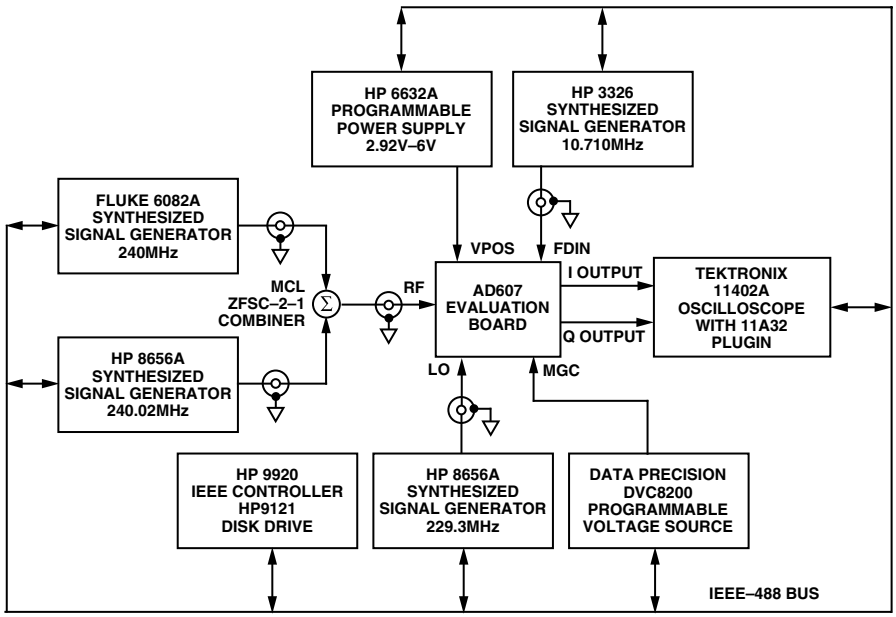
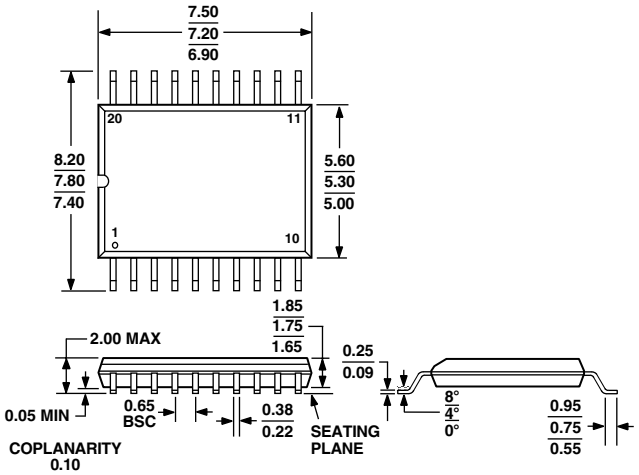


Figure 28. Evaluation Board Test Setup

OUTLINE DIMENSIONS

20-Lead Shrink Small Outline Package [SSOP] (RS-20)

Dimensions shown in millimeters



Revision History

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Edits to SPECIFICATIONS	2
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