



Complete Quad, 16-Bit, High Accuracy, Serial Input, Bipolar Voltage Output DAC

Enhanced Product

AD5764-EP

FEATURES

Complete quad, 16-bit digital-to-analog converter (DAC)
Programmable output range: ± 10 V, ± 10.2564 V, or ± 10.5263 V
 ± 2 LSB maximum INL error, ± 1 LSB maximum DNL error
Low noise: 60 nV/ $\sqrt{\text{Hz}}$
Settling time: 10 μs maximum
Integrated reference buffers
Output control during power-up/brownout
Programmable short-circuit protection
Simultaneous updating via $\overline{\text{LDAC}}$
Asynchronous $\overline{\text{CLR}}$ to zero code
Digital offset and gain adjust
Logic output control pins
DSP-/microcontroller-compatible serial interface
Temperature range: -55°C to $+105^{\circ}\text{C}$
iCMOS process technology¹

ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications (AQEC standard)
Extended temperature range: -55°C to $+105^{\circ}\text{C}$
Controlled manufacturing baseline
One assembly/test site
One fabrication site
Enhanced product change notification
Qualification data available on request

APPLICATIONS

Industrial automation
Open-loop/closed-loop servo control
Process control
Data acquisition systems
Automatic test equipment
Automotive test and measurement
High accuracy instrumentation

GENERAL DESCRIPTION

The [AD5764-EP](#) is a quad, 16-bit, serial input, bipolar voltage output DAC that operates from supply voltages of ± 11.4 V to ± 16.5 V. The nominal full-scale output range is ± 10 V. The [AD5764-EP](#) provides integrated output amplifiers, reference buffers, and proprietary power-up/power-down control circuitry. The device also features a digital I/O port that is programmed via the serial interface. The [AD5764-EP](#) incorporates digital offset and gain adjust registers per channel.

The [AD5764-EP](#) is a high performance converter that offers guaranteed monotonicity, integral nonlinearity (INL) of ± 2 LSB, low noise, and 10 μs settling time. During power-up (when the supply voltages are changing), VOUTx is clamped to 0 V via a low impedance path.

The [AD5764-EP](#) uses a serial interface that operates at clock rates of up to 30 MHz and is compatible with DSP and microcontroller interface standards. Double buffering allows the simultaneous updating of all DACs. The input coding is programmable to either twos complement or offset binary format. The asynchronous clear function clears the data register to either bipolar zero or zero scale depending on the coding used. The [AD5764-EP](#) is ideal for both closed-loop servo control and open-loop control applications. The [AD5764-EP](#) is available in a 32-lead TQFP and offers guaranteed specifications over the -55°C to $+105^{\circ}\text{C}$ industrial temperature range. See Figure 1 for the functional block diagram.

Additional application and technical information can be found in the [AD5764](#) data sheet.

Table 1. Related Devices

Part No.	Description
AD5764R	AD5764 with internal voltage reference
AD5744R	Complete quad, 14-bit, high accuracy, serial input, bipolar voltage output DAC with internal voltage reference

¹ For analog systems designers within industrial/instrumentation equipment OEMs who need high performance ICs at higher voltage levels, iCMOS® is a technology platform that enables the development of analog ICs capable of 30 V and operating at ± 15 V supplies, allowing dramatic reductions in power consumption and package size, and increased ac and dc performance.

Rev. 0

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TABLE OF CONTENTS

Features	1	Timing Characteristics	6
Enhanced Product Features	1	Absolute Maximum Ratings	9
Applications.....	1	ESD Caution.....	9
General Description	1	Pin Configuration and Function Descriptions.....	10
Revision History	2	Typical Performance Characteristics	12
Functional Block Diagram	3	Outline Dimensions	17
Specifications.....	4	Ordering Guide	17
AC Performance Characteristics	5		

REVISION HISTORY

12/13—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

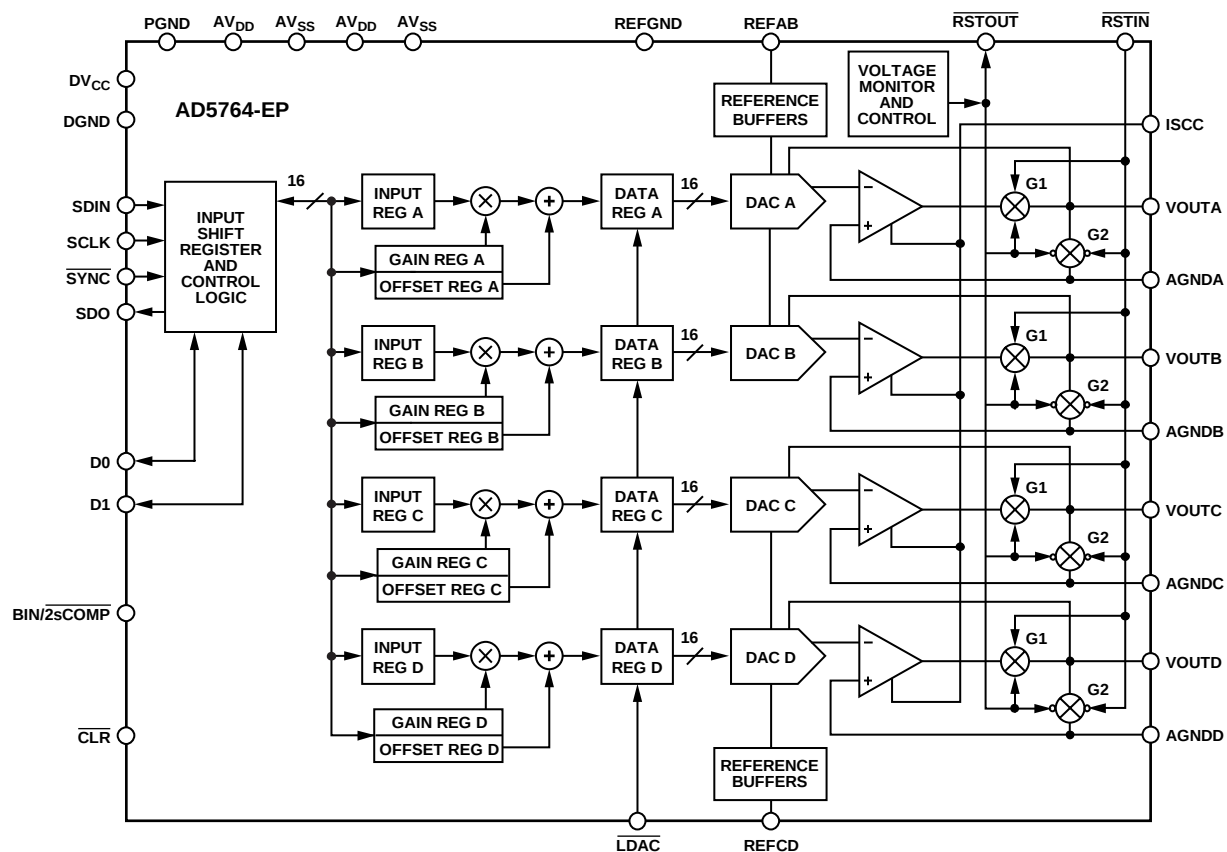


Figure 1.

SPECIFICATIONS

$AV_{DD} = 11.4\text{ V to }16.5\text{ V}$, $AV_{SS} = -11.4\text{ V to }-16.5\text{ V}$, $AGND_x = DGND = REFGND = PGND = 0\text{ V}$; $REFAB = REFCD = 5\text{ V}$;
 $DV_{CC} = 2.7\text{ V to }5.25\text{ V}$, $R_{LOAD} = 10\text{ k}\Omega$, $C_{LOAD} = 200\text{ pF}$. Temperature range: $-55^\circ\text{C to }+105^\circ\text{C}$; typical at $+25^\circ\text{C}$. All specifications
 T_{MIN} to T_{MAX} , unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY					Outputs unloaded
Resolution	16			Bits	
Relative Accuracy (INL)			± 2	LSB	
Differential Nonlinearity (DNL)			± 1	LSB	Guaranteed monotonic
Bipolar Zero Error			± 2	mV	At 25°C ; error at other temperatures obtained using bipolar zero TC
Bipolar Zero Temperature Coefficient (TC) ¹			± 2	ppm FSR/ $^\circ\text{C}$	
Zero-Scale Error			± 3	mV	At 25°C ; error at other temperatures obtained using zero-scale TC
Zero-Scale TC ¹			± 2	ppm FSR/ $^\circ\text{C}$	
Gain Error			± 0.02	% FSR	At 25°C ; error at other temperatures obtained using gain TC
Gain TC ¹			± 2	ppm FSR/ $^\circ\text{C}$	
DC Crosstalk ¹			0.5	LSB	
REFERENCE INPUT ¹					
Reference Input Voltage		5		V	$\pm 1\%$ for specified performance
DC Input Impedance	1			M Ω	Typically 100 M Ω
Input Current			± 10	μA	Typically $\pm 30\text{ nA}$
Reference Range	1		7	V	
OUTPUT CHARACTERISTICS ¹					
Output Voltage Range ²	-10.5263 -14		$+10.5263$ $+14$	V V	$AV_{DD}/AV_{SS} = \pm 11.4\text{ V}$, $V_{REFIN} = 5\text{ V}$ $AV_{DD}/AV_{SS} = \pm 16.5\text{ V}$, $V_{REFIN} = 7\text{ V}$
Output Voltage Drift vs. Time		± 13 ± 15		ppm FSR/ 500 hours ppm FSR/ 1000 hours	
Short-Circuit Current		10		mA	$R_{ISCC} = 6\text{ k}\Omega$; see Figure 31
Load Current			± 1	mA	For specified performance
Capacitive Load Stability					
$R_{LOAD} = \infty$			200	pF	
$R_{LOAD} = 10\text{ k}\Omega$			1000	pF	
DC Output Impedance			0.3	Ω	
DIGITAL INPUTS					$DV_{CC} = 2.7\text{ V to }5.25\text{ V}$, JEDEC compliant
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}			0.8	V	
Input Current			± 1	μA	Per pin
Pin Capacitance			10	pF	Per pin
DIGITAL OUTPUTS (D0, D1, SDO) ¹					
Output Low Voltage, V_{OL}			0.4	V	$DV_{CC} = 5\text{ V} \pm 5\%$, sinking 200 μA
			0.4	V	$DV_{CC} = 2.7\text{ V to }3.6\text{ V}$, sinking 200 μA
Output High Voltage, V_{OH}	$DV_{CC} - 1$ $DV_{CC} - 0.5$			V V	$DV_{CC} = 5\text{ V} \pm 5\%$, sourcing 200 μA $DV_{CC} = 2.7\text{ V to }3.6\text{ V}$, sourcing 200 μA
High Impedance Leakage Current			± 1	μA	SDO only
High Impedance Output Capacitance		5		pF	SDO only

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
AV_{DD}/AV_{SS}	± 11.4		± 16.5	V	
DV_{CC}	2.7		5.25	V	
Power Supply Sensitivity ¹					
$\Delta V_{OUT}/\Delta AV_{DD}$		-85		dB	
AI_{DD}			3.75	mA/channel	Outputs unloaded
AI_{SS}			-3	mA/channel	Outputs unloaded
DI_{CC}			1.4	mA	$V_{IH} = DV_{CC}$, $V_{IL} = DGND$, 750 μ A typical
Power Dissipation		275		mW	± 12 V operation, output unloaded

¹ Guaranteed by design and characterization; not production tested.

² Output amplifier headroom requirement is 1.4 V minimum.

AC PERFORMANCE CHARACTERISTICS

$AV_{DD} = 11.4$ V to 16.5 V, $AV_{SS} = -11.4$ V to -16.5 V, $AGND_x = DGND = REFGND = PGND = 0$ V; $REFAB = REFCD = 5$ V; $DV_{CC} = 2.7$ V to 5.25 V, $R_{LOAD} = 10$ k Ω , $C_{LOAD} = 200$ pF. All specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE¹					
Output Voltage Settling Time		8	10	μ s	Full-scale step to ± 1 LSB
		2		μ s	512 LSB step settling
Slew Rate		5		V/ μ s	
Digital-to-Analog Glitch Energy		8		nV-sec	
Glitch Impulse Peak Amplitude			37	mV p-p	
Channel-to-Channel Isolation		80		dB	
DAC-to-DAC Crosstalk		8		nV-sec	
Digital Crosstalk		2		nV-sec	
Digital Feedthrough		2		nV-sec	Effect of input bus activity on DAC outputs
Output Noise					
0.1 Hz to 10 Hz		0.1		LSB p-p	
0.1 Hz to 100 kHz			45	μ V rms	
1/f Corner Frequency		1		kHz	
Output Noise Spectral Density		60		nV/ $\sqrt{\text{Hz}}$	Measured at 10 kHz
Complete System Output Noise Spectral Density ²		80		nV/ $\sqrt{\text{Hz}}$	Measured at 10 kHz

¹ Guaranteed by design and characterization; not production tested.

² Includes noise contributions from integrated reference buffers, 16-bit DAC, and output amplifier.

TIMING CHARACTERISTICS

$AV_{DD} = 11.4\text{ V to }16.5\text{ V}$, $AV_{SS} = -11.4\text{ V to }-16.5\text{ V}$, $AGND_x = DGND = REFGND = PGND = 0\text{ V}$; $REFAB = REFCD = 5\text{ V}$; $DV_{CC} = 2.7\text{ V to }5.25\text{ V}$, $R_{LOAD} = 10\text{ k}\Omega$, $C_{LOAD} = 200\text{ pF}$. All specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 4.

Parameter ^{1, 2, 3}	Limit at T_{MIN} , T_{MAX}	Unit	Description
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK high time
t_3	13	ns min	SCLK low time
t_4	13	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5^4	13	ns min	24 th SCLK falling edge to $\overline{SYNC}$ rising edge
t_6	90	ns min	Minimum $\overline{SYNC}$ high time
t_7	2	ns min	Data setup time
t_8	9	ns min	Data hold time
t_9	1.7	$\mu\text{s min}$	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (all DACs updated)
	480	ns min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (single DAC updated)
t_{10}	17	ns min	$\overline{LDAC}$ pulse width low
t_{11}	500	ns max	$\overline{LDAC}$ falling edge to DAC output response time
t_{12}	10	$\mu\text{s max}$	DAC output settling time
t_{13}	17	ns min	$\overline{CLR}$ pulse width low
t_{14}	2	$\mu\text{s max}$	$\overline{CLR}$ pulse activation time
$t_{15}^{5, 6}$	25	ns max	SCLK rising edge to SDO valid
t_{16}	13	ns min	$\overline{SYNC}$ rising edge to SCLK falling edge
t_{17}	2	$\mu\text{s max}$	$\overline{SYNC}$ rising edge to DAC output response time ($\overline{LDAC} = 0$)
t_{18}	170	ns min	$\overline{LDAC}$ falling edge to $\overline{SYNC}$ rising edge

¹ Guaranteed by design and characterization; not production tested.

² All input signals are specified with $t_R = t_F = 5\text{ ns}$ (10% to 90% of DV_{CC}) and timed from a voltage level of 1.2 V.

³ See Figure 3, Figure 4, and Figure 5.

⁴ Standalone mode only.

⁵ Measured with the load circuit of Figure 2.

⁶ Daisy-chain mode only.

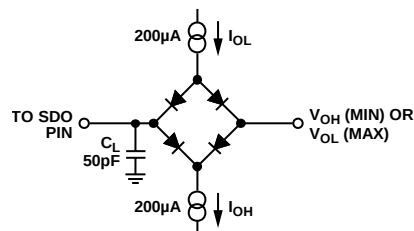
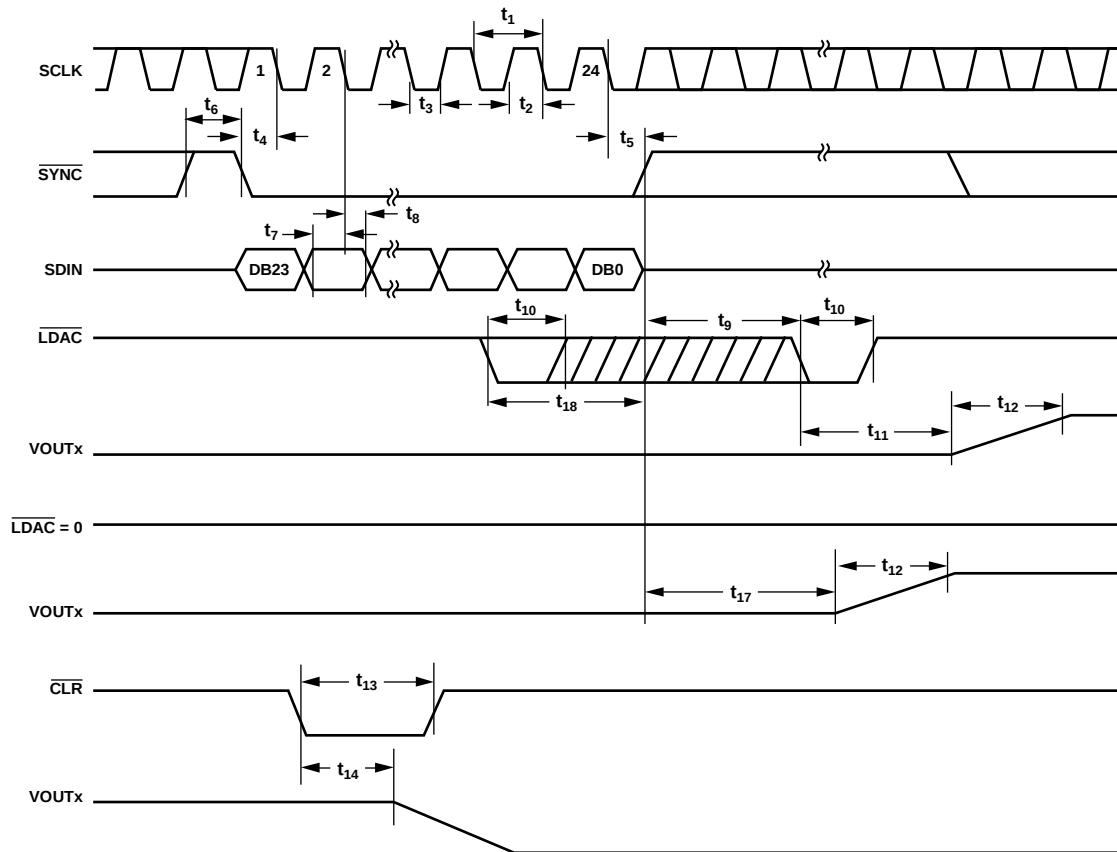


Figure 2. Load Circuit for SDO Timing Diagram

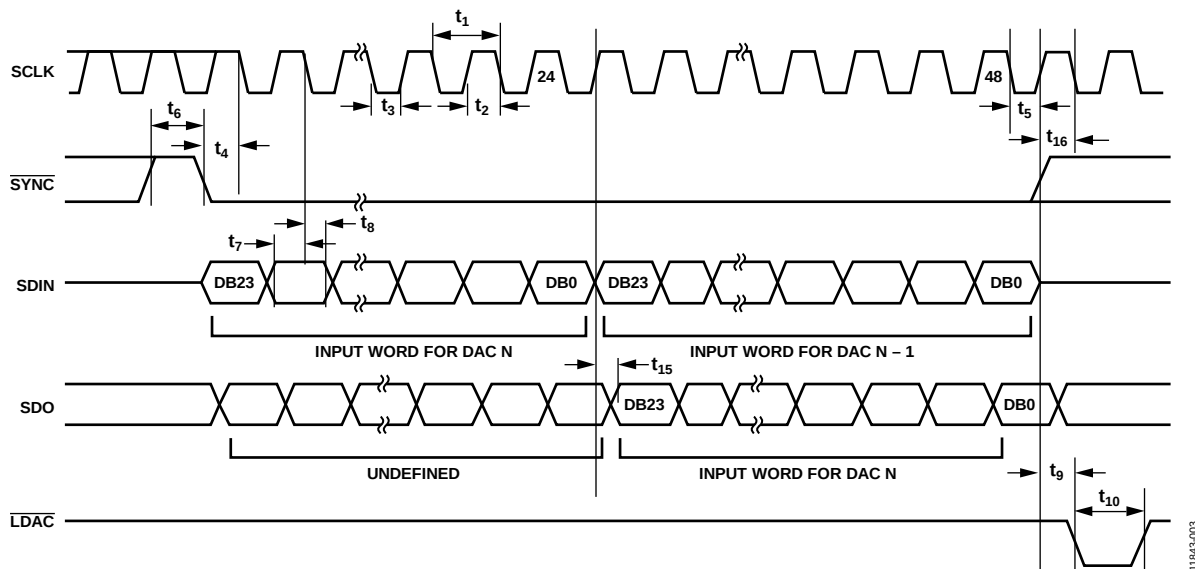
11843-005

Timing Diagrams



11843-002

Figure 3. Serial Interface Timing Diagram



11843-003

Figure 4. Daisy-Chain Timing Diagram

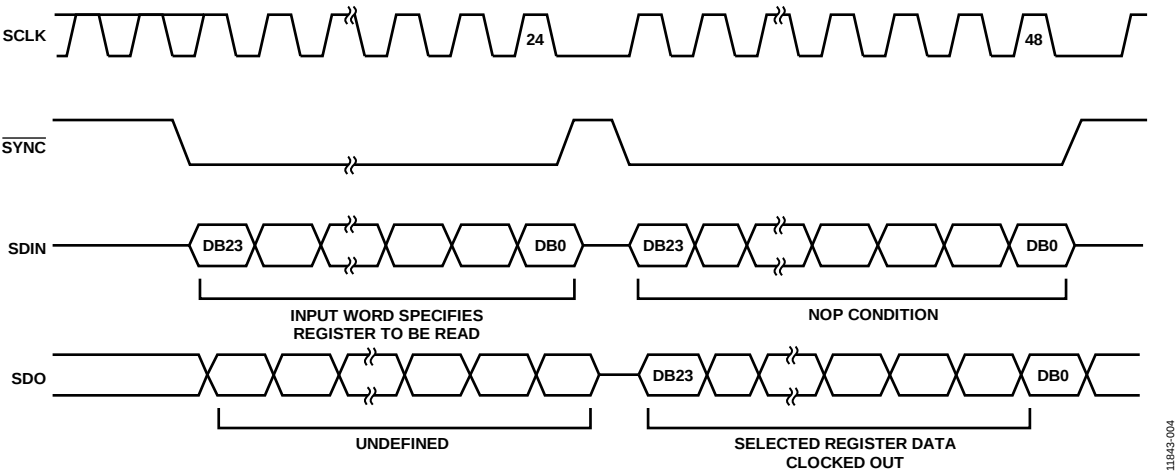


Figure 5. Readback Timing Diagram

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 5.

Parameter	Rating
AV_{DD} to AGNDx, DGND	$-0.3\text{ V to }+17\text{ V}$
AV_{SS} to AGNDx, DGND	$+0.3\text{ V to }-17\text{ V}$
DV_{CC} to DGND	$-0.3\text{ V to }+7\text{ V}$
Digital Inputs to DGND	$-0.3\text{ V to }DV_{CC} + 0.3\text{ V}$ or 7 V (whichever is less)
Digital Outputs to DGND	$-0.3\text{ V to }DV_{CC} + 0.3\text{ V}$
REFAB, REFCD to AGNDx, PGND	$-0.3\text{ V to }AV_{DD} + 0.3\text{ V}$
VOUTA, VOUTB, VOUTC, VOUTD to AGNDx	AV_{SS} to AV_{DD}
AGNDx to DGND	$-0.3\text{ V to }+0.3\text{ V}$
Operating Temperature Range Industrial	$-55^\circ\text{C to }+105^\circ\text{C}$
Storage Temperature Range	$-65^\circ\text{C to }+150^\circ\text{C}$
Junction Temperature (T_J max)	150°C
32-Lead TQFP	
θ_{JA} Thermal Impedance	65°C/W
θ_{JC} Thermal Impedance	12°C/W
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

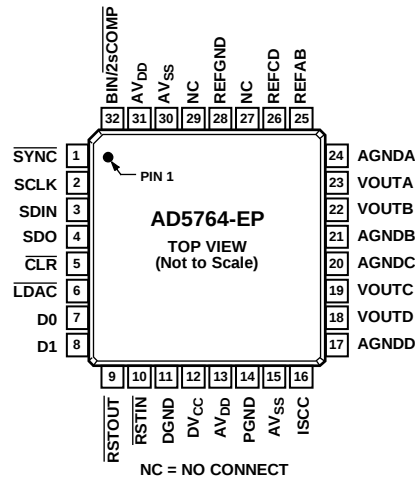


Figure 6. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SYNC	Active Low Input. This pin is the frame synchronization signal for the serial interface. While SYNC is low, data is transferred in on the falling edge of SCLK.
2	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of SCLK. This input operates at clock speeds up to 30 MHz.
3	SDIN	Serial Data Input. Data must be valid on the falling edge of SCLK.
4	SDO	Serial Data Output. This pin is used to clock data from the serial register in daisy-chain or readback mode.
5	CLR	Negative Edge Triggered Input. Asserting this pin sets the data register to 0x0000. This logic input has an internal pull-up device. Therefore, this pin can be left floating and defaults to a Logic 1 condition.
6	LDAC	Load DAC. This logic input is used to update the data register and, consequently, the analog outputs. When LDAC is tied permanently low, the addressed data register is updated on the rising edge of SYNC. If LDAC is held high during the write cycle, the DAC input shift register is updated, but the update of the output is delayed until the falling edge of LDAC. In this mode, all analog outputs can be updated simultaneously on the falling edge of LDAC. The LDAC pin must not be left unconnected.
7, 8	D0, D1	Digital I/O Port. These pins can be inputs or outputs that are configurable and readable over the serial interface. When configured as inputs, D0 and D1 have weak internal pull-ups to DVCC. When configured as outputs, D0 and D1 are referenced by DVCC and DGND.
9	RSTOUT	Reset Logic Output. This pin is the output from the on-chip voltage monitor and is used in the reset circuit. If desired, this pin can be used to control other system components.
10	RSTIN	Reset Logic Input. This input allows external access to the internal reset logic. Applying a Logic 0 to this input clamps the DAC outputs to 0 V. In normal operation, RSTIN should be tied to Logic 1. Register values remain unchanged.
11	DGND	Digital Ground.
12	DVCC	Digital Supply Voltage (2.7 V to 5.25 V).
13, 31	AVDD	Positive Analog Supply Voltage (11.4 V to 16.5 V).
14	PGND	Ground Reference Point for the Analog Circuitry.
15, 30	AVSS	Negative Analog Supply Voltage (–11.4 V to –16.5 V).
16	ISCC	Resistor Connection for Pin Programmable Short-Circuit Current. This pin is used with an optional external resistor to AGND to program the short-circuit current of the output amplifiers.
17	AGNDD	Ground Reference Pin for DAC D Output Amplifier.
18	VOUTD	Analog Output Voltage of DAC D. This buffered output has a nominal full-scale output range of ± 10 V. The output amplifier is capable of directly driving a 10 k Ω , 200 pF load.
19	VOUTC	Analog Output Voltage of DAC C. This buffered output has a nominal full-scale output range of ± 10 V. The output amplifier is capable of directly driving a 10 k Ω , 200 pF load.
20	AGNDC	Ground Reference Pin for DAC C Output Amplifier.

Pin No.	Mnemonic	Description
21	AGNDB	Ground Reference Pin for DAC B Output Amplifier.
22	VOUTB	Analog Output Voltage of DAC B. This buffered output has a nominal full-scale output range of ± 10 V. The output amplifier is capable of directly driving a 10 k Ω , 200 pF load.
23	VOUTA	Analog Output Voltage of DAC A. This buffered output has a nominal full-scale output range of ± 10 V. The output amplifier is capable of directly driving a 10 k Ω , 200 pF load.
24	AGNDA	Ground Reference Pin for DAC A Output Amplifier.
25	REFAB	External Reference Voltage Input for Channel A and Channel B. Reference input range is 1 V to 7 V. This pin programs the full-scale output voltage. $V_{REFIN} = 5$ V for specified performance.
26	REFCD	External Reference Voltage Input for Channel C and Channel D. Reference input range is 1 V to 7 V. This pin programs the full-scale output voltage. $V_{REFIN} = 5$ V for specified performance.
27, 29	NC	No Connect.
28	REFGND	Reference Ground Return for the Reference Generator and Buffers.
32	BIN/ $\overline{2sCOMP}$	This pin determines the DAC coding. This pin should be hardwired to either DV_{CC} or DGND. When the pin is hardwired to DV_{CC} , the input coding is offset binary. When the pin is hardwired to DGND, the input coding is twos complement.

TYPICAL PERFORMANCE CHARACTERISTICS

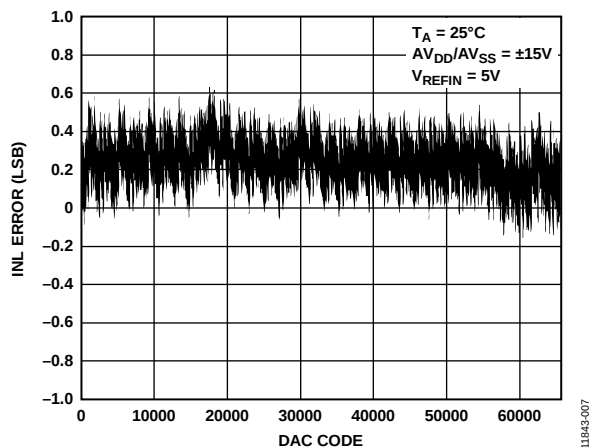


Figure 7. Integral Nonlinearity Error vs. Code,
 $AV_{DD}/AV_{SS} = \pm 15\text{ V}$

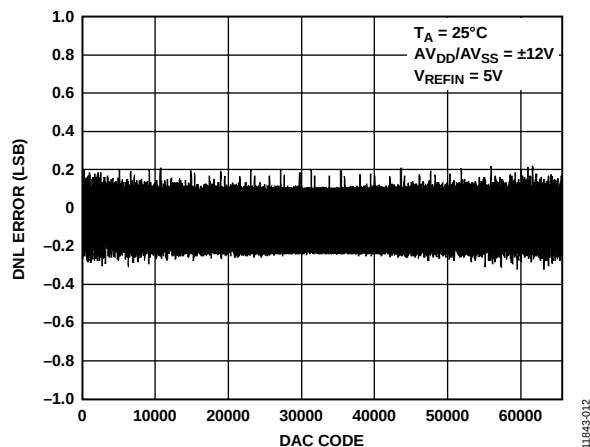


Figure 10. Differential Nonlinearity Error vs. Code,
 $AV_{DD}/AV_{SS} = \pm 12\text{ V}$

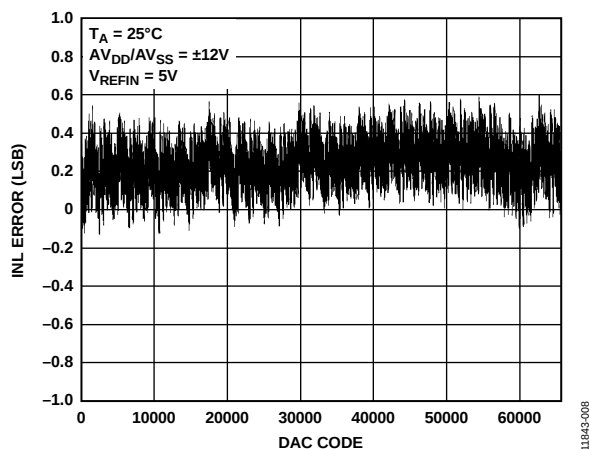


Figure 8. Integral Nonlinearity Error vs. Code,
 $AV_{DD}/AV_{SS} = \pm 12\text{ V}$

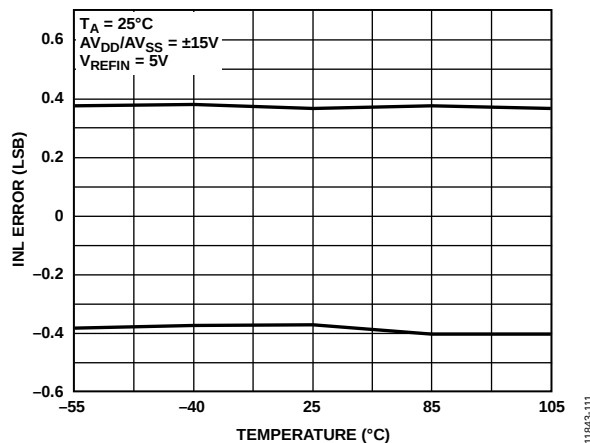


Figure 11. Integral Nonlinearity Error vs. Temperature,
 $AV_{DD}/AV_{SS} = \pm 15\text{ V}$

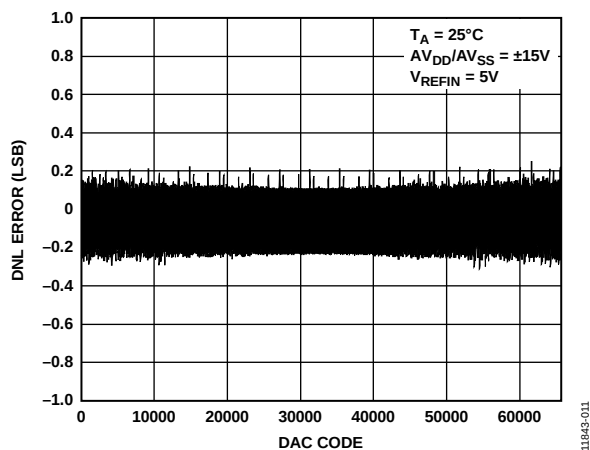


Figure 9. Differential Nonlinearity Error vs. Code,
 $AV_{DD}/AV_{SS} = \pm 15\text{ V}$

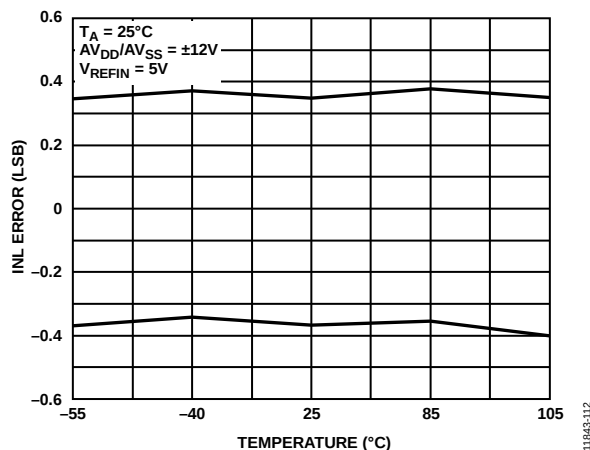


Figure 12. Integral Nonlinearity Error vs. Temperature,
 $AV_{DD}/AV_{SS} = \pm 12\text{ V}$

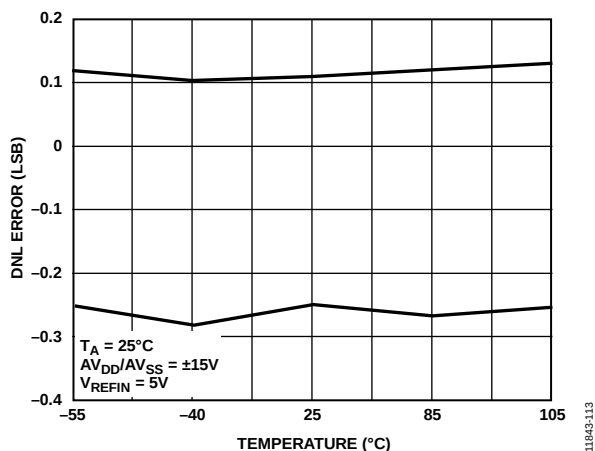


Figure 13. Differential Nonlinearity Error vs. Temperature, $AV_{DD}/AV_{SS} = \pm 15\text{ V}$

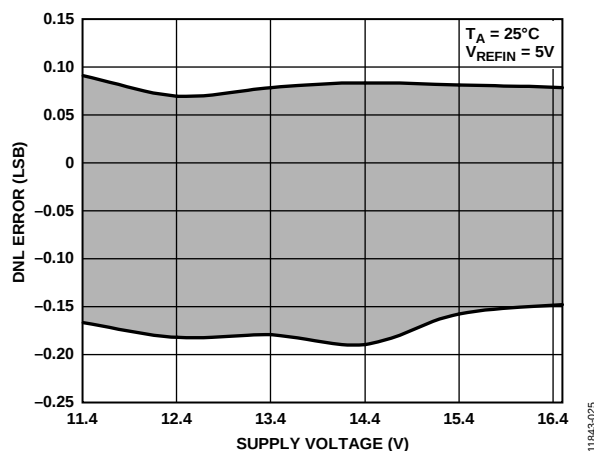


Figure 16. Differential Nonlinearity Error vs. Supply Voltage

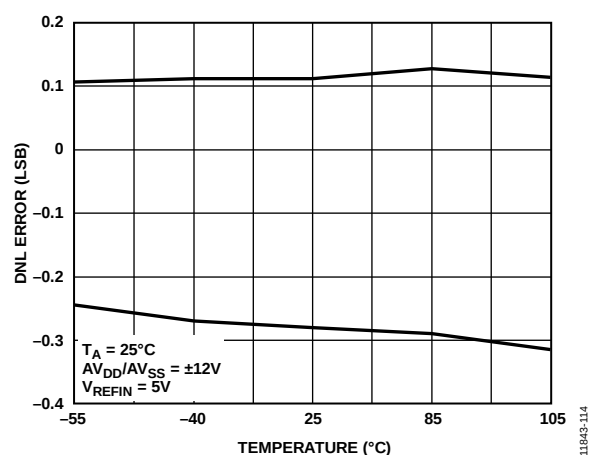


Figure 14. Differential Nonlinearity Error vs. Temperature, $AV_{DD}/AV_{SS} = \pm 12\text{ V}$

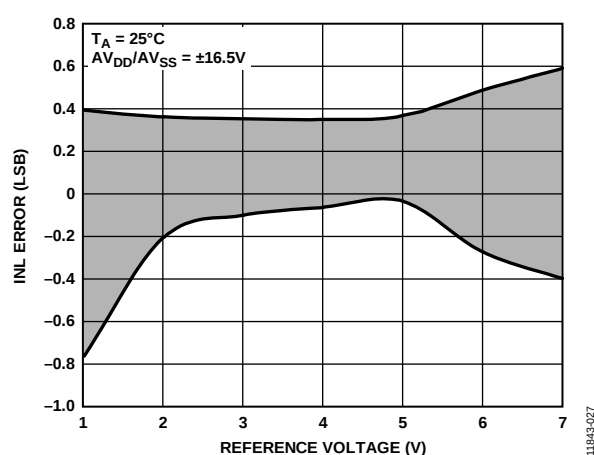


Figure 17. Integral Nonlinearity Error vs. Reference Voltage, $AV_{DD}/AV_{SS} = \pm 16.5\text{ V}$

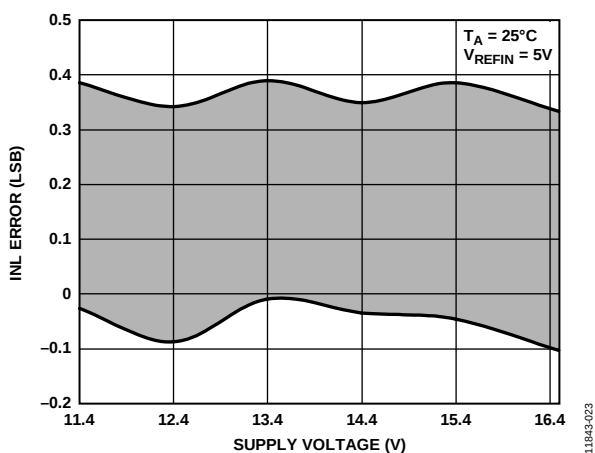


Figure 15. Integral Nonlinearity Error vs. Supply Voltage

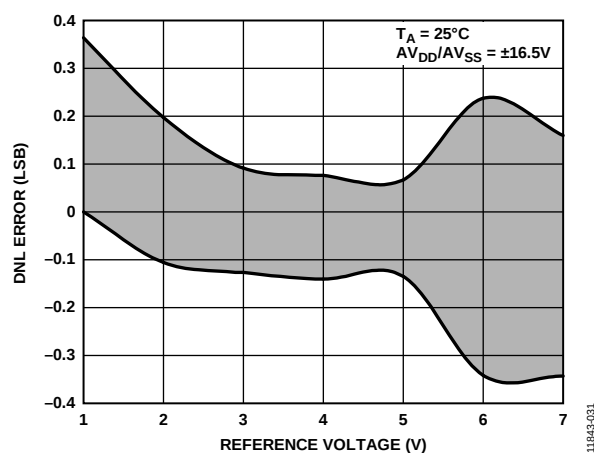


Figure 18. Differential Nonlinearity Error vs. Reference Voltage, $AV_{DD}/AV_{SS} = \pm 16.5\text{ V}$

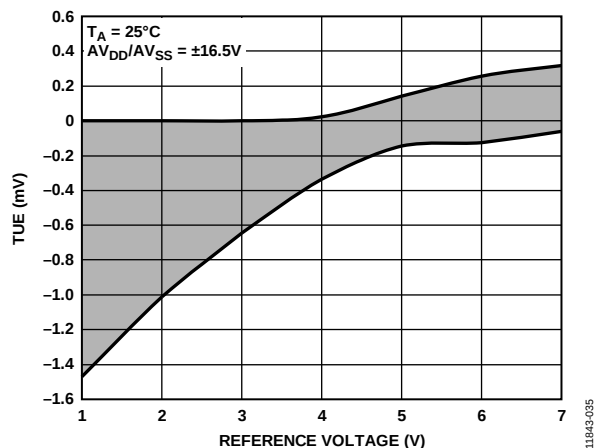


Figure 19. Total Unadjusted Error vs. Reference Voltage,
 $AV_{DD}/AV_{SS} = \pm 16.5V$

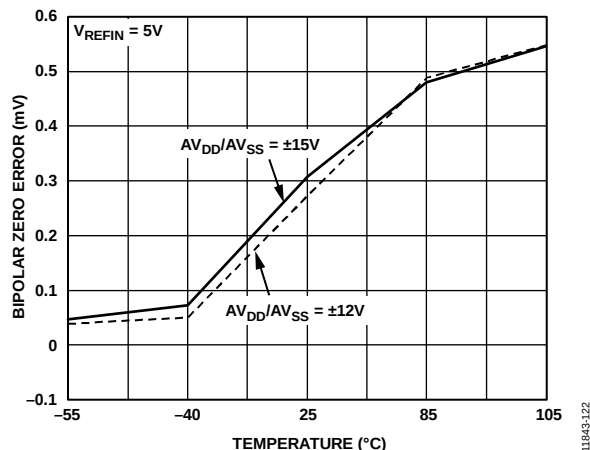


Figure 22. Bipolar Zero Error vs. Temperature

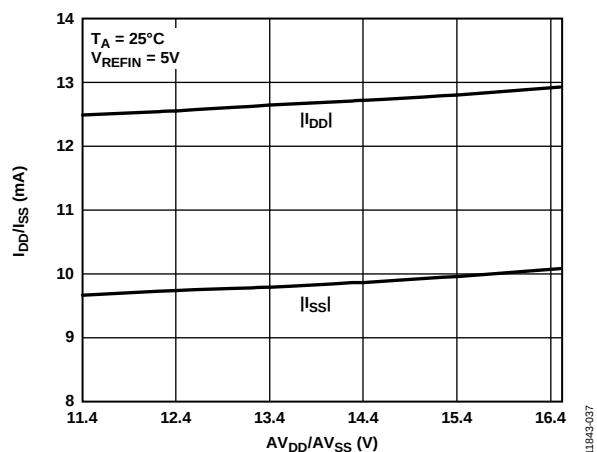


Figure 20. I_{DD}/I_{SS} vs. AV_{DD}/AV_{SS}

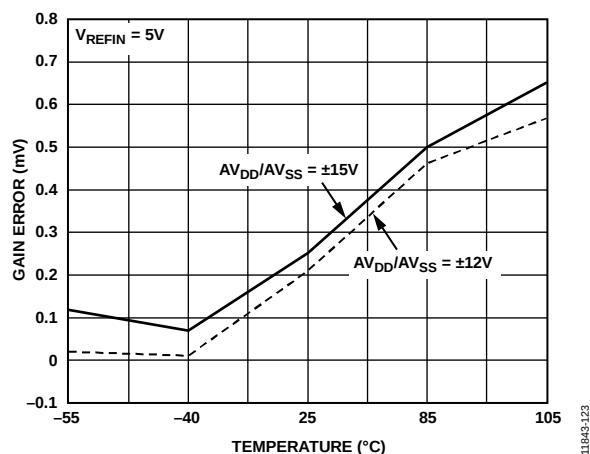


Figure 23. Gain Error vs. Temperature

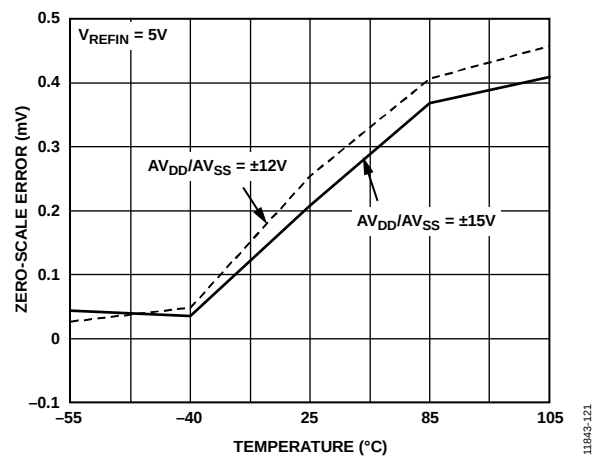


Figure 21. Zero-Scale Error vs. Temperature

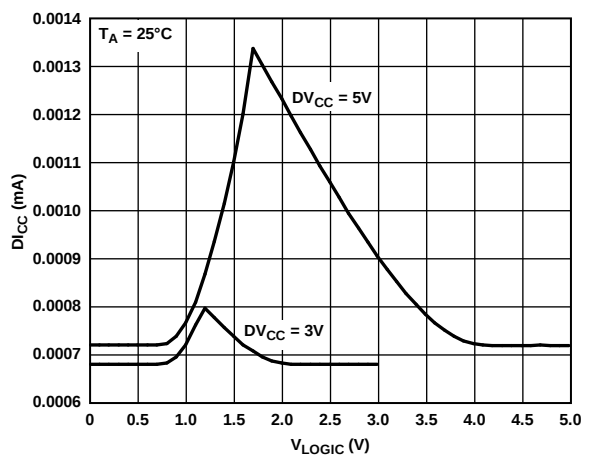


Figure 24. $D_{I_{CC}}$ vs. Logic Input Voltage

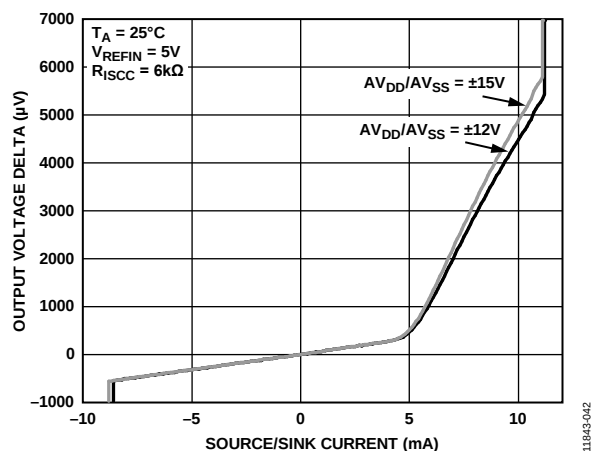


Figure 25. Source and Sink Capability of Output Amplifier with Positive Full Scale Loaded

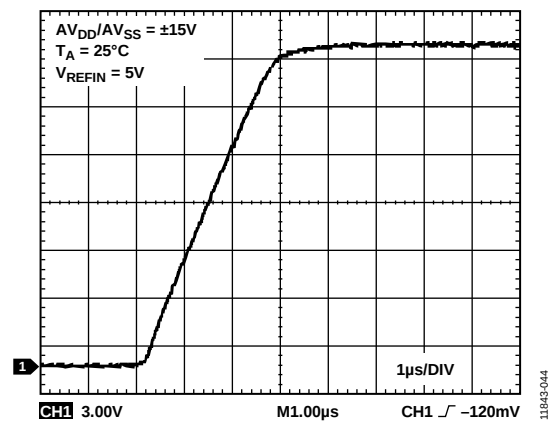


Figure 27. Full-Scale Settling Time

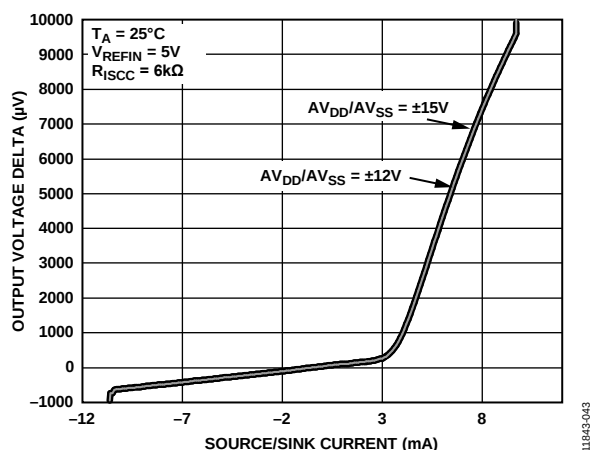


Figure 26. Source and Sink Capability of Output Amplifier with Negative Full Scale Loaded

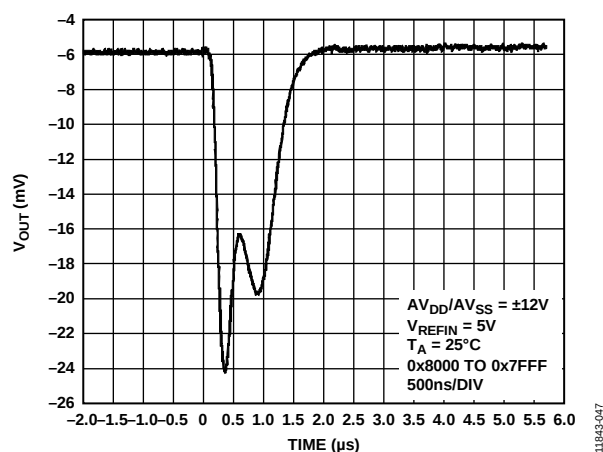


Figure 28. Major Code Transition Glitch Energy, $AV_{DD}/AV_{SS} = \pm 12V$

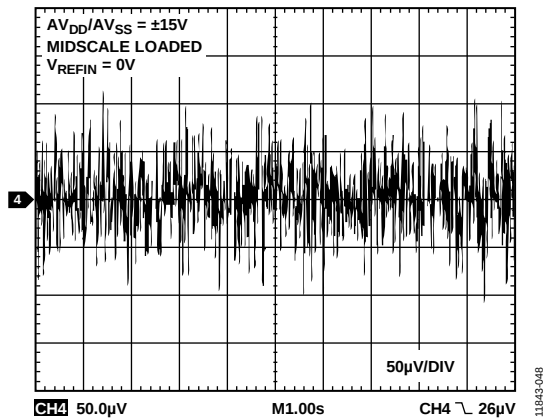


Figure 29. Peak-to-Peak Noise (100 kHz Bandwidth)

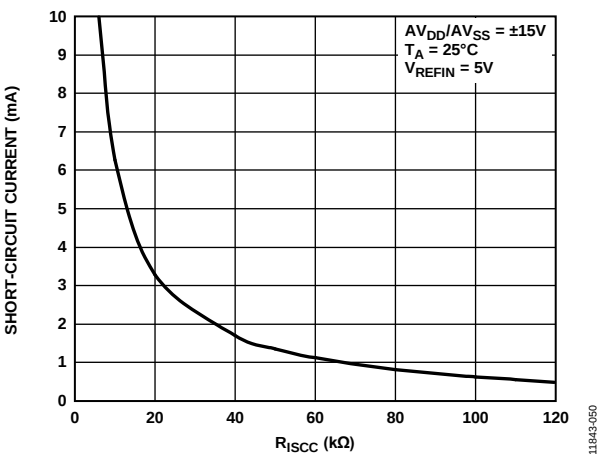


Figure 31. Short-Circuit Current vs. RISCC

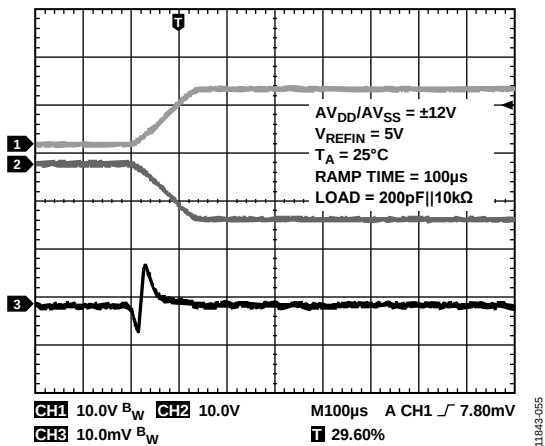
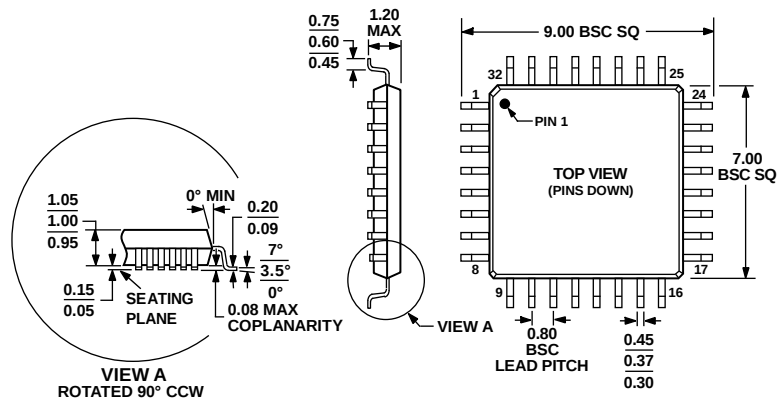


Figure 30. VOUT vs. AVDD/AVSS on Power-Up

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-AB A

Figure 32. 32-Lead Thin Plastic Quad Flat Package [TQFP]
(SU-32-2)

Dimensions shown in millimeters

022607-A

ORDERING GUIDE

Model ¹	INL	Temperature Range	Package Description	Package Option
AD5764SSUZ-EP-RL7	±2 LSB max	−55°C to +105°C	32-Lead TQFP	SU-32-2

¹ Z = RoHS Compliant Part.

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