Quad-Channel, 12-Bit, Serial Input, 4 mA to 20 mA Output DAC with Dynamic Power Control and HART Connectivity

Data Sheet **AD5737**

FEATURES

- **12-bit resolution and monotonicity**
- **Dynamic power control for thermal management or external PMOS mode**
- **Current output ranges: 0 mA to 20 mA, 4 mA to 20 mA, and 0 mA to 24 mA**
- **±0.1% total unadjusted error (TUE) maximum**
- **User-programmable offset and gain**
- **On-chip diagnostics**
- **On-chip reference: ±10 ppm/°C maximum**
- **–40°C to +105°C temperature range**

APPLICATIONS

- **Process control**
- **Actuator control**
- **PLCs**
- **HART network connectivity**

GENERAL DESCRIPTION

The AD5737 is a quad-channel current output DAC that operates with a power supply range from 10.8 V to 33 V. On-chip dynamic power control minimizes package power dissipation by regulating the voltage on the output driver from 7.4 V to 29.5 V using a dc-to-dc boost converter optimized for minimum on-chip power dissipation.

Each channel has a corresponding CHART pin so that HART signals can be coupled onto the current output of the AD5737.

The AD5737 uses a versatile 3-wire serial interface that operates at clock rates of up to 30 MHz and is compatible with standard SPI, QSPI™, MICROWIRE®, DSP, and microcontroller interface standards. The serial interface also features optional CRC-8 packet error checking, as well as a watchdog timer that monitors activity on the interface.

PRODUCT HIGHLIGHTS

1. Dynamic power control for thermal management.
2. 12-bit performance.
3. Quad channel.
4. HART compliant.

COMPANION PRODUCTS

Product Family: AD5755, AD5755-1, AD5757, AD5735
HART Modem: AD5700, AD5700-1
External References: ADR445, ADR02
Digital Isolators: ADuM1410, ADuM1411
Power: ADP2302, ADP2303
Additional companion products on the AD5737 product page

FUNCTIONAL BLOCK DIAGRAM

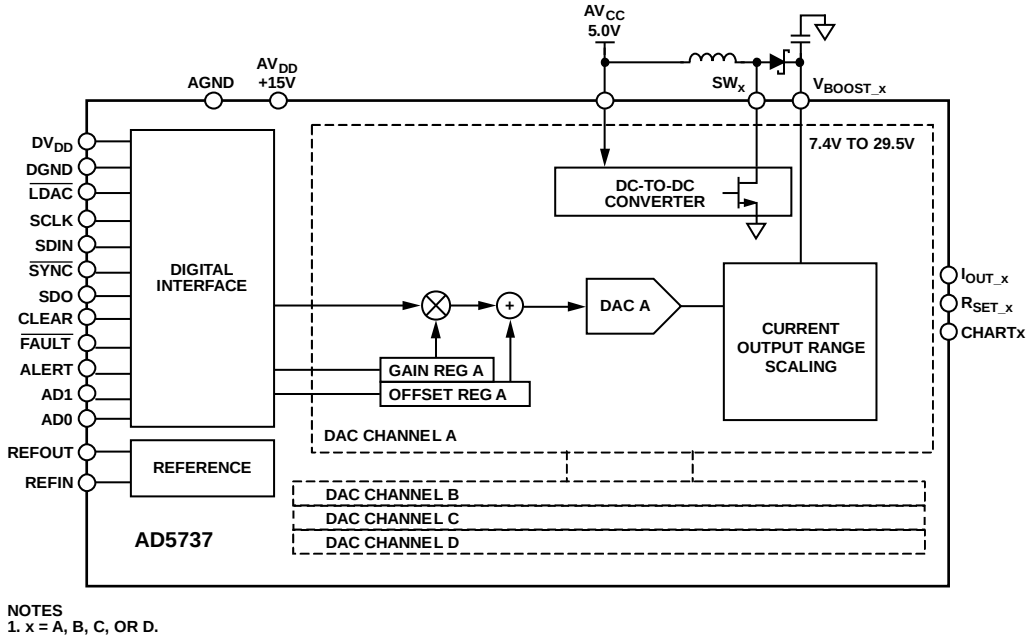


Figure 1.

Rev. F **Document Feedback**

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REVISION HISTORY

5/2017—Rev. E to Rev. F

Changes to Readback Operation Section 31
Removed Table 30 and Table 31; Renumbered Sequentially 31
Changes to Asynchronous Clear Section 33

9/2014—Rev. D to Rev. E

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Changes to Packet Error Checking Section 35

6/2014—Rev. C to Rev. D

Change to Thermal Hysteresis Parameter, Table 1 6
Changes to Table 3 7
Changes to Figure 5 and Added Figure 6; Renumbered Sequentially 9
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Changes to Readback Operation Section and Table 34, Added Table 30 and Table 31; Renumbered Sequentially 31
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11/2012—Rev. B to Rev. C

Changed Thermal Impedance from 20°C/W to 28°C/W 10
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5/2012—Rev. A to Rev. B

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Added Industrial HART Capable Analog Output Application Section and Figure 65, Renumbered Sequentially 42
Updated Outline Dimensions 43

11/2011—Rev. 0 to Rev. A

Change to Accuracy, External R_{SET} Parameter in Table 1 4
Changes to Power-On State of the AD5737 Section 21
Changes to Readback Operation Section and Readback Example Section 30

7/2011—Revision 0: Initial Version

DETAILED FUNCTIONAL BLOCK DIAGRAM

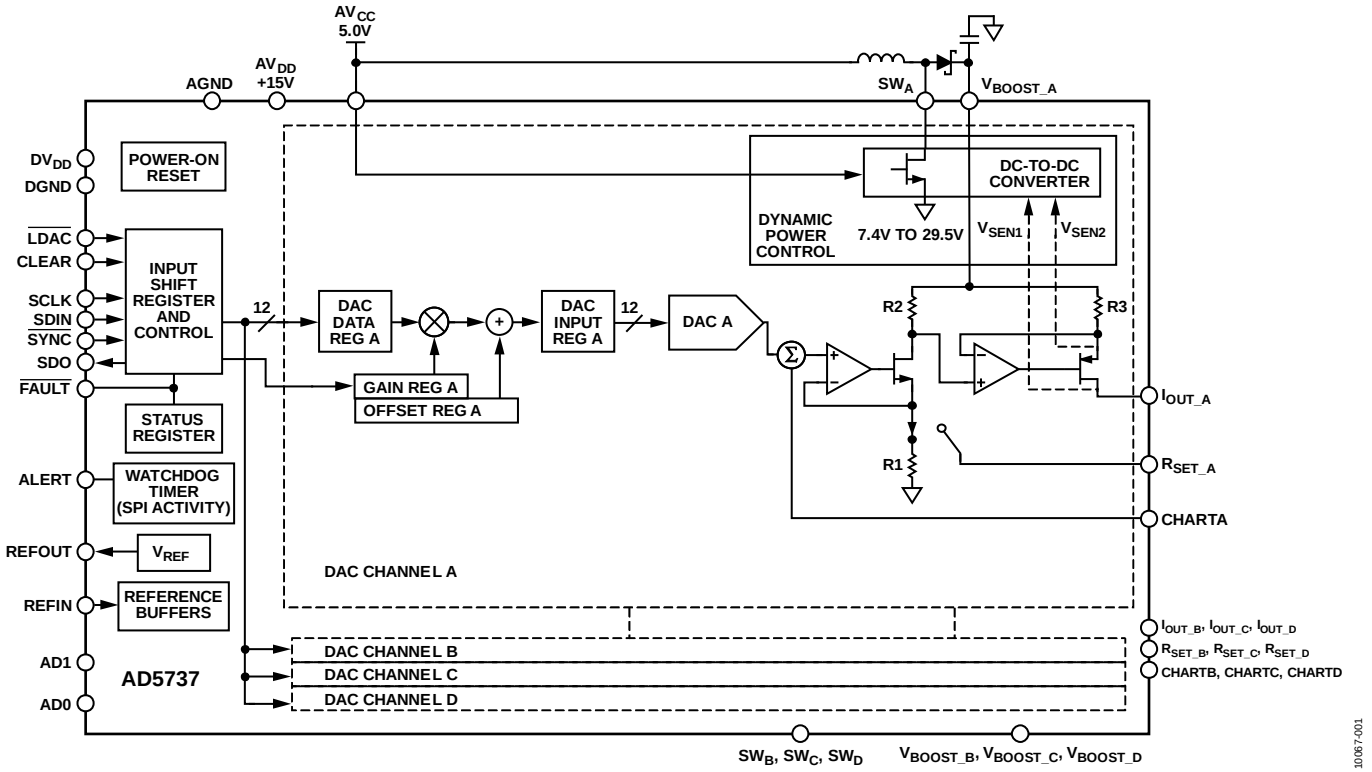


Figure 2.

SPECIFICATIONS

AV_{DD} = V_{BOOST_x} = 15 V; DV_{DD} = 2.7 V to 5.5 V; AV_{CC} = 4.5 V to 5.5 V; dc-to-dc converter disabled; AGND = DGND = $GNDSW_x$ = 0 V; REFIN = 5 V; R_L = 300 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT OUTPUT					
Output Current Ranges	0		24	mA	
	0		20	mA	
	4		20	mA	
Resolution	12			Bits	
ACCURACY, EXTERNAL R_{SET}					Assumes ideal resistor (see the External Current Setting Resistor section for more information)
Total Unadjusted Error (TUE)	−0.1	±0.019	+0.1	% FSR	
TUE Long-Term Stability		100		ppm FSR	Drift after 1000 hours, T_J = 150°C
Relative Accuracy (INL)	−0.032	±0.006	+0.032	% FSR	
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Offset Error	−0.1	±0.012	+0.1	% FSR	
Offset Error Drift[2]		±4		ppm FSR/°C	
Gain Error	−0.1	±0.004	+0.1	% FSR	
Gain TC[2]		±3		ppm FSR/°C	
Full-Scale Error	−0.1	±0.014	+0.1	% FSR	
Full-Scale TC[2]		±5		ppm FSR/°C	
DC Crosstalk		0.0005		% FSR	External R_{SET}
ACCURACY, INTERNAL R_{SET}					
Total Unadjusted Error (TUE)[3, 4]	−0.14	±0.022	+0.14	% FSR	
TUE Long-Term Stability		180		ppm FSR	Drift after 1000 hours, T_J = 150°C
Relative Accuracy (INL)	−0.032	±0.006	+0.032	% FSR	
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Offset Error[3, 4]	−0.1	±0.017	+0.1	% FSR	
Offset Error Drift[2]		±6		ppm FSR/°C	
Gain Error	−0.12	±0.004	+0.12	% FSR	
Gain TC[2]		±9		ppm FSR/°C	
Full-Scale Error[3, 4]	−0.14	±0.02	+0.14	% FSR	
Full-Scale TC[2]		±14		ppm FSR/°C	
DC Crosstalk[4]		−0.011		% FSR	Internal R_{SET}
OUTPUT CHARACTERISTICS[2]					
Current Loop Compliance Voltage		V_{BOOST_x} − 2.4	V_{BOOST_x} − 2.7	V	
Output Current Drift vs. Time					Drift after 1000 hours, ¾ scale output, T_J = 150°C
		90		ppm FSR	External R_{SET}
		140		ppm FSR	Internal R_{SET}
Resistive Load			1000	Ω	The dc-to-dc converter has been characterized with a maximum load of 1 kΩ, chosen such that compliance is not exceeded; see Figure 31 and the DC-DC MaxV bits in Table 27
DC Output Impedance		100		MΩ	
DC PSRR		0.02	1	µA/V	
REFERENCE INPUT/OUTPUT					
Reference Input[2]					
Reference Input Voltage	4.95	5	5.05	V	For specified performance
DC Input Impedance	45	150		MΩ	
Reference Output					
Output Voltage	4.995	5	5.005	V	T_A = 25°C
Reference TC[2]	−10	±5	+10	ppm/°C	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
Output Noise (0.1 Hz to 10 Hz)[2]		7		µV p-p	
Noise Spectral Density[2]		100		nV/√Hz	At 10 kHz
Output Voltage Drift vs. Time[2]		180		ppm	Drift after 1000 hours, T_J = 150°C
Capacitive Load[2]		1000		nF	
Load Current		9		mA	See Figure 42
Short-Circuit Current		10		mA	
Line Regulation[2]		3		ppm/V	See Figure 43
Load Regulation[2]		95		ppm/mA	See Figure 42
Thermal Hysteresis[2]		200		ppm	
DC-TO-DC CONVERTER					
Switch					
Switch On Resistance		0.425		Ω	
Switch Leakage Current		10		nA	
Peak Current Limit		0.8		A	
Oscillator					
Oscillator Frequency	11.5	13	14.5	MHz	This oscillator is divided down to provide the dc-to-dc converter switching frequency
Maximum Duty Cycle		89.6		%	At 410 kHz dc-to-dc switching frequency
DIGITAL INPUTS[2]					JEDEC compliant
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}			0.8	V	
Input Current	−1		+1	µA	Per pin
Pin Capacitance		2.6		pF	Per pin
DIGITAL OUTPUTS[2]					
SDO, ALERT Pins					
Output Low Voltage, V_{OL}			0.4	V	Sinking 200 µA
Output High Voltage, V_{OH}	DV_{DD} − 0.5			V	Sourcing 200 µA
High Impedance Leakage Current	−1		+1	µA	
High Impedance Output Capacitance		2.5		pF	
$\overline{\text{FAULT}}$ Pin					
Output Low Voltage, V_{OL}			0.4	V	10 kΩ pull-up resistor to DV_{DD}
		0.6		V	At 2.5 mA
Output High Voltage, V_{OH}	3.6			V	10 kΩ pull-up resistor to DV_{DD}
POWER REQUIREMENTS					
AV_{DD}	9		33	V	
DV_{DD}	2.7		5.5	V	
AV_{CC}	4.5		5.5	V	
AI_{DD}		7	7.5	mA	
DI_{CC}		9.2	11	mA	V_{IH} = DV_{DD}, V_{IL} = DGND, internal oscillator running, over supplies
AI_{CC}			1	mA	Outputs unloaded, over supplies
I_{BOOST}[5]			1	mA	Per channel, 0 mA output
Power Dissipation		155		mW	AV_{DD} = 15 V, DV_{DD} = 5 V, dc-to-dc converter enabled, outputs disabled

[1] Temperature range: −40°C to +105°C; typical at +25°C.
[2] Guaranteed by design and characterization; not production tested.
[3] For current outputs with internal R_{SET}, the offset, full-scale, and TUE measurements exclude dc crosstalk. The measurements are made with all four channels enabled and loaded with the same code.
[4] See the Current Output Mode with Internal R_{SET} section for more information about dc crosstalk.
[5] Efficiency plots in Figure 33 through Figure 36 include the I_{BOOST} quiescent current.

AC PERFORMANCE CHARACTERISTICS

AV_{DD} = V_{BOOST_x} = 15 V; DV_{DD} = 2.7 V to 5.5 V; AV_{CC} = 4.5 V to 5.5 V; dc-to-dc converter disabled; AGND = DGND = $GNDSW_x$ = 0 V; REFIN = 5 V; R_L = 300 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE, CURRENT OUTPUT					
Output Current Settling Time		15		µs	To 0.1% FSR, 0 mA to 24 mA range
		See Test Conditions/Comments		ms	For settling times when using the dc-to-dc converter, see Figure 26, Figure 27, and Figure 28
Output Noise (0.1 Hz to 10 Hz Bandwidth)		0.15		LSB p-p	12-bit LSB, 0 mA to 24 mA range
Output Noise Spectral Density		0.5		nA/√Hz	Measured at 10 kHz, midscale output, 0 mA to 24 mA range

[1] Guaranteed by design and characterization; not production tested.

TIMING CHARACTERISTICS

AV_{DD} = V_{BOOST_x} = 15 V; DV_{DD} = 2.7 V to 5.5 V; AV_{CC} = 4.5 V to 5.5 V; dc-to-dc converter disabled; AGND = DGND = $GNDSW_x$ = 0 V; REFIN = 5 V; R_L = 300 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK high time
t_3	13	ns min	SCLK low time
t_4	13	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	13	ns min	24th/32nd SCLK falling edge to $\overline{SYNC}$ rising edge (see Figure 54)
t_6	198	ns min	$\overline{SYNC}$ high time following a configuration write
	5	µs min	$\overline{SYNC}$ high time following a DAC update write
t_7	5	ns min	Data setup time
t_8	5	ns min	Data hold time
t_9	20	µs min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (applies to any channel with digital slew rate control enabled; single DAC updated)
	5	µs min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (single DAC updated)
t_{10}	10	ns min	$\overline{LDAC}$ pulse width low
t_{11}	500	ns max	$\overline{LDAC}$ falling edge to DAC output response time
t_{12}	See Table 2	µs max	DAC output settling time
t_{13}	10	ns min	CLEAR high time
t_{14}	5	µs max	CLEAR activation time
t_{15}	40	ns max	SCLK rising edge to SDO valid
t_{16}	5	µs min	$\overline{SYNC}$ rising edge to DAC output response time ($\overline{LDAC}$ = 0) (single DAC updated)
t_{17}	500	ns min	$\overline{LDAC}$ falling edge to $\overline{SYNC}$ rising edge
t_{18}	800	ns min	$\overline{RESET}$ pulse width
t_{19}	20	µs min	$\overline{SYNC}$ rising edge to next $\overline{SYNC}$ low (falling edge (digital slew rate control enabled; single DAC updated)
	5	µs min	$\overline{SYNC}$ rising edge to next $\overline{SYNC}$ low (falling edge (digital slew rate control disabled; single DAC updated)

[1] Guaranteed by design and characterization; not production tested.
[2] All input signals are specified with t_{RISE} = t_{FALL} = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.2 V.
[3] See Figure 3, Figure 4, Figure 5, and Figure 7.

Timing Diagrams

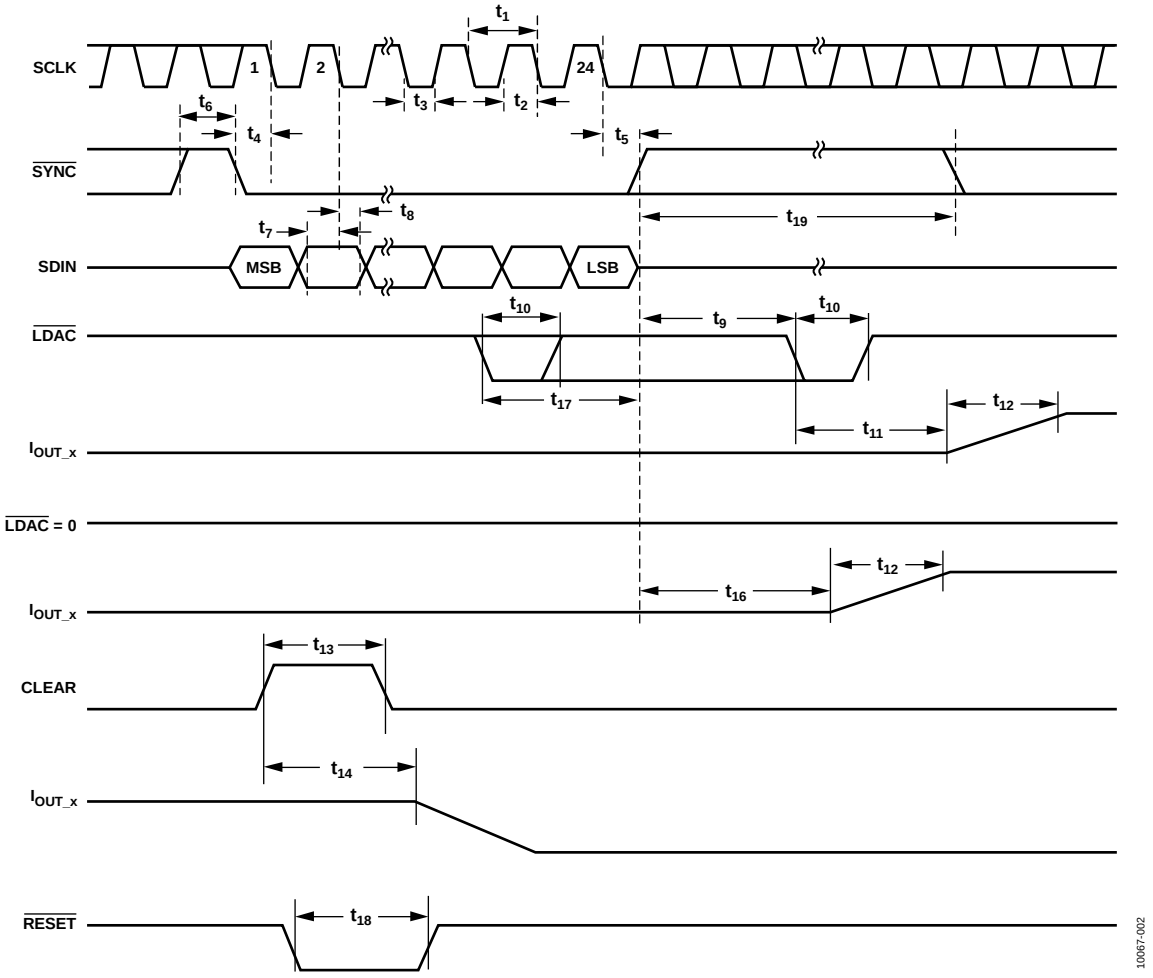
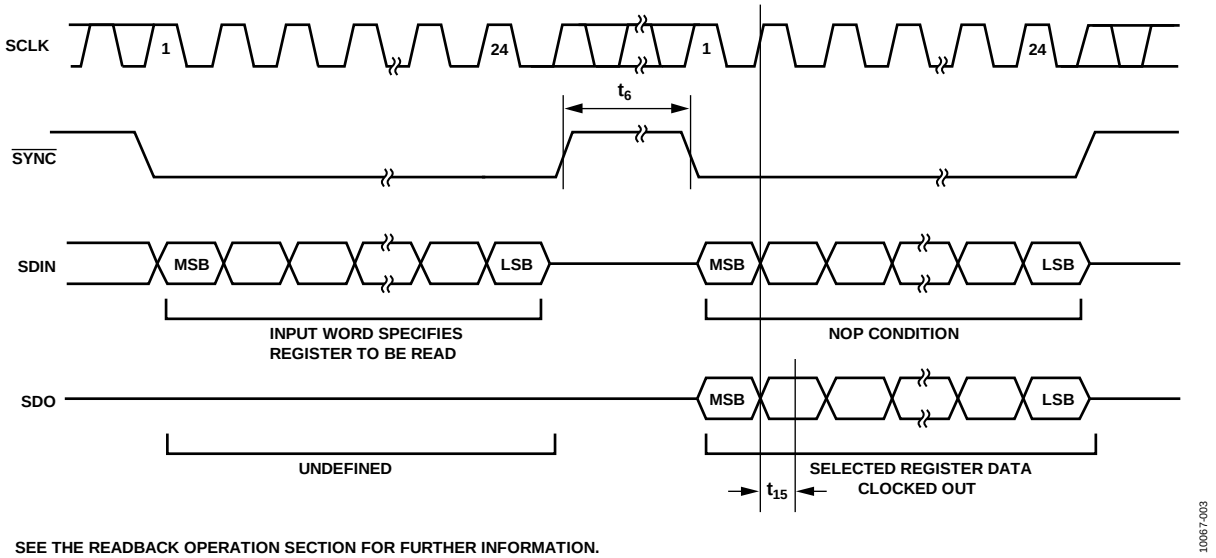


Figure 3. Serial Interface Timing Diagram



SEE THE READBACK OPERATION SECTION FOR FURTHER INFORMATION.

Figure 4. Readback Timing Diagram (Packet Error Checking Disabled)

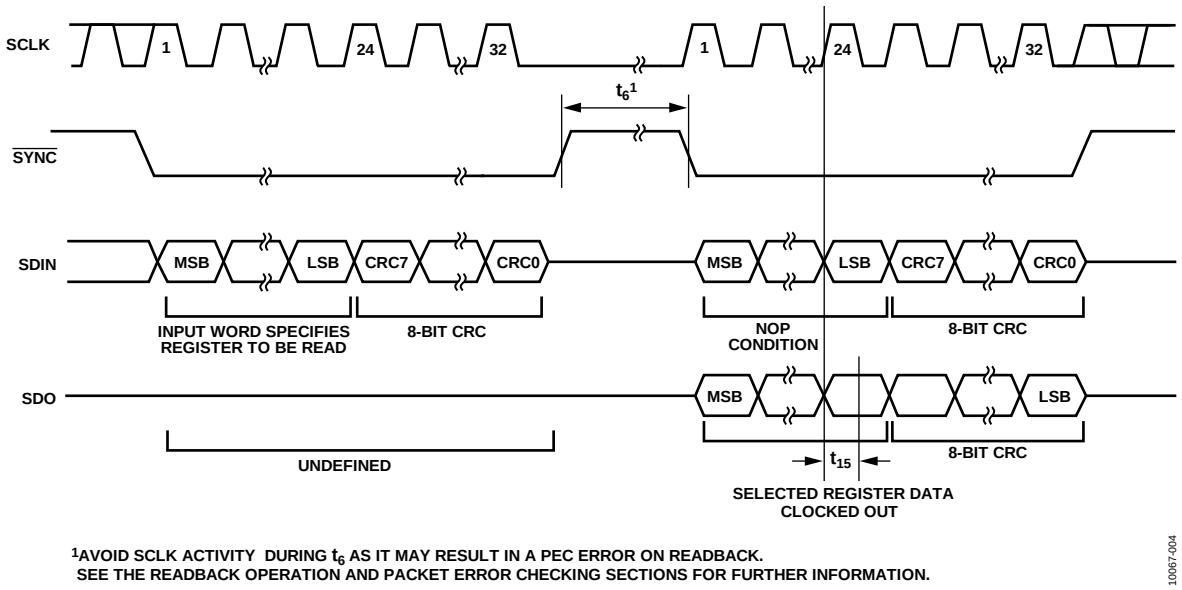


Figure 5. Readback Timing Diagram (Packet Error Checking Enabled)

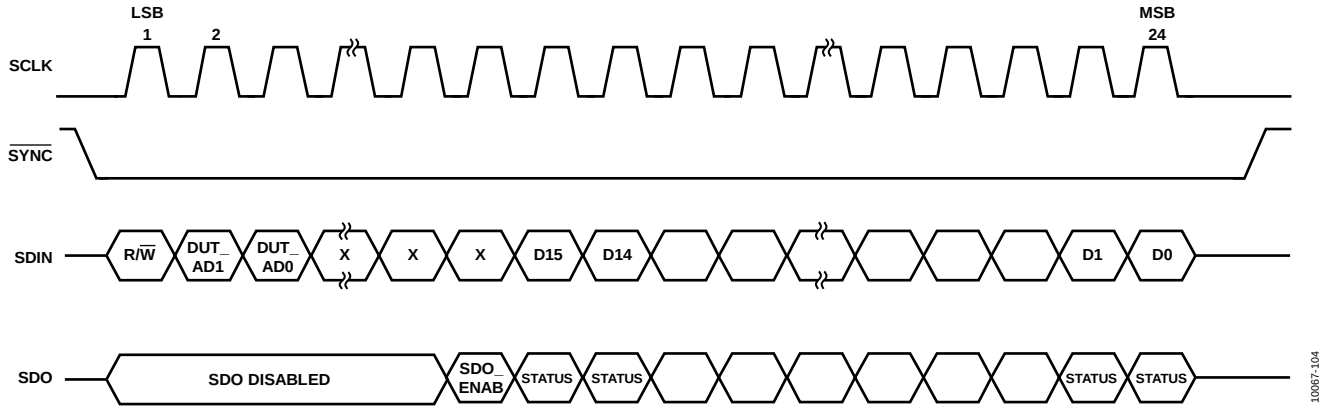


Figure 6. Status Readback During a Write

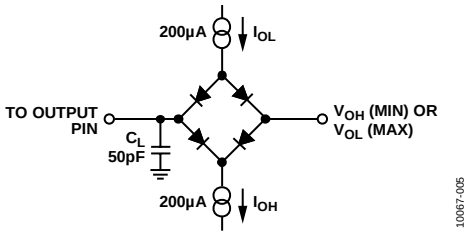


Figure 7. Load Circuit for SDO Timing Diagrams

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 4.

Parameter	Rating
AV_{DD}, V_{BOOST_x} to AGND, DGND	−0.3 V to +33 V
AV_{CC} to AGND	−0.3 V to +7 V
DV_{DD} to DGND	−0.3 V to +7 V
Digital Inputs to DGND	−0.3 V to DV_{DD} + 0.3 V or +7 V (whichever is less)
Digital Outputs to DGND	−0.3 V to DV_{DD} + 0.3 V or +7 V (whichever is less)
REFIN, REFOUT to AGND	−0.3 V to AV_{DD} + 0.3 V or +7 V (whichever is less)
I_{OUT_x} to AGND	AGND to V_{BOOST_x} or 33 V if using the dc-to-dc converter
SW_x to AGND	−0.3 V to +33 V
AGND, $GNDSW_x$ to DGND	−0.3 V to +0.3 V
Operating Temperature Range (T_A)	
Industrial[1]	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	125°C
Power Dissipation	(T_J max − T_A)/θ_{JA}
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020

[1] Power dissipated on chip must be derated to keep the junction temperature below 125°C.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Junction-to-air thermal resistance (θ_{JA}) is specified for a JEDEC 4-layer test board.

Table 5. Thermal Resistance

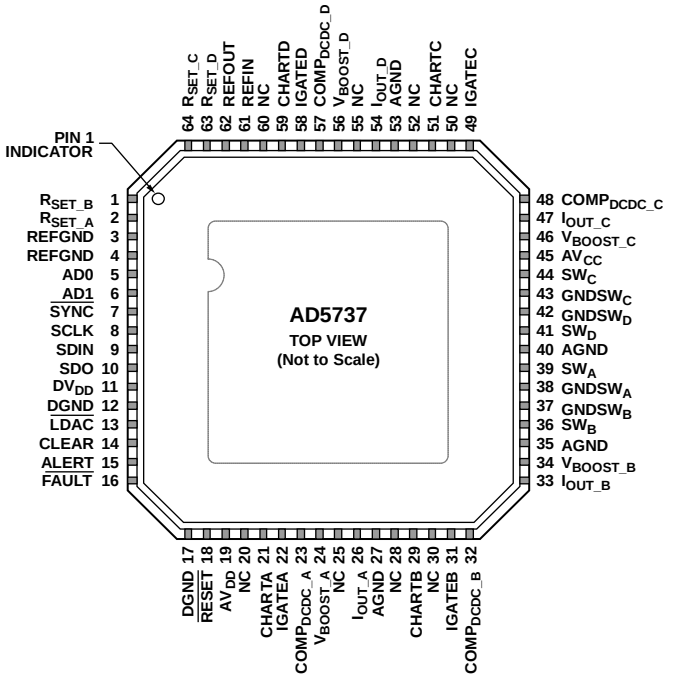
Package Type	θ_{JA}	Unit
64-Lead LFCSP (CP-64-3)	28	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EXPOSED PADDLE SHOULD BE CONNECTED TO AGND, OR, ALTERNATIVELY, IT CAN BE LEFT ELECTRICALLY UNCONNECTED. IT IS RECOMMENDED THAT THE PADDLE BE THERMALLY CONNECTED TO A COPPER PLANE FOR ENHANCED THERMAL PERFORMANCE.

10067-006

Figure 8. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	R_{SET_B}	An external, precision, low drift, 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_B} temperature drift performance. For more information, see the External Current Setting Resistor section.
2	R_{SET_A}	An external, precision, low drift, 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_A} temperature drift performance. For more information, see the External Current Setting Resistor section.
3	REFGND	Ground Reference Point for Internal Reference.
4	REFGND	Ground Reference Point for Internal Reference.
5	AD0	Address Decode for the Device Under Test (DUT) on the Board.
6	AD1	Address Decode for the DUT on the Board. It is not recommended to tie both AD1 and AD0 low when using PEC (see the Packet Error Checking section).
7	$\overline{SYNC}$	Frame Synchronization Signal for the Serial Interface. Active low input. When $\overline{SYNC}$ is low, data is clocked into the input shift register on the falling edge of SCLK.
8	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of SCLK. The serial interface operates at clock speeds of up to 30 MHz.
9	SDIN	Serial Data Input. Data must be valid on the falling edge of SCLK.
10	SDO	Serial Data Output. Used to clock data from the serial register in readback mode (see Figure 4 and Figure 5).
11	DV_{DD}	Digital Supply Pin. The voltage range is from 2.7 V to 5.5 V.
12	DGND	Digital Ground.
13	$\overline{LDAC}$	Load DAC. This active low input is used to update the DAC register and, consequently, the DAC outputs. When $\overline{LDAC}$ is tied permanently low, the addressed DAC data register is updated on the rising edge of $\overline{SYNC}$. If $\overline{LDAC}$ is held high during the write cycle, the DAC input register is updated, but the DAC output is updated only on the falling edge of $\overline{LDAC}$ (see Figure 3). Using this mode, all analog outputs can be updated simultaneously. Do not leave the $\overline{LDAC}$ pin unconnected.

Pin No.	Mnemonic	Description
14	CLEAR	Active High, Edge Sensitive Input. When this pin is asserted, the output current is set to the programmed clear code bit setting. Only channels enabled to be cleared are cleared. For more information, see the Asynchronous Clear section. When CLEAR is active, the DAC output register cannot be written to.
15	ALERT	Active High Output. This pin is asserted when there is no SPI activity on the interface pins for a preset time. For more information, see the Alert Output section.
16	$\overline{\text{FAULT}}$	Active Low, Open-Drain Output. This pin is asserted low when any of the following conditions is detected: open circuit, PEC error, or an overtemperature condition (see the Fault Output section).
17	DGND	Digital Ground.
18	$\overline{\text{RESET}}$	Hardware Reset, Active Low Input.
19	AV_{DD}	Positive Analog Supply Pin. The voltage range is from 9 V to 33 V.
20	NC	No Connect. Do not connect to this pin.
21	CHARTA	HART Input Connection for DAC Channel A. For more information, see the HART Connectivity section.
22	IGATEA	Optional Connection for External Pass Transistor. Leave this pin unconnected when using the dc-to-dc converter. For more information, see the External PMOS Mode section.
23	$COMP_{DCDC_A}$	DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of the Channel A dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin. For more information, see the DC-to-DC Converter Compensation Capacitors section and the AI_{CC} Supply Requirements—Slewing section.
24	V_{BOOST_A}	Supply for Channel A Current Output Stage (see Figure 49). To use the dc-to-dc converter, connect this pin as shown in Figure 56.
25	NC	No Connect. Do not connect to this pin.
26	I_{OUT_A}	Current Output Pin for DAC Channel A.
27	AGND	Ground Reference Point for Analog Circuitry. This pin must be connected to 0 V.
28	NC	No Connect. Do not connect to this pin.
29	CHARTB	HART Input Connection for DAC Channel B. For more information, see the HART Connectivity section.
30	NC	No Connect. Do not connect to this pin.
31	IGATEB	Optional Connection for External Pass Transistor. Leave this pin unconnected when using the dc-to-dc converter. For more information, see the External PMOS Mode section.
32	$COMP_{DCDC_B}$	DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of the Channel B dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin. For more information, see the DC-to-DC Converter Compensation Capacitors section and the AI_{CC} Supply Requirements—Slewing section.
33	I_{OUT_B}	Current Output Pin for DAC Channel B.
34	V_{BOOST_B}	Supply for Channel B Current Output Stage (see Figure 49). To use the dc-to-dc converter, connect this pin as shown in Figure 56.
35	AGND	Ground Reference Point for Analog Circuitry. This pin must be connected to 0 V.
36	SW_B	Switching Output for Channel B DC-to-DC Circuitry. To use the dc-to-dc converter, connect this pin as shown in Figure 56.
37	$GNDSW_B$	Ground Connection for DC-to-DC Switching Circuit. This pin must always be connected to ground.
38	$GNDSW_A$	Ground Connection for DC-to-DC Switching Circuit. This pin must always be connected to ground.
39	SW_A	Switching Output for Channel A DC-to-DC Circuitry. To use the dc-to-dc converter, connect this pin as shown in Figure 56.
40	AGND	Ground Reference Point for Analog Circuitry. This pin must be connected to 0 V.
41	SW_D	Switching Output for Channel D DC-to-DC Circuitry. To use the dc-to-dc converter, connect this pin as shown in Figure 56.
42	$GNDSW_D$	Ground Connection for DC-to-DC Switching Circuit. This pin must always be connected to ground.
43	$GNDSW_C$	Ground Connection for DC-to-DC Switching Circuit. This pin must always be connected to ground.
44	SW_C	Switching Output for Channel C DC-to-DC Circuitry. To use the dc-to-dc converter, connect this pin as shown in Figure 56.
45	AV_{CC}	Supply for DC-to-DC Circuitry. The voltage range is from 4.5 V to 5.5 V.
46	V_{BOOST_C}	Supply for Channel C Current Output Stage (see Figure 49). To use the dc-to-dc converter, connect this pin as shown in Figure 56.
47	I_{OUT_C}	Current Output Pin for DAC Channel C.
48	$COMP_{DCDC_C}$	DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of the Channel C dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin. For more information, see the DC-to-DC Converter Compensation Capacitors section and the AI_{CC} Supply Requirements—Slewing section.

Pin No.	Mnemonic	Description
49	IGATEC	Optional Connection for External Pass Transistor. Leave this pin unconnected when using the dc-to-dc converter. For more information, see the External PMOS Mode section.
50	NC	No Connect. Do not connect to this pin.
51	CHARTC	HART Input Connection for DAC Channel C. For more information, see the HART Connectivity section.
52	NC	No Connect. Do not connect to this pin.
53	AGND	Ground Reference Point for Analog Circuitry. This pin must be connected to 0 V.
54	I_{OUT_D}	Current Output Pin for DAC Channel D.
55	NC	No Connect. Do not connect to this pin.
56	V_{BOOST_D}	Supply for Channel D Current Output Stage (see Figure 49). To use the dc-to-dc converter, connect this pin as shown in Figure 56.
57	$COMP_{DCDC_D}$	DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of the Channel D dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin. For more information, see the DC-to-DC Converter Compensation Capacitors section and the AI_{CC} Supply Requirements—Slewing section.
58	IGATED	Optional Connection for External Pass Transistor. Leave this pin unconnected when using the dc-to-dc converter. For more information, see the External PMOS Mode section.
59	CHARTD	HART Input Connection for DAC Channel D. For more information, see the HART Connectivity section.
60	NC	No Connect. Do not connect to this pin.
61	REFIN	External Reference Voltage Input.
62	REFOUT	Internal Reference Voltage Output. It is recommended that a 0.1 µF capacitor be placed between REFOUT and REFGND. REFOUT must be connected to REFIN to use the internal reference.
63	R_{SET_D}	An external, precision, low drift, 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_D} temperature drift performance. For more information, see the External Current Setting Resistor section.
64	R_{SET_C}	An external, precision, low drift, 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_C} temperature drift performance. For more information, see the External Current Setting Resistor section.
	EPAD	Exposed Pad. The exposed paddle must be connected to AGND, or, alternatively, it can be left electrically unconnected. It is recommended that the paddle be thermally connected to a copper plane for enhanced thermal performance.

TYPICAL PERFORMANCE CHARACTERISTICS

CURRENT OUTPUTS

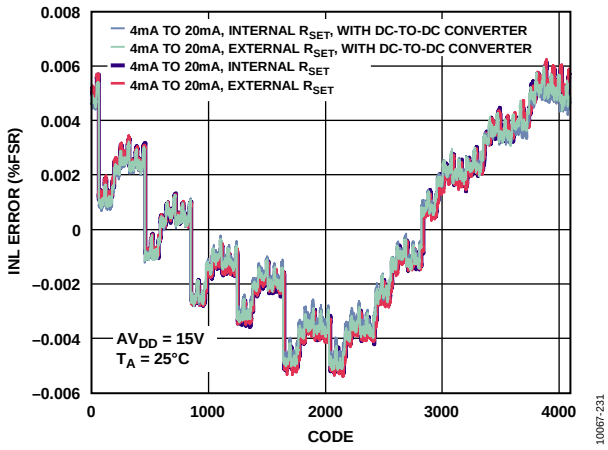


Figure 9. Integral Nonlinearity Error vs. DAC Code

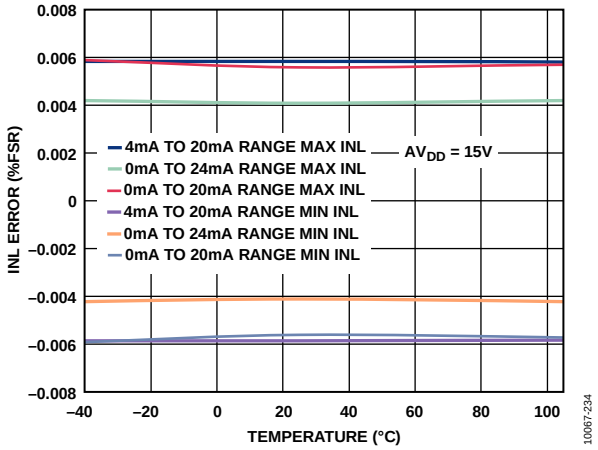


Figure 12. Integral Nonlinearity Error vs. Temperature, Internal R_{SET}

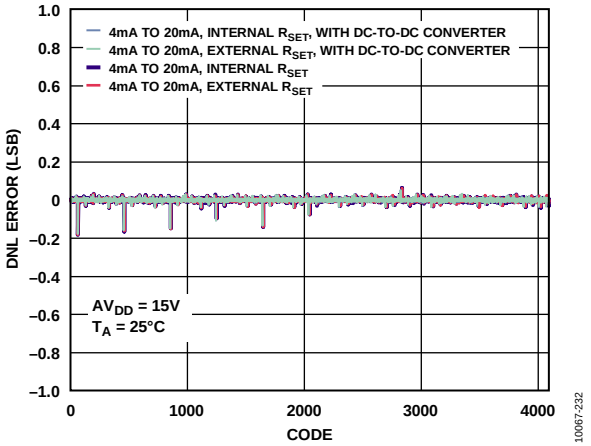


Figure 10. Differential Nonlinearity Error vs. DAC Code

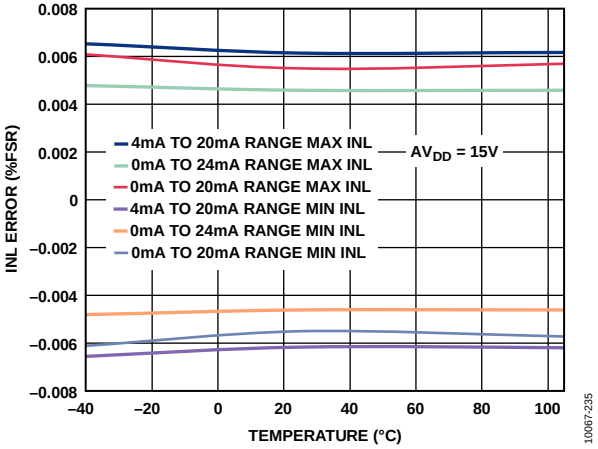


Figure 13. Integral Nonlinearity Error vs. Temperature, External R_{SET}

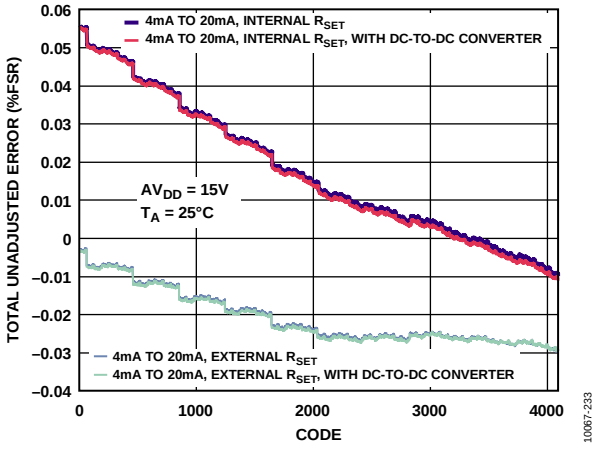


Figure 11. Total Unadjusted Error vs. DAC Code

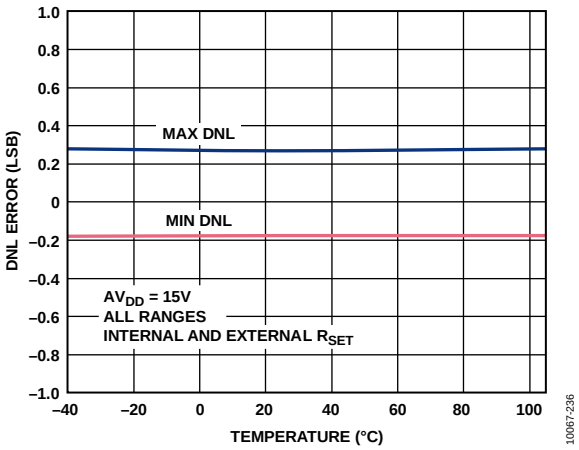


Figure 14. Differential Nonlinearity Error vs. Temperature

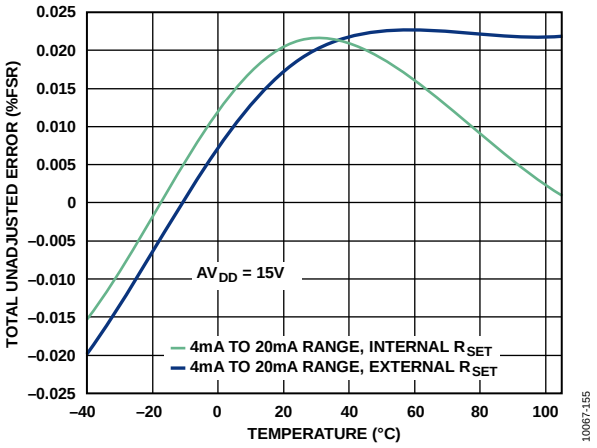


Figure 15. Total Unadjusted Error vs. Temperature

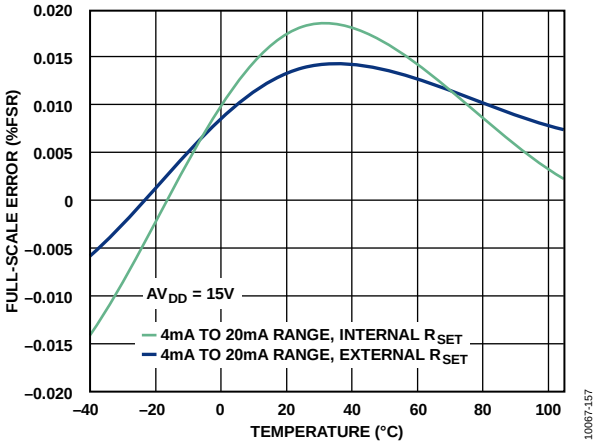


Figure 16. Full-Scale Error vs. Temperature

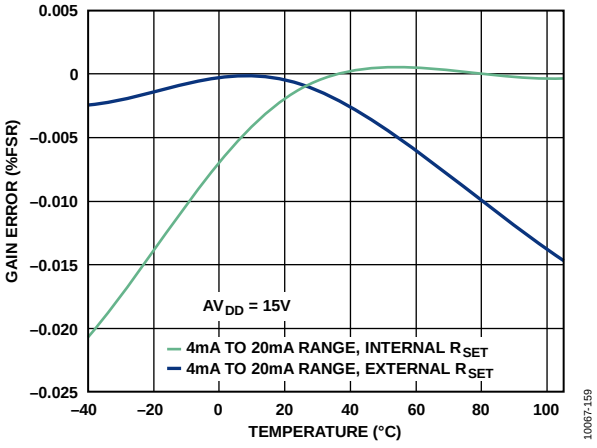


Figure 17. Gain Error vs. Temperature

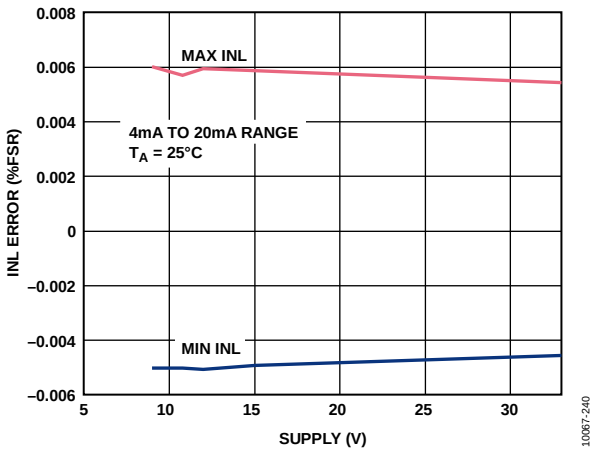


Figure 18. Integral Nonlinearity Error vs. Supply, External R_{SET}

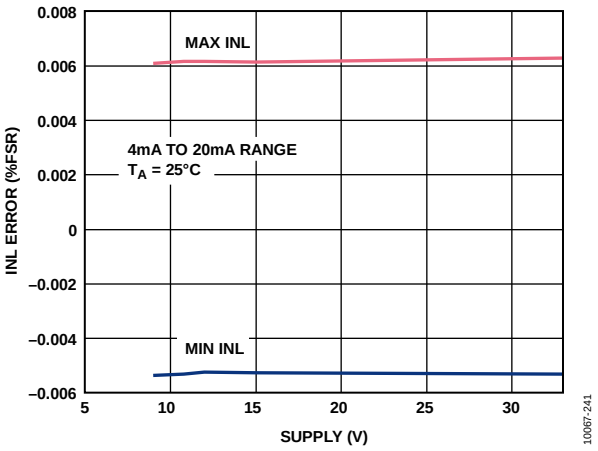


Figure 19. Integral Nonlinearity Error vs. Supply, Internal R_{SET}

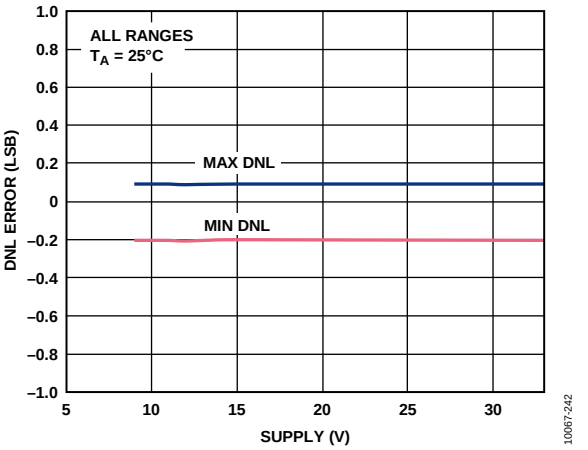


Figure 20. Differential Nonlinearity Error vs. Supply

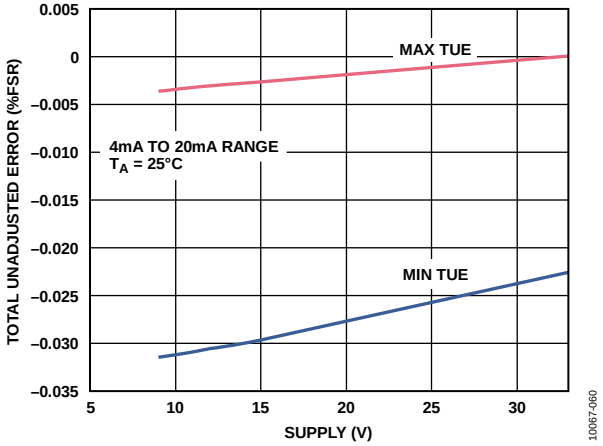


Figure 21. Total Unadjusted Error vs. Supply, External R_{SET}

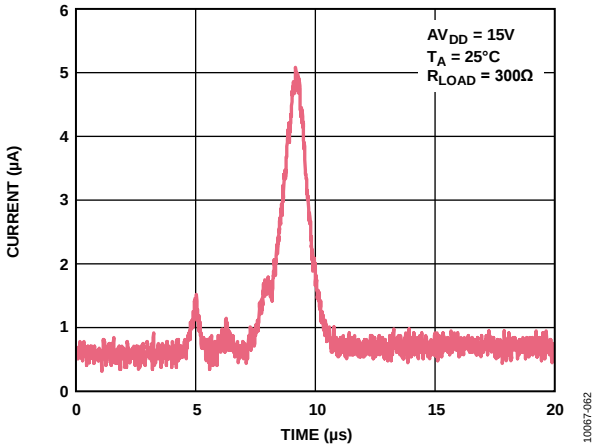


Figure 24. Current vs. Time on Power-Up

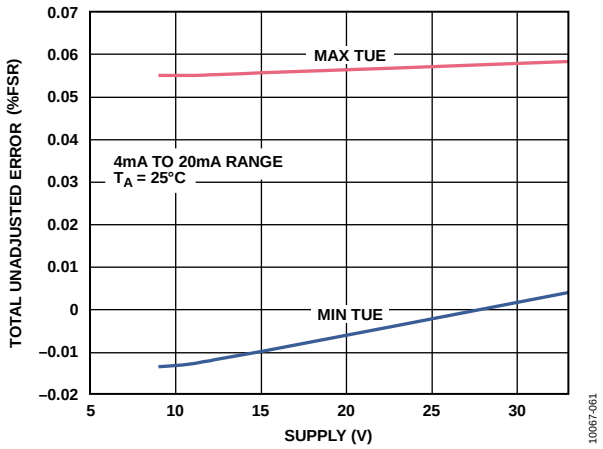


Figure 22. Total Unadjusted Error vs. Supply, Internal R_{SET}

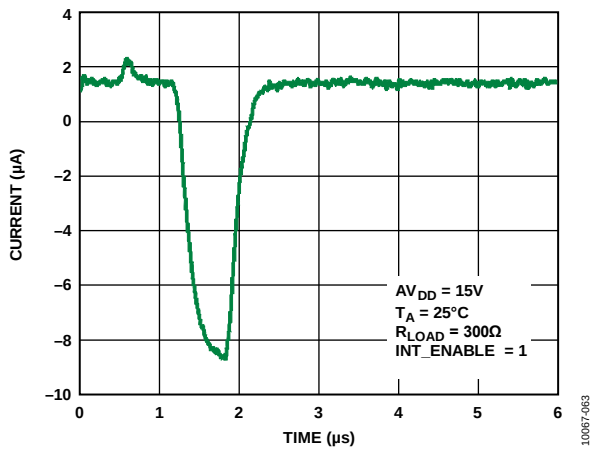


Figure 25. Current vs. Time on Output Enable

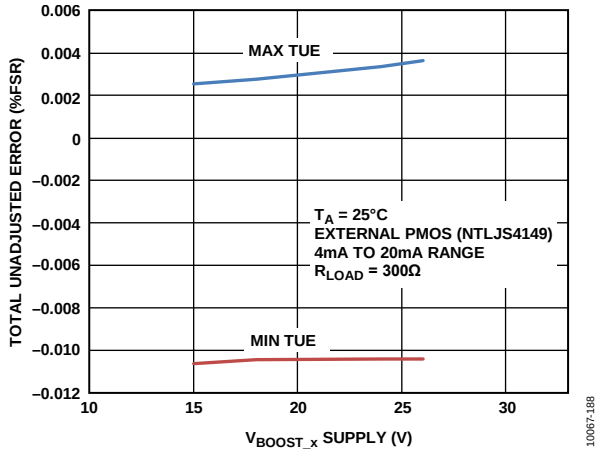


Figure 23. Total Unadjusted Error vs. V_{BOOST_x} Supply Using External PMOS Mode

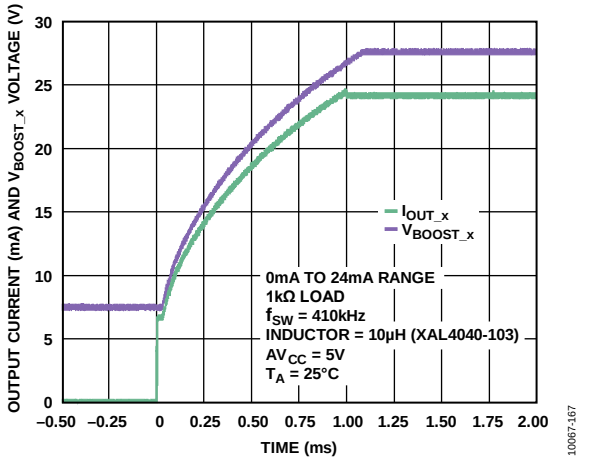


Figure 26. Output Current and V_{BOOST_x} Settling Time with DC-to-DC Converter (See Figure 56)

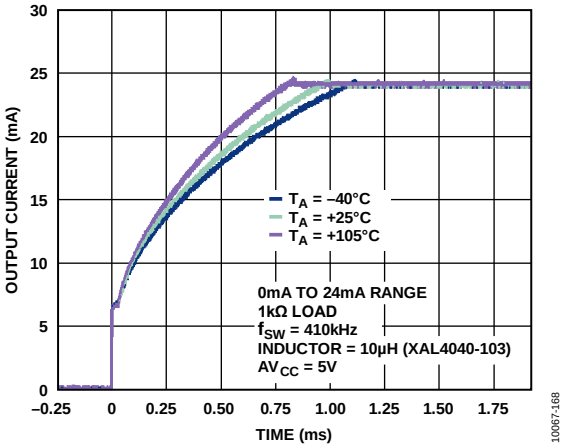


Figure 27. Output Current Settling Time with DC-to-DC Converter over Temperature (See Figure 56)

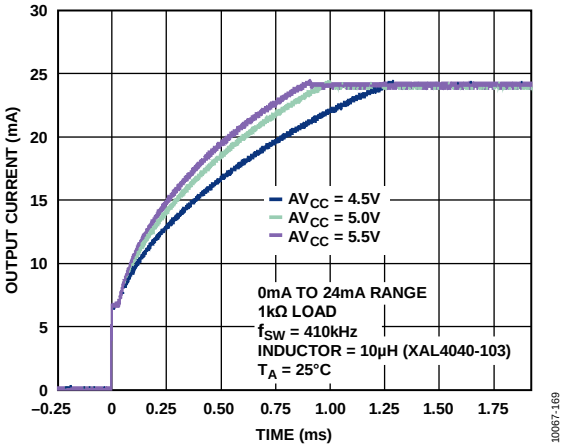


Figure 28. Output Current Settling Time with DC-to-DC Converter over AV_{CC} (See Figure 56)

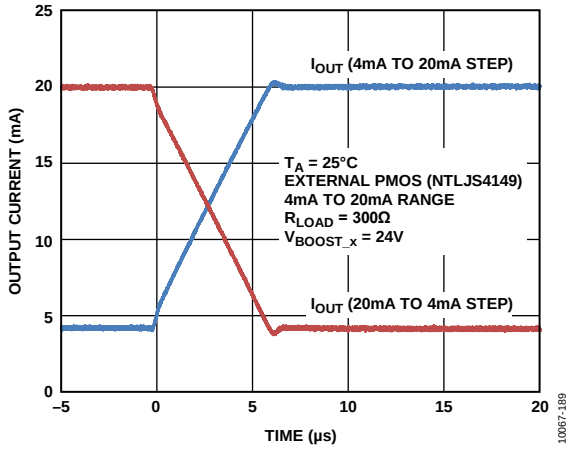


Figure 29. Output Current Settling Time with External PMOS Transistor

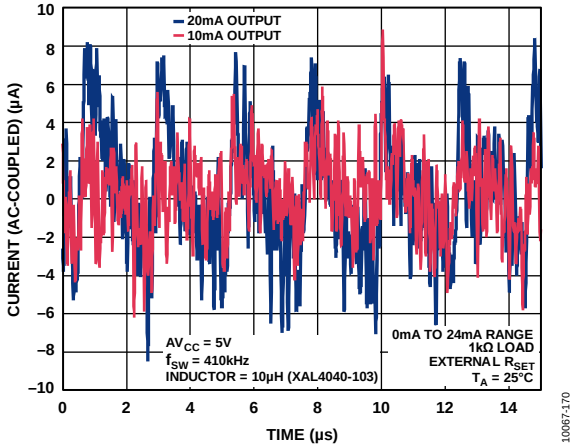


Figure 30. Output Current, AC-Coupled vs. Time with DC-to-DC Converter (See Figure 56)

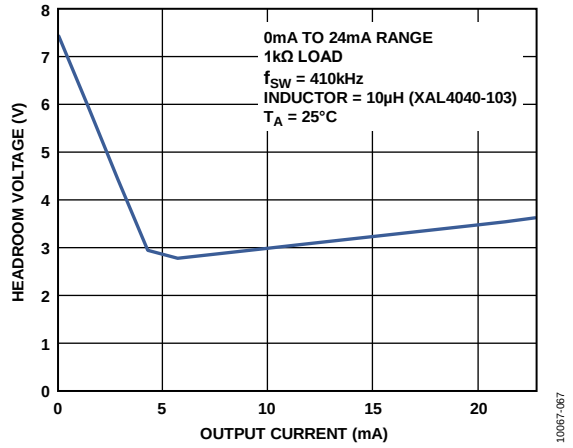


Figure 31. DC-to-DC Converter Headroom vs. Output Current (See Figure 56)

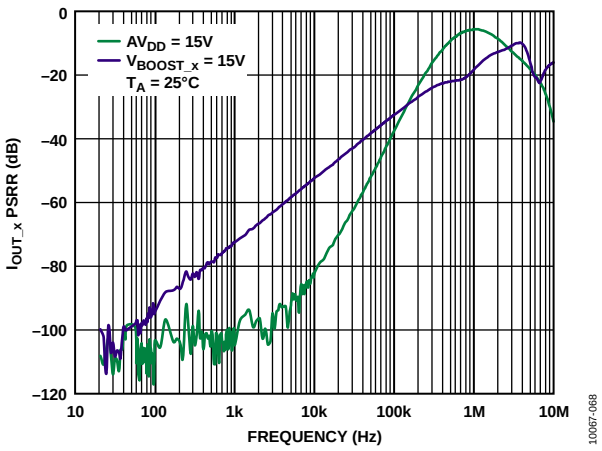


Figure 32. I_{OUT_x} PSRR vs. Frequency

DC-TO-DC CONVERTER

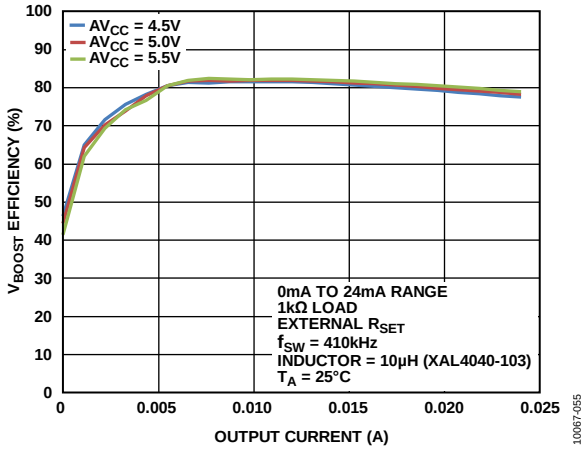


Figure 33. Efficiency at V_{BOOST_x} vs. Output Current (See Figure 56)

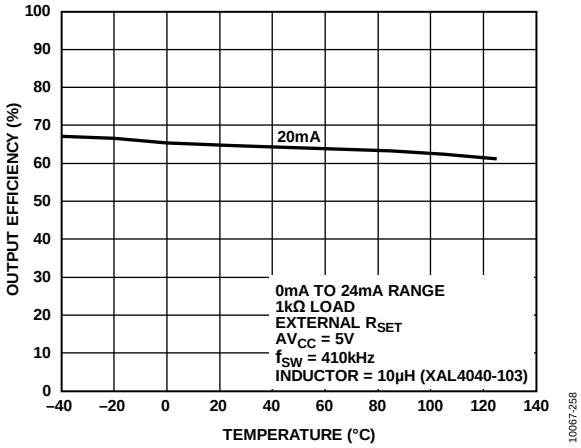


Figure 36. Output Efficiency vs. Temperature (See Figure 56)

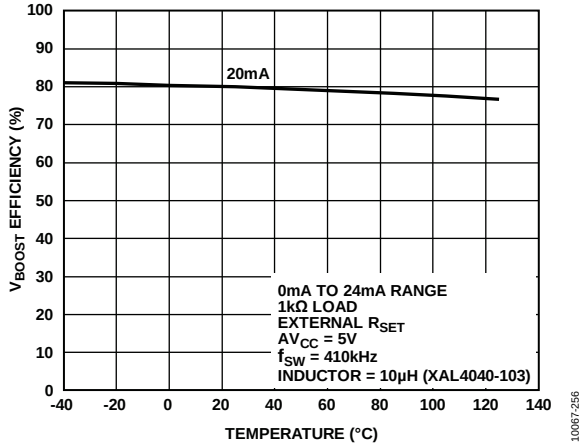


Figure 34. Efficiency at V_{BOOST_x} vs. Temperature (See Figure 56)

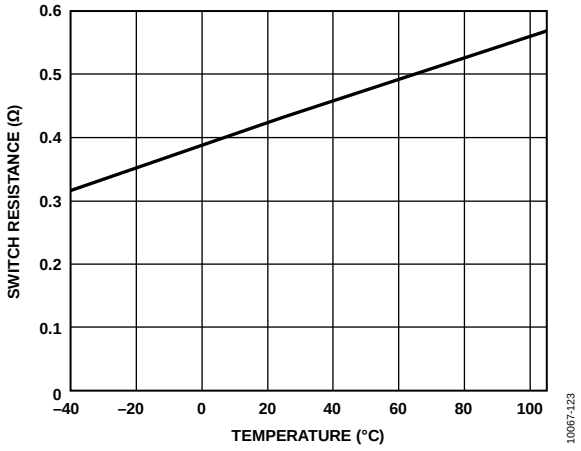


Figure 37. Switch Resistance vs. Temperature

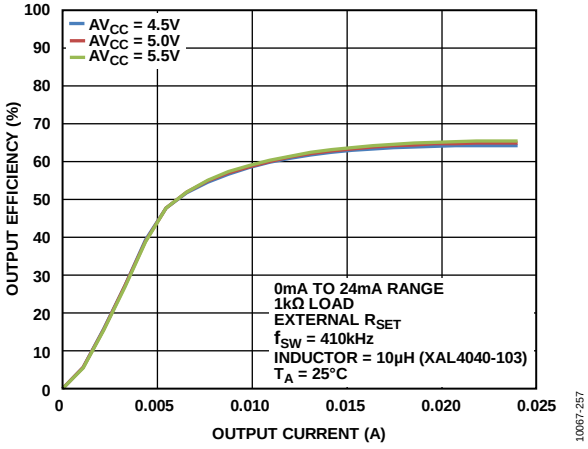


Figure 35. Output Efficiency vs. Output Current (See Figure 56)

REFERENCE

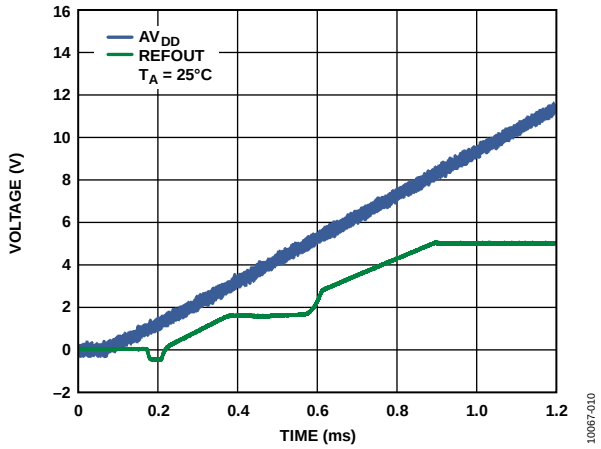


Figure 38. REFOUT Voltage Turn-On Transient

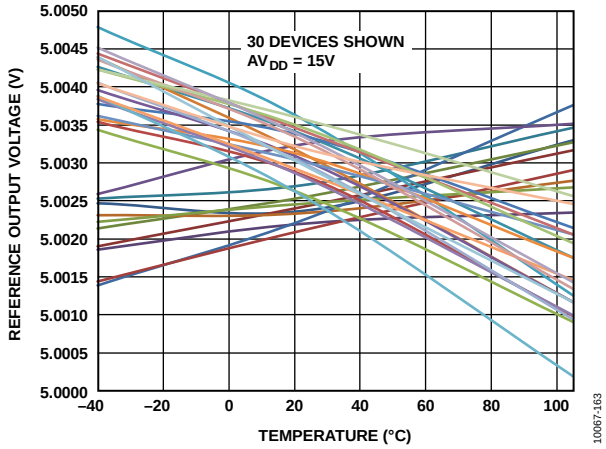


Figure 41. REFOUT Voltage vs. Temperature (When the AD5737 is soldered onto a PCB, the reference shifts due to thermal shock on the package. The average output voltage shift is −4 mV. Measurement of these parts after seven days shows that the outputs typically shift back 2 mV toward their initial values. This second shift is due to the relaxation of stress incurred during soldering.)

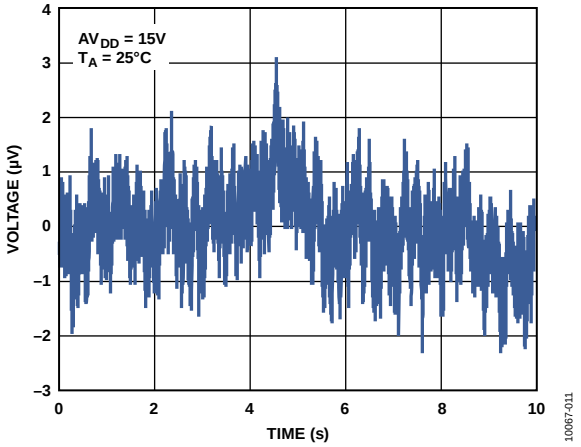


Figure 39. REFOUT Output Noise (0.1 Hz to 10 Hz Bandwidth)

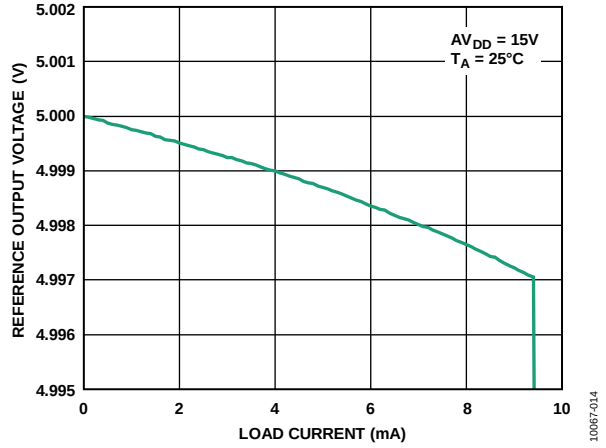


Figure 42. REFOUT Voltage vs. Load Current

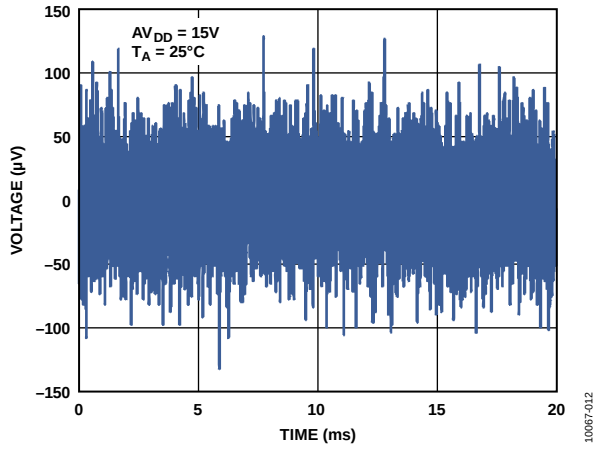


Figure 40. REFOUT Output Noise (100 kHz Bandwidth)

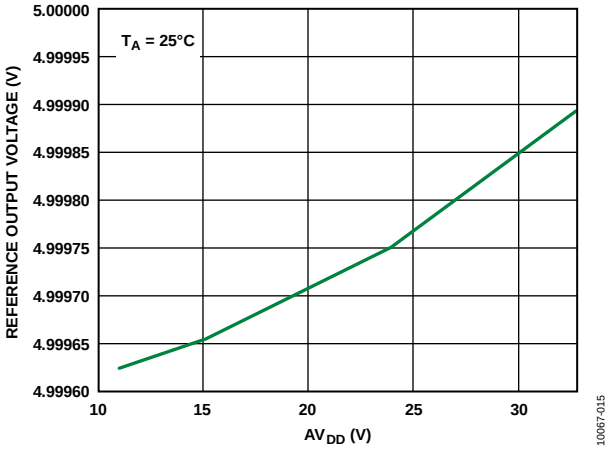


Figure 43. REFOUT Voltage vs. AV_{DD}

GENERAL

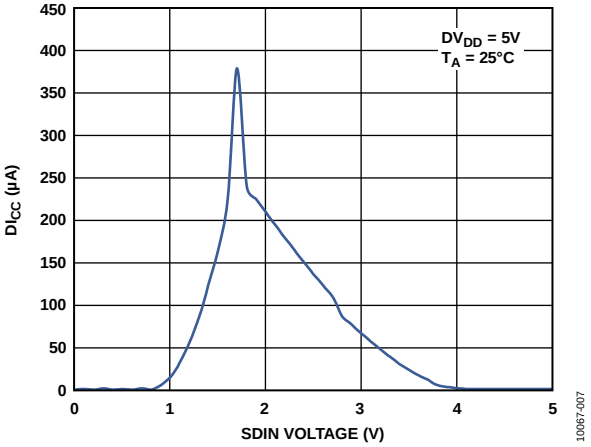


Figure 44. DI$_{CC}$ vs. Logic Input Voltage

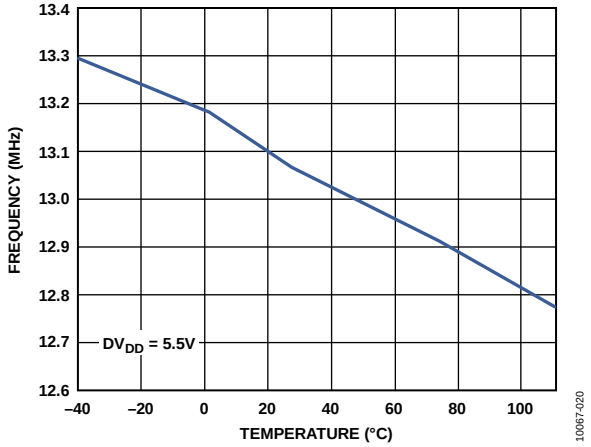


Figure 46. Internal Oscillator Frequency vs. Temperature

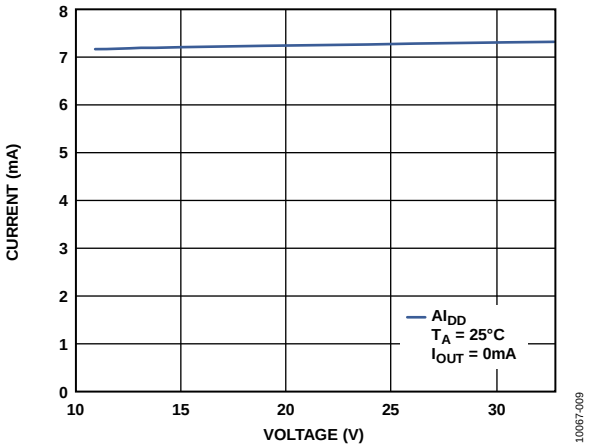


Figure 45. Supply Current (AI$_{DD}$) vs. Supply Voltage (AV$_{DD}$)

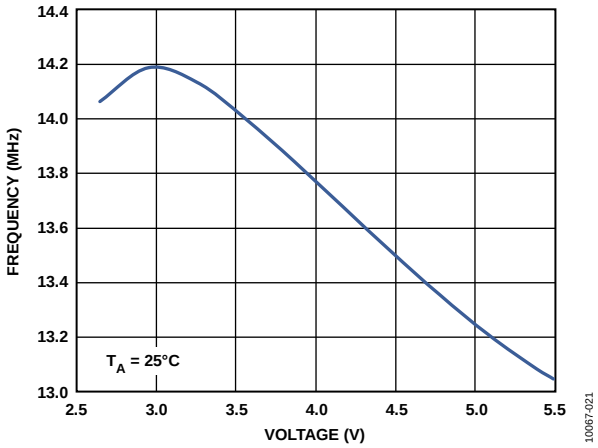


Figure 47. Internal Oscillator Frequency vs. DV$_{DD}$ Supply Voltage

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
Relative accuracy, or integral nonlinearity (INL), is a measure of the maximum deviation from the best fit line through the DAC transfer function. INL is expressed in percent of full-scale range (% FSR). A typical INL vs. code plot is shown in Figure 9.

Differential Nonlinearity (DNL)
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified DNL of ±1 LSB maximum ensures monotonicity. The AD5737 is guaranteed monotonic by design. A typical DNL vs. code plot is shown in Figure 10.

Monotonicity
A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5737 is monotonic over its full operating temperature range.

Offset Error
Offset error is the deviation of the analog output from the ideal zero-scale output when all DAC registers are loaded with 0x0000. It is expressed in % FSR.

Offset Error Drift or Offset TC
Offset error drift, or offset TC, is a measure of the change in offset error with changes in temperature and is expressed in ppm FSR/°C.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer function from the ideal, expressed in % FSR.

Gain Temperature Coefficient (TC)
Gain TC is a measure of the change in gain error with changes in temperature and is expressed in ppm FSR/°C.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code is loaded to the DAC register. Ideally, the output is full-scale − 1 LSB. Full-scale error is expressed in % FSR.

Full-Scale Temperature Coefficient (TC)
Full-scale TC is a measure of the change in full-scale error with changes in temperature and is expressed in ppm FSR/°C.

Total Unadjusted Error (TUE)
Total unadjusted error (TUE) is a measure of the output error that includes all the error measurements: INL error, offset error, gain error, temperature, and time. TUE is expressed in % FSR.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC, which is at midscale.

Current Loop Compliance Voltage
The current loop compliance voltage is the maximum voltage at the I_{OUT_x} pin for which the output current is equal to the programmed value.

Voltage Reference Thermal Hysteresis
Voltage reference thermal hysteresis is the difference in output voltage measured at +25°C compared to the output voltage measured at +25°C after cycling the temperature from +25°C to −40°C to +105°C and back to +25°C. The hysteresis is expressed in ppm.

Power-On Glitch Energy
Power-on glitch energy is the impulse injected into the analog output when the AD5737 is powered on. It is specified as the area of the glitch in nV-sec (see Figure 24).

Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the power supply voltage.

Reference Temperature Coefficient (TC)
Reference TC is a measure of the change in the reference output voltage with changes in temperature. It is expressed in ppm/°C.

Line Regulation
Line regulation is the change in the reference output voltage due to a specified change in supply voltage. It is expressed in ppm/V.

Load Regulation
Load regulation is the change in the reference output voltage due to a specified change in load current. It is expressed in ppm/mA.

DC-to-DC Converter Headroom
DC-to-DC converter headroom is the difference between the voltage required at the current output and the voltage supplied by the dc-to-dc converter (see Figure 31).

Output Efficiency

Output efficiency is defined as the ratio of the power delivered to a channel's load and the power delivered to the channel's dc-to-dc input. The V_{BOOST_x} quiescent current is considered part of the dc-to-dc converter's losses.

$$\frac{I_{OUT}{}^2 \times R_{LOAD}}{AV_{CC} \times AI_{CC}}$$

Efficiency at V_{BOOST_x}

The efficiency at V_{BOOST_x} is defined as the ratio of the power delivered to a channel's V_{BOOST_x} supply and the power delivered to the channel's dc-to-dc input. The V_{BOOST_x} quiescent current is considered part of the dc-to-dc converter's losses.

$$\frac{I_{OUT} \times V_{BOOST_x}}{AV_{CC} \times AI_{CC}}$$

THEORY OF OPERATION

The AD5737 is a quad, precision digital-to-current loop converter designed to meet the requirements of industrial process control applications. It provides a high precision, fully integrated, low cost, single-chip solution for generating current loop outputs. The current ranges available are 0 mA to 20 mA, 4 mA to 20 mA, and 0 mA to 24 mA. The output configuration is user-selectable via the DAC control register.

On-chip dynamic power control minimizes package power dissipation (see the Dynamic Power Control section).

DAC ARCHITECTURE

The DAC core architecture of the AD5737 consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 48. The four MSBs of the 12-bit data-word are decoded to drive 15 switches, E1 to E15. Each switch connects one of 15 matched resistors either to ground or to the reference buffer output. The remaining eight bits of the data-word drive Switch S0 to Switch S7 of an 8-bit voltage mode R-2R ladder network.

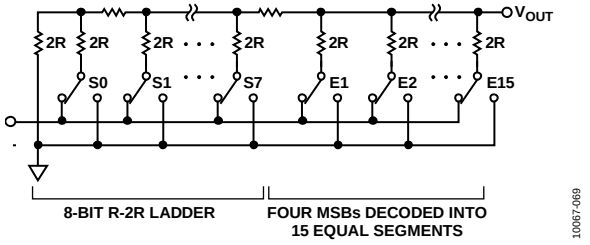


Figure 48. DAC Ladder Structure

The voltage output from the DAC core is converted to a current, which is then mirrored to the supply rail so that the application sees only a current source output (see Figure 49). The current outputs are supplied by V_{BOOST_x}.

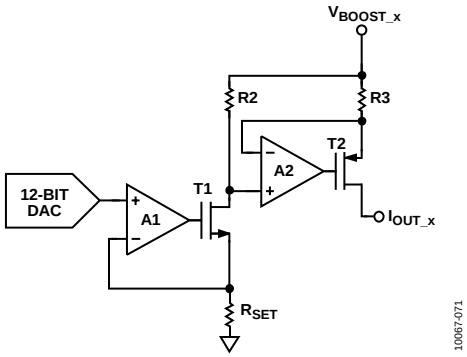


Figure 49. Voltage-to-Current Conversion Circuitry

Reference Buffers

The AD5737 can operate with either an external or internal reference. The reference input requires a 5 V reference for specified performance. This input voltage is then buffered before it is applied to the DAC.

POWER-ON STATE OF THE AD5737

When the AD5737 is first powered on, the I_{OUT_x} pins are in tristate mode. After a device power-on or a device reset, it is recommended that the user wait at least 100 µs before writing to the device to allow time for internal calibrations to take place.

SERIAL INTERFACE

The AD5737 is controlled by a versatile 3-wire serial interface that operates at clock rates of up to 30 MHz and is compatible with SPI, QSPI, MICROWIRE, and DSP standards. Data coding is always straight binary.

Input Shift Register

The input shift register is 24 bits wide. Data is loaded into the device MSB first as a 24-bit word under the control of the serial clock input, SCLK. Data is clocked in on the falling edge of SCLK.

If packet error checking (PEC) is enabled, an additional eight bits must be written to the AD5737, creating a 32-bit serial interface (see the Packet Error Checking section).

The DAC outputs can be updated in one of two ways: individual DAC updating or simultaneous updating of all DACs.

Individual DAC Updating

To update an individual DAC, $\overline{\text{LDAC}}$ is held low while data is clocked into the DAC data register. The addressed DAC output is updated on the rising edge of $\overline{\text{SYNC}}$. See Table 3 and Figure 3 for timing information.

Simultaneous Updating of All DACs

To update all DACs simultaneously, $\overline{\text{LDAC}}$ is held high while data is clocked into the DAC data register. After $\overline{\text{LDAC}}$ is taken high, only the first write to the DAC data register of each channel is valid; subsequent writes to the DAC data register are ignored, although these subsequent writes are returned if a readback is initiated. All DAC outputs are updated by taking $\overline{\text{LDAC}}$ low after $\overline{\text{SYNC}}$ is taken high.

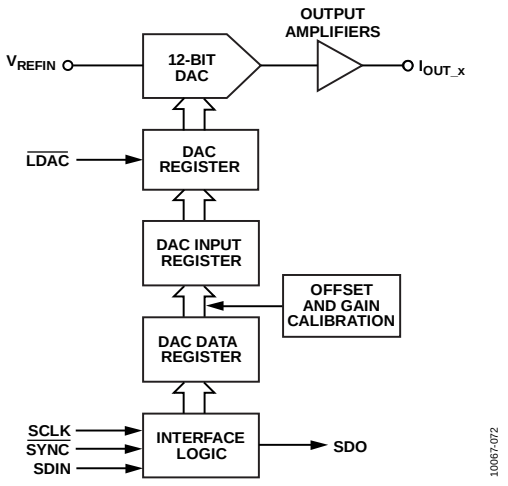


Figure 50. Simplified Serial Interface of the Input Loading Circuitry for One DAC Channel

TRANSFER FUNCTION

For the 0 mA to 20 mA, 0 mA to 24 mA, and 4 mA to 20 mA current output ranges, the output current is expressed by the following equations:

For the 0 mA to 20 mA range,

$$I_{OUT} = \left(\frac{20\,\text{mA}}{2^N} \right) \times D$$

For the 0 mA to 24 mA range,

$$I_{OUT} = \left(\frac{24\,\text{mA}}{2^N} \right) \times D$$

For the 4 mA to 20 mA range,

$$I_{OUT} = \left(\frac{16\,\text{mA}}{2^N} \right) \times D + 4\,\text{mA}$$

where:
D is the decimal equivalent of the code loaded to the DAC.
N is the bit resolution of the DAC.

REGISTERS

Table 7, Table 8, and Table 9 provide an overview of the registers for the AD5737.

Table 7. Data Registers for the AD5737

Register	Description
DAC Data Registers	The four DAC data registers (one register per DAC channel) are used to write a DAC code to each DAC channel. The DAC data bits are D15 to D4.
Gain Registers	The four gain registers (one register per DAC channel) are used to program the gain trim on a per-channel basis. The gain data bits are D15 to D4.
Offset Registers	The four offset registers (one register per DAC channel) are used to program the offset trim on a per-channel basis. The offset data bits are D15 to D4.
Clear Code Registers	The four clear code registers (one register per DAC channel) are used to program the clear code on a per-channel basis. The clear code data bits are D15 to D4.

Table 8. Control Registers for the AD5737

Register	Description
Main Control Register	The main control register is used to configure functions for the entire part. These functions include the following: enabling status readback during a write; enabling the output on all four DAC channels simultaneously; power-on of the dc-to-dc converter on all four DAC channels simultaneously; and enabling and configuring the watchdog timer. For more information, see the Main Control Register section.
DAC Control Registers	The four DAC control registers (one register per DAC channel) are used to configure the following functions on a per-channel basis: output range (for example, 4 mA to 20 mA); selection of the internal current sense resistor or an external current sense resistor; enabling/disabling the use of a clear code; enabling/disabling the internal circuitry (dc-to-dc converter, DAC, and internal amplifiers); power-on/power-off of the dc-to-dc converter; and enabling/disabling the output channel.
Software Register	The software register is used to perform a reset, to toggle the user bit in the status register, and, as part of the watchdog timer feature, to verify correct data communication operation.
DC-to-DC Control Register	The dc-to-dc control register is used to set the control parameters for the dc-to-dc converter: maximum output voltage, phase, and switching frequency. This register is also used to select the internal compensation resistor or an external compensation resistor for the dc-to-dc converter.
Slew Rate Control Registers	The four slew rate control registers (one register per DAC channel) are used to program the slew rate of the DAC output.

Table 9. Readback Register for the AD5737

Register	Description
Status Register	The status register contains any fault information, as well as a user toggle bit.

ENABLING THE OUTPUT

To correctly write to and set up the part from a power-on condition, use the following sequence:

1. Perform a hardware or software reset after initial power-on.
2. Configure the dc-to-dc converter supply block. Set the dc-to-dc switching frequency, the maximum output voltage allowed, and the dc-to-dc converter phase between channels.
3. Configure the DAC control register on a per-channel basis. Select the output range, and enable the dc-to-dc converter block (DC_DC bit). Other control bits can also be configured. Set the INT_ENABLE bit, but do not set the OUTEN (output enable) bit.
4. Write the required code to the DAC data register. This step implements a full internal DAC calibration. For reduced output glitch, allow at least 200 µs before performing Step 5.
5. Write to the DAC control register again to enable the output (set the OUTEN bit).

Figure 51 provides a flowchart of this sequence.

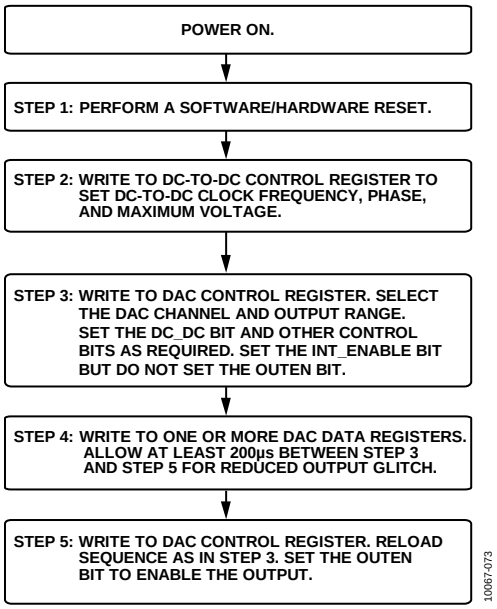


Figure 51. Programming Sequence to Correctly Enable the Output

REPROGRAMMING THE OUTPUT RANGE

When changing the range of an output, use the same sequence described in the Enabling the Output section. Set the range to 0 V (zero scale or midscale) before the output is disabled. Because the dc-to-dc switching frequency, maximum output voltage, and phase are already selected, there is no need to reprogram these values. Figure 52 provides a flowchart of this sequence.

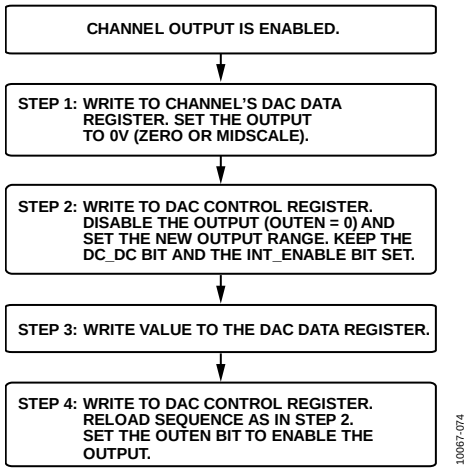


Figure 52. Programming Sequence to Change the Output Range

DATA REGISTERS

The input shift register is 24 bits wide. When PEC is enabled, the input shift register is 32 bits wide, with the last eight bits corresponding to the PEC code (see the Packet Error Checking section for more information about PEC). When writing to a data register, the format shown in Table 10 must be used.

DAC Data Register

When writing to a DAC data register, Bit D15 to Bit D4 are the DAC data bits. Table 12 shows the register format, and Table 11 describes the functions of Bit D23 to Bit D16.

Table 10. Input Shift Register for a Write Operation to a Data Register

MSB **LSB**

D23	D22	D21	D20	D19	D18	D17	D16	D15 to D0
R/$\overline{W}$	DUT_AD1	DUT_AD0	DREG2	DREG1	DREG0	DAC_AD1	DAC_AD0	Data

Table 11. Descriptions of Data Register Bits[D23:D16]

Bit Name	Description			
R/$\overline{W}$	This bit indicates whether the addressed register is written to or read from. 0 = write to the addressed register. 1 = read from the addressed register.			
DUT_AD1, DUT_AD0	Used in association with the external pins AD1 and AD0, these bits determine which AD5737 device is being addressed by the system controller. It is not recommended to tie both AD1 and AD0 low when using PEC (see the Packet Error Checking section).			
	DUT_AD1	**DUT_AD0**	**Part Addressed**	
	0	0	Pin AD1 = 0, Pin AD0 = 0	
	0	1	Pin AD1 = 0, Pin AD0 = 1	
	1	0	Pin AD1 = 1, Pin AD0 = 0	
	1	1	Pin AD1 = 1, Pin AD0 = 1	
DREG2, DREG1, DREG0	These bits select the register to be written to. If a control register is selected (DREG[2:0] = 111), the CREG bits in the control register select the specific control register to be written to (see Table 19).			
	DREG2	**DREG1**	**DREG0**	**Function**
	0	0	0	Write to DAC data register (one DAC channel)
	0	0	1	Reserved
	0	1	0	Write to gain register (one DAC channel)
	0	1	1	Write to gain registers (all DAC channels)
	1	0	0	Write to offset register (one DAC channel)
	1	0	1	Write to offset registers (all DAC channels)
	1	1	0	Write to clear code register (one DAC channel)
	1	1	1	Write to a control register
DAC_AD1, DAC_AD0	These bits are used to specify the DAC channel. If a write to the part does not apply to a specific DAC channel, these bits are don't care bits.			
	DAC_AD1	**DAC_AD0**	**DAC Channel**	
	0	0	DAC A	
	0	1	DAC B	
	1	0	DAC C	
	1	1	DAC D	

Table 12. Programming the DAC Data Register

D23	D22	D21	D20	D19	D18	D17	D16	D15 to D4	D3 to D0
R/$\overline{W}$	DUT_AD1	DUT_AD0	0	0	0	DAC_AD1	DAC_AD0	DAC data	X[1]

[1] X = don't care.

Gain Register

The 12-bit gain register allows the user to adjust the gain of each channel in steps of 1 LSB. To write to the gain register of one DAC channel, set the DREG[2:0] bits to 010 (see Table 13). To write the same gain code to all four DAC channels at the same time, set the DREG[2:0] bits to 011. The gain register coding is straight binary, as shown in Table 14. The default code in the gain register is 0xFFFF. The maximum recommended gain trim is approximately 50% of the programmed range to maintain accuracy (for more information, see the Digital Offset and Gain Control section).

Offset Register

The 12-bit offset register allows the user to adjust the offset of each channel by −2048 LSB to +2047 LSB in steps of 1 LSB. To write to the offset register of one DAC channel, set the DREG[2:0] bits to 100 (see Table 15). To write the same offset code to all four DAC channels at the same time, set the DREG[2:0] bits to 101. The offset register coding is straight binary, as shown in Table 16. The default code in the offset register is 0x8000, which results in zero offset programmed to the output (for more information, see the Digital Offset and Gain Control section).

Clear Code Register

The 12-bit clear code register allows the user to set the clear value of each channel. To configure a channel to be cleared when the CLEAR pin is activated, set the CLR_EN bit in the DAC control register for that channel (see Table 23). To write to the clear code register, set the DREG[2:0] bits to 110 (see Table 17). The default clear code is 0x0000 (for more information, see the Asynchronous Clear section).

Table 13. Programming the Gain Register

R/$\overline{W}$	DUT_AD1	DUT_AD0	DREG2	DREG1	DREG0	DAC_AD1	DAC_AD0	D15 to D4	D3 to D0
0	Device address		0	1	0	DAC channel address		Gain adjustment	1111

Table 14. Gain Register Bit Descriptions

Gain Adjustment	G15	G14	G13 to G5	G4	G3 to G0
+4096 LSB	1	1	111111111	1	1111
+4095 LSB	1	1	111111111	0	1111
…	…	…	…	…	1111
1 LSB	0	0	000000000	1	1111
0 LSB	0	0	000000000	0	1111

Table 15. Programming the Offset Register

R/$\overline{W}$	DUT_AD1	DUT_AD0	DREG2	DREG1	DREG0	DAC_AD1	DAC_AD0	D15 to D4	D3 to D0
0	Device address		1	0	0	DAC channel address		Offset adjustment	0000

Table 16. Offset Register Bit Descriptions

Offset Adjustment	OF15	OF14	OF13	OF12 to OF5	OF4	OF3 to OF0
+2047 LSB	1	1	1	11111111	1	0000
+2046 LSB	1	1	1	11111111	0	0000
…	…	…	…	…	…	0000
No Adjustment (Default)	1	0	0	00000000	0	0000
…	…	…	…	…	…	0000
−2047 LSB	0	0	0	00000000	1	0000
−2048 LSB	0	0	0	00000000	0	0000

Table 17. Programming the Clear Code Register

R/$\overline{W}$	DUT_AD1	DUT_AD0	DREG2	DREG1	DREG0	DAC_AD1	DAC_AD0	D15 to D4	D3 to D0
0	Device address		1	1	0	DAC channel address		Clear code	0000

CONTROL REGISTERS

When writing to a control register, the format shown in Table 18 must be used. See Table 11 for information about the configuration of Bit D23 to Bit D16. The control registers are addressed by setting the DREG[2:0] bits (Bits[D20:D18] in the input shift register) to 111 and then setting the CREG[2:0] bits to select the specific control register (see Table 19).

Main Control Register

The main control register options are shown in Table 20 and Table 21. See the Device Features section for more information about the features controlled by the main control register.

Table 18. Input Shift Register for a Write Operation to a Control Register

MSB **LSB**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12 to D0
R/$\overline{W}$	DUT_AD1	DUT_AD0	1	1	1	DAC_AD1	DAC_AD0	CREG2	CREG1	CREG0	Data

Table 19. Control Register Addresses (CREG[2:0] Bits)

CREG2 (D15)	CREG1 (D14)	CREG0 (D13)	Control Register
0	0	0	Slew rate control register (one per channel)
0	0	1	Main control register
0	1	0	DAC control register (one per channel)
0	1	1	DC-to-DC control register
1	0	0	Software register

Table 20. Programming the Main Control Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3 to D0
0	0	1	0	STATREAD	EWD	WD1	WD0	X[1]	X[1]	OUTEN_ALL	DCDC_ALL	X[1]

[1] X = don't care.

Table 21. Main Control Register Bit Descriptions

Bit Name	Description		
STATREAD	Enable status readback during a write. See the Status Readback During a Write section. 0 = disable status readback (default). 1 = enable status readback.		
EWD	Enable the watchdog timer. See the Watchdog Timer section. 0 = disable the watchdog timer (default). 1 = enable the watchdog timer.		
WD1, WD0	Timeout select bits. Used to select the timeout period for the watchdog timer.		
	WD1	**WD0**	**Timeout Period (ms)**
	0	0	5
	0	1	10
	1	0	100
	1	1	200
OUTEN_ALL	Setting this bit to 1 enables the output on all four DACs simultaneously. Do not use the OUTEN_ALL bit when using the OUTEN bit in the DAC control register.		
DCDC_ALL	Setting this bit to 1 powers up the dc-to-dc converter on all four channels simultaneously. To power down the dc-to-dc converters, all channel outputs must first be disabled. Do not use the DCDC_ALL bit when using the DC_DC bit in the DAC control register.		

DAC Control Register

The DAC control register is used to configure each DAC channel. The DAC control register options are shown in Table 22 and Table 23.

Table 22. Programming the DAC Control Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	X[1]	X[1]	X[1]	X[1]	INT_ENABLE	CLR_EN	OUTEN	RSET	DC_DC	X[1]	R2	R1	R0

[1] X = don't care.

Table 23. DAC Control Register Bit Descriptions

Bit Name	Description			
INT_ENABLE	Powers up the dc-to-dc converter, DAC, and internal amplifiers for the selected channel. This bit applies to individual channels only; it does not enable the output. After setting this bit, it is recommended that a >200 µs delay be observed before enabling the output to reduce the output enable glitch. See Figure 25 for plots of this glitch.			
CLR_EN	Per-channel clear enable bit. This bit specifies whether the selected channel is cleared when the CLEAR pin is activated. 0 = channel is not cleared when the part is cleared (default). 1 = channel is cleared when the part is cleared.			
OUTEN	Enables or disables the selected output channel. 0 = channel disabled (default). 1 = channel enabled.			
RSET	Selects the internal current sense resistor or an external current sense resistor for the selected DAC channel. 0 = external resistor selected (default). 1 = internal resistor selected.			
DC_DC	Powers up or powers down the dc-to-dc converter on the selected channel. All dc-to-dc converters can be powered up simultaneously using the DCDC_ALL bit in the main control register. To power down the dc-to-dc converter, the OUTEN and INT_ENABLE bits must also be set to 0. 0 = dc-to-dc converter is powered down (default). 1 = dc-to-dc converter is powered up.			
R2, R1, R0	Selects the output range to be enabled.			
	R2	**R1**	**R0**	**Output Range Selected**
	0	0	0	Reserved
	0	0	1	Reserved
	0	1	0	Reserved
	0	1	1	Reserved
	1	0	0	4 mA to 20 mA current range
	1	0	1	0 mA to 20 mA current range
	1	1	0	0 mA to 24 mA current range

Software Register

The software register allows the user to perform a software reset of the part. This register is also used to set the user toggle bit, D11, in the status register and as part of the watchdog timer feature when that feature is enabled.

Bit D12 in the software register can be used to ensure that communication has not been lost between the MCU and the AD5737 and that the datapath lines are working properly (that is, SDIN, SCLK, and $\overline{\text{SYNC}}$).

When the watchdog timer feature is enabled, the user must write 0x195 to Bits[D11:D0] of the software register within the timeout period. If this command is not received within the timeout period, the ALERT pin signals a fault condition. This command is only required when the watchdog timer feature is enabled.

DC-to-DC Control Register

The dc-to-dc control register allows the user to configure the dc-to-dc switching frequency and phase, as well as the maximum allowable dc-to-dc output voltage. The dc-to-dc control register options are shown in Table 26 and Table 27.

Table 24. Programming the Software Register

D15	D14	D13	D12	D11 to D0
1	0	0	User program	Reset code/SPI code

Table 25. Software Register Bit Descriptions

Bit Name	Description	
User Program	This bit is mapped to Bit D11 of the status register. When this bit is set to 1, Bit D11 of the status register is set to 1. When this bit is set to 0, Bit D11 of the status register is also set to 0. This feature can be used to ensure that the SPI pins are working correctly by writing a known bit value to this register and then reading back Bit D11 from the status register.	
Reset Code/SPI Code	**Option**	**Description**
	Reset code	Writing 0x555 to Bits[D11:D0] performs a software reset of the AD5737.
	SPI code	If the watchdog timer feature is enabled, 0x195 must be written to the software register (Bits[D11:D0]) within the programmed timeout period (see Table 21).

Table 26. Programming the DC-to-DC Control Register

D15	D14	D13	D12 to D7	D6	D5 to D4	D3 to D2	D1 to D0
0	1	1	X[1]	DC-DC comp	DC-DC phase	DC-DC freq	DC-DC MaxV

[1] X = don't care.

Table 27. DC-to-DC Control Register Bit Descriptions

Bit Name	Description
DC-DC Comp	Selects the internal compensation resistor or an external compensation resistor for the dc-to-dc converter. See the DC-to-DC Converter Compensation Capacitors section and the AI_{CC} Supply Requirements—Slewing section. 0 = selects the internal 150 kΩ compensation resistor (default). 1 = bypasses the internal compensation resistor. When this bit is set to 1, an external compensation resistor must be used; this resistor is placed at the $COMP_{DCDC_x}$ pin in series with the 10 nF dc-to-dc compensation capacitor to ground. Typically, a resistor of ~50 kΩ is recommended.
DC-DC Phase	User-programmable dc-to-dc converter phase (between channels). 00 = all dc-to-dc converters clock on the same edge (default). 01 = Channel A and Channel B clock on the same edge; Channel C and Channel D clock on the opposite edge. 10 = Channel A and Channel C clock on the same edge; Channel B and Channel D clock on the opposite edge. 11 = Channel A, Channel B, Channel C, and Channel D clock 90° out of phase from each other.
DC-DC Freq	Switching frequency for the dc-to-dc converter; this frequency is divided down from the internal 13 MHz oscillator (see Figure 46 and Figure 47). 00 = 250 kHz ± 10%. 01 = 410 kHz ± 10% (default). 10 = 650 kHz ± 10%.
DC-DC MaxV	Maximum allowed V_{BOOST_x} voltage supplied by the dc-to-dc converter. 00 = 23 V + 1 V/−1.5 V (default). 01 = 24.5 V ± 1 V. 10 = 27 V ± 1 V. 11 = 29.5 V ± 1 V.

Slew Rate Control Register

This register is used to program the slew rate control for the selected DAC channel. The slew rate control is enabled/disabled and programmed on a per-channel basis. See Table 28 and the Digital Slew Rate Control section for more information.

READBACK OPERATION

Readback mode is invoked by setting the R/$\overline{W}$ bit = 1 in the serial input register write. See Table 29 and Table 30 for the bits associated with a readback operation. The DUT_AD1 and DUT_AD0 bits, in association with bits RD[4:0], select the register to be read. The remaining data bits in the write sequence are don't cares.

During the next SPI transfer (see Figure 4), either a NOP or a request to read another register must be issued. Meanwhile the SDO returns 24 bits, the 8 MSBs are don't cares, and the 16 LSBs contain the data from the addressed register. The SDO is loaded on each rising edge of SCLK and read on each falling edge of SCLK.

If PEC is enabled, the SDO returns 32 bits (see Figure 5), with 8 CRC bits appended to the data readback. There must be no activity on SCLK between read command and NOP command, or an incorrect PEC may be read back.

Readback Example

To read back the gain register of AD5737 Device 1, Channel A, implement the following sequence:

1. Write 0xA80000 to the input register to configure Device Address 1 for read mode with the gain register of Channel A selected. The data bits, D15 to D0, are don't care bits.
2. Execute another read command or a no operation command (0x3CE000). During this command, the data from the Channel A gain register is clocked out on the SDO line.

Table 28. Programming the Slew Rate Control Register

D15	D14	D13	D12	D11 to D7	D6 to D3	D2 to D0
0	0	0	SREN	X[1]	SR_CLOCK	SR_STEP

[1] X = don't care.

Table 29. Input Shift Register for a Read Operation

MSB **LSB**

D23	D22	D21	D20	D19	D18	D17	D16	D15 to D0
R/$\overline{W}$	DUT_AD1	DUT_AD0	RD4	RD3	RD2	RD1	RD0	X[1]

[1] X = don't care.

Table 30. Read Addresses (Bits[RD4:RD0])

RD4	RD3	RD2	RD1	RD0	Function
0	0	0	0	0	Read DAC A data register
0	0	0	0	1	Read DAC B data register
0	0	0	1	0	Read DAC C data register
0	0	0	1	1	Read DAC D data register
0	0	1	0	0	Read DAC A control register
0	0	1	0	1	Read DAC B control register
0	0	1	1	0	Read DAC C control register
0	0	1	1	1	Read DAC D control register
0	1	0	0	0	Read DAC A gain register
0	1	0	0	1	Read DAC B gain register
0	1	0	1	0	Read DAC C gain register
0	1	0	1	1	Read DAC D gain register
0	1	1	0	0	Read DAC A offset register
0	1	1	0	1	Read DAC B offset register
0	1	1	1	0	Read DAC C offset register
0	1	1	1	1	Read DAC D offset register
1	0	0	0	0	Read DAC A clear code register
1	0	0	0	1	Read DAC B clear code register
1	0	0	1	0	Read DAC C clear code register
1	0	0	1	1	Read DAC D clear code register
1	0	1	0	0	Read DAC A slew rate control register
1	0	1	0	1	Read DAC B slew rate control register
1	0	1	1	0	Read DAC C slew rate control register
1	0	1	1	1	Read DAC D slew rate control register
1	1	0	0	0	Read status register
1	1	0	0	1	Read main control register
1	1	0	1	0	Read dc-to-dc control register

Status Register

The status register is a read-only register. This register contains any fault information, as a well as a ramp active bit (Bit D9) and the status of the packet error checking feature (Bit D10). When the STATREAD bit in the main control register is set, the status register contents can be read back on the SDO pin during every write sequence. Alternatively, if the STATREAD bit is not set, the status register can be read using the normal readback operation (see the Readback Operation section).

Table 31. Decoding the Status Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
DC-DCD	DC-DCC	DC-DCB	DC-DCA	User toggle	PEC error	Ramp active	Over temp	X[1]	X[1]	X[1]	X[1]	I_{OUT_D} fault	I_{OUT_C} fault	I_{OUT_B} fault	I_{OUT_A} fault

[1] X = don't care.

Table 32. Status Register Bit Descriptions

Bit Name	Description
DC-DCD	This bit is set if the dc-to-dc converter on Channel D cannot maintain compliance, for example, if the dc-to-dc converter is reaching its V_{MAX} voltage; in this case, the I_{OUT_D} fault bit is also set. See the DC-to-DC Converter V_{MAX} Functionality section for more information about the operation of this bit under this condition.
DC-DCC	This bit is set if the dc-to-dc converter on Channel C cannot maintain compliance, for example, if the dc-to-dc converter is reaching its V_{MAX} voltage; in this case, the I_{OUT_C} fault bit is also set. See the DC-to-DC Converter V_{MAX} Functionality section for more information about the operation of this bit under this condition.
DC-DCB	This bit is set if the dc-to-dc converter on Channel B cannot maintain compliance, for example, if the dc-to-dc converter is reaching its V_{MAX} voltage; in this case, the I_{OUT_B} fault bit is also set. See the DC-to-DC Converter V_{MAX} Functionality section for more information about the operation of this bit under this condition.
DC-DCA	This bit is set if the dc-to-dc converter on Channel A cannot maintain compliance, for example, if the dc-to-dc converter is reaching its V_{MAX} voltage; in this case, the I_{OUT_A} fault bit is also set. See the DC-to-DC Converter V_{MAX} Functionality section for more information about the operation of this bit under this condition.
User Toggle	User toggle bit. This bit is set or cleared via the software register and can be used to verify data communications, if needed.
PEC Error	Denotes a PEC error on the last data-word received over the SPI interface.
Ramp Active	This bit is set while any output channel is slewing (digital slew rate control is enabled on at least one channel).
Over Temp	This bit is set if the AD5737 core temperature exceeds approximately 150°C.
I_{OUT_D} Fault	This bit is set if a fault is detected on the I_{OUT_D} pin.
I_{OUT_C} Fault	This bit is set if a fault is detected on the I_{OUT_C} pin.
I_{OUT_B} Fault	This bit is set if a fault is detected on the I_{OUT_B} pin.
I_{OUT_A} Fault	This bit is set if a fault is detected on the I_{OUT_A} pin.

DEVICE FEATURES

FAULT OUTPUT

The AD5737 is equipped with a $\overline{\text{FAULT}}$ pin, an active low, open-drain output that allows several AD5737 devices to be connected together to one pull-up resistor for global fault detection. The $\overline{\text{FAULT}}$ pin is forced active by any one of the following fault conditions:

- The voltage at I_{OUT_x} attempts to rise above the compliance range due to an open-loop circuit or insufficient power supply voltage. The internal circuitry that develops the fault output avoids using a comparator with windowed limits because this requires an actual output error before the $\overline{\text{FAULT}}$ output becomes active. Instead, the signal is generated when the internal amplifier in the output stage has less than approximately 1 V of remaining drive capability. Thus, the $\overline{\text{FAULT}}$ output is activated slightly before the compliance limit is reached.
- An interface error is detected due to a PEC failure (see the Packet Error Checking section).
- The core temperature of the AD5737 exceeds approximately 150°C.

The I_{OUT_x} fault, PEC error, and over temp bits of the status register are used in conjunction with the $\overline{\text{FAULT}}$ output to inform the user which fault condition caused the $\overline{\text{FAULT}}$ output to be activated.

DIGITAL OFFSET AND GAIN CONTROL

Each DAC channel has a gain (M) register and an offset (C) register, which allow trimming out of the gain and offset errors of the entire signal chain. Data from the DAC data register is operated on by a digital multiplier and adder controlled by the contents of the gain and offset registers; the calibrated DAC data is then stored in the DAC input register (see Figure 53).

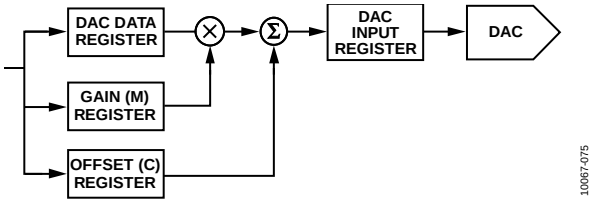


Figure 53. Digital Offset and Gain Control

Although Figure 53 indicates a multiplier and adder for each channel, the device has only one multiplier and one adder, which are shared by all four channels. This design has implications for the update speed when several channels are updated at once (see Table 3).

When data is written to the gain (M) or offset (C) register, the output is not automatically updated. Instead, the next write to the DAC channel uses the new gain and offset values to perform a new calibration and automatically updates the channel.

The output data from the calibration is routed to the DAC input register. This data is then loaded to the DAC, as described in the Serial Interface section. Both the gain register and the offset register have 12 bits of resolution. The correct order to calibrate the gain and offset is to first calibrate the gain and then calibrate the offset.

The value (in decimal) that is written to the DAC input register can be calculated as follows:

$$Code_{DACRegister} = D \times \frac{(M+1)}{2^{12}} + C - 2^{11} \quad (1)$$

where:
D is the code loaded to the DAC data register of the DAC channel.
M is the code in the gain register (default code = $2^{12} - 1$).
C is the code in the offset register (default code = 2^{11}).

STATUS READBACK DURING A WRITE

The AD5737 can be configured to read back the contents of the status register during every write sequence. This feature is enabled using the STATREAD bit in the main control register. When this feature is enabled, the user can continuously monitor the status register and act quickly in the case of a fault.

When status readback during a write is enabled, the contents of the 16-bit status register (see Table 32) are output on the SDO pin, as shown in Figure 5.

When the AD5737 is powered up, the status readback during a write feature is disabled. When this feature is enabled, readback of registers other than the status register is not available. To read back any other register, clear the STATREAD bit before following the readback sequence (see the Readback Operation section). The STATREAD bit can be set high again after the register read.

If multiple units on the same SDO bus have the STATREAD feature enabled, ensure that each unit is provided a unique physical address (AD1 and AD0) to prevent contention on the bus.

If packet error checking is enabled, ignore the PEC values returned on a status readback during a write operation. See the Packet Error Checking section.

ASYNCHRONOUS CLEAR

CLEAR is an active high, edge sensitive input that allows the output to be cleared to a preprogrammed 12-bit code. This code is user-programmable via a per-channel 12-bit clear code register.

For a channel to be cleared, set the CLR_EN bit in the DAC control register for that channel. If the clear function on a channel is not enabled, the output remains in its current state, independent of the level of the CLEAR pin.

When the CLEAR signal returns low, the relevant outputs remain cleared until a new value is programmed to them.

The CLEAR pin must not be asserted between the first and second commands of a normal SPI read when SYNC is high

(represented by t6 in Figure 4). Failure to comply with this will result in the DAC outputs not being cleared and may cause the AD5737 SPI port to become unresponsive requiring a hardware reset to restore SPI communications. If automatic readback of status registers is enabled then there are no restrictions to the use of the CLEAR pin.

PACKET ERROR CHECKING

To verify that data has been received correctly in noisy environments, the AD5737 offers the option of packet error checking based on an 8-bit cyclic redundancy check (CRC-8). The device controlling the AD5737 generates an 8-bit frame check sequence using the following polynomial:

$$C(x) = x_8 + x_2 + x_1 + 1$$

This value is added to the end of the data-word, and 32 bits are sent to the AD5737 before $\overline{\text{SYNC}}$ goes high. If the AD5737 sees a 32-bit frame, it performs the error check when $\overline{\text{SYNC}}$ goes high. If the error check is valid, the data is written to the selected register. If the error check fails, the $\overline{\text{FAULT}}$ pin goes low and the PEC error bit in the status register is set. After the status register is read, $\overline{\text{FAULT}}$ returns high (assuming that there are no other faults), and the PEC error bit is cleared automatically. It is not recommended to tie both AD1 and AD0 low as a short low on SDIN could possibly lead to a zero-scale update for DAC A.

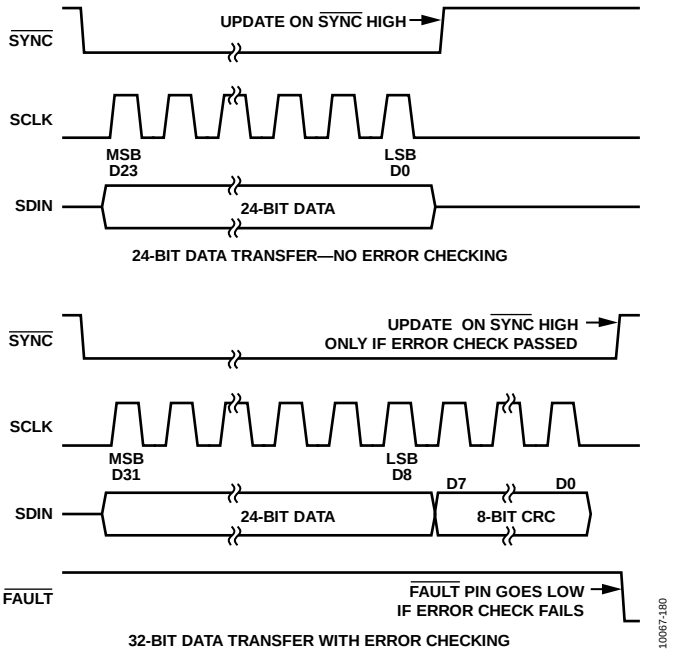


Figure 54. PEC Timing

Packet error checking can be used for transmitting and receiving data packets. If status readback during a write is enabled, ignore the PEC values returned during the status readback operation. If status readback during a write is disabled, the user can still use the normal readback operation to monitor status register activity with PEC.

If PEC is enabled when receiving data packets, there must be no activity on SCLK between the read command and the NOP command, or an incorrect PEC may be read back. See Figure 5 and the Readback Operation section for further information.

WATCHDOG TIMER

When enabled, an on-chip watchdog timer generates an alert signal if 0x195 is not written to the software register within the programmed timeout period. This feature is useful to ensure that communication is not lost between the MCU and the AD5737 and that the datapath lines are working properly (that is, SDIN, SCLK, and $\overline{\text{SYNC}}$). If 0x195 is not received by the software register within the timeout period, the ALERT pin signals a fault condition. The ALERT pin is active high and can be connected directly to the CLEAR pin to enable a clear in the event that communication from the MCU is lost.

To enable the watchdog timer and set the timeout period (5 ms, 10 ms, 100 ms, or 200 ms), program the main control register (see Table 20 and Table 21).

ALERT OUTPUT

The AD5737 is equipped with an ALERT pin. This pin is an active high CMOS output. The AD5737 also has an internal watchdog timer. When enabled, the watchdog timer monitors SPI communications. If 0x195 is not received by the software register within the timeout period, the ALERT pin is activated.

INTERNAL REFERENCE

The AD5737 contains an integrated 5 V voltage reference with initial accuracy of ±5 mV maximum and a temperature coefficient of ±10 ppm/°C maximum. The reference voltage is buffered and is externally available for use elsewhere within the system. REFOUT must be connected to REFIN to use the internal reference.

EXTERNAL CURRENT SETTING RESISTOR

R_{SET} is an internal sense resistor that is part of the voltage-to-current conversion circuitry (see Figure 49). The stability of the output current value over temperature is dependent on the stability of the R_{SET} value. To improve the stability of the output current over temperature, the internal R_{SET} resistor, R1, can be bypassed and an external, 15 kΩ, low drift resistor can be connected to the R_{SET_x} pin of theAD5737. The external resistor is selected via the DAC control register (see Table 23).

Table 1 provides the performance specifications for the AD5737 with both the internal R_{SET} resistor and an external, 15 kΩ R_{SET} resistor. The use of an external R_{SET} resistor allows for improved performance over the internal R_{SET} resistor option. The external R_{SET} resistor specifications assume an ideal resistor; the actual performance depends on the absolute value and temperature coefficient of the resistor used. This directly affects the gain error of the output and, thus, the total unadjusted error. To arrive at the gain/TUE error of the output with a specific external R_{SET} resistor, add the absolute error percentage of the R_{SET} resistor directly to the gain/TUE error of the AD5737 with the external R_{SET} resistor, as shown in Table 1 (expressed in % FSR).

HART CONNECTIVITY

The AD5737 has four CHART pins, one corresponding to each output channel. A HART signal can be coupled into these pins. The HART signal appears on the corresponding current output, if the output is enabled. Table 33 shows the recommended input voltages for the HART signal at the CHART pin. If these voltages are used, the current output meets HART amplitude specifications.

Table 33. CHART Input Voltage to HART Output Current

R_{SET}	CHART Input Voltage	Current Output (HART)
Internal R_{SET}	150 mV p-p	1 mA p-p
External R_{SET}	170 mV p-p	1 mA p-p

Figure 55 shows the recommended circuit for attenuating and coupling the HART signal. A minimum capacitance of C1 + C2 is required to ensure that the 1.2 kHz and 2.2 kHz HART frequencies are not significantly attenuated at the output. The recommended values are C1 = 22 nF and C2 = 47 nF.

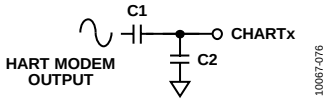


Figure 55. Coupling the HART Signal

Digitally controlling the slew rate of the output is necessary to meet the analog rate of change requirements for HART.

If the HART feature is not required, leave the CHART pins open circuit.

DIGITAL SLEW RATE CONTROL

The digital slew rate control feature of the AD5737 allows the user to control the rate at which the output value changes. With the slew rate control feature disabled, the output value changes at a rate limited by the output drive circuitry and the attached load. To reduce the slew rate, the user can enable the digital slew rate control feature using the SREN bit of the slew rate control register (see Table 28).

When slew rate control is enabled, the output, instead of slewing directly between two values, steps digitally at a rate defined by the SR_CLOCK and SR_STEP parameters. These parameters are accessible via the slew rate control register (see Table 28).

- SR_CLOCK defines the rate at which the digital slew is updated; for example, if the selected update rate is 8 kHz, the output is updated every 125 µs.
- SR_STEP defines by how much the output value changes at each update.

Together, these parameters define the rate of change of the output value. Table 34 and Table 35 list the range of values for the SR_CLOCK and SR_STEP parameters, respectively.

Table 34. Slew Rate Update Clock Options

SR_CLOCK	Update Clock Frequency[1]
0000	64 kHz
0001	32 kHz
0010	16 kHz
0011	8 kHz
0100	4 kHz
0101	2 kHz
0110	1 kHz
0111	500 Hz
1000	250 Hz
1001	125 Hz
1010	64 Hz
1011	32 Hz
1100	16 Hz
1101	8 Hz
1110	4 Hz
1111	0.5 Hz

[1] These clock frequencies are divided down from the 13 MHz internal oscillator (see Table 1, Figure 46, and Figure 47).

Table 35. Slew Rate Step Size Options

SR_STEP	Step Size (LSB)
000	1
001	2
010	4
011	16
100	32
101	64
110	128
111	256

The following equation describes the slew rate as a function of the step size, the update clock frequency, and the LSB size.

$$Slew\ Rate = \frac{Output\ Change}{Step\ Size \times Update\ Clock\ Frequency \times LSB\ Size}$$

where:
Slew Rate is expressed in seconds.
Output Change is expressed in amperes.

The update clock frequency for any given value is the same for all output ranges. The step size, however, varies across output ranges for a given value of step size because the LSB size is different for each output range.

When the slew rate control feature is enabled, all output changes occur at the programmed slew rate (see the DC-to-DC Converter Settling Time section for more information). For example, if the CLEAR pin is asserted, the output slews to the clear value at the programmed slew rate (assuming that the channel is enabled to be cleared).

If more than one channel is enabled for digital slew rate control, care must be taken when asserting the CLEAR pin. If a channel under slew rate control is slewing when the CLEAR pin is asserted, other channels under slew rate control may change directly to their clear code not under slew rate control.

DYNAMIC POWER CONTROL

The AD5737 provides integrated dynamic power control using a dc-to-dc boost converter circuit. This circuit reduces power consumption compared with standard designs.

In standard current input module designs, the load resistor values can range from typically 50 Ω to 750 Ω. Output module systems must source enough voltage to meet the compliance voltage requirement across the full range of load resistor values. For example, in a 4 mA to 20 mA loop when driving 20 mA, a compliance voltage of >15 V is required. When driving 20 mA into a 50 Ω load, a compliance voltage of only 1 V is required.

The AD5737 circuitry senses the output voltage and regulates this voltage to meet the compliance requirements plus a small headroom voltage. The AD5737 is capable of driving up to 24 mA through a 1 kΩ load.

DC-TO-DC CONVERTERS

The AD5737 contains four independent dc-to-dc converters. These are used to provide dynamic control of the V_{BOOST_x} supply voltage for each channel (see Figure 49). Figure 56 shows the discrete components needed for the dc-to-dc circuitry, and the following sections describe component selection and operation of this circuitry.

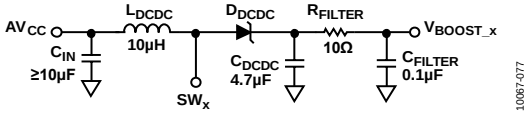


Figure 56. DC-to-DC Circuit

Table 36. Recommended Components for a DC-to-DC Converter

Symbol	Component	Value	Manufacturer
L_{DCDC}	XAL4040-103	10 µH	Coilcraft®
C_{DCDC}	GRM32ER71H475KA88L	4.7 µF	Murata
D_{DCDC}	PD3S160-7	0.55 V_F	Diodes, Inc.

It is recommended that a 10 Ω, 100 nF low-pass RC filter be placed after C_{DCDC}. This filter consumes a small amount of power but reduces the amount of ripple on the V_{BOOST_x} supply.

DC-to-DC Converter Operation

The on-board dc-to-dc converters use a constant frequency, peak current mode control scheme to step up an AV_{CC} input of 4.5 V to 5.5 V to drive the AD5737 output channel. These converters are designed to operate in discontinuous conduction mode with a duty cycle of <90% typical. Discontinuous conduction mode refers to a mode of operation where the inductor current goes to zero for an appreciable percentage of the switching cycle. The dc-to-dc converters are nonsynchronous; that is, they require an external Schottky diode.

DC-to-DC Converter Output Voltage

When a channel current output is enabled, the converter regulates the V_{BOOST_x} supply to 7.4 V (±5%) or ($I_{OUT} \times R_{LOAD}$ + Headroom), whichever is greater (see Figure 31 for a plot of headroom supplied vs. output current). When the output is disabled, the converter regulates the V_{BOOST_x} supply to 7.4 V (±5%).

DC-to-DC Converter Settling Time

The settling time for a step greater than ~1 V ($I_{OUT} \times R_{LOAD}$) is dominated by the settling time of the dc-to-dc converter. The exception to this is when the required voltage at the I_{OUT_x} pin plus the compliance voltage is below 7.4 V (±5%). Figure 26 shows a typical plot of the output settling time. This plot is for a 1 kΩ load. The settling time for smaller loads is faster. The settling time for current steps less than 24 mA is also faster.

DC-to-DC Converter V_{MAX} Functionality

The maximum V_{BOOST_x} voltage is set in the dc-to-dc control register (23 V, 24.5 V, 27 V, or 29.5 V; see Table 27). When the maximum voltage is reached, the dc-to-dc converter is disabled, and the V_{BOOST_x} voltage is allowed to decay by ~0.4 V. After the V_{BOOST_x} voltage decays by ~0.4 V, the dc-to-dc converter is reenabled, and the voltage ramps up again to V_{MAX}, if still required. This operation is shown in Figure 57.

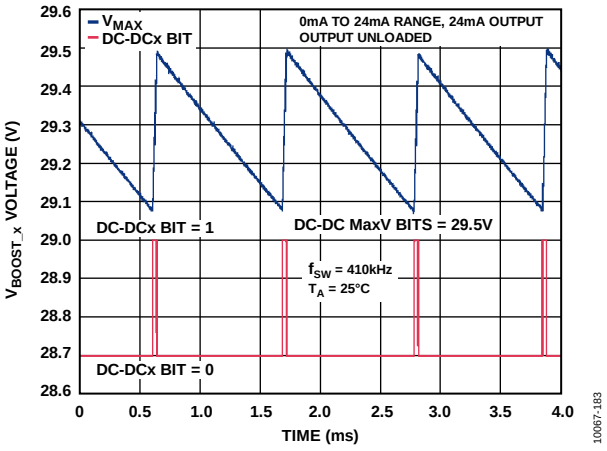


Figure 57. Operation on Reaching V_{MAX}

As shown in Figure 57, the DC-DCx bit in the status register is asserted when the AD5737 ramps up to the V_{MAX} value but is deasserted when the voltage decays to V_{MAX} − ~0.4 V.

DC-to-DC Converter On-Board Switch

The AD5737 contains a 0.425 Ω internal switch. The switch current is monitored on a pulse-by-pulse basis and is limited to 0.8 A peak current.

DC-to-DC Converter Switching Frequency and Phase

The AD5737 dc-to-dc converter switching frequency can be selected from the dc-to-dc control register (see Table 27). The phasing of the channels can also be adjusted so that the dc-to-dc converters can clock on different edges. For typical applications, a 410 kHz frequency is recommended. At light loads (low output current and small load resistor), the dc-to-dc converter enters a pulse-skipping mode to minimize switching power dissipation.

DC-to-DC Converter Inductor Selection

For typical 4 mA to 20 mA applications, a 10 µH inductor (such as the XAL4040-103 from Coilcraft), combined with a switching frequency of 410 kHz, allows up to 24 mA to be driven into a load resistance of up to 1 kΩ with an AV_{CC} supply of 4.5 V to 5.5 V. It is important to ensure that the inductor can handle the peak current without saturating, especially at the maximum ambient temperature. If the inductor enters saturation mode, efficiency decreases. The inductance value also drops during saturation and may result in the dc-to-dc converter circuit not being able to supply the required output power.

DC-to-DC Converter External Schottky Diode Selection

The AD5737 requires an external Schottky diode for correct operation. Ensure that the Schottky diode is rated to handle the maximum reverse breakdown voltage expected in operation and that the maximum junction temperature of the diode is not exceeded. The average current of the diode is approximately equal to the I_{LOAD} current. Diodes with larger forward voltage drops result in a decrease in efficiency.

DC-to-DC Converter Compensation Capacitors

Because the dc-to-dc converter operates in discontinuous conduction mode, the uncompensated transfer function is essentially a single-pole transfer function. The pole frequency of the transfer function is determined by the output capacitance, input and output voltage, and output load of the dc-to-dc converter. The AD5737 uses an external capacitor in conjunction with an internal 150 kΩ resistor to compensate the regulator loop.

Alternatively, an external compensation resistor can be used in series with the compensation capacitor by setting the DC-DC comp bit in the dc-to-dc control register (see Table 27). In this case, a resistor of ~50 kΩ is recommended. The advantages of this configuration are described in the AI_{CC} Supply Requirements—Slewing section. For typical applications, a 10 nF dc-to-dc compensation capacitor is recommended.

DC-to-DC Converter Input and Output Capacitor Selection

The output capacitor affects the ripple voltage of the dc-to-dc converter and indirectly limits the maximum slew rate at which the channel output current can rise. The ripple voltage is caused by a combination of the capacitance and the equivalent series resistance (ESR) of the capacitor. For typical applications, a ceramic capacitor of 4.7 µF is recommended. Larger capacitors or parallel capacitors improve the ripple at the expense of reduced slew rate. Larger capacitors also affect the current requirements of the AV_{CC} supply while slewing (see the AI_{CC} Supply Requirements—Slewing section). The capacitance at the output of the dc-to-dc converter must be >3 µF under all operating conditions.

The input capacitor provides much of the dynamic current required for the dc-to-dc converter and must be a low ESR component. For the AD5737, a low ESR tantalum or ceramic capacitor of 10 µF is recommended for typical applications. Ceramic capacitors must be chosen carefully because they can exhibit a large sensitivity to dc bias voltages and temperature. X5R or X7R dielectrics are preferred because these capacitors remain stable over wider operating voltage and temperature ranges. Care must be taken if selecting a tantalum capacitor to ensure a low ESR value.

AI_{CC} SUPPLY REQUIREMENTS—STATIC

The dc-to-dc converter is designed to supply a V_{BOOST_x} voltage of

$$V_{BOOST_x} = I_{OUT} \times R_{LOAD} + Headroom \quad (2)$$

See Figure 31 for a plot of headroom supplied vs. output current. Therefore, for a fixed load and output voltage, the output current of the dc-to-dc converter can be calculated by the following formula:

$$AI_{CC} = \frac{Power\ Out}{Efficiency \times AV_{CC}} = \frac{I_{OUT} \times V_{BOOST}}{\eta_{V_{BOOST}} \times AV_{CC}} \quad (3)$$

where:
I_{OUT} is the output current from I_{OUT_x} in amperes.
$\eta_{V_{BOOST}}$ is the efficiency at V_{BOOST_x} as a fraction (see Figure 33 and Figure 34).

AI_{CC} SUPPLY REQUIREMENTS—SLEWING

The AI_{CC} current requirement while slewing is greater than in static operation because the output power increases to charge the output capacitance of the dc-to-dc converter. This transient current can be quite large (see Figure 58), although the methods described in the Reducing AI_{CC} Current Requirements section can reduce the requirements on the AV_{CC} supply.

If not enough AI_{CC} current can be provided, the AV_{CC} voltage drops. Due to this AV_{CC} drop, the AI_{CC} current required for slewing increases further, causing the voltage at AV_{CC} to drop further (see Equation 3). In this case, the V_{BOOST_x} voltage and, therefore, the output voltage, may never reach their intended values. Because the AV_{CC} voltage is common to all channels, this voltage drop may also affect other channels.

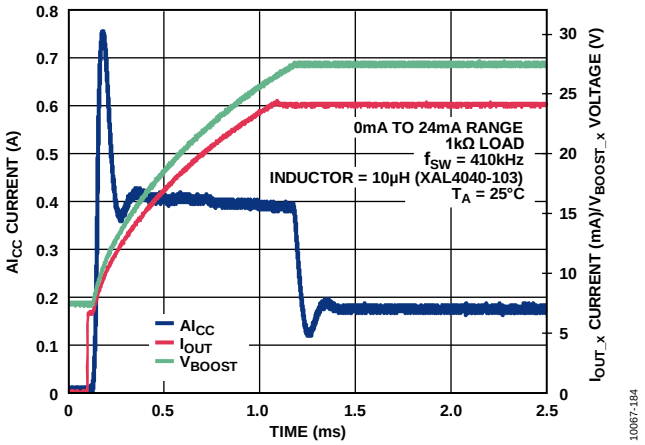


Figure 58. AI_{CC} Current vs. Time for 24 mA Step Through 1 kΩ Load with Internal Compensation Resistor

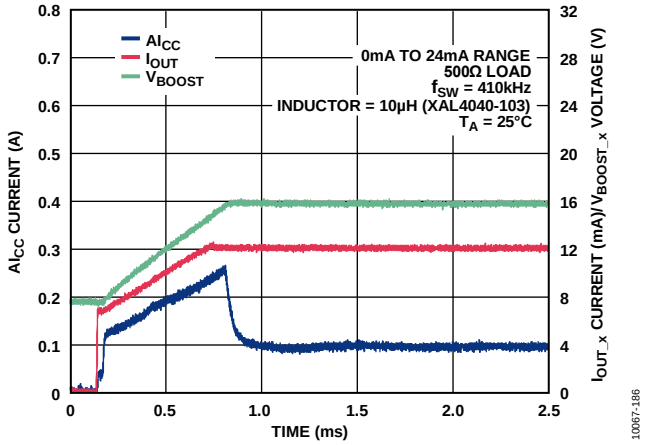


Figure 60. AI_{CC} Current vs. Time for 24 mA Step Through 500 Ω Load with External 51 kΩ Compensation Resistor

Reducing AI_{CC} Current Requirements

Two main methods can be used to reduce the AI_{CC} current requirements. One method is to add an external compensation resistor, and the other is to use slew rate control. These methods can be used together.

Adding an External Compensation Resistor

A compensation resistor can be placed at the $COMP_{DCDC_x}$ pin in series with the 10 nF compensation capacitor. A 51 kΩ external compensation resistor is recommended. This compensation increases the slew time of the current output but reduces the AI_{CC} transient current requirements. Figure 59 shows a plot of AI_{CC} current for a 24 mA step through a 1 kΩ load when using a 51 kΩ compensation resistor. The compensation resistor reduces the current requirements through smaller loads even further, as shown in Figure 60.

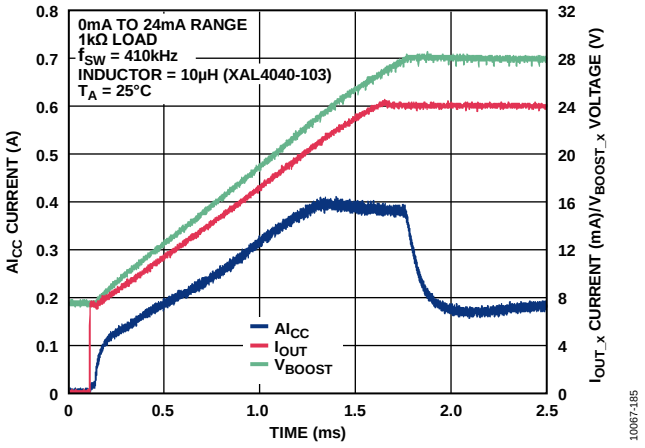


Figure 59. AI_{CC} Current vs. Time for 24 mA Step Through 1 kΩ Load with External 51 kΩ Compensation Resistor

Using Slew Rate Control

Using slew rate control can greatly reduce the current requirements of the AV_{CC} supply, as shown in Figure 61.

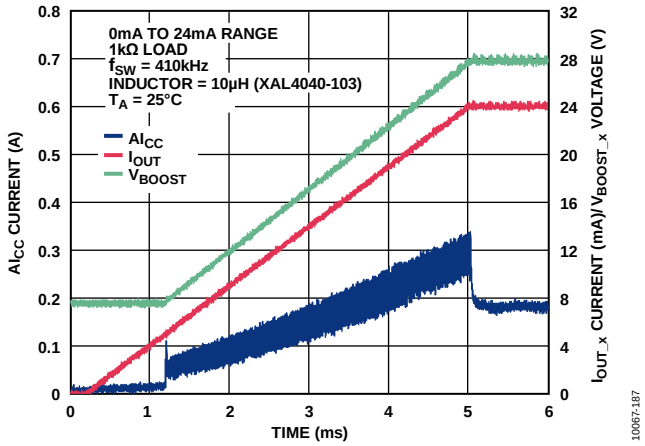


Figure 61. AI_{CC} Current vs. Time for 24 mA Step Through 1 kΩ Load with Slew Rate Control

When using slew rate control, it is important to remember that the output cannot slew faster than the dc-to-dc converter. The dc-to-dc converter slews slowest at higher currents through large loads (for example, 1 kΩ). The slew rate is also dependent on the configuration of the dc-to-dc converter. Two examples of the dc-to-dc converter output slew are shown in Figure 59 and Figure 60. (V_{BOOST} corresponds to the output voltage of the dc-to-dc converter.)

EXTERNAL PMOS MODE

The AD5737 can also be used with an external PMOS transistor per channel, as shown in Figure 62. This mode can be used to limit the on-chip power dissipation of the AD5737, although this mode does not reduce the power dissipation of the total system. The IGATEx functionality is not typically required when using the dynamic power control feature; therefore, Figure 62 shows the configuration of the device for a fixed V_{BOOST_x} supply.

In this configuration, the SW_x pin is left floating, and the $GNDSW_x$ pin is grounded. The V_{BOOST_x} pin is connected to a minimum

supply of 7.4 V and a maximum supply of 33 V. This supply can be sized according to the maximum load required to be driven.

The IGATEx functionality works by holding the gate of the external PMOS transistor at (V_{BOOST_x} − 5 V). This means that the majority of the power dissipation of the channel takes place in the external PMOS transistor.

Select the external PMOS transistor to tolerate a V_{DS} voltage of at least the V_{BOOST_x} voltage, as well as to handle the power dissipation required. Choose the V_{GS} to accommodate for the I_{OUT} headroom. The external PMOS transistor typically has minimal effect on the current output performance.

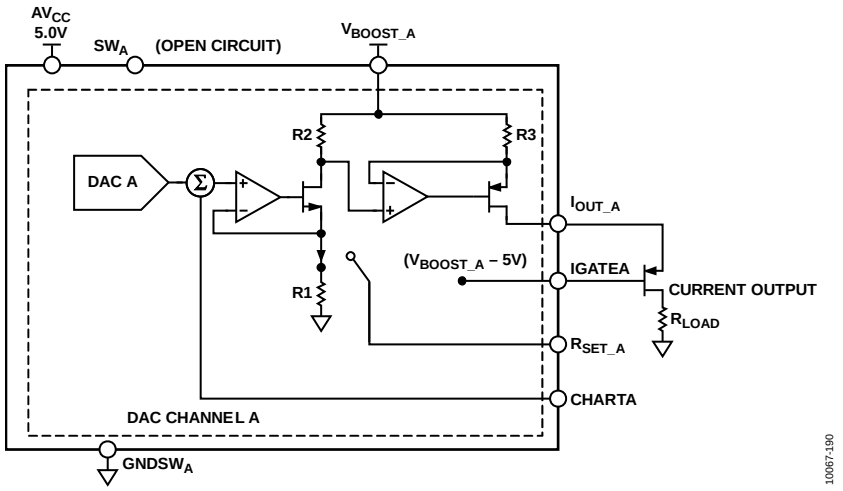


Figure 62. Configuration of Channel A Using IGATEx

APPLICATIONS INFORMATION

CURRENT OUTPUT MODE WITH INTERNAL R_{SET}

When using the internal R_{SET} resistor, the current output is significantly affected by how many other channels using the internal R_{SET} are enabled and by the dc crosstalk from these channels. The internal R_{SET} specifications in Table 1 are for all four channels enabled with the internal R_{SET} selected and outputting the same code.

For every channel enabled with the internal R_{SET}, the offset error decreases. For example, with one current output enabled using the internal R_{SET}, the offset error is 0.075% FSR. This value decreases proportionally as more current channels are enabled; the offset error is 0.056% FSR on each of two channels, 0.029% FSR on each of three channels, and 0.01% FSR on each of four channels.

Similarly, the dc crosstalk when using the internal R_{SET} is proportional to the number of current output channels enabled with the internal R_{SET}. For example, with the measured channel at 0x8000 and another channel going from zero to full scale, the dc crosstalk is −0.011% FSR. With two other channels going from zero to full scale, the dc crosstalk is −0.019% FSR, and with all three other channels going from zero to full scale, it is −0.025% FSR.

For the full-scale error measurement in Table 1, all channels are at 0xFFFF. This means that as any channel goes to zero scale, the full-scale error increases due to the dc crosstalk. For example, with the measured channel at 0xFFFF and three channels at zero scale, the full-scale error is 0.025% FSR. Similarly, if only one channel is enabled with the internal R_{SET}, the full-scale error is 0.025% FSR + 0.075% FSR = 0.1% FSR.

PRECISION VOLTAGE REFERENCE SELECTION

To achieve the optimum performance from the AD5737 over its full operating temperature range, a precision voltage reference must be used. Take care with the selection of the precision voltage reference. The voltage applied to the reference inputs is used to provide a buffered reference for the DAC cores. Therefore, any error in the voltage reference is reflected in the outputs of the AD5737.

Four possible sources of error must be considered when choosing a voltage reference for high accuracy applications: initial accuracy, long-term drift, temperature coefficient of the output voltage, and output voltage noise.

Initial accuracy error on the output voltage of an external reference can lead to a full-scale error in the DAC. Therefore, to minimize these errors, a reference with a low initial accuracy error specification is preferred. Choosing a reference with an output trim adjustment, such as the ADR435, allows a system designer to trim out system errors by setting the reference voltage to a voltage other than the nominal. The trim adjustment can be used at any temperature to trim out any error.

Long-term drift is a measure of how much the reference output voltage drifts over time. A reference with a tight long-term drift specification ensures that the overall solution remains relatively stable over its entire lifetime.

The temperature coefficient of the reference output voltage affects INL, DNL, and TUE. Choose a reference with a tight temperature coefficient specification to reduce the dependence of the DAC output voltage on ambient temperature.

In high accuracy applications, which have a relatively low noise budget, reference output voltage noise must be considered. Choosing a reference with as low an output noise voltage as practical for the system resolution required is important. Precision voltage references such as the ADR435 (XFET® design) produce low output noise in the 0.1 Hz to 10 Hz bandwidth. However, as the circuit bandwidth increases, filtering the output of the reference may be required to minimize the output noise.

DRIVING INDUCTIVE LOADS

When driving inductive or poorly defined loads, a capacitor may be required between the I_{OUT_x} pin and the AGND pin to ensure stability. A 0.01 µF capacitor between I_{OUT_x} and AGND ensures stability of a load of 50 mH. The capacitive component of the load may cause slower settling, although this may be masked by the settling time of the AD5737. There is no maximum capacitance limit for the current output of the AD5737.

Table 37. Recommended Precision Voltage References

Part No.	Initial Accuracy (mV Maximum)	Long-Term Drift (ppm Typical)	Temperature Coefficient (ppm/°C Maximum)	0.1 Hz to 10 Hz Noise (µV p-p Typical)
ADR445	±2	50	3	2.25
ADR02	±3	50	3	10
ADR435	±2	40	3	8
ADR395	±5	50	9	8
AD586	±2.5	15	10	4

TRANSIENT VOLTAGE PROTECTION

The AD5737 contains ESD protection diodes that prevent damage from normal handling. The industrial control environment can, however, subject I/O circuits to much higher transients. To protect the AD5737 from excessively high voltage transients, external power diodes and a surge current limiting resistor (R_P) are required, as shown in Figure 63. A typical value for R_P is 10 Ω. The two protection diodes and the resistor (R_P) must have appropriate power ratings.

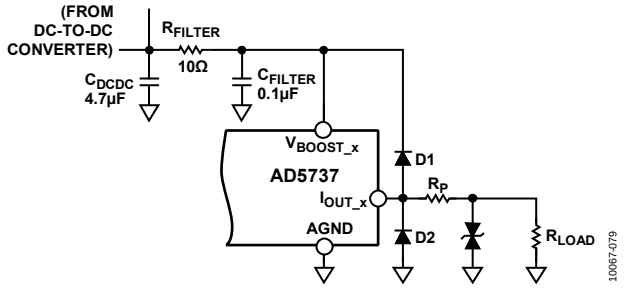


Figure 63. Output Transient Voltage Protection

Further protection can be provided using transient voltage suppressors (TVSs), also referred to as transorbs. These components are available as unidirectional suppressors, which protect against positive high voltage transients, and as bidirectional suppressors, which protect against both positive and negative high voltage transients. Transient voltage suppressors are available in a wide range of standoff and breakdown voltage ratings. The TVS must be sized with the lowest breakdown voltage possible while not conducting in the functional range of the current output.

It is recommended that all field connected nodes be protected.

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5737 is via a serial bus that uses a protocol compatible with microcontrollers and DSP processors. The communication channel is a 3-wire minimum interface consisting of a clock signal, a data signal, and a latch signal. The AD5737 requires a 24-bit data-word with data valid on the falling edge of SCLK.

The DAC output update is initiated either on the rising edge of $\overline{\text{LDAC}}$ or, if $\overline{\text{LDAC}}$ is held low, on the rising edge of $\overline{\text{SYNC}}$. The contents of the registers can be read using the readback function.

AD5737-to-ADSP-BF527 Interface

The AD5737 can be connected directly to the SPORT interface of the ADSP-BF527, an Analog Devices, Inc., Blackfin® DSP. Figure 64 shows how the SPORT interface can be connected to control the AD5737.

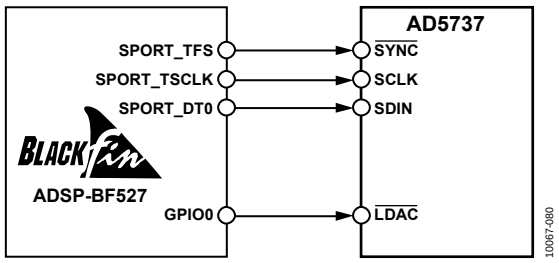


Figure 64. AD5737-to-ADSP-BF527 SPORT Interface

LAYOUT GUIDELINES

Grounding

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5737 is mounted must be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5737 is in a system where multiple devices require an AGND-to-DGND connection, the connection must be made at one point only. The star ground point must be established as close as possible to the device.

The $GNDSW_x$ pin and the ground connection for the AV_{CC} supply are referred to as PGND. PGND must be confined to certain areas of the board, and the PGND-to-AGND connection must be made at one point only.

Supply Decoupling

The AD5737 must have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply, located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitors must have low effective series resistance (ESR) and low effective series inductance (ESL), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

Traces

The power supply lines of the AD5737 must use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks must be shielded with digital ground to prevent radiating noise to other parts of the board and must never be run near the reference inputs. A ground line routed between the SDIN and SCLK traces helps reduce crosstalk between them (not required on a multilayer board that has a separate ground plane, but separating the lines helps). It is essential to minimize noise on the REFIN line because it couples through to the DAC output.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board must run at right angles to each other to reduce the effects of feedthrough on the board. A microstrip technique is by far the best method, but it is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane, and signal traces are placed on the solder side.

DC-to-DC Converters

To achieve high efficiency, good regulation, and stability, a well-designed printed circuit board layout is required.

Follow these guidelines when designing printed circuit boards (see Figure 56):

- Keep the low ESR input capacitor, C_{IN}, close to AV_{CC} and PGND.
- Keep the high current path from C_{IN} through the inductor (L_{DCDC}) to SW_x and PGND as short as possible.
- Keep the high current path from C_{IN} through the inductor (L_{DCDC}), the diode (D_{DCDC}), and the output capacitor (C_{DCDC}) as short as possible.
- Keep high current traces as short and as wide as possible. The path from C_{IN} through the inductor (L_{DCDC}) to SW_x and PGND must be able to handle a minimum of 1 A.
- Place the compensation components as close as possible to the $COMP_{DCDC_x}$ pin.
- Avoid routing high impedance traces near any node connected to SW_x or near the inductor to prevent radiated noise injection.

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. The Analog Devices *i*Coupler® products can provide voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5737 makes it ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 65 shows a 4-channel isolated interface to the AD5737 using an ADuM1411. For more information, visit www.analog.com.

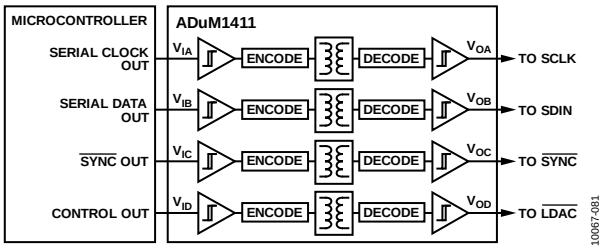


Figure 65. 4-Channel Isolated Interface to the AD5737

INDUSTRIAL HART CAPABLE ANALOG OUTPUT APPLICATION

Many industrial control applications have requirements for accurately controlled current output signals, and the AD5737 is ideal for such applications. Figure 66 shows the AD5737 in a circuit design for a HART-enabled output module, specifically for use in an industrial control application.

The design provides for a HART-enabled current output, with the HART capability provided by the AD5700/AD5700-1 HART modem, the industry's lowest power and smallest footprint HART-compliant IC modem. For additional space-savings, the AD5700-1 offers a 0.5% precision internal oscillator. The HART_OUT signal from the AD5700 is attenuated and ac-coupled into the CHARTx pin of the AD5737. Such a configuration results in the AD5700 HART modem output modulating the 4 mA to 20 mA analog current without affecting the dc level of the current. This circuit adheres to the HART physical layer specifications as defined by the HART Communication Foundation.

For transient overvoltage protection, a 24 V transient voltage suppressor (TVS) is placed on the I_{OUT}/V_{OUT} connection. For added protection, clamping diodes are connected from the I_{OUT_x}/V_{OUT_x} pin to the AV_{DD} and GND power supply pins. A 5 kΩ current limiting resistor is also placed in series with the $+V_{SENSE_x}$ input. This is to limit the current to an acceptable level during a transient event. The recommended external band-pass filter for the AD5700 HART modem includes a 150 kΩ resistor, which limits current to a sufficiently low level to adhere to intrinsic safety requirements. In this case, the input has higher transient voltage protection and, therefore, does not require additional protection circuitry, even in the most demanding of industrial environments.

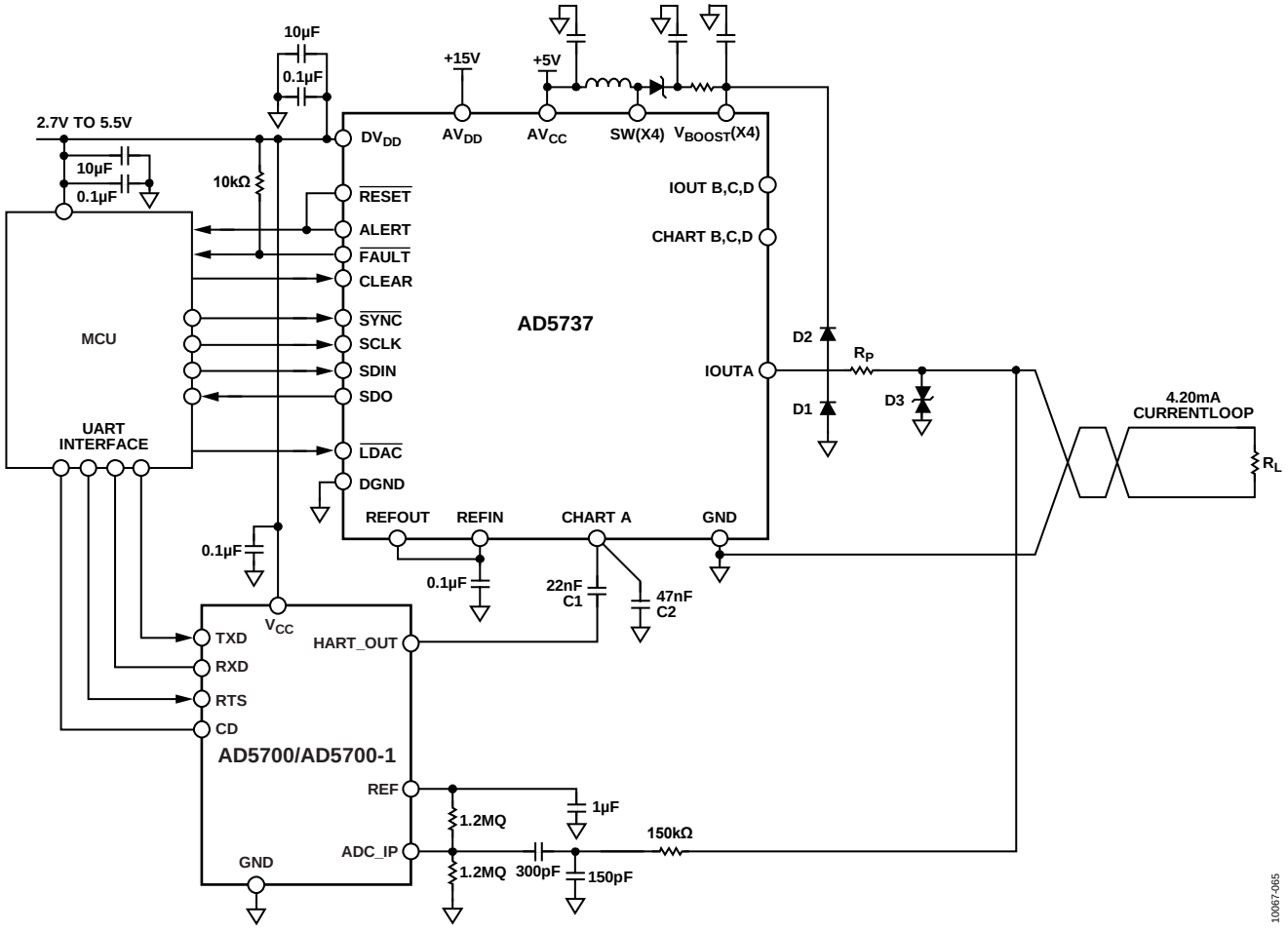


Figure 66. AD5737 in HART Configuration

OUTLINE DIMENSIONS

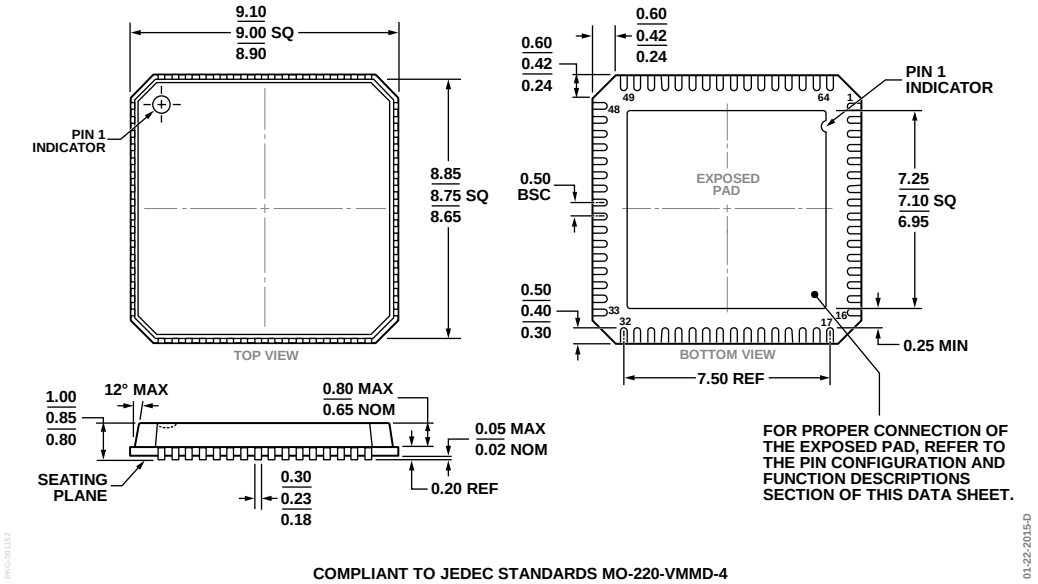


Figure 67. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Resolution (Bits)	Temperature Range	Package Description	Package Option
AD5737ACPZ	12	−40°C to +105°C	64-Lead LFCSP_VQ	CP-64-3
AD5737ACPZ-RL7	12	−40°C to +105°C	64-Lead LFCSP_VQ	CP-64-3

[1] Z = RoHS Compliant Part.

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