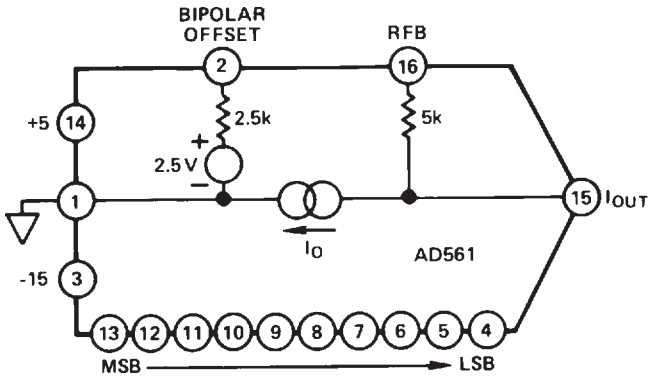
Low Cost 10-Bit Monolithic D/A Converter

AD561

FEATURES

- **Complete Current Output Converter**
- **High Stability Buried Zener Reference**
- **Laser Trimmed to High Accuracy (1/4 LSB Max Error, AD561K, T)**
- **Trimmed Output Application Resistors for 0 V to +10 V, ±5 V Ranges**
- **Fast Settling – 250 ns to 1/2 LSB**
- **Guaranteed Monotonicity Over Full Operating Temperature Range**
- **TTL/DTL and CMOS Compatible (Positive True Logic)**
- **Single Chip Monolithic Construction**
- **Available in Chip Form**
- **MIL-STD-883-Compliant Versions Available**

FUNCTIONAL BLOCK DIAGRAM
TO-116



PRODUCT DESCRIPTION

The AD561 is an integrated circuit 10-bit digital-to-analog converter combined with a high stability voltage reference fabricated on a single monolithic chip. Using ten precision high-speed current-steering switches, a control amplifier, voltage reference, and laser-trimmed thin-film SiCr resistor network, the device produces a fast, accurate analog output current. Laser trimmed output application resistors are also included to facilitate accurate, stable current-to-voltage conversion; they are trimmed to 0.1% accuracy, thus eliminating external trimmers in many situations.

Several important technologies combine to make the AD561 the most accurate and most stable 10-bit DAC available. The low temperature coefficient, high stability thin-film network is trimmed at the wafer level by a fine resolution laser system to 0.01% typical linearity. This results in an accuracy specification of ±1/4 LSB max for the K and T versions, and 1/2 LSB max for the J and S versions.

The AD561 also incorporates a low noise, high stability subsurface zener diode to produce a reference voltage with excellent long term stability and temperature cycle characteristics, which challenge the best discrete Zener references. A temperature compensation circuit is laser-trimmed to allow custom correction of the temperature coefficient of each device. This results in a typical full-scale temperature coefficient of 15 ppm/°C; the TC is tested and guaranteed to 30 ppm/°C max for the K and T versions, 60 ppm/°C max for the S, and 80 ppm/°C for the J.

The AD561 is available in four performance grades. The AD561J and K are specified for use over the 0°C to +70°C temperature range and are available in either a 16-pin hermetically-sealed ceramic DIP or a 16-pin molded plastic DIP. The AD561S and T grades are specified for the –55°C to +125°C range and are available in the ceramic package.

PRODUCT HIGHLIGHTS

1. Advanced monolithic processing and laser trimming at the wafer level have made the AD561 the most accurate 10-bit converter available, while keeping costs consistent with large volume integrated circuit production. The AD561K and T have 1/4 LSB max relative accuracy and 1/2 LSB max differential nonlinearity. The low TC R-2R ladder guarantees that all AD561 units will be monotonic over the entire operating temperature range.
2. Digital system interfacing is simplified by the use of a positive true straight binary code. The digital input voltage threshold is a function of the positive supply level; connecting V_{CC} to the digital logic supply automatically sets the threshold to the proper level for the logic family being used. Logic sink current requirement is only 25 μA.
3. The high speed current steering switches are designed to settle in less than 250 ns for the worst case digital code transition. This allows construction of successive-approximation A/D converters in the 3 μs to 5 μs range.
4. The AD561 has an output voltage compliance range from –2 V to +10 V, allowing direct current-to-voltage conversion with just an output resistor, omitting the op amp. The 40 MΩ open collector output impedance results in negligible errors due to output leakage currents.
5. The AD561 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD561/883B data sheet for detailed specifications.

REV. A

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AD561—SPECIFICATIONS (T_A = +25°C, V_{CC} = –15 V, unless otherwise noted.)

Model	AD561J Min	AD561J Typ	AD561J Max	AD561K Min	AD561K Typ	AD561K Max	Units
RESOLUTION		10 Bits			10 Bits		
ACCURACY (Error Relative to Full Scale)		±1/4 (0.025)	±1/2 (0.05)		±1/8 (0.012)	±1/4 (0.025)	LSB % of FS
DIFFERENTIAL NONLINEARITY		±1/2			±1/4	±1/2	LSB
DATA INPUTS							
TTL, V_{CC} = +5 V							
Bit ON Logic "1"	+2.0			*			V
Bit OFF Logic "0"			+0.8			*	V
CMOS, 10 V ≤ V_{CC} ≤ 16.5 V							
Bit ON Logic " 1 "	70% V_{CC}			*			V
Bit OFF Logic "0"			30% V_{CC}			*	V
Logic Current (Each Bit) (T_{MIN} to T_{MAX})							
Bit ON Logic "1"		+5	+100		*	*	nA
Bit OFF Logic "0"		–5	–25		*	*	μA
OUTPUT							
Current							
Unipolar	1.5	2.0	2.4	*	*	*	mA
Bipolar	±0.75	±1.0	±1.2	*	*	*	mA
Resistance (Exclusive of Application Resistors)		40 M			*		Ω
Unipolar Zero (All Bits OFF)		0.01	0.05		*	*	% of FS
Capacitance		25			*		pF
Compliance Voltage	–2	–3	+10	*	*	*	V
SETTLING TIME TO 1/2 LSB							
All Bits ON-to-OFF or OFF-to-ON		250			*		ns
POWER REQUIREMENTS							
V_{CC}, +4.5 V dc to +16.5 V dc		8	10		*	*	mA
V_{EE}, –10.8 V dc to –16.5 V dc		12	16		*	*	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC}, +4.5 V dc to +16.5 V dc		2	10		*	*	ppm of FS/%
V_{EE}, –10.8 V dc to –16.5 V dc		4	25		*	*	ppm of FS/%
TEMPERATURE RANGE							
Operating		0 to +70			*	*	°C
Storage ("D" Package)		–65 to +150			*	*	°C
("N" Package)		–25 to +85			*	*	°C
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	10		1	5	ppm of FS/°C
Bipolar Zero		2	20		2	10	ppm of FS/°C
Full Scale		15	80		15	30	ppm of FS/°C
Differential Nonlinearity		2.5			2.5		ppm of FS/°C
MONOTONICITY	Guaranteed Over Full Operating Temperature Range			Guaranteed Over Full Operating Temperature Range			
PROGRAMMABLE OUTPUT RANGES		0 to +10 –5 to +5			* *		V V
CALIBRATION ACCURACY							
Full-Scale Error with Fixed 25 Ω ` Resistor		±0.1			*		% of FS
Bipolar Zero Error with Fixed 10 Ω Resistor		±0.1			*		% of FS
CALIBRATION ADJUSTMENT RANGE							
Full Scale (With 50 Ω Trimmer)		±0.5			*		% of FS
Bipolar Zero (With 50 Ω Trimmer)		±0.5			*		% of FS

NOTES

*Specifications same as AD561J specifications.

Specifications subject to change without notice.

Model	AD561S Min	AD561S Typ	AD561S Max	AD561T Min	AD561T Typ	AD561T Max	Units
RESOLUTION		10 Bits			10 Bits		
ACCURACY (Error Relative to Full Scale)		±1/4 (0.025)	±1/2 (0.05)		±1/8 (0.012)	±1/4 (0.025)	LSB % of FS
DIFFERENTIAL NONLINEARITY		±1/2			±1/4	±1/2	LSB
DATA INPUTS							
TTL, V_{CC} = +5 V							
Bit ON Logic "1"	+2.0			**			V
Bit OFF Logic "0"			+0.8			**	V
CMOS, 10 V ≤ V_{CC} ≤ 16.5 V							
Bit ON Logic " 1 "	70% V_{CC}			**			V
Bit OFF Logic "0"			30% V_{CC}			**	V
Logic Current (Each Bit) (T_{MIN} to T_{MAX})							
Bit ON Logic "1"		+20	+100		**	**	nA
Bit OFF Logic "0"		–25	–100		**	**	μA
OUTPUT							
Current							
Unipolar	1.5	2.0	2.4	**	**	**	mA
Bipolar	±0.75	±1.0	±1.2	**	**	**	mA
Resistance (Exclusive of							
Application Resistors)		40 M			**		Ω
Unipolar Zero (All Bits OFF)		0.01	0.05		**	**	% of FS
Capacitance		25			**		pF
Compliance Voltage	–2	–3	+10	**	**	**	V
SETTLING TIME TO 1/2 LSB							
All Bits ON-to-OFF or OFF-to-ON		250			**		ns
POWER REQUIREMENTS							
V_{CC}, +4.5 V dc to +16.5 V dc		6	10		**	**	mA
V_{EE}, –10.8 V dc to –16.5 V dc		11	16		**	**	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC}, +4.5 V dc to +16.5 V dc		2	10		**	**	ppm of FS/%
V_{EE}, –10.8 V dc to –16.5 V dc		4	25		**	**	ppm of FS/%
TEMPERATURE RANGE							
Operating		–55 to +125			**	**	°C
Storage		–65 to +150			**	**	°C
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	10		1	5	ppm of FS/°C
Bipolar Zero		2	20		2	10	ppm of FS/°C
Full Scale		15	60		15	30	ppm of FS/°C
Differential Nonlinearity		2.5			2.5		ppm of FS/°C
MONOTONICITY	Guaranteed Over Full Operating Temperature Range			Guaranteed Over Full Operating Temperature Range			
PROGRAMMABLE OUTPUT		0 to +10			**		V
RANGES		–5 to +5			**		V
CALIBRATION ACCURACY							
Full-Scale Error with Fixed 25 Ω							
Resistor		±0.1			**		% of FS
Bipolar Zero Error with Fixed 10 Ω							
Resistor		±0.1			**		% of FS
CALIBRATION ADJUSTMENT							
RANGE							
Full Scale (With 50 Ω Trimmer)		±0.5			**		% of FS
Bipolar Zero (With 50 Ω Trimmer)		±0.5			**		% of FS

NOTES

**Specifications same as AD561S specifications.

Specifications subject to change without notice.

THE AD561 OFFERS TRUE 10-BIT RESOLUTION OVER FULL TEMPERATURE RANGE

Accuracy: Analog Devices defines accuracy as the maximum deviation of the actual, adjusted DAC output (see page 5) from the ideal analog output (a straight line drawn from 0 to FS – 1 LSB) for any bit combination. The AD561 is laser trimmed to 1/4 LSB (0.025% of FS) maximum error at +25°C for the K and T versions – 1/2 LSB for the J and S.

Monotonicity: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a single-valued function of the input. All versions of the AD561 are monotonic over their full operating temperature range.

Differential Nonlinearity: Monotonic behavior requires that the differential nonlinearity error be less than 1 LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code. For example, for a 10 volt full scale output, a change of 1 LSB in digital input code should result in a 9.8 mV change in the analog output (1 LSB = 10 V × 1/1024 = 9.8 mV). If in actual use, however, a 1 LSB change in the input code results in a change of only 2.45 mV (1/4 LSB) in analog output, the differential nonlinearity error would be 7.35 mV, or 3/4 LSB The AD561K and T have a max differential linearity error of 1/2 LSB.

The differential nonlinearity temperature coefficient must also be considered if the device is to remain monotonic over its full operating temperature range. A differential nonlinearity temperature coefficient of 2.5 ppm/°C could, under worst case conditions for a temperature change of +25°C to +125°C, add 0.025% (100 × 2.5 ppm/°C of error). The resulting error could then be as much as 0.025% + 0.025% = 0.05% of FS (1/2 LSB represents 0.05% of FS). To be sure of accurate performance all versions of the AD561 are therefore 100% tested to be monotonic over the full operating temperature range.

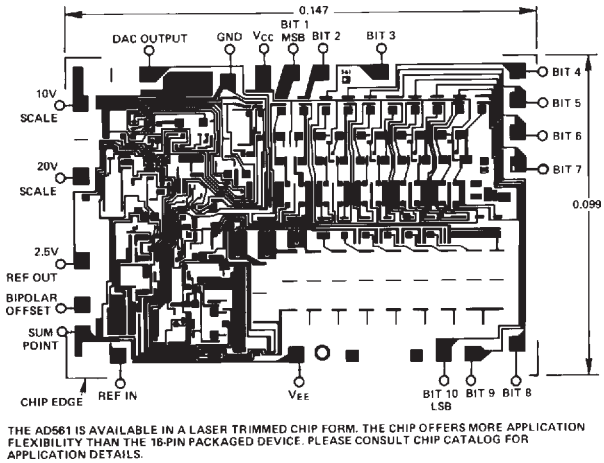


Figure 1. Chip Bonding Diagram

CONNECTING THE AD561 FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510, AD741L, AD301AL) is used, excellent performance can be obtained in many situations without trimming. (A 5 mV op amp offset is equivalent to 1/2 LSB on a 10 volt scale.) If a 25 Ω fixed resistor is substituted for the 50 Ω trimmer, unipolar zero will typically be within ±1/10 LSB (plus op amp offset), and full scale accuracy will be within ±1 LSB. Substituting a 25 Ω resistor for the 50 Ω bipolar offset trimmer will give a bipolar zero error typically within ±1 LSB.

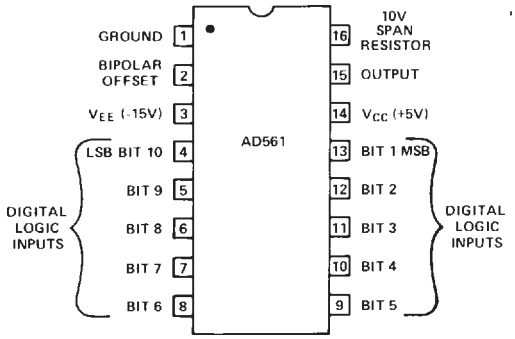
The AD509 is recommended for buffered voltage-output applications that require a settling time to ±1/2 LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

ORDERING GUIDE

MODEL[1]	TEMP RANGE	ACCURACY @ +25°C	GAIN T C (of FS/°C)	PACKAGE OPTION[2]
AD561JD	0°C to +70°C	±1/2 LSB max	80 ppm max	D-16
AD561JN	0°C to +70°C	±1/2 LSB max	80 ppm max	N-16
AD561KD	0°C to +70°C	±1/4 LSB max	30 ppm max	D-16
AD561KN	0°C to +70°C	±1/4 LSB max	30 ppm max	N-16
AD561SD	–55°C to +125°C	±1/2 LSB max	60 ppm max	D-16
AD561TD	–55°C to +125°C	±1/4 LSB max	30 ppm max	D-16
AD561/883B	–55°C to +125°C	*	*	*

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD561/883B data sheet.
[2]D = Ceramic DIP; N = Plastic DIP.
*Refer to AD561/883B military data sheet.

PIN CONFIGURATION TOP VIEW



UNIPOLAR CONFIGURATION
This configuration, shown in Figure 2, will provide a unipolar 0 V to +10 V output range.

STEP I . . . ZERO ADJUST
Turn all bits OFF and adjust op amp trimmer, R_1, until the output reads 0.000 volts (1 LSB = 9.76 mV).

STEP 11. . . GAIN ADJUST
Turn all bits ON and adjust 50 Ω gain trimmer, R_2, until the output is 9.990 volts. (Full scale is adjusted to 1 LSB less than nominal full scale of 10.000 volts.) If a 10.23 V full scale is desired (exactly 10 mV/bit), insert a 120 Ω resistor in series with R_2.

BIPOLAR CONFIGURATION
This configuration, shown in Figure 3, will provide a bipolar output voltage from –5.000 to +4.990 volts, with positive full scale occurring with all bits ON (all 1s).

STEP 1. . . ZERO ADJUST
Turn ON MSB only, turn OFF all other bits. Adjust 50 Ω trimmer R_3, to give 0.000 output volts. For maximum resolution a 120 Ω resistor may be placed in parallel with R_3.

STEP 11. . . GAIN ADJUST
Turn OFF all bits, adjust 50 Ω gain trimmer to give a reading of –5.000 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, the op amp trimmer is unnecessary unless the untrimmed offset drift of the op amp is excessive.

±10 VOLT BUFFERED BIPOLAR OUTPUT
The AD561 can also be connected for a ±10 volt bipolar range with an additional external resistor as shown in Figure 4. A larger value trimmer is required to compensate for tolerance in the thin film resistors, which are trimmed to match the full-scale current. For best full scale temperature coefficient performance, the external resistors should have a TC of –50 ppm/°C.

CIRCUIT DESCRIPTION
A simplified schematic with the essential circuit features of the AD561 is shown in Figure 5. The voltage reference, CR1, is a buried Zener (or subsurface breakdown diode). This device exhibits far better all-around performance than the NPN base-emitter reverse-breakdown diode (surface Zener), which is in nearly universal use in integrated circuits as a voltage reference. Greatly improved long-term stability and lower noise are the major benefits the buried Zener derives from isolating the breakdown point from surface stress and mobile oxide charge effects. The nominal 7.5 volt device (including temperature compensation circuitry) is driven by a current source to the negative supply so the positive supply can be allowed to drop as low as 4.5 volts. The temperature coefficient of each diode is individually determined; this data is then used to laser trim a compensating circuit to balance the overall TC to zero. The typical resulting TC is 0 to ±15 ppm/°C. The negative reference level is inverted and scaled by A_1 to give a +2.5 volt reference, which can be driven by the low positive supply. The AD561, packaged in the 16-pin DIP, has the +2.5 volt reference (REF OUT) connected directly to the input of the control amplifier (REF IN). The buffered reference is not directly available externally except through the 2.5 kΩ bipolar offset resistor.

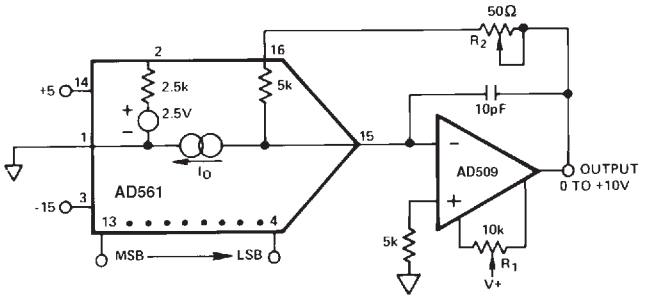


Figure 2. 0 V to +10 V Unipolar Voltage Output

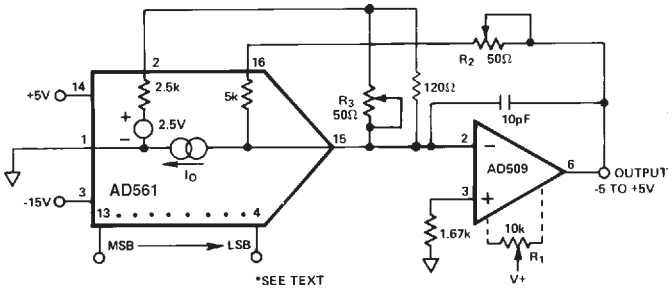


Figure 3. ±5 V Buffered Bipolar Voltage Output

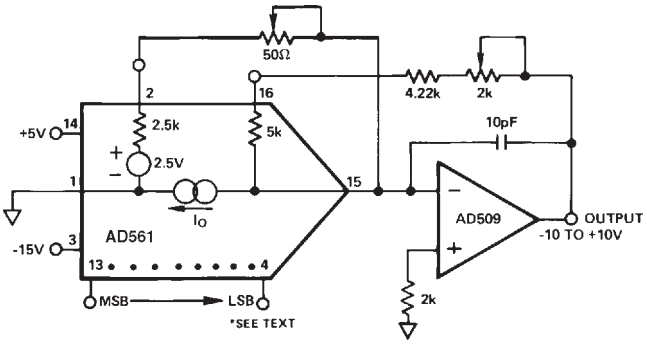


Figure 4. ±10 V Buffered Voltage Output

The 2.5 kΩ scaling resistor and control amplifier A_2 then force a 1 mA reference current to flow through reference transistor Q_1, which has a relative emitter area of 8A. This is accomplished by forcing the bottom of the ladder to the proper voltage. Since Q_1 and Q_2 have equal emitter areas and equal 5 kΩ emitter resistors, Q_2 also carries 1 mA. The ladder voltage drop constrains Q_7 (with area 4A) to carry only 0.5 mA; Q_8 carries 0.25 mA, etc.

The first four significant bit cells are exactly scaled in emitter area to match Q_1 for optimum V_{BE} and V_{BE} drift match, as well as for beta match. These effects are insignificant for the lower order bits, which account for a total of only 1/16 of full scale. However, the 18 mV V_{BE} difference between two matched transistors carrying emitter currents in a ratio of 2:1 must be corrected. This is achieved by forcing 120 μA through the 150 Ω interbase resistors. These resistors, and the R-2R ladder resistors, are actively laser-trimmed at the wafer level to bring total device accuracy to better than 1/4 LSB. Sufficient ratio accuracy in the last two bits is obtained by simple emitter area

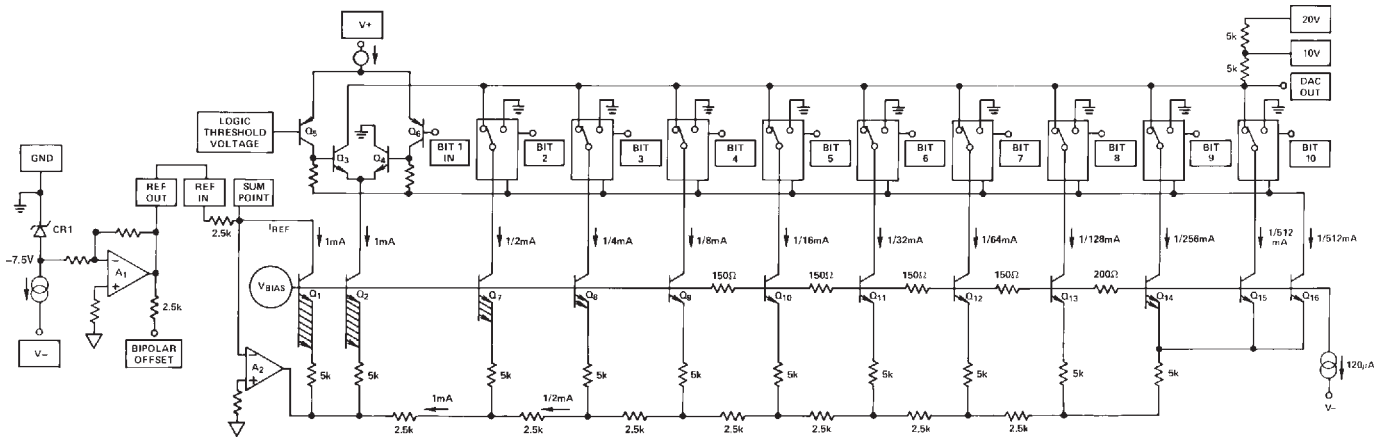


Figure 5. Circuit Diagram Showing Reference, Control Amplifier, Switching Cell, R-2R Ladder, and Bit Arrangement of AD561

ratio such that it is unnecessary to use additional area for ladder resistors. The current in Q_{16} is added to the ladder to balance it properly, but is not switched to the output; thus, full scale is 1023/1024 × 2 mA.

The switching cell of Q_3, Q_4, Q_5 and Q_6 serves to steer the cell current either to ground (BIT 1 low) or to the DAC output (BIT 1 high). The entire switching cell carries the same current whether the bit is on or off, minimizing thermal transients and ground current errors. The logic threshold, which is generated from the positive supply (see Digital Logic Interface), is applied to one side of each cell.

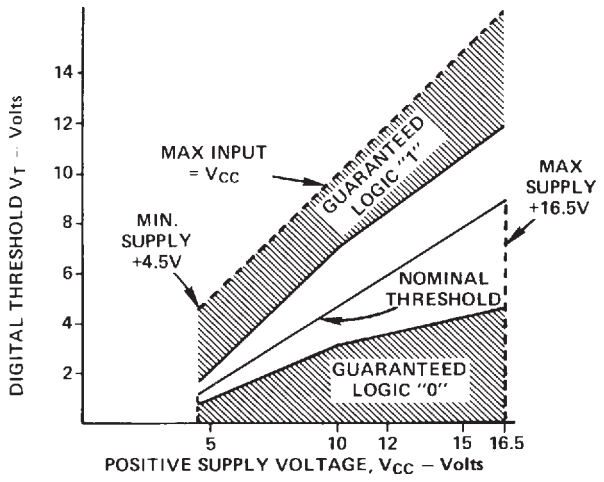


Figure 6. Digital Threshold vs. Positive Supply

DIGITAL LOGIC INTERFACE

All standard positive supply logic families interface easily with the AD561. The digital code is positive true binary (all bits high, Logic "1," gives positive full scale output). The logic input load factor (100 nA max at Logic "1," –25 μA max at Logic "0," 3 pF capacitance), is less than one equivalent digital load for all logic families, including unbuffered CMOS. The digital threshold is set internally as a function of the positive supply, as shown in Figure 6. For most applications, connecting V_{CC} to the positive logic supply will set the threshold at the proper level for maximum noise immunity. For nonstandard applications, refer to Figure 6 for threshold levels. Uncommitted bit input lines will assume a "1" state (similar to TTL), but they are high impedance and subject to noise pickup. Unused digital inputs should be directly connected to ground or V_{CC}, as desired.

SETTLING TIME

The high speed NPN current steering switching cell and internally compensated reference amplifier of the AD561 are specifically designed for fast settling operation. The typical settling time to ±0.05% (1/2 LSB) for the worst case transition (major carry, 0111111111 to 1000000000) is less than 250 ns; the lower order bits all settle in less than 200 ns. (Worst case settling occurs when all bits are switched, especially the MSB.) Full realization of this high speed performance requires strict attention to detail by the user in all areas of application and testing.

The settling time for the AD561 is specified in terms of the current output, an inherently high speed DAC operating mode. However, most DAC applications require a current-to-voltage conversion at some point in the signal path, although an unbuffered voltage level (not using an op amp) is suitable for use in a successive-approximation A/D converter (see page 8), or in many display applications. This form of conversion can give very fast operation if proper design and layout is done. The fastest voltage conversion is achieved by connecting a low value resistor directly to the output, as shown in Figure 9. In this case, the settling time is primarily determined by the cell switching time and by the RC time constant of the AD561 output capacitance of 25 picofarads (plus stray capacitance) combined with the output resistor value. Settling to 0.05% of full scale (for a full-scale transition) requires 7.6 time constants. This effect is important for R > 1 kΩ.

If an op amp must be used to provide a low impedance output signal, some loss in settling time will be seen due to op amp dynamics. The normal current-to-voltage converter op amp circuits are shown in the applications circuits on page 5, using the fast settling AD509. The circuits shown settle to ±1/2 LSB in 600 ns unipolar and 1.1 μs bipolar. The DAC output capacitance, which acts as a stray capacitance at the op amp inverting input, must be compensated by a feedback capacitor, as shown. The value should be carefully chosen for each application and each op amp type.

Fastest operation will be obtained by minimizing lead lengths, stray capacitance and impedance levels. Both supplies should be bypassed near the devices; 0.1 μF will be sufficient since the AD561 runs at constant supply current regardless of input code.

POWER SUPPLY SELECTION

The AD561 will operate over a wide range of power supply voltages, with a total supply from 15.3 to 33 volts. Symmetrical supplies are not required, and in many applications not recommended. Maximum allowable supplies are ±16.5 V.

The positive supply level determines the digital threshold level, as explained on page 6 and shown in Figure 6. It is therefore recommended that V_{CC} be connected directly to the digital supply for best threshold match.

Positive output voltage compliance range is unaffected by the positive supply level because of the open collector output stage design; thus the full +10 volt compliance is available even with a +5 volt V_{CC} level. Power supply rejection is excellent, so that digital supply noise will not be reflected to the output. but use of a 0.1 μF bypass capacitor near the AD561 is recommended for decoupling.

The nominal negative supply level is –15 volts, with an allowable range of –10.8 to –16.5 volts. The negative supply level affects the negative compliance range, as shown in Figure 7.

OUTPUT VOLTAGE COMPLIANCE

The AD561 has a typical output compliance range from –3 to +10 volts. The output current is unaffected by changes in the output terminal voltage over that range. This results from the use of open collector output switching stages in a cascade configuration, and gives an output impedance of 40 MΩ. Positive compliance range is limited only by collector breakdown (and is independent of positive supply level), but the negative range is limited by the required bias levels and resistor ladder voltage. Negative compliance varies with negative supply, as shown in Figure 7. The compliance range is guaranteed to be –2 to +10 volts with V_{EE} = –15 volts.

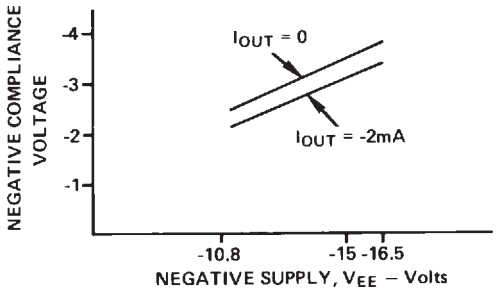


Figure 7. Typical Negative Compliance Range vs. Negative Supply

DIRECT UNBUFFERED VOLTAGE OUTPUT

The wide compliance range allows direct current-to-voltage conversion with just an output resistor. Figure 8 shows a connection using the gain and bipolar output resistors to give a ±1.66 volt bipolar swing. In this situation, the digital code is complementary binary. Other combinations of internal and external output resistors (R_X) can be used to scale to alternate voltage ranges, simply by appropriately scaling the 0 to –2 mA unipolar output current and using the 2.5 volt reference voltage for bipolar offset. For example, setting R_X = 2.5 kΩ gives a ±1 volt range with a 1 kΩ equivalent output impedance. A 0 to +10 volt output can be obtained by connecting the 5 kΩ gain resistor to 9.99 volts; again the digital code is complementary binary.

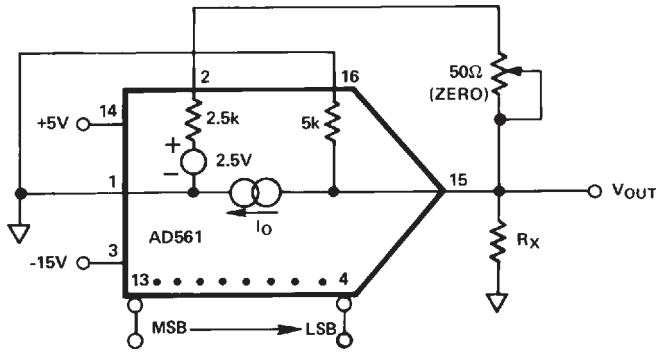


Figure 8. Unbuffered Bipolar Voltage Output

HIGH SPEED 10-BIT A/D CONVERTERS

The fast settling characteristics of the AD561 make it ideal for high speed successive approximation A/D converters. The internal reference and trimmed application resistors allow a 10-bit converter system to be constructed with a minimum parts count. Shown here is a configuration using standard components; this system completes a full 10-bit conversion in 5.5 μs unipolar or 12 μs bipolar. This converter will be accurate to ±1/2 LSB of 10 bits and have a typical gain TC of 10 ppm/°C.

In the unipolar mode, the system range is 0 to 9.99 volts, with each bit having a value of 9.76 mV. For true conversion accuracy, an A/D converter should be trimmed so that a given bit code output results from input levels from 1/2 LSB below to 1/2 LSB above the exact voltage which that code represents. Therefore, the converter zero point should be trimmed with an input voltage of +4.9 mV; trim R_1 until the LSB just begins to appear in the output code (all other bits "0"). For full scale, use an input voltage of +9.985 volts (10 volts – 1 LSB – 1/2 LSB); then trim R_2 again until the LSB just begins to appear (all other bits "1").

The bipolar signal range is –5.0 to +4.99 volts. Bipolar offset trimming is done by applying a +4.9 mV input signal and trimming R_1 for the LSB transition (MSB "1," all other bits "0.") Full scale is set by applying –4.995 volts and trimming R_2 for the LSB transition (all other bits "0"). In many applications, the pretrimmed application resistors are sufficiently accurate that external trimmers will be unnecessary, especially in situations requiring less than full 10-bit ± 1/2 LSB accuracy.

For fastest operation, the impedance at the comparator summing node must be minimized, as mentioned in the section on settling time. However, lowering the impedance will reduce the voltage signal to the comparator (at an equivalent impedance of 1 kΩ, 1 LSB = 2 mV) to the point that comparator performance will be sacrificed. A 1 kΩ resistor is the optimum value for this application for 10-bit accuracy. The chart shown in the figure gives the speed of the ADC for ±1/2 LSB accuracy (and no missing codes) for 6-, 8- and 10-bit resolution.

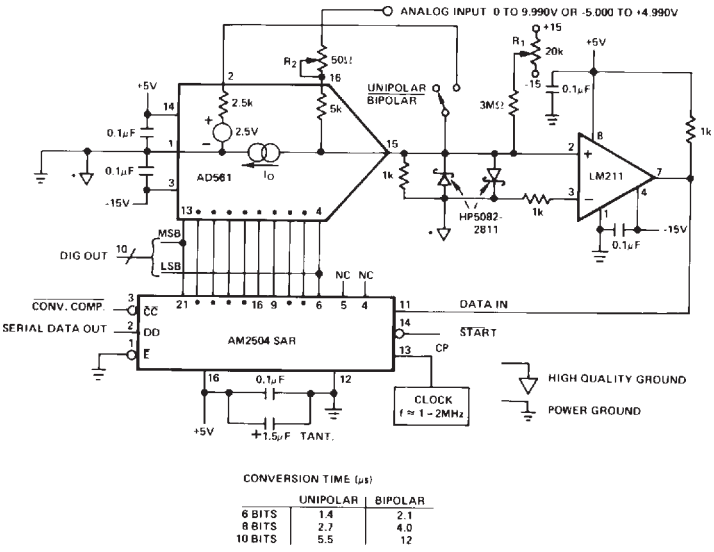


Figure 9. Fast Precision Analog to Digital Converter

A much faster converter can be constructed by using higher performance external components. Each individual high-order bit settles in less than 250 ns; the low-order bits in less than 200 ns. Because of this, a staged clock, which speeds up for lower bits will improve the speed. Also, a faster comparator and Schottky TTL or ECL logic would be necessary. 10-bit converters in the 3 μs to 5 μs range could be built around the AD561 with these techniques.

DIGITAL 4-TO-20 mA OR 1-TO-5 VOLT CONVERTER

A direct digital 4-to-20 mA or 1-to-5 volt line driver can be built with the AD561 as shown in Figure 10. The 2.5 volt reference is divided to provide 1 volt at the op amp noninverting input – thus a zero input code results in a 1 volt output at the Darlington emitter (V_{OUT}). The 2 k feedback resistance converts the nominal 2 mA (±20%) full-scale output from the AD561 to 4 volts, for a total output of 5 volts FS. The voltage at the emitter forces a proportional current through the 250 Ω (which appears at the collector as I_{OUT}) The AD561 current is added to the 4–20 mA line; thus 5 volts full scale gives 22 mA in the current loop. For exactly 20 mA, trim the 1 k pot for 4.5 V FS. (A single op amp circuit will not produce both 1 to 5 volt and 4-to-20 mA outputs simultaneously.)

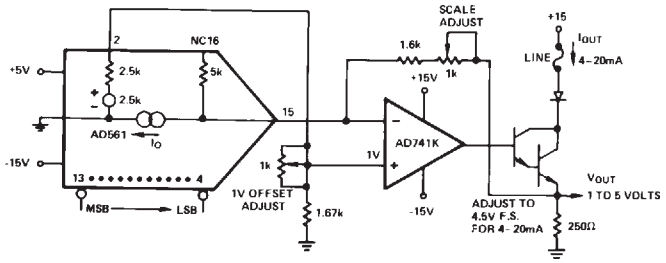


Figure 10. Digital 4-to-20 mA or 1-to-5 Volt Line Driver

DIGITALLY PROGRAMMABLE SETPOINT COMPARATOR

Figure 11 demonstrates a high accuracy systems-oriented setpoint comparator. The 2.5 volt reference is buffered and amplified by the AD741K to produce an exact 10.000 volt reference which could be used as a primary system reference for several such circuits. The +10 volt compliance of the AD561 then allows it to generate a zero to +10 volt output swing through the 5 kΩ application resistor without an additional op amp. The digital code for this system will be complementary binary (all 1s give 0.00 volts out).

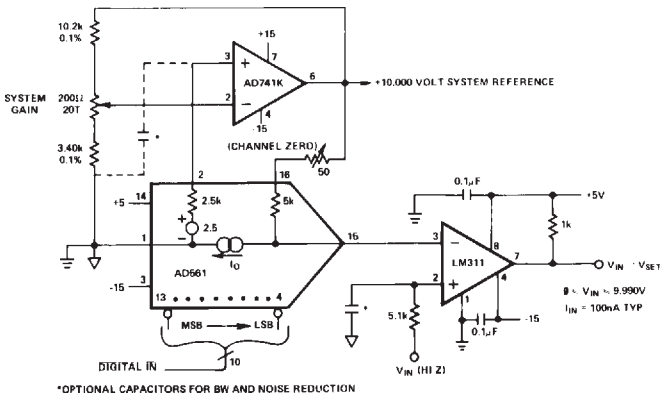
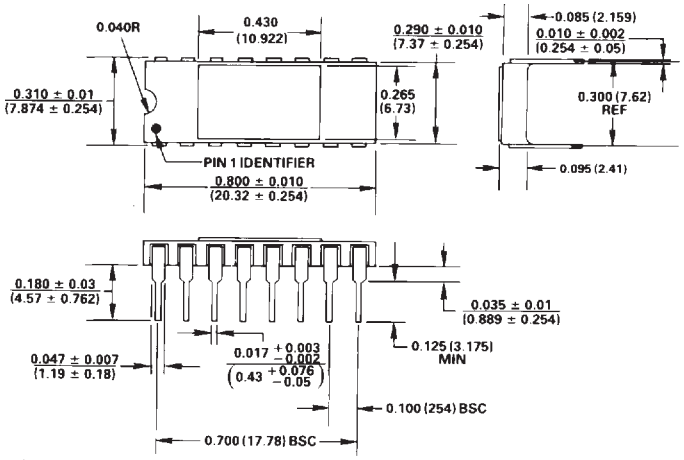


Figure 11. Digitally Programmable Set-Point Comparator

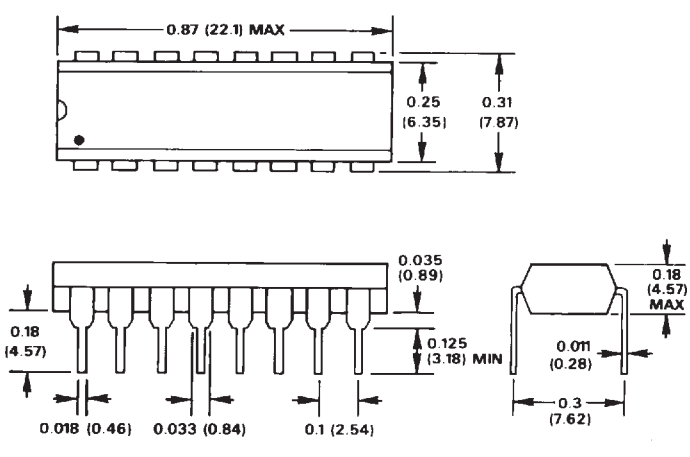
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Pin Ceramic Package
D-16



16-Pin Plastic Package
N-16



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