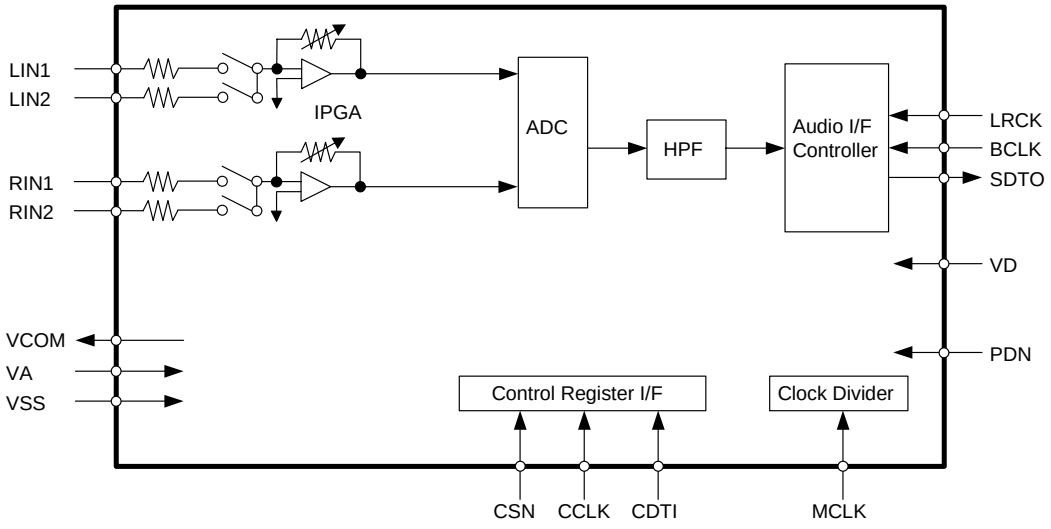
# AK5354
## Low Power 20bit ΔΣ ADC with PGA

### FEATURES

The AK5354 is a low voltage 20bit A/D converter for digital audio system. The AK5354 also includes Analog input PGA, therefore is suitable for microphone application and etc. As digital power supply of the AK5354 corresponds to 1.8V, the interface with microprocessor can operate at low voltage. Analog signal input of the AK5354 is single-ended, therefore, any external filters are not required. As the package is 16pin TSSOP, the AK5354 is a suitable for minimizing system.

### FEATURES

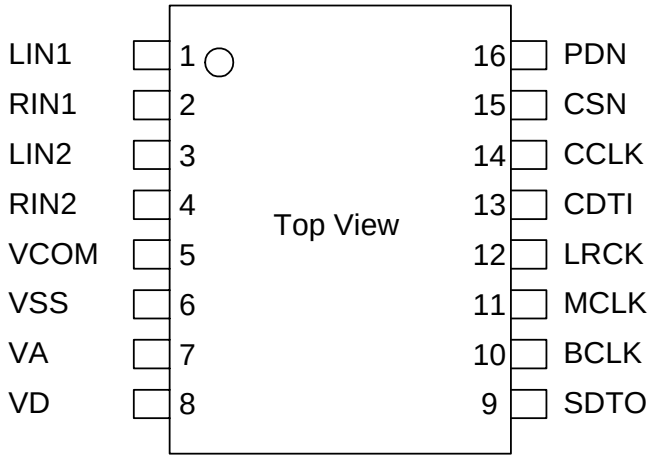
1. **Resolution : 20bits**
2. **Recording Functions**
   - **2-Stereo Inputs Selector**
   - **Analog Input PGA**
   - **Monaural Mixing**
   - **Digital HPF for DC-offset cancellation (fc=3.4Hz@fs=44.1kHz)**
3. **ADC Characteristics**
   - **Input Level : 1.5Vpp@VA=2.5V (= 0.6 x VA)**
   - **S/(N+D) : 84dB**
   - **DR, S/N : 89dB**
4. **3-wire Serial Control I/F**
5. **Master Clock : 256fs/384fs**
6. **Audio Data Format : MSB First, 2's compliment**
   - **20bit MSB justified or $I^2S$**
8. **Power Supply**
   - **VA : 2.1 ~ 3.3V (typ. 2.5V)**
   - **VD : 1.8 ~ 3.3V (typ. 2.5V)**
9. **Power Supply Current**
   - **IPGA + ADC : 7mA**
10. **Ta = -40 ~ 85°C**
11. **Package : 16pin TSSOP**



## ■ Ordering Guide

| | | |
|---|---|---|
| AK5354VT | -40 ~ +85°C | 16pin TSSOP (0.65mm pitch) |
| AKD5354 | Evaluation Board for AK5354 | |

## ■ Pin Layout




**PIN/FUNCTION**

| No. | Pin Name | I/O | Function |
|---|---|---|---|
| 1 | LIN1 | I | Lch #1 Input Pin |
| 2 | RIN1 | I | Rch #1 Input Pin |
| 3 | LIN2 | I | Lch #2 Input Pin |
| 4 | RIN2 | I | Rch #2 Input Pin |
| 5 | VCOM | O | ADC Common Voltage Output Pin |
| 6 | VSS | - | Ground Pin |
| 7 | VA | - | Analog Power Supply Pin, +2.5V |
| 8 | VD | - | Digital Power Supply Pin, +2.5V |
| 9 | SDTO | O | Audio Serial Data Output Pin |
| 10 | BCLK | I | Audio Serial Data Clock Pin |
| 11 | MCLK | I | Master Clock Input Pin |
| 12 | LRCK | I | Input/Output Channel Clock Pin |
| 13 | CDTI | I | Control Data Input Pin |
| 14 | CCLK | I | Control Clock Input Pin |
| 15 | CSN | I | Chip Select Pin |
| 16 | PDN | I | Reset & Power Down Pin<br>"L" : Reset & Power down<br>"H" : Normal operation |

Note: All digital input pins should not be left floating.

## ABSOLUTE MAXIMUM RATINGS

(VSS=0V; Note 1)

| Parameter | | Symbol | min | max | Units |
|---|---|---|---|---|---|
| Power Supply | Analog | VA | -0.3 | 4.6 | V |
| | Digital | VD | -0.3 | 4.6 | V |
| Input Current (Any Pin Except Supplies) | | IIN | - | ±10 | mA |
| Analog Input Voltage (LIN2-1, RIN2-1 pins) | | VINA | -0.3 | VA+0.3 | V |
| Digital Input Voltage | | VIND | -0.3 | VD+0.3 | V |
| Ambient Temperature (power applied) | | Ta | -40 | 85 | °C |
| Storage Temperature | | Tstg | -65 | 150 | °C |

Note: 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may results in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

## RECOMMENDED OPERATING CONDITIONS

(VSS=0V; Note 1)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| Power Supply | Analog (VA pin) | VA | 2.1 | 2.5 | 3.3 | V |
| | Digital (VD pin) | VD | 1.8 | 2.5 | VA | V |

Note: 1. All voltages with respect to ground.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

## ANALOG CHARACTERISTICS

(Ta=25°C; VA, VD=2.5V; fs=44.1kHz; Signal Frequency=1kHz; Measurement frequency=10Hz ~ 20kHz; unless otherwise specified)

| Parameter | | min | typ | max | Units |
|---|---|---|---|---|---|
| Resolution | | | | 20 | bits |
| **Input PGA Characteristics (IPGA):** | | | | | |
| Input Voltage (LIN1, LIN2, RIN1, RIN2) (Note 2) | | 1.35 | 1.5 | 1.65 | Vpp |
| Input Impedance | | 6.3 | 9 | 15 | kΩ |
| Step Width | +28dB ~ -8dB | 0.1 | 0.5 | 1 | dB |
| | -8dB ~ -16dB | 0.1 | 1 | 2 | dB |
| | -16dB ~ -32dB | 0.1 | 2 | 4 | dB |
| | -32dB ~ -40dB | - | 2 | - | dB |
| | -40dB ~ -52dB | - | 4 | - | dB |
| **ADC Analog Input Characteristics:** (Note 3) | | | | | |
| S/(N+D) (-0.5dBFS Input) | | 74 | 84 | | dB |
| D-Range (EIAJ) | | 82 | 89 | | dB |
| S/N (EIAJ) | | 82 | 89 | | dB |
| Interchannel Isolation | | 90 | 100 | | dB |
| Interchannel Gain Mismatch | | | 0.2 | 0.5 | dB |
| **Power Supplies** | | | | | |
| Power Supply Current: VA+VD | | | | | |
| Normal Operation (PDN="H") | | | | | |
| IPGA+AD (PM0=1, PM1=1) | | | 7 | 10 | mA |
| Power Down (PDN="L") (Note 4) | | | 10 | 100 | μA |

Note: 2. Analog input voltage (full-scale voltage: IPGA = 0dB) scale with VREF. (IPGA = ADC = 0.6 x VREF)

Note: 3. ADC is input from LIN1/RIN1 or LIN2/RIN2 and it measures included in IPGA. The value of IPGA is set 0dB. Internal HPF cancels the offset of IPGA and ADC.

Note: 4. In case of power-down mode, all digital input pins including clocks pins (MCLK, BCLK and LRCK) are held VD or VSS. PDN pin is held VSS.

## FILTER CHARACTERISTICS

(Ta=25°C; VA=2.1 ~ 3.3V, VD=1.8 ~ 3.3; fs=44.1kHz)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **ADC Digital Filter (Decimation LPF):** | | | | | | |
| Passband (Note 5) | ±0.1dB | PB | 0 | | 17.4 | kHz |
| | -1.0dB | | | 20.0 | | kHz |
| | -3.0dB | | | 21.1 | | kHz |
| Stopband (Note 5) | | SB | 27.0 | | | kHz |
| Passband Ripple | | PR | | | ±0.1 | dB |
| Stopband Attenuation | | SA | 65 | | | dB |
| Group Delay (Note 6) | | GD | | 17.0 | | 1/fs |
| Group Delay Distortion | | ΔGD | | 0 | | μs |
| **ADC Digital Filter (HPF):** | | | | | | |
| Frequency Response (Note 5) | -3dB | FR | | 3.4 | | Hz |
| | -0.5dB | | | 10 | | Hz |
| | -0.1dB | | | 22 | | Hz |

Note:5. The passband and stopband frequencies scale with fs (sampling frequency).
For examples, PB=0.454 x fs(@ADC: -1.0dB), PB=0.454 x fs(@DAC: -0.1dB).

Note: 6. The calculating delay time which occurred by digital filtering. This time is from the input of analog signal to setting the 20bit data of both channels to the output register for ADC and include group delay of HPF.

## DC CHARACTERISTICS

(Ta=25°C; VA=2.1 ~ 3.3V, VD=1.8 ~ 3.3V)

| Parameter | Symbol | min | Typ | max | Units |
|---|---|---|---|---|---|
| High-Level Input Voltage | VIH | 75%VD | - | - | V |
| Low-Level Input Voltage | VIL | - | - | 25%VD | V |
| High-Level Output Voltage (Iout=-80μA) | VOH | VD-0.4 | - | - | V |
| Low-Level Output Voltage (Iout=80μA) | VOL | - | | 0.4 | V |
| Input Leakage Current | Iin | - | - | ± 10 | μA |

## SWITCHING CHARACTERISTICS

(Ta=25°C; VA=2.1 ~ 3.3V, VD=1.8 ~ 3.3V; $C_L$=20pF)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| **Control Clock Frequency** | | | | | |
| **Master Clock (MCLK)** 256fs: Frequency | fCLK | 2.048 | 11.2896 | 12.8 | MHz |
| Pulse Width Low | tCLKL | 28 | | | ns |
| Pulse Width High | tCLKH | 28 | | | ns |
| 384fs: | fCLK | 3.072 | 16.9344 | 19.2 | MHz |
| Frequency | tCLKL | 23 | | | ns |
| Pulse Width Low | tCLKH | 23 | | | ns |
| Pulse Width High | fs | 8 | 44.1 | 50 | kHz |
| **Channel Clock (LRCK)** Frequency | | 45 | | 55 | % |
| Duty Cycle | | | | | |
| **Audio Interface Timing** | | | | | |
| BCLK Period | tBLK | 312.5 | | | ns |
| BCLK Pulse Width Low | tBLKL | 130 | | | ns |
| Pulse Width High | tBLKH | 130 | | | ns |
| BCLK "↓" to LRCK | tBLR | -tBLKH+50 | | tBLKL-50 | ns |
| LRCK Edge to SDTO (MSB) | tDLR | | | 80 | ns |
| BCLK "↓" to SDTO | tDSS | | | 80 | ns |
| **Control Interface Timing** | | | | | |
| CCLK Period | tCCK | 200(Note 7) | | | ns |
| CCLK Pulse Width Low | tCCKL | 80 | | | ns |
| Pulse Width High | tCCKH | 80 | | | ns |
| CDATA Setup Time | tCDS | 50 | | | ns |
| CDATA Hold Time | tCDH | 50 | | | ns |
| CSN "H" Time | tCSW | 150(Note 7) | | | ns |
| CSN "↓" to CCLK "↑" | tCSS | 50(Note 7) | | | ns |
| CCLK "↑" to CSN "↑" | tCSH | 50 | | | ns |
| **Reset / Calibration Timing** | | | | | |
| PDN Pulse Width | tPW | 150 | | | ns |
| PDN "↑" to SDTO (Note 8) | tPWV | | 4128 | | 1/fs |

Note: 7. fs ≥ 19.6kHz.
In the case of fs <19.6kHz, these three parameters must meet a relationship of
(tCSW + tCSS + 7 × tCCK) > 1/(32 × fs) in addition to these specifications.
For example, When tCCK=200ns and tCSS=50ns at fs=8kHz, tCSW(min) is 2457ns. When tCSW=150ns and tCSS=50ns fs=8kHz, tCCK(min) is 530ns.

Note: 8. These cycles are the numbers of LRCK rising from PDN pin rising.

## ■ Timing Diagram

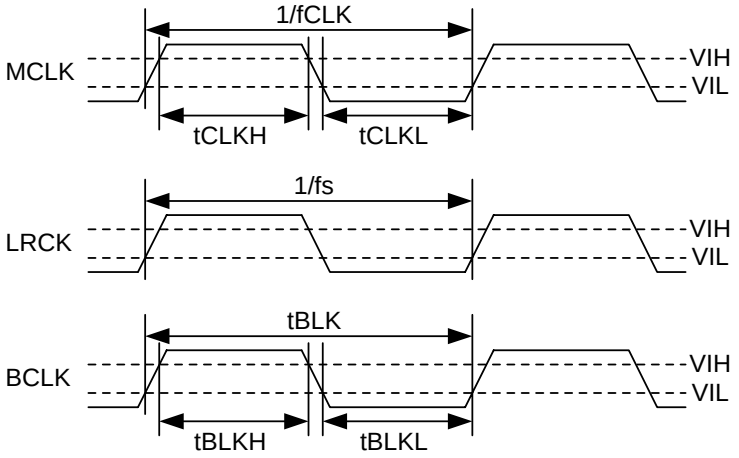



Figure 1. Clock Timing

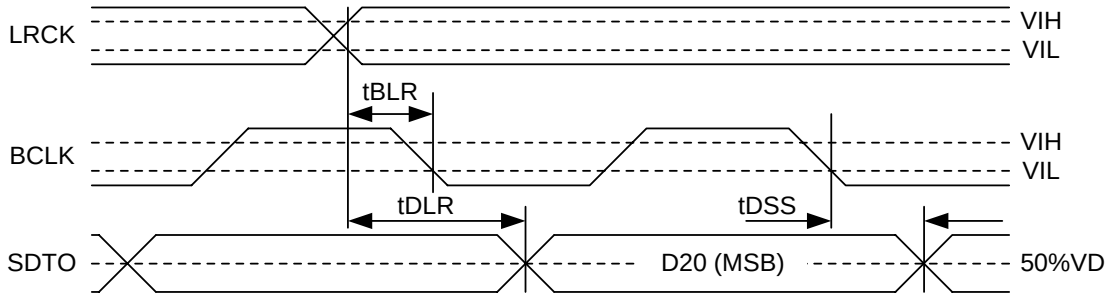



Figure 2. Audio Data Input/Output Timing (Audio I/F = No.0)

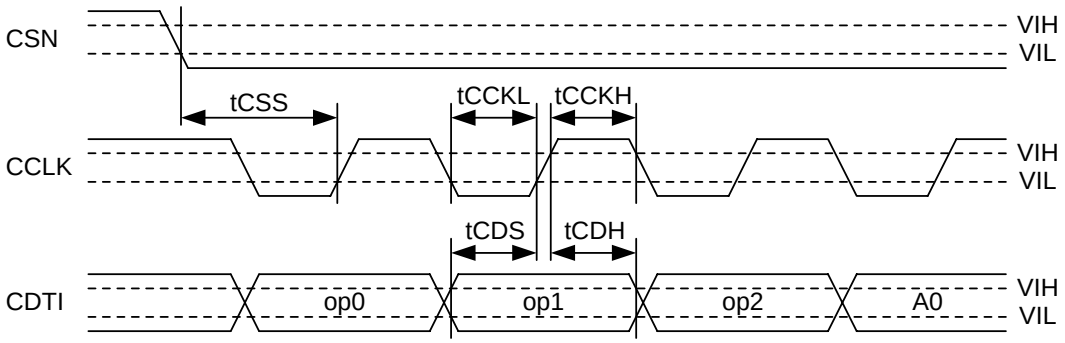



Figure 3. WRITE Command Input Timing

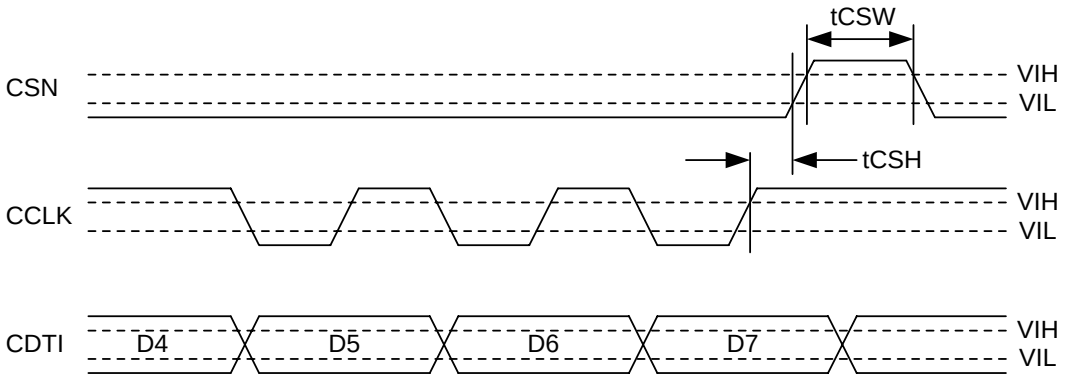



Figure 4. WRITE Data Input Timing

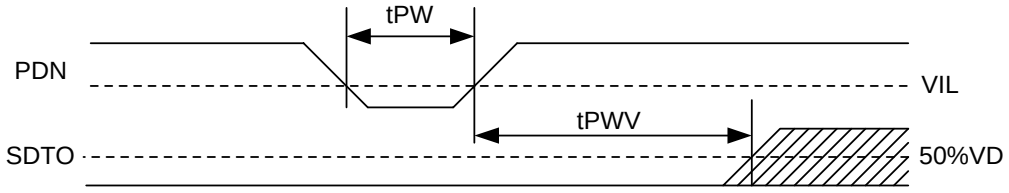



Figure 5. Reset Timing

## OPERATION OVERVIEW

### ■ System Clock

The clocks that are required to operate are MCLK (256fs/384fs), LRCK (fs) and BCLK (40fs~). The master clock (MCLK) should be synchronized with LRCK but the phase is free of care. The frequency of MCLK can be input 256fs or 384fs. When the 384fs is input, the internal master clock is divided into 2/3 automatically.
*fs is sampling frequency.

All external clocks (MCLK, BCLK and LRCK) should always be present whenever ADC is in operation. If these clocks are not provided, the AK5354 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed internally. If the external clocks are not present, the AK5354 should be in the power-down mode.

### ■ Audio Data I/F Format

Using SDTO, BCLK and LRCK pins are connected to external system. Audio data format has two kinds of mode, the data format is MSB-first, 2's compliment. Setting by DIF bit. The initial value is DIF = "0".

| No. | DIF bit | SDTO (ADC) | LRCK | BCLK |
|---|---|---|---|---|
| 0 | 0 | 20bit MSB justified | Lch: "H", Rch: "L" | ≥ 40fs |
| 1 | 1 | $I^2S$ Compatible | Lch: "L", Rch: "H" | ≥ 40fs |

Table 1. Audio Data Format

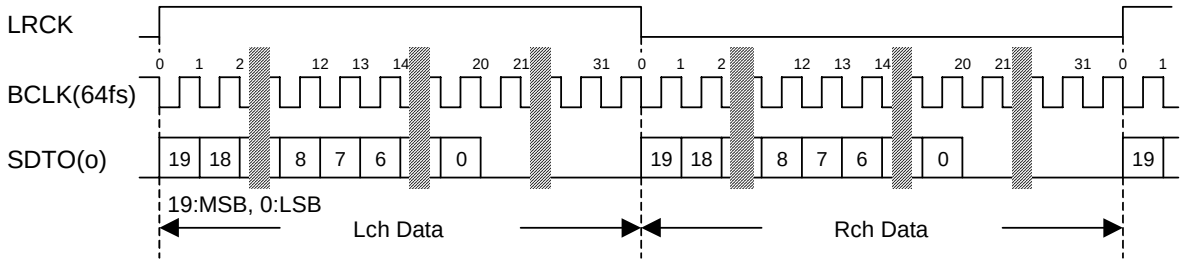



Figure 6. Audio Data Format (No.0)

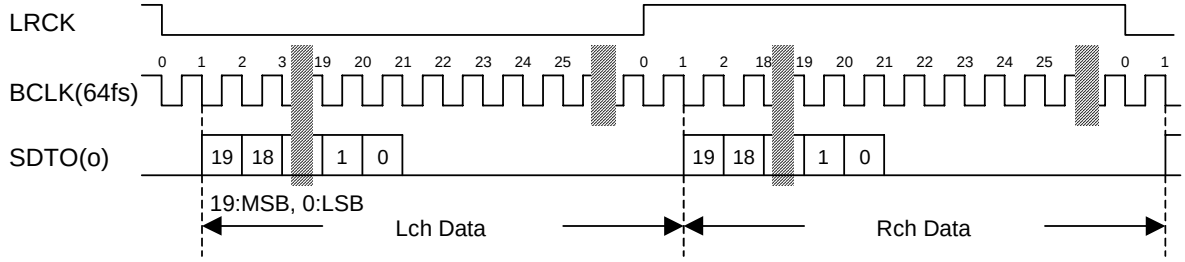



Figure 7. Audio Data Format (No.1)

### ■ Digital High Pass Filter

The AK5354 has a Digital High Pass Filter (HPF) to cancel DC-offset in ADC and IPGA. The cut-off frequency of the HPF is 3.4Hz at fs=44.1kHz. It also scales with the sampling frequency (fs). And digital HPF can be selected by ON/OFF of HPF bit.

## ■ System Reset & Offset Calibration

The AK5354 should be reset once by bringing PDN pin "L" after power-up. The control register values are initialized by PDN "L".

Offset calibration starts by PDN pin "L" to "H". It takes 4128/fs to offset calibration cycle. During offset calibration, the ADC digital data outputs of both channels are forced to a 2's compliment "0". Output data of settles data equivalent for analog input signal after offset calibration. IPGA is set MUTE during offset calibration and after offset calibration.

As a normal offset calibration may not be executed, nothing write at address 01H during offset calibration.

When offset calibration is executed once, the calibration memory is held even if each block is powered down (PM0 = "0" or PM1 = "0") by power management bits.

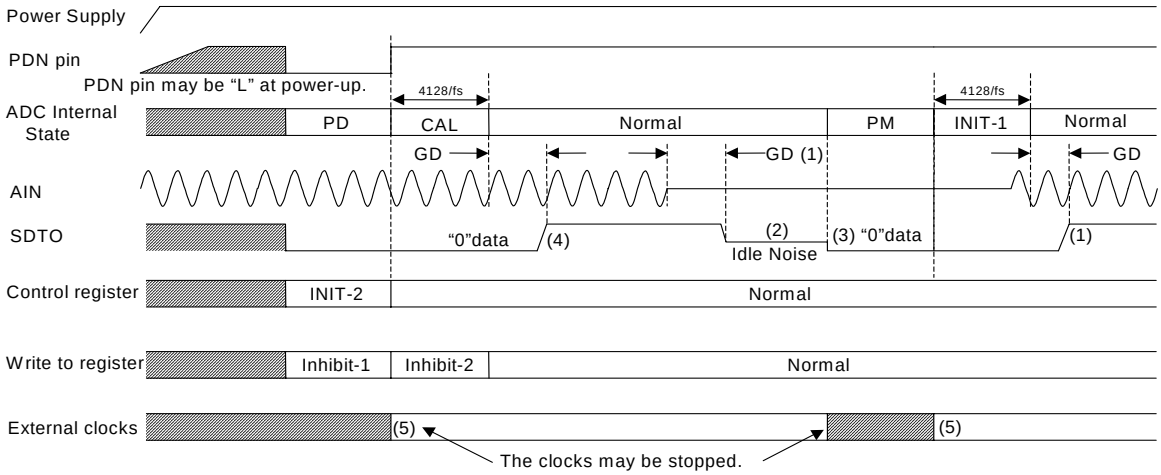



Figure 8. Power up / Power down Timing Example

- PD: Power-down state. ADC is output "0".
- PM: Power-down state by Power Management bit. ADC is output "0".
- CAL: During offset calibration cycle. IPGA is set MUTE state.
- INIT-1: Initializing all control registers.
- Inhibit-1: Inhibits writing to all control registers.
- Inhibit-2: Enable writing to control registers except address 01H.

Note: See "Register Definitions" about the condition of each register.

(1). Digital output corresponding to analog input and analog output corresponding to digital input have the group delay (GD). Output signal gradually comes to settle to input signal during a group delay.

(2). If the analog signal does not be input, digital outputs have the offset to op-amp of input and some offset error of a internal ADC.

(3). ADC output is "0" at power down.

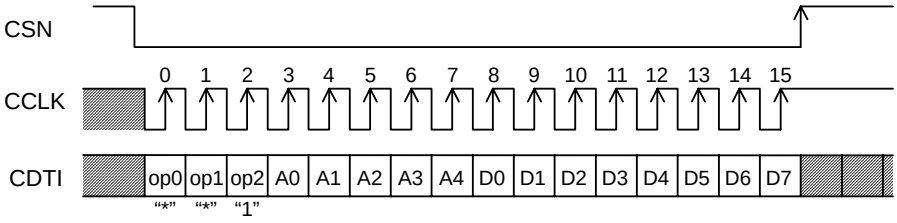
(4). This figure shows that MUTE of IPGA is canceled during offset calibration. If MUTE of IPGA is canceled, SDTO outputs Idle Noise.

(5). When the external clocks (MCLK, BCLK and LRCK) are stopped, the AK5354 should be in the power down (PDN pin = "L" or PM1 bit = "0") mode.

## ■ Timing of Control Register

The internal registers are written by the 3-wire μP interface pins: CSN, CCLK, CDTI. These data are included by Op-code (3bit), Address (LSB-first, 5bit) and Control data (LSB-first, 8bit). A side of transmitted data is output to each bit by "↓" of CCLK, a side of receiving data is input by "↑" of CCLK. Writing of data becomes effective by "↑" of CSN. CSN should be held to "H" at no access.

Address except 00H ~ 03H inhibits control of writing. And CCLK always need 16 edges of "↑" during CSN = "L".




op0-op2: Op code (Fixed to "**1:WRITE")
A0-A4: Register Address
D0-D7: Control data

Figure 9. Control Data Timing

## ■ Register Map

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Input Select | 0 | 0 | 0 | HPF | RIN2 | RIN1 | LIN2 | LIN1 |
| 01H | Mode Control 1 | 0 | 0 | 0 | 0 | 0 | 0 | PM1 | PM0 |
| 02H | Mode Control 2 | MONO1 | MONO0 | ZTM1 | ZTM0 | 0 | 0 | DIF | 0 |
| 03H | Input Analog PGA Control | ZEIP | IPGA6 | IPGA5 | IPGA4 | IPGA3 | IPGA2 | IPGA1 | IPGA0 |

All registers are reset at PDN = "L", then inhibits writing to all registers.

## ■ Register Definition

### Input Select

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Input Select | 0 | 0 | 0 | HPF | RIN2 | RIN1 | LIN2 | LIN1 |
| RESET | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

HPF: Select ON/OFF of the digital HPF. (0: ON, 1: OFF)

LIN2-1: Select ON/OFF of Lch input. (0: OFF, 1: ON)
RIN2-1: Select ON/OFF of Rch input. (0: OFF, 1: ON)

### Mode Control 1

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 01H | Mode Control 1 | 0 | 0 | 0 | 0 | 0 | 0 | PM1 | PM0 |
| RESET | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

PM1-0: Power Management (0: Power down, 1: Power up)
PM0: Power control of IPGA
PM1: Power control of ADC

When PDN pin goes “L”, all circuit in the AK5354 can be powered-down in no relation to PM1-0. When PM1-0 goes all “0”, all circuit in the AK5354 can be also powered-down. However, the contents of control registers are held.

In case of PM1 = “1”, MCLK is not stopped.

### Mode Control 2

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 02H | Mode Control 2 | MONO1 | MONO0 | ZTM1 | ZTM0 | 0 | 0 | DIF | 0 |
| RESET | | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

MONO1-0: Monaural Mixing
- 00: Stereo (RESET)
- 01: (L+R)/2
- 10: LL
- 11: RR

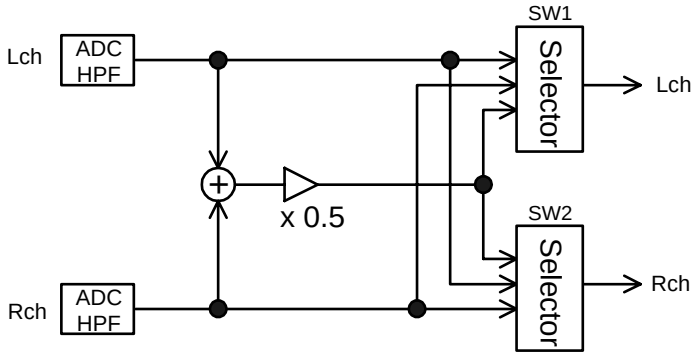



Figure 10. Monaural mixing block

| Mode | SW1 | SW2 | MONO1 | MONO0 |
|---|---|---|---|---|
| Stereo Recording | Lch | Rch | 0 | 0 |
| Monaural Recording Stereo Input | (L+R)/2 | (L+R)/2 | 0 | 1 |
| Monaural Recording Lch Input | Lch | Lch | 1 | 0 |
| Monaural Recording Rch Input | Rch | Rch | 1 | 1 |

Table 2. Monaural Mode Setting

ZTM1-0: Setting of Zero Crossing Timeout for IPGA
- 00: 256/fs
- 01: 512/fs
- 10: 1024/fs
- 11: 2048/fs (RESET)

DIF: Select Digital Interface Format

| No. | DIF bit | SDTO(ADC) | LRCK | BCLK | |
|---|---|---|---|---|---|
| 0 | 0 | 20bit MSB justified | Lch: “H”, Rch: “L” | ≥ 40fs | Reset |
| 1 | 1 | $I^2S$ Compatible | Lch: “L”, Rch: “H” | ≥ 40fs | |

Table 3. Audio Data Format

Inhibits writing at PM1 = “0”.

### Input Analog PGA Control

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 03H | Input Analog PGA Control | ZEIP | IPGA6 | IPGA5 | IPGA4 | IPGA3 | IPGA2 | IPGA1 | IPGA0 |
| RESET | | 0 | 00H (MUTE) | | | | | | |

ZEIP: Select IPGA zero crossing operation (0: Disable, 1: Enable)

Writing to IPGA value at ZEIP = "1", IPGA value of L/R channels changes by zero crossing detection or timeout independently.

In the timeout cycle, it is possible to set in ZTM1-0 bit.
When ZTM1-0 is "11", timeout cycle is 2048/fs = 46.4ms (@fs=44.kHz).
When ZEIP is "0", IPGA changes immediately. When PM1 is "0", ZEIP is ignored and IPGA does the operation which is the same as the case of ZEIP = "0".

IPGA6-0: Input Analog PGA. 97 levels. 00H=MUTE.

ON/OFF of zero crossing detection can be controlled by ZEIP bit.
Inhibits writing at PM0 = "0".

| DATA | GAIN(dB) | Step | Level |
|---|---|---|---|
| 60H | +28.0 | 0.5dB | 73 |
| 5FH | +27.5 | | |
| 5EH | +27.0 | | |
| • | • | | |
| 28H | +0.0 | | |
| 27H | -0.5 | | |
| • | • | | |
| 19H | -7.5 | | |
| 18H | -8.0 | | |
| 17H | -9.0 | 1dB | 8 |
| 16H | -10.0 | | |
| • | • | | |
| 11H | -15.0 | | |
| 10H | -16.0 | | |
| 0FH | -18.0 | 2dB | 12 |
| 0EH | -20.0 | | |
| • | • | | |
| 05H | -38.0 | | |
| 04H | -40.0 | | |
| 03H | -44.0 | 4dB | 3 |
| 02H | -48.0 | | |
| 01H | -52.0 | | |
| 00H | MUTE | | 1 |

Table 4. Input Gain Setting

• About zero crossing operation

Comparator for zero crossing detection in the AK5354 has offset. Therefore, it is a possible that IPGA value is changed by zero crossing timeout as zero crossing detection does not occur by a little offset of comparator.

For example, when Lch and Rch are in the state of IPGA = 30H, both channels are set to IPGA = 31H. And then the only Lch completed zero crossing, Rch is waiting for zero crossing detection, zero crossing counter is reset when IPGA is newly written 32H, zero crossing operation starts toward IPGA = 32H in state Lch = 31H, Rch = 30H. Internal IPGA value in the AK5354 has the registers of L/R channels independently, according to change IPGA value independently, IPGA value of L/R channels may become a difference in level.

Therefore, if IPGA is written before zero crossing detection on zero crossing timeout, IPGA is keeping the same value. When IPGA is finished by normal zero crossing timeout on IPGA value of L/R channels does not give a difference in level, the change of IPGA should be written after zero crossing timeout cycle and over.

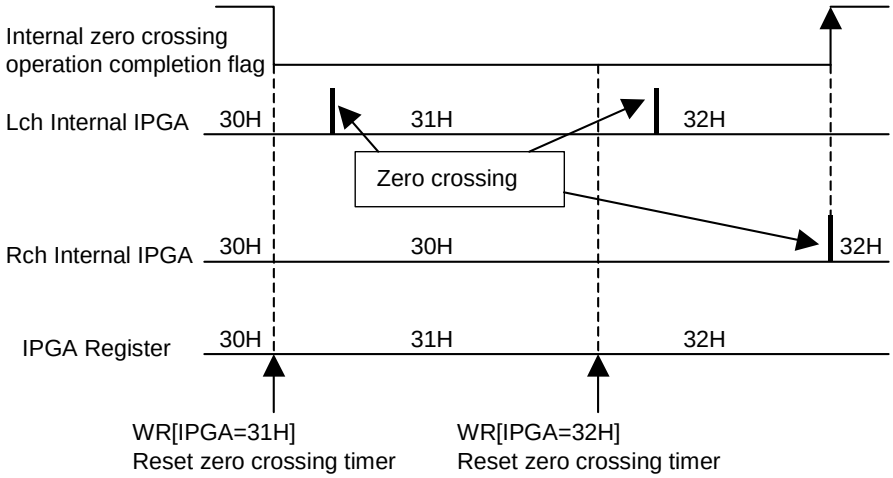



Figure 11. About Zero Crossing Operation

## SYSTEM DESIGN

Figure 12 shows the system connection diagram. An evaluation board [AKD5354] is available which demonstrates application circuit, optimum layout, power supply arrangements and measurement results.

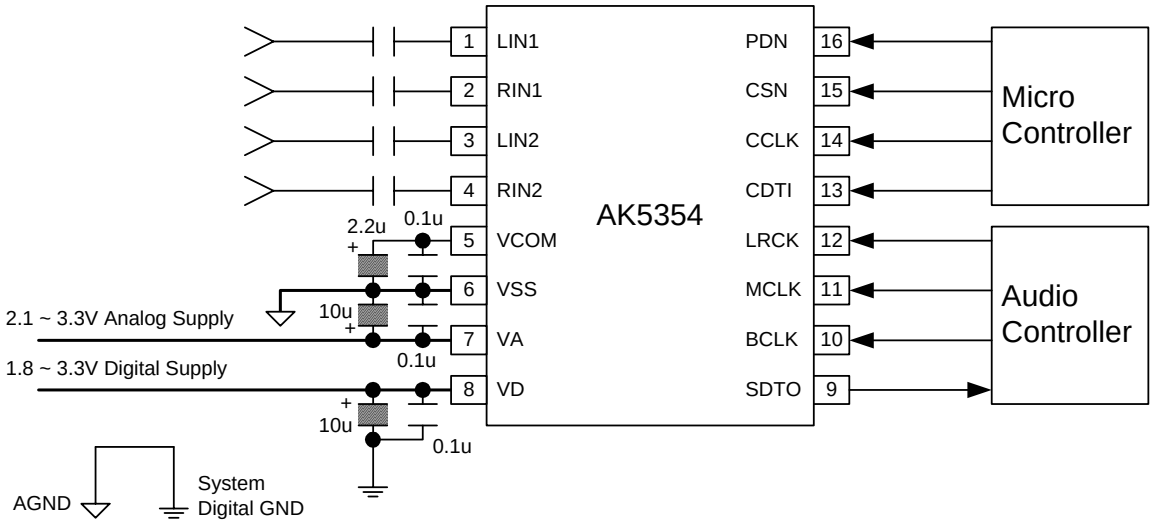



Figure 12. System Connection Diagram Example

Notes:

- Electrolytic capacitor value of VCOM depends on low frequency noise of supply voltage.

**1. Grounding and Power Supply Decoupling**

The AK5354 requires careful attention to power supply and grounding arrangements. VA is usually supplied from analog supply in system. VD is a power supply pin to interface with the external ICs and is supplied from digital supply in system. VSS of the AK5354 should be connected to analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK5354 as possible, with the small value ceramic capacitor being the nearest.

**2. Voltage Reference**

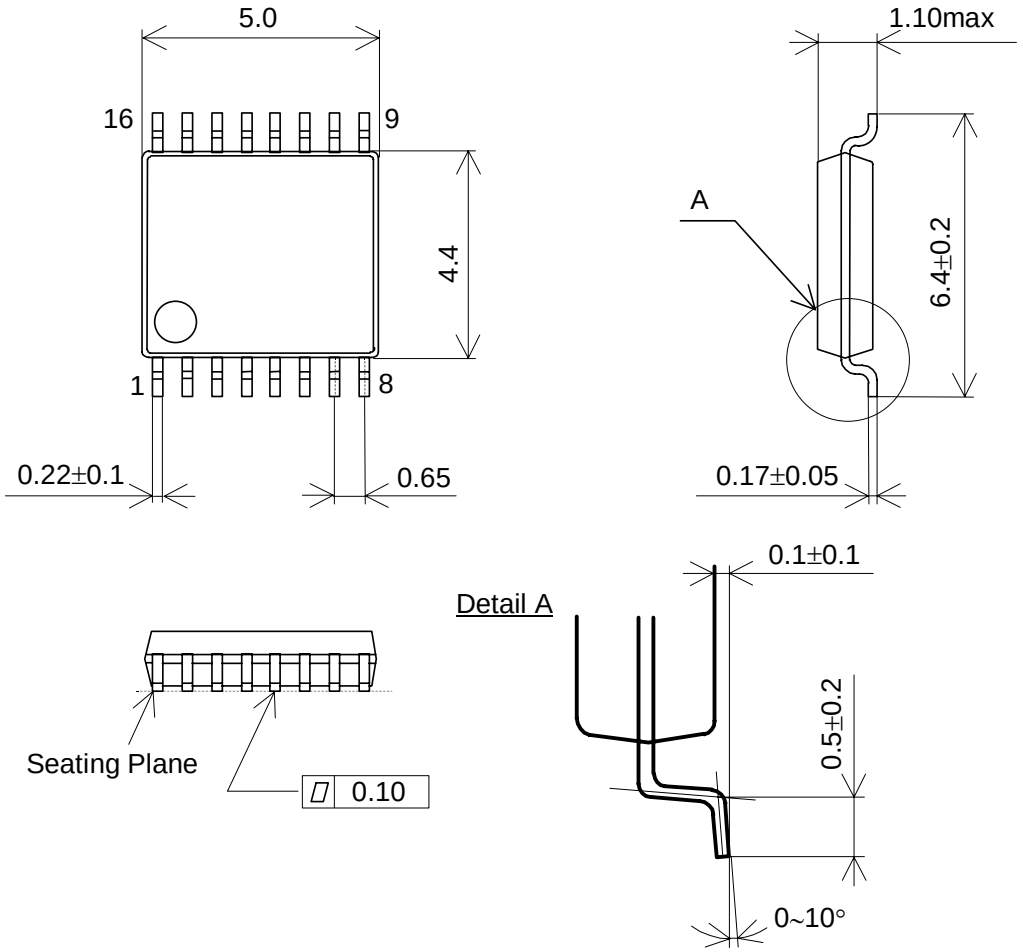
The input to VA Voltage sets the analog input range. A 0.1μF ceramic capacitor and a 10μF electrolytic capacitor is connected to VA and VSS pins, normally. VCOM is a signal ground of this chip. An electrolytic 2.2μF in parallel with a 0.1μF ceramic capacitor attached to these pins eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clock, should be kept away from the VA, VD and VCOM pins in order to avoid unwanted coupling into the AK5354.

**3. Analog Inputs**

The analog inputs are single-ended and the input resistance 9kΩ (typ). The input signal range scales with nominally 0.6 x VA Vpp (typ) centered in the internal common voltage (typ. 0.45 x VA). Usually, the input signal cuts DC with a capacitor. The cut-off frequency is fc=(1/2πRC). The AK5354 can accept input voltages from VSS to VA. The ADC output data format is 2's complement. The DC offset including ADC own DC offset removed by the internal HPF (fc=3.4Hz@fs=44.1kHz).

## PACKAGE

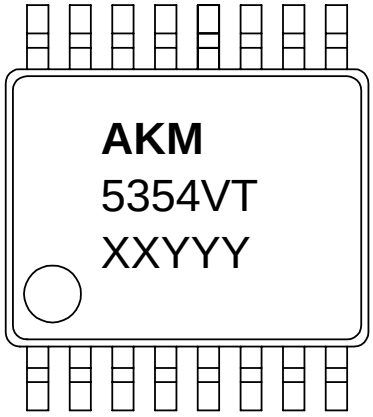
16pin TSSOP (Unit: mm)




■ **Package & Lead frame material**

| | |
|---|---|
| Package molding compound: | Epoxy |
| Lead frame material: | Cu |
| Lead frame surface treatment: | Solder plate |

## MARKING




1) Pin #1 indication
2) Date Code : XXYYY (5 digits)
   XX : lot#
   YYY : Date Code
3) Marketing Code : 5354VT
4) Asahi Kasei Logo

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