256-Position, One-Time Programmable, Dual-Channel, I²C Digital Potentiometers

FEATURES

- 2-channel, 256-position potentiometers
- One-time programmable (OTP) set-and-forget resistance setting provides a low cost alternative to EEMEM
- Unlimited adjustments before OTP activation
- OTP overwrite allows dynamic adjustments with user defined preset
- End-to-end resistance: 2.5 kΩ, 10 kΩ, and 100 kΩ
- Compact 10-lead MSOP: 3 mm × 4.9 mm
- Fast settling time: t_S = 5 µs typical on power-up
- Full read/write of wiper register
- Power-on preset to midscale
- Extra package address decode pins: AD0 and AD1 (AD5173)
- Single supply: 2.7 V to 5.5 V
- Low temperature coefficient: 35 ppm/°C
- Low power: I_{DD} = 6 µA maximum
- Wide operating temperature: −40°C to +125°C

APPLICATIONS

- Systems calibration
- Electronics level setting
- Mechanical trimmers replacement in new designs
- Permanent factory PCB setting
- Transducer adjustment of pressure, temperature, position, chemical, and optical sensors
- RF amplifier biasing
- Gain control and offset adjustment

FUNCTIONAL BLOCK DIAGRAMS

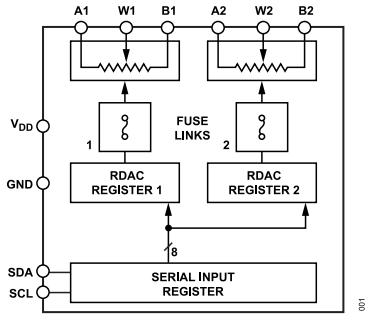


Figure 1. AD5172 Functional Block Diagram

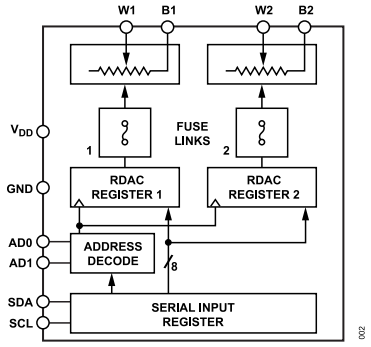


Figure 2. AD5173 Functional Block Diagram

GENERAL DESCRIPTION

The AD5172/AD5173 are dual-channel, 256-position, one-time programmable (OTP) digital potentiometers that employ fuse link technology to achieve memory retention of resistance settings. The digital potentiometer, VR, and RDAC terms are used interchangeably. OTP is a cost-effective alternative to EEMEM for users who do not need to program the digital potentiometer setting in memory more than once. These devices perform the same electronic adjustment function as mechanical potentiometers or variable resistors but with enhanced resolution, solid-state reliability, and superior low temperature coefficient performance.

TheAD5172/AD5173 are programmed using a 2-wire, I²C-compatible digital interface. Unlimited adjustments are allowed before permanently setting the resistance value. During OTP activation, a permanent blow fuse command freezes the wiper position (analogous to placing epoxy on a mechanical trimmer).

Unlike traditional OTP digital potentiometers, the AD5172/AD5173 have a unique temporary OTP overwrite feature that allows for new adjustments even after a fuse is blown. However, the OTP setting is restored during subsequent power-up conditions. This allows users to treat these digital potentiometers as volatile potentiometers with a programmable preset.

DOCUMENT FEEDBACK
TECHNICAL SUPPORT

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REVISION HISTORY

1/2022—Rev. I to Rev. J

Changes to Features Section ... 1
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Changes to OTP Supply Current Parameter and Power Supply Range Parameter, Table 1 ... 3
Changed Electrical Characteristics 10 kΩ, 50 kΩ, and 100 kΩ Section to Electrical Characteristics: 10 kΩ and 100 kΩ Section ... 4
Changes to OTP Supply Current Parameter, Bandwidth, −3 dB Parameter, and Power Supply Range Parameter, Table 2 ... 4
Deleted Figure 21; Renumbered Sequentially ... 9
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Moved Figure 46 ... 16
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Changes to Ordering Guide ... 21

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS: 2.5 KΩ

V_{DD} = 5 V ± 10%, or 3 V ± 10%; $V_A = V_{DD}$; V_B = 0 V; −40°C < T_A < +125°C; unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	−2	±0.1	+2	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−14	±2	+14	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	−20		+55	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$			35		ppm/°C
Wiper Resistance	R_{WB}	Code = 0x00, V_{DD} = 5 V		160	200	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE[4]						
Differential Nonlinearity[5]	DNL		−1.5	±0.1	+1.5	LSB
Integral Nonlinearity[5]	INL		−2	±0.6	+2	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	−14	−5.5	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	4.5	12	LSB
RESISTOR TERMINALS						
Voltage Range[6]	V_A, V_B, V_W		GND		V_{DD}	V
Capacitance A, B[7]	C_A, C_B	f = 1 MHz, measured to GND, code = 0x80		45		pF
Capacitance W[7]	C_W	f = 1 MHz, measured to GND, code = 0x80		60		pF
Shutdown Supply Current[8]	I_{A_SD}	V_{DD} = 5.5 V		0.01	1	µA
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
SDA and SCL						
Input Logic High[9]	V_{IH}	V_{DD} = 5 V	0.7 V_{DD}		V_{DD} + 0.5	V
Input Logic Low[9]	V_{IL}	V_{DD} = 5 V	−0.5		+0.3 V_{DD}	V
AD0 and AD1						
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[7]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD}		2.7		5.5	V
OTP Supply Voltage[9, 10]	V_{DD_OTP}	T_A = 25°C	5.6	5.7	5.8	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3.5	6	µA
OTP Supply Current[9, 11, 12]	I_{DD_OTP}	V_{DD_OTP} = 5.7 V, T_A = 25°C		100		mA
Power Dissipation[13]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			33	µW
Power Supply Sensitivity	PSS	V_{DD} = 5 V ± 10%, code = midscale		±0.02	±0.08	%/%
DYNAMIC CHARACTERISTICS[14]						
Bandwidth, −3 dB	BW	Code = 0x80		4.8		MHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		0.1		%
V_W Settling Time	t_S	V_A = 5 V, V_B = 0 V, ±1 LSB error band		1		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 1.25 kΩ, R_S = 0 Ω		3.2		nV/√Hz

[1] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.

SPECIFICATIONS

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit

[2] Resistor position nonlinearity error, R-INL, is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. Parts are guaranteed monotonic.

[3] $V_A = V_{DD}$, $V_B = 0$ V, wiper (V_W) = no connect.

[4] Specifications apply to all VRs.

[5] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and $V_B = 0$ V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.

[6] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other.

[7] Guaranteed by design, but not subject to production test.

[8] Measured at Terminal A. Terminal A is open circuited in shutdown mode.

[9] The minimum voltage requirement on the V_{IH} is 0.7 V × V_{DD}. For example, V_{IH} minimum = 3.5 V when V_{DD} = 5 V. It is typical for the SCL and SDA resistors to be pulled up to V_{DD}. However, care must be taken to ensure that the minimum V_{IH} is met when the SCL and SDA are driven directly from a low voltage logic controller without pull-up resistors.

[10] Different from the operating power supply; the power supply for OTP is used one time only.

[11] Different from the operating current; the supply current for OTP lasts approximately 400 ms for one time only.

[12] See Figure 29 for an energy plot during an OTP program.

[13] P_{DISS} is calculated from (I_{DD} × V_{DD}). CMOS logic level inputs result in minimum power dissipation.

[14] All dynamic characteristics use V_{DD} = 5 V.

ELECTRICAL CHARACTERISTICS: 10 KΩ AND 100 KΩ

V_{DD} = 5 V ± 10% or 3 V ± 10%; $V_A = V_{DD}$; V_B = 0 V; −40°C < T_A < +125°C; unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	−1	±0.1	+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−2.5	±0.25	+2.5	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	−20		+20	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T$			35		ppm/°C
Wiper Resistance	R_{WB}	Code = 0x00, V_{DD} = 5 V		160	200	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE[4]						
Differential Nonlinearity[5]	DNL		−1	±0.1	+1	LSB
Integral Nonlinearity[5]	INL		−1	±0.3	+1	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	−2.5	−1	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	1	2.5	LSB
RESISTOR TERMINALS						
Voltage Range[6]	V_A, V_B, V_W		GND		V_{DD}	V
Capacitance A, B[7]	C_A, C_B	f = 1 MHz, measured to GND, code = 0x80		45		pF
Capacitance W[7]	C_W	f = 1 MHz, measured to GND, code = 0x80		60		pF
Shutdown Supply Current[8]	I_{A_SD}	V_{DD} = 5.5 V		0.01	1	µA
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
SDA and SCL						
Input Logic High[9]	V_{IH}	V_{DD} = 5 V	0.7 V_{DD}		V_{DD} + 0.5	V

SPECIFICATIONS

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
Input Logic Low[9]	V_{IL}	V_{DD} = 5 V	−0.5		+0.3 V_{DD}	V
AD0 and AD1						
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[7]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD}		2.7		5.5	V
OTP Supply Voltage[9, 10]	V_{DD_OTP}	T_A = 25°C	5.6	5.7	5.8	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3.5	6	µA
OTP Supply Current[9, 11, 12]	I_{DD_OTP}	V_{DD_OTP} = 5.7 V, T_A = 25°C		100		mA
Power Dissipation[13]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			33	µW
Power Supply Sensitivity	PSS	V_{DD} = 5 V ± 10%, code = midscale		±0.02	±0.08	%/%
DYNAMIC CHARACTERISTICS[14]						
Bandwidth, −3 dB	BW	R_{AB} = 10 kΩ, code = 0x80		600		kHz
		R_{AB} = 100 kΩ, code = 0x80		40		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 10 kΩ		0.1		%
V_W Settling Time	t_S	V_A = 5 V, V_B = 0 V, ±1 LSB error band		2		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 5 kΩ, R_S = 0 Ω		9		nV/√Hz

[1] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.

[2] Resistor position nonlinearity error, R-INL, is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. Parts are guaranteed monotonic.

[3] V_A = V_{DD}, V_B = 0 V, wiper (V_W) = no connect.

[4] Specifications apply to all VRs.

[5] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.

[6] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other.

[7] Guaranteed by design, but not subject to production test.

[8] Measured at Terminal A. Terminal A is open circuited in shutdown mode.

[9] The minimum voltage requirement on the V_{IH} is 0.7 V × V_{DD}. For example, V_{IH} minimum = 3.5 V when V_{DD} = 5 V. It is typical for the SCL and SDA resistors to be pulled up to V_{DD}. However, care must be taken to ensure that the minimum V_{IH} is met when the SCL and SDA are driven directly from a low voltage logic controller without pull-up resistors.

[10] Different from the operating power supply; the power supply for OTP is used one time only.

[11] Different from the operating current; the supply current for OTP lasts approximately 400 ms for one time only.

[12] See Figure 29 for an energy plot during an OTP program.

[13] P_{DISS} is calculated from (I_{DD} × V_{DD}). CMOS logic level inputs result in minimum power dissipation.

[14] All dynamic characteristics use V_{DD} = 5 V.

SPECIFICATIONS

TIMING CHARACTERISTICS

V_{DD} = 5 V ± 10%, or 3 V ± 10%; $V_A = V_{DD}$; V_B = 0 V; −40°C < T_A < +125°C; unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
I^2C INTERFACE TIMING CHARACTERISTICS[1]						
SCL Clock Frequency	f_{SCL}				400	kHz
Bus-Free Time Between Stop and Start, t_{BUF}	t_1		1.3			µs
Hold Time (Repeated Start), $t_{HD;STA}$	t_2	After this period, the first clock pulse is generated.	0.6			µs
Low Period of SCL Clock, t_{LOW}	t_3		1.3			µs
High Period of SCL Clock, t_{HIGH}	t_4		0.6			µs
Setup Time for Repeated Start Condition, $t_{SU;STA}$	t_5		0.6			µs
Data Hold Time, $t_{HD;DAT}$[2]	t_6				0.9	µs
Data Setup Time, $t_{SU;DAT}$	t_7		100			ns
Fall Time of Both SDA and SCL Signals, t_F	t_8				300	ns
Rise Time of Both SDA and SCL Signals, t_R	t_9				300	ns
Setup Time for Stop Condition, $t_{SU;STO}$	t_{10}		0.6			µs
OTP Program Time	t_{11}			400		ms

[1] See the timing diagrams for the locations of measured values (that is, see Figure 3 and Figure 47 to Figure 50).

[2] The maximum $t_{HD;DAT}$ has to be met only if the device does not stretch the low period (t_{LOW}) of the SCL signal.

Timing Diagram

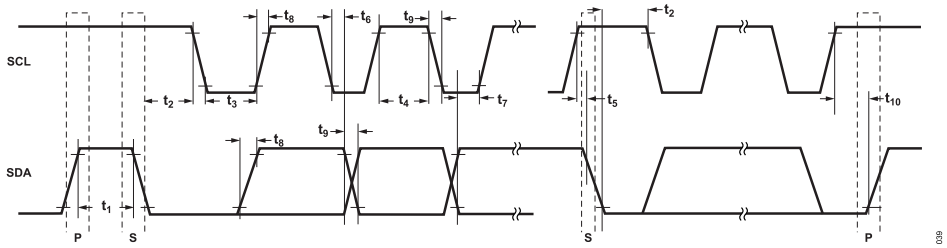


Figure 3. I^2C Interface Detailed Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_A, V_B, V_W to GND	−0.3 V to +7 V or V_{DD} + 0.3 V (whichever is less)
Terminal Current, Ax to Bx, Ax to Wx, Bx to Wx	
Pulsed	±20 mA
Continuous	±5 mA
Digital Inputs and Output Voltage to GND	−0.3 V to +7 V or V_{DD} + 0.3 V (whichever is less)
Operating Temperature Range	−40°C to +125°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Thermal Resistance	
θ_{JA} for 10-Lead MSOP	200°C/W

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

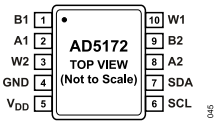


Figure 4. AD5172 Pin Configuration

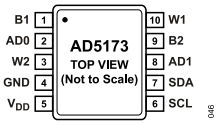


Figure 5. AD5173 Pin Configuration

Table 5. AD5172 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	B1	B1 Terminal. GND ≤ V_{B1} ≤ V_{DD}.
2	A1	A1 Terminal. GND ≤ V_{A1} ≤ V_{DD}.
3	W2	W2 Terminal. GND ≤ V_{W2} ≤ V_{DD}.
4	GND	Digital Ground.
5	V_{DD}	Positive Power Supply. Specified for operation from 2.7 V to 5.5 V. For OTP programming, V_{DD} needs to be a minimum of 5.6 V but no more than 5.8 V and to be capable of driving 100 mA.
6	SCL	Serial Clock Input. Positive-edge triggered. Requires a pull-up resistor. If this pin is driven directly from a logic controller without a pull-up resistor, ensure that the V_{IH} minimum is 0.7 V × V_{DD}.
7	SDA	Serial Data Input/Output. Requires a pull-up resistor. If this pin is driven directly from a logic controller without a pull-up resistor, ensure that the V_{IH} minimum is 0.7 V × V_{DD}.
8	A2	A2 Terminal. GND ≤ V_{A2} ≤ V_{DD}.
9	B2	B2 Terminal. GND ≤ V_{B2} ≤ V_{DD}.
10	W1	W1 Terminal. GND ≤ V_{W1} ≤ V_{DD}.

Table 6. AD5173 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	B1	B1 Terminal. GND ≤ V_{B1} ≤ V_{DD}.
2	AD0	Programmable Address Bit 0 for Multiple Package Decoding.
3	W2	W2 Terminal. GND ≤ V_{W2} ≤ V_{DD}.
4	GND	Digital Ground.
5	V_{DD}	Positive Power Supply. Specified for operation from 2.7 V to 5.5 V. For OTP programming, V_{DD} needs to be a minimum of 5.6 V but no more than 5.8 V and to be capable of driving 100 mA.
6	SCL	Serial Clock Input. Positive-edge triggered. Requires a pull-up resistor. If this pin is driven directly from a logic controller without a pull-up resistor, ensure that the V_{IH} minimum is 0.7 V × V_{DD}.
7	SDA	Serial Data Input/Output. Requires a pull-up resistor. If this pin is driven directly from a logic controller without a pull-up resistor, ensure that the V_{IH} minimum is 0.7 V × V_{DD}.
8	AD1	Programmable Address Bit 1 for Multiple Package Decoding.
9	B2	B2 Terminal. GND ≤ V_{B2} ≤ V_{DD}.
10	W1	W1 Terminal. GND ≤ V_{W1} ≤ V_{DD}.

TYPICAL PERFORMANCE CHARACTERISTICS

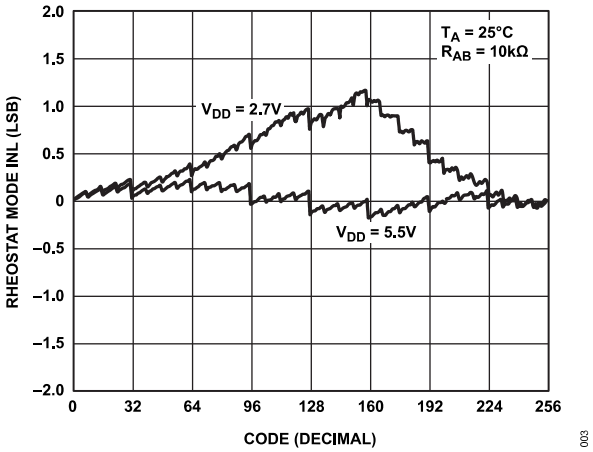


Figure 6. R-INL vs. Code vs. Supply Voltages

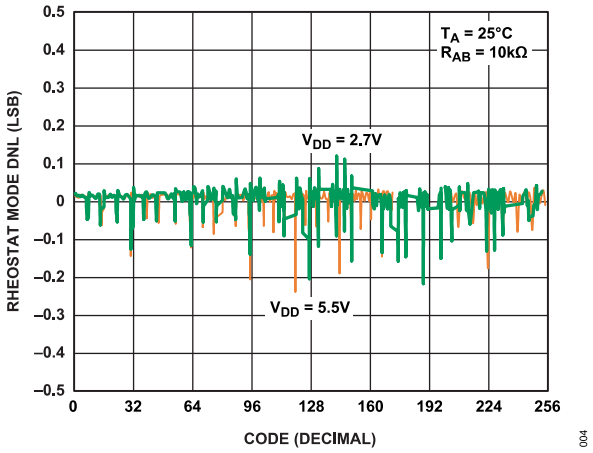


Figure 7. R-DNL vs. Code vs. Supply Voltages

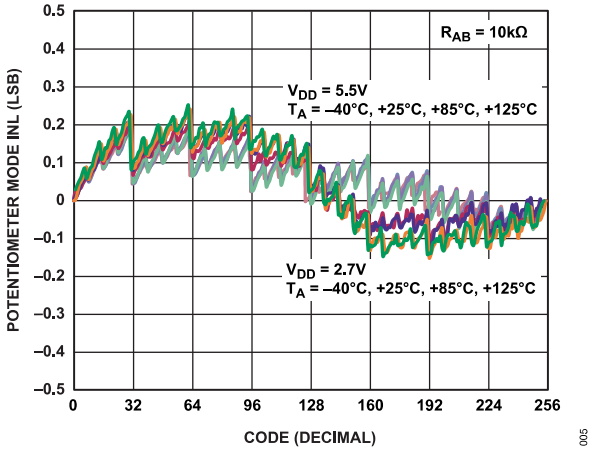


Figure 8. INL vs. Code vs. Temperature

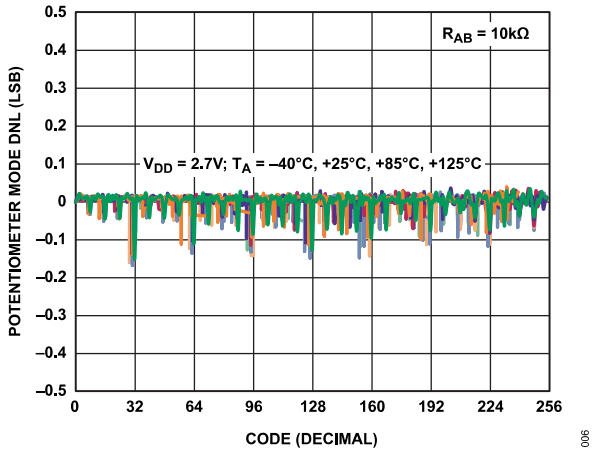


Figure 9. DNL vs. Code vs. Temperature

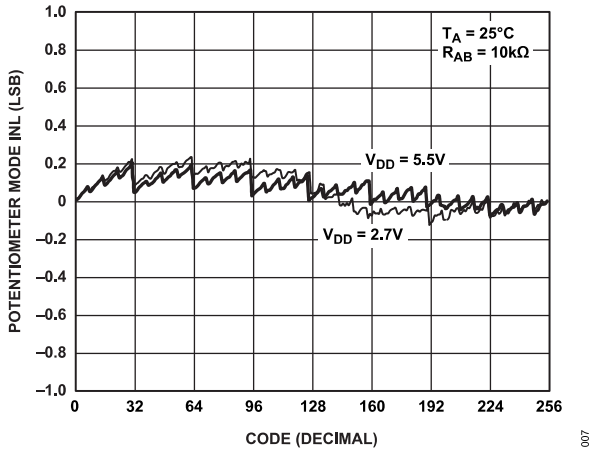


Figure 10. INL vs. Code vs. Supply Voltages

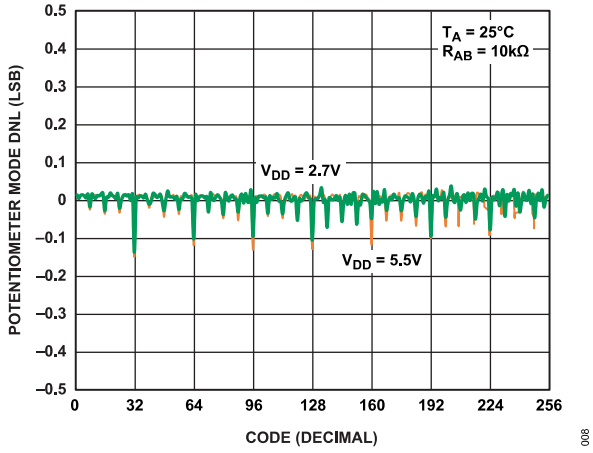


Figure 11. DNL vs. Code vs. Supply Voltages

TYPICAL PERFORMANCE CHARACTERISTICS

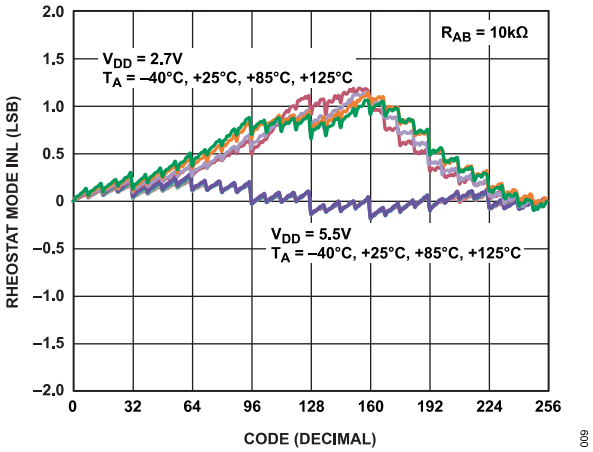


Figure 12. R-INL vs. Code vs. Temperature

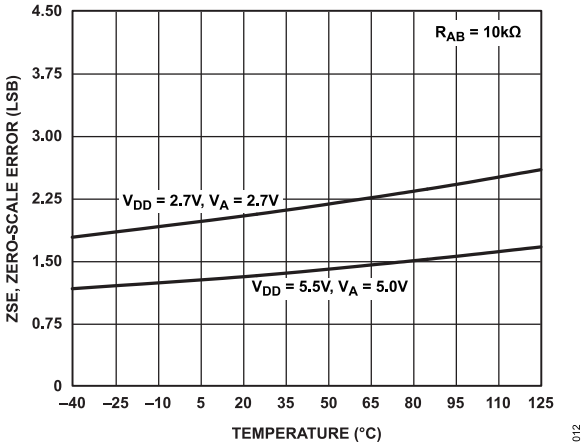


Figure 15. Zero-Scale Error vs. Temperature

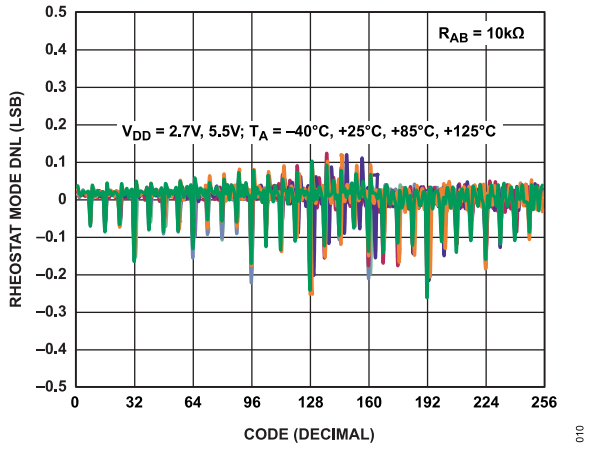


Figure 13. R-DNL vs. Code vs. Temperature

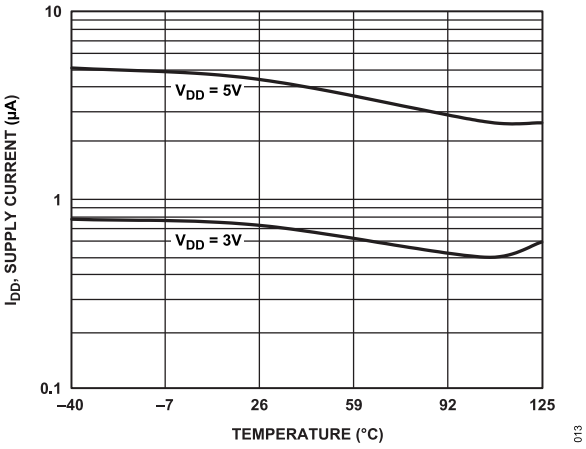


Figure 16. Supply Current vs. Temperature

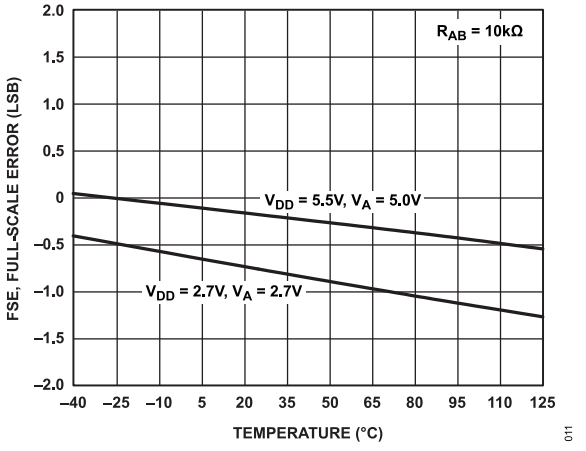


Figure 14. Full-Scale Error vs. Temperature

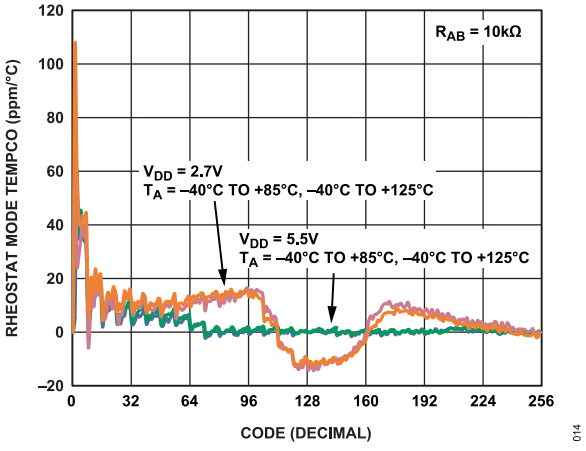


Figure 17. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

TYPICAL PERFORMANCE CHARACTERISTICS

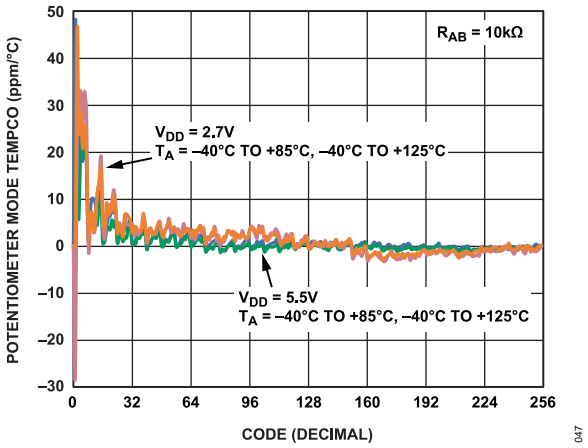


Figure 18. AD5172 Potentiometer Mode Tempco $\Delta V_{WB}/\Delta T$ vs. Code

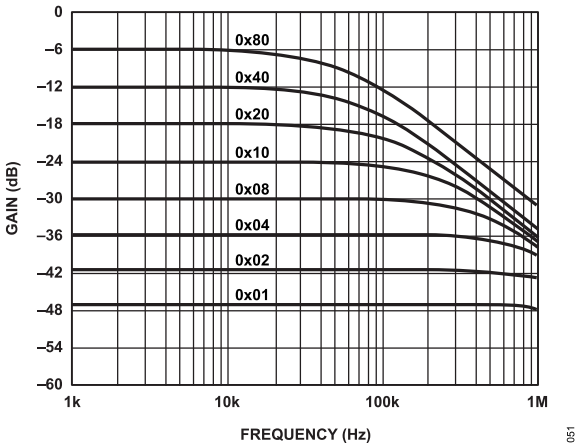


Figure 21. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ

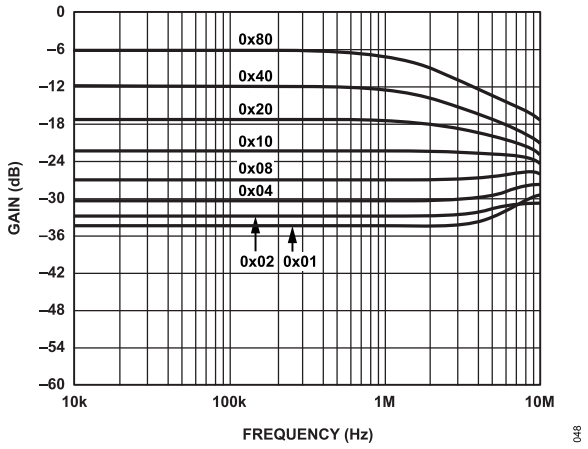


Figure 19. Gain vs. Frequency vs. Code, R_{AB} = 2.5 kΩ

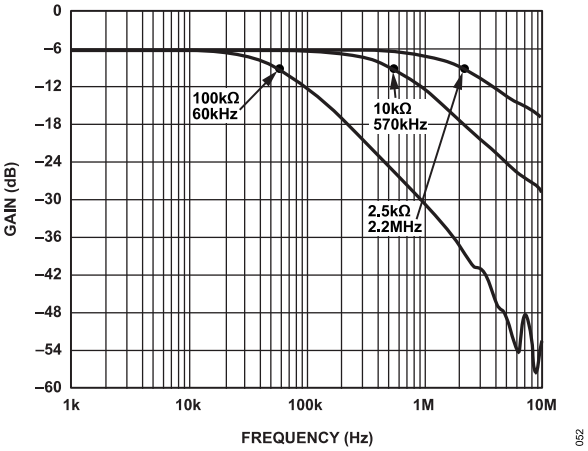


Figure 22. −3 dB Bandwidth at Code = 0x80

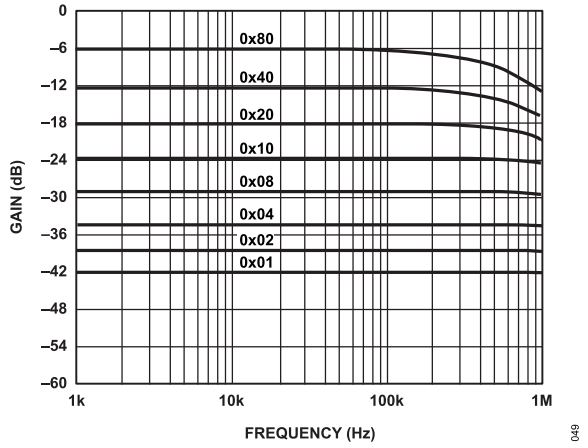


Figure 20. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ

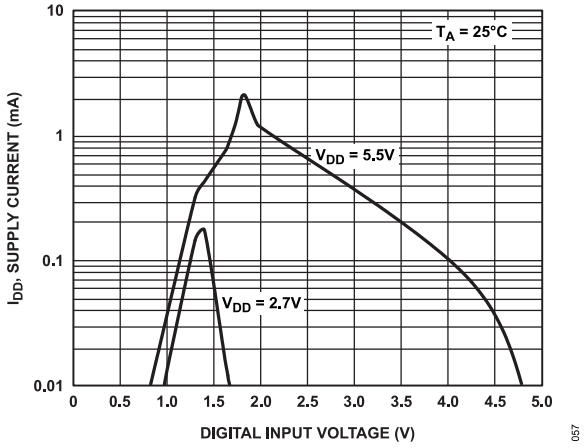


Figure 23. Supply Current vs. Digital Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

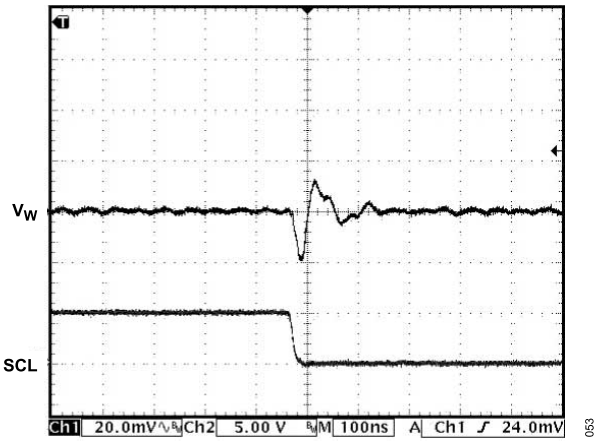


Figure 24. Digital Feedthrough

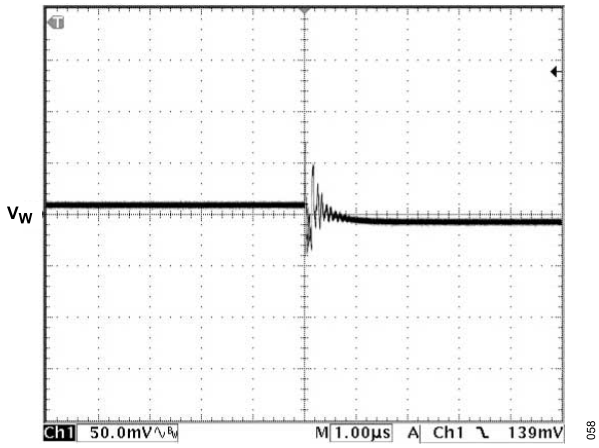


Figure 27. Midscale Glitch, Code 0x80 to Code 0x7F

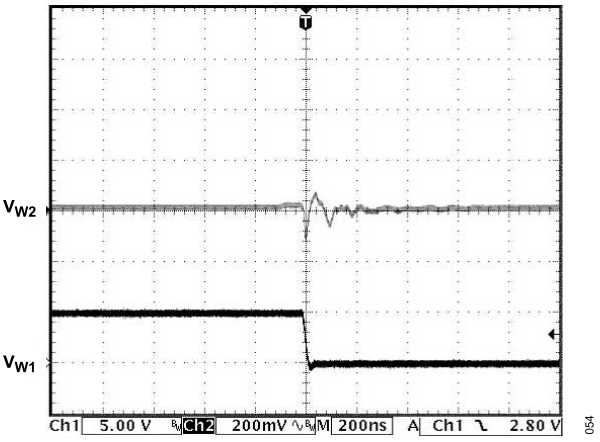


Figure 25. Digital Crosstalk

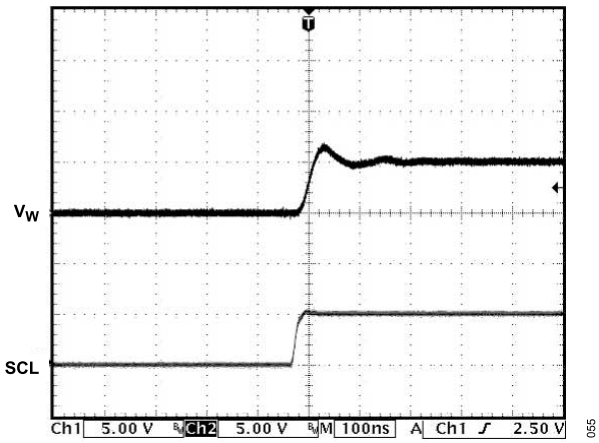


Figure 28. Large-Signal Settling Time

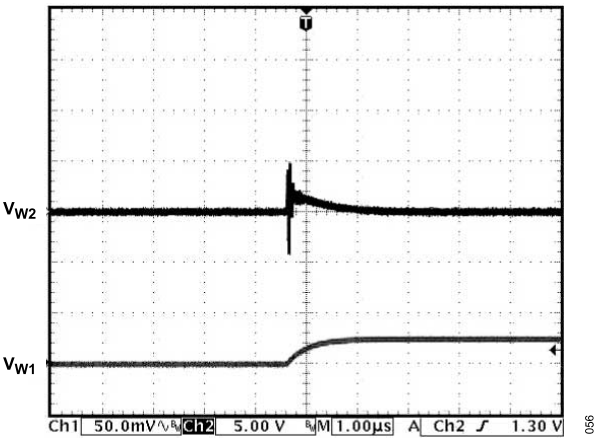


Figure 26. Analog Crosstalk

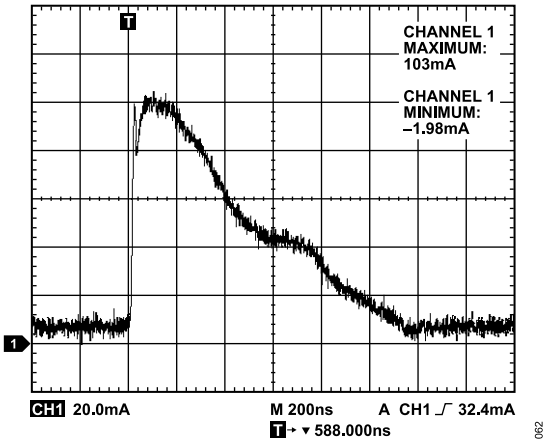


Figure 29. OTP Program Energy for Single Fuse

TEST CIRCUITS

Figure 30 to Figure 37 illustrate the test circuits that define the test conditions used in the product specification tables (see Table 1 and Table 2).

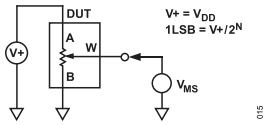


Figure 30. Potentiometer Divider Nonlinearity Error (INL, DNL)

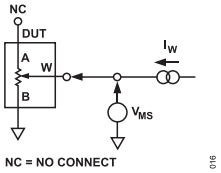


Figure 31. Resistor Position Nonlinearity Error (Rheostat Operation: R-INL, R-DNL)

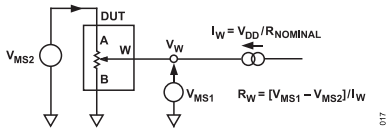


Figure 32. Wiper Resistance

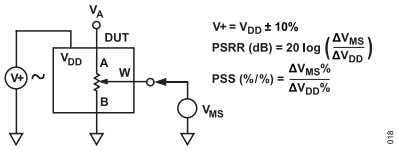


Figure 33. Power Supply Sensitivity (PSS, PSSR)

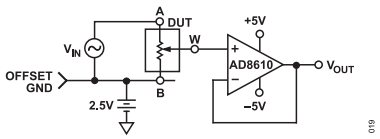


Figure 34. Test Circuit for Gain vs. Frequency

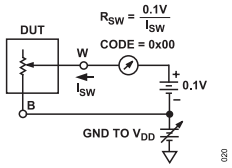


Figure 35. Incremental On Resistance

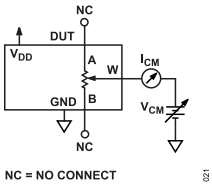


Figure 36. Common-Mode Leakage Current

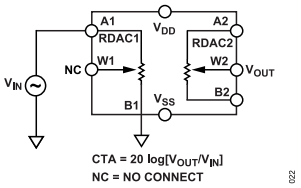


Figure 37. Analog Crosstalk

THEORY OF OPERATION

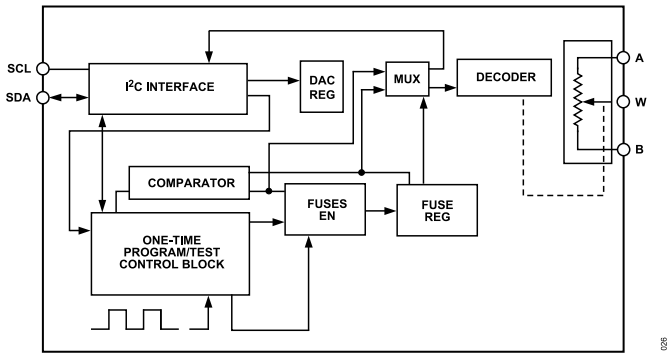


Figure 38. Detailed Functional Block Diagram

The AD5172/AD5173 are 256-position, digitally controlled variable resistors (VRs) that employ fuse link technology to achieve memory retention of the resistance setting.

An internal power-on preset places the wiper at midscale during power-on. If the OTP function is activated, the device powers up at the user-defined permanent setting.

ONE-TIME PROGRAMMING (OTP)

Prior to OTP activation, the AD5172/AD5173 presets to midscale during initial power-on. After the wiper is set to the desired position, the resistance can be permanently set by programming the T bit high, with the proper coding (see Table 8 and Table 9), and one-time V_{DD_OTP}. The fuse link technology of the AD517x family of digital potentiometers requires V_{DD_OTP} to be between 5.6 V and 5.8 V to blow the fuses to achieve a given nonvolatile setting. However, during operation, V_{DD} can be 2.7 V to 5.5 V. As a result, an external supply is required for one-time programming. The user is allowed only one attempt to blow the fuses. If the user fails to blow the fuses during this attempt, the structure of the fuses can change such that they may never be blown, regardless of the energy applied during subsequent events. For details, see the Power Supply Considerations section.

The device control circuit has two validation bits, E1 and E0, that can be read back to check the programming status (see Table 7). Users should always read back the validation bits to ensure that the fuses are properly blown. After the fuses are blown, all fuse latches are enabled upon subsequent power-on; therefore, the output corresponds to the stored setting. Figure 38 shows a detailed functional block diagram.

Table 7. Validation Status

E1	E0	Status
0	0	Ready for programming.
1	0	Fatal error. Some fuses are not blown. Do not retry. Discard this unit.
1	1	Successful. No further programming is possible.

PROGRAMMING THE VARIABLE RESISTOR AND VOLTAGE

Rheostat Operation

The nominal resistance of the RDAC between Terminal A and Terminal B is available in 2.5 kΩ, 10 kΩ, and 100 kΩ. The nominal resistance (R_{AB}) of the VR has 256 contact points accessed by the wiper terminal and the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings.

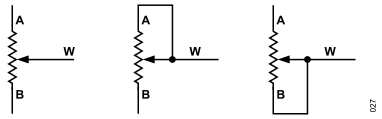


Figure 39. Rheostat Mode Configuration

Assuming a 10 kΩ part is used, the first connection of the wiper starts at the B terminal for Data 0x00. Because there is a 160 Ω wiper contact resistance, such a connection yields a minimum of 320 Ω (2 × 160 Ω) resistance between Terminal W and Terminal B. The second connection is the first tap point, which corresponds to 359 Ω ($R_{WB} = R_{AB}/256 + 2 \times R_W$ = 39 Ω + 2 × 160 Ω) for Data 0x01. The third connection is the next tap point, representing 398 Ω (2 × 39 Ω + 2 × 160 Ω) for Data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10281 Ω (R_{AB} − 1 LSB + 2 × R_W).

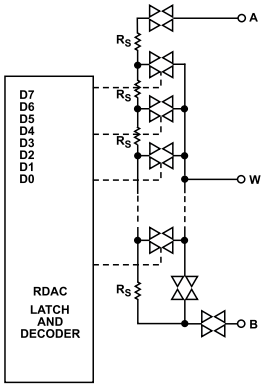


Figure 40. AD5172/AD5173 Equivalent RDAC Circuit

THEORY OF OPERATION

The general equation that determines the digitally programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + 2 \times R_W \quad (1)$$

where:
D is the decimal equivalent of the binary code loaded in the 8-bit RDAC register.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance contributed by the on resistance of the internal switch.

In summary, if R_{AB} is 10 kΩ and the A terminal is open circuited, the output resistance, R_{WB}, is set according to the RDAC latch codes, as listed in Table 8.

Table 8. Codes and Corresponding R_{WB} Resistance

D (Dec)	R_{WB} (Ω)	Output State
255	10,281	Full scale (R_{AB} – 1 LSB + 2 × R_W)
128	5320	Midscale
1	359	1 LSB
0	320	Zero scale (wiper contact resistance)

Note that in the zero-scale condition, a finite wiper resistance of 160 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact may occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between Wiper W and Terminal A also produces a digitally controlled complementary resistance, R_{WA}. When these terminals are used, the B terminal can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + 2 \times R_W \quad (2)$$

When R_{AB} is 10 kΩ and the B terminal is open circuited, the output resistance, R_{WA}, is set according to the RDAC latch codes, as listed in Table 9.

Table 9. Codes and Corresponding R_{WA} Resistance

D (Dec)	R_{WA} (Ω)	Output State
255	359	Full scale
128	5320	Midscale
1	10,281	1 LSB
0	10,320	Zero scale

Typical device-to-device matching is process lot dependent and can vary up to ±30%. Because the resistance element is processed using thin film technology, the change in R_{AB} with temperature has a very low temperature coefficient of 35 ppm/°C.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper to B and at wiper to A, proportional to the input voltage at A to B. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across A to B, W to A, and W to B can be at either polarity.

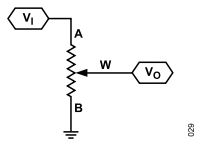


Figure 41. Potentiometer Mode Configuration

If ignoring the effect of the wiper resistance for approximation, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at the wiper to B, starting at 0 V up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across Terminal A and Terminal B divided by the 256 positions of the potentiometer divider. The general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to Terminal A and Terminal B is

$$V_W(D) = \frac{D}{256}V_A + \frac{256 - D}{256}V_B \quad (3)$$

A more accurate calculation, which includes the effect of wiper resistance, V_W, is

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}}V_A + \frac{R_{WA}(D)}{R_{AB}}V_B \quad (4)$$

Operation of the digital potentiometer in the divider mode results in more accurate operation over temperature. Unlike in the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors, R_{WA} and R_{WB}, not on the absolute values. Therefore, the temperature drift reduces to 15 ppm/°C.

ESD PROTECTION

All digital inputs, SDA, SCL, AD0, and AD1, are protected with a series input resistor and parallel Zener ESD structures, as shown in Figure 42 and Figure 43.

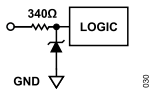


Figure 42. ESD Protection of Digital Pins

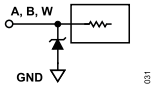


Figure 43. ESD Protection of Resistor Terminals

THEORY OF OPERATION

TERMINAL VOLTAGE OPERATING RANGE

The AD5172/AD5173 to GND power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on Terminal A, Terminal B, and Terminal W that exceed V_{DD} or GND are clamped by the internal forward-biased diodes (see Figure 44).

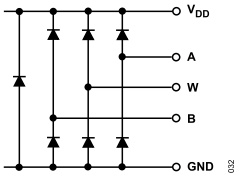


Figure 44. Maximum Terminal Voltages Set by V_{DD} and GND

POWER-UP SEQUENCE

Because the ESD protection diodes limit the voltage compliance at Terminal A, Terminal B, and Terminal W (see Figure 44), it is important to power V_{DD}/GND before applying voltage to Terminal A, Terminal B, and Terminal W. Otherwise, the diode is forward-biased such that V_{DD} is powered unintentionally and may affect the rest of the user's circuit. The ideal power-up sequence is GND, V_{DD}, digital inputs, and then V_A/V_B/V_W. The relative order of powering V_A, V_B, V_W, and the digital inputs is not important, as long as they are powered after V_{DD}/GND.

POWER SUPPLY CONSIDERATIONS

To minimize the package pin count, both the one-time programming and normal operating voltage supplies are applied to the same V_{DD} terminal of the device. The AD5172/AD5173 employ fuse link technology that requires 5.6 V to 5.8 V to blow the internal fuses to achieve a given setting, but normal V_{DD} can be 2.7 V to 5.5 V. Such dual-voltage requirements need isolation between the supplies if V_{DD} is lower than the required V_{DD_OTP}. The fuse programming supply (either an on-board regulator or rack-mount power supply) must be rated at 5.6 V to 5.8 V and must be able to provide a 100 mA transient current for 400 ms for successful one-time programming. When programming is completed, the V_{DD_OTP} supply must be removed to allow normal operation at 2.7 V to 5.5 V; the device consumes only microamps of current.

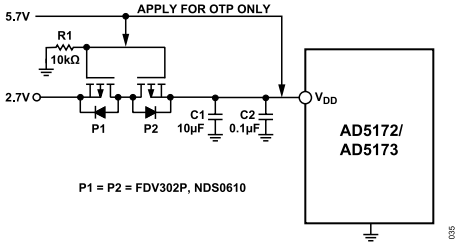


Figure 45. Isolate 5.7 V OTP Supply from 2.7 V Normal Operating Supply

For example, for those who operate their systems at 2.7 V, use of the bidirectional, low threshold, P-channel MOSFETs is recommended for the isolation of the supply. As shown in Figure 45, this assumes that the 2.7 V system voltage is applied first and that the P1 and P2 gates are pulled to ground, thus turning on P1 and then P2. As a result, V_{DD} of the AD5172/AD5173 approaches 2.7 V. When the AD5172/AD5173 setting is found, the factory tester applies the V_{DD_OTP} to both the V_{DD} and the MOSFET gates, thus turning P1 and P2 off. To program the AD5172/AD5173 while the 2.7 V source is protected, execute the OTP command at this time. When the OTP is completed, the tester withdraws the V_{DD_OTP}, and the setting of the AD5172/AD5173 is fixed permanently.

The AD5172/AD5173 achieve the OTP function by blowing internal fuses. Always apply the 5.6 V to 5.8 V one-time program voltage requirement at the first fuse programming attempt. Failure to comply with this requirement may lead to changing the fuse structures, rendering programming inoperable.

Care should be taken when SCL and SDA are driven from a low voltage logic controller. Users must ensure that the logic high level is between 0.7 V × V_{DD} and V_{DD} + 0.5 V.

Poor PCB layout introduces parasitics that can affect fuse programming. Therefore, it is recommended to add a 1 µF to 10 µF tantalum capacitor in parallel with a 1 nF ceramic capacitor as close as possible to the VDD pin. The type and value chosen for both capacitors are important. These capacitors work together to provide both fast responsiveness and large supply current handling with minimum supply droop during transients. As a result, these capacitors increase the OTP programming success by not inhibiting the proper energy needed to blow the internal fuses. Additionally, C1 minimizes transient disturbance and low frequency ripple, whereas C2 reduces high frequency noise during normal operation.

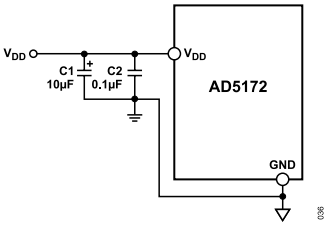


Figure 46. Power Supply Bypassing

LAYOUT CONSIDERATIONS

In PCB layout, it is a good practice to employ compact, minimum lead length design. The leads to the inputs should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Note that the digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.

I²C INTERFACE

WRITE MODE

Table 10. AD5172 Write Mode

S	0	1	0	1	1	1	1	$\overline{W}$	A	A0	SD	T	0	OW	X	X	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave address byte									Instruction byte									Data byte									

Table 11. AD5173 Write Mode

S	0	1	0	1	1	AD1	AD0	$\overline{W}$	A	A0	SD	T	0	OW	X	X	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave address byte									Instruction byte									Data byte									

READ MODE

Table 12. AD5172 Read Mode

S	0	1	0	1	1	1	1	R	A	D7	D6	D5	D4	D3	D2	D1	D0	A	E1	E0	X	X	X	X	X	X	A	P
	Slave address byte									Instruction byte									Data byte									

Table 13. AD5173 Read Mode

S	0	1	0	1	1	AD1	AD0	R	A	D7	D6	D5	D4	D3	D2	D1	D0	A	E1	E0	X	X	X	X	X	X	A	P
	Slave address byte									Instruction byte									Data byte									

SDA BITS DESCRIPTIONS

Table 14. SDA Bits Descriptions

Bit	Description
S	Start condition.
P	Stop condition.
A	Acknowledge.
AD0, AD1	Package pin-programmable address bits.
X	Don't care.
$\overline{W}$	Write.
R	Read.
A0	RDAC subaddress select bit.
SD	Shutdown connects wiper to B terminal and open circuits the A terminal. It does not change the contents of the wiper register.
T	OTP programming bit. Logic 1 programs the wiper permanently.
OW	Overwrites the fuse setting and programs the digital potentiometer to a different setting. Upon power-up, the digital potentiometer is preset to either midscale or fuse setting, depending on whether the fuse link was blown.
D7, D6, D5, D4, D3, D2, D1, D0	Data bits.
E1, E0	OTP validation bits.
	00 = ready to program.
	10 = fatal error. Some fuses not blown. Do not retry. Discard this unit.
	11 = programmed successfully. No further adjustments are possible.

I²C CONTROLLER PROGRAMMING

Write Bit Patterns

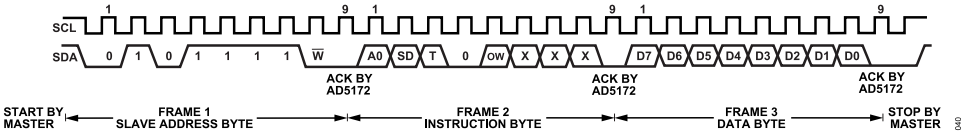


Figure 47. Writing to the RDAC Register—AD5172

I²C INTERFACE

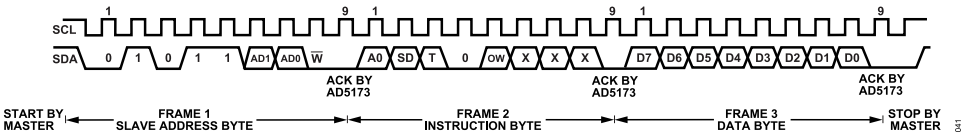


Figure 48. Writing to the RDAC Register—AD5173

Read Bit Patterns

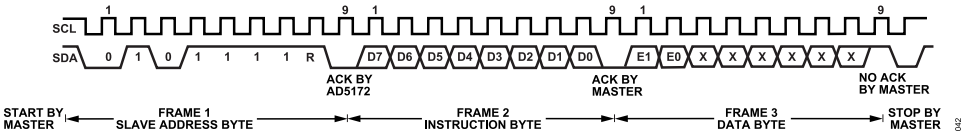


Figure 49. Reading Data from a Previously Selected RDAC Register in Write Mode—AD5172

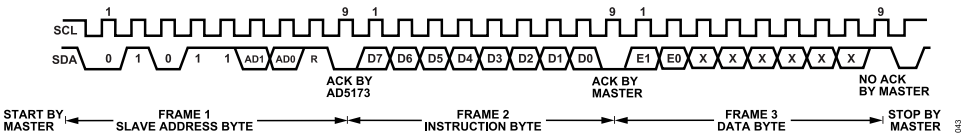


Figure 50. Reading Data from a Previously Selected RDAC Register in Write Mode—AD5173

I²C INTERFACE

I²C-COMPATIBLE, 2-WIRE SERIAL BUS

This section describes how the 2-wire, I²C-compatible serial bus protocol operates.

The master initiates a data transfer by establishing a start condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 47 and Figure 48). The following byte is the slave address byte, which consists of the slave address followed by an R/$\overline{W}$ bit (this bit determines whether data is read from or written to the slave device). The AD5172 has a fixed slave address byte, whereas the AD5173 has two configurable address bits, AD0 and AD1 (see Figure 47 and Figure 48).

The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is called the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/$\overline{W}$ bit is high, the master reads from the slave device. If the R/$\overline{W}$ bit is low, the master writes to the slave device.

In write mode, the second byte is the instruction byte. The first bit (MSB) of the instruction byte is the RDAC subaddress select bit. Logic low selects Channel 1; logic high selects Channel 2.

The second MSB, SD, is a shutdown bit. A logic high causes an open circuit at Terminal A while shorting the wiper to Terminal B. This operation yields almost 0 Ω in rheostat mode or 0 V in potentiometer mode. It is important to note that the shutdown operation does not disturb the contents of the register. When brought out of shutdown, the previous setting is applied to the RDAC. In addition, during shutdown, new settings can be programmed. When the part is returned from shutdown, the corresponding VR setting is applied to the RDAC.

The third MSB, T, is the OTP programming bit. A logic high blows the polyfuses and programs the resistor setting permanently. The OTP program time is 400 ms.

The fourth MSB must always be at Logic 0.

The fifth MSB, OW, is an overwrite bit. When raised to a logic high, OW allows the RDAC setting to be changed even after the internal fuses are blown. However, when OW is returned to Logic 0, the position of the RDAC returns to the setting prior to the overwrite. Because OW is not static, if the device is powered off and on, the RDAC presets to midscale or to the setting at which the fuses were blown, depending on whether the fuses had been permanently set.

The remainder of the bits in the instruction byte are don't cares (see Figure 47 and Figure 48).

After acknowledging the instruction byte, the last byte in write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 3).

In read mode, the data byte follows immediately after the acknowledgment of the slave address byte. Data is transmitted over the serial bus in sequences of nine clock pulses (a slight difference from the write mode, where there are eight data bits followed by an acknowledge bit). Similarly, transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 49 and Figure 50).

Note that the channel of interest is the one that is previously selected in write mode. If users need to read the RDAC values of both channels, they must program the first channel in write mode and then change to read mode to read the first channel value. After that, the user must return to write mode with the second channel selected and read the second channel value in read mode. It is not necessary for users to issue the Frame 3 data byte in write mode for subsequent readback operations. Refer to Figure 49 and Figure 50 for the programming format.

Following the data byte, the validation byte contains two validation bits, E0 and E1 (see Table 7). These bits signify the status of the one-time programming (see Figure 49 and Figure 50).

After all data bits are read or written, the master establishes a stop condition. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition (see Figure 47 and Figure 48). In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master brings the SDA line low before the 10th clock pulse and then brings the SDA line high to establish a stop condition (see Figure 49 and Figure 50).

A repeated write function provides the user with the flexibility of updating the RDAC output multiple times after addressing and instructing the part only once. For example, after the RDAC has acknowledged its slave address and instruction bytes in write mode, the RDAC output is updated on each successive byte. If different instructions are needed, however, the write/read mode must restart with a new slave address, instruction, and data byte. Similarly, a repeated read function of the RDAC is also allowed.

Multiple Devices on One Bus (AD5173 Only)

Figure 51 shows four AD5173 devices on the same serial bus. Each has a different slave address because the states of the AD0 and AD1 pins are different. This allows each device on the bus to be written to or read from independently. The master device output bus line drivers are open-drain pull-downs in a fully I²C-compatible interface.

I²C INTERFACE

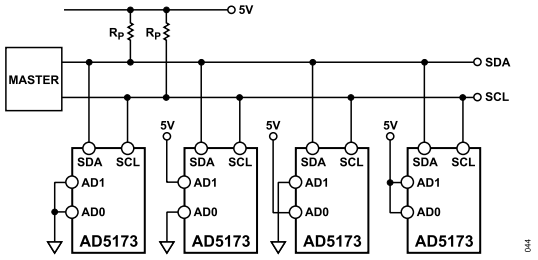


Figure 51. Multiple AD5173 Devices on One I²C Bus

LEVEL SHIFTING FOR DIFFERENT VOLTAGE OPERATION

If the SCL and SDA signals come from a low voltage logic controller and are below the minimum V_{IH} level (0.7 V × V_{DD}), level shift the signals for read/write communications between the AD5172/AD5173 and the controller. Figure 52 shows one of the implementations. For example, when SDA1 is at 2.5 V, M1 turns off, and SDA2 becomes 5 V. When SDA1 is at 0 V, M1 turns on, and SDA2 approaches 0 V. As a result, proper level shifting is established. It is best practice for M1 and M2 to be low threshold N-channel power MOSFETs, such as the FDV301N from On Semiconductor.

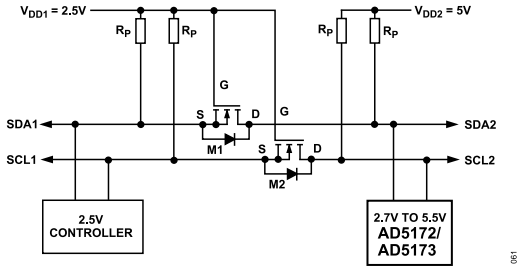


Figure 52. Level Shifting for Different Voltage Operation

OUTLINE DIMENSIONS

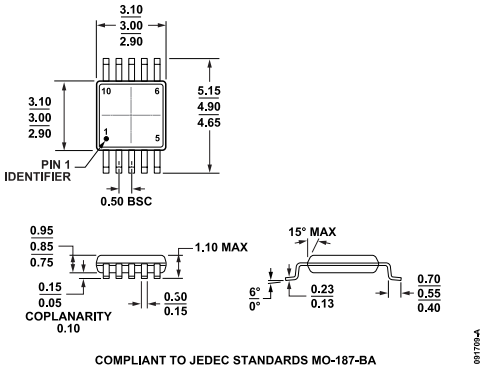


Figure 53. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

Updated: October 12, 2021

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option	Marking Code
AD5172BRMZ10	-40°C to +125°C	10-Lead MSOP	Tube, 50	RM-10	DCT
AD5172BRMZ100	-40°C to +125°C	10-Lead MSOP	Tube, 50	RM-10	DCV
AD5172BRMZ100-RL7	-40°C to +125°C	10-Lead MSOP	Reel, 1000	RM-10	DCV
AD5172BRMZ10-RL7	-40°C to +125°C	10-Lead MSOP	Reel, 1000	RM-10	DCT
AD5172BRMZ2.5	-40°C to +125°C	10-Lead MSOP	Tube, 50	RM-10	DCR
AD5173BRMZ10	-40°C to +125°C	10-Lead MSOP	Tube, 50	RM-10	DCL
AD5173BRMZ10-RL7	-40°C to +125°C	10-Lead MSOP	Reel, 1000	RM-10	DCL
AD5173BRMZ2.5	-40°C to +125°C	10-Lead MSOP	Tube, 50	RM-10	DCH
AD5173BRMZ2.5-RL7	-40°C to +125°C	10-Lead MSOP	Reel, 1000	RM-10	DCH

[1] Z = RoHS Compliant Part.

R_{AB} OPTIONS

Model[1, 2]	R_{AB} (kΩ) Options
AD5172BRMZ10	10
AD5172BRMZ100	100
AD5172BRMZ100-RL7	100
AD5172BRMZ10-RL7	10
AD5172BRMZ2.5	2.5
AD5173BRMZ10	10
AD5173BRMZ10-RL7	10
AD5173BRMZ2.5	2.5
AD5173BRMZ2.5-RL7	2.5

[1] Z = RoHS Compliant Part.

[2] The part has a YWW or #YWW label and an assembly lot number label on the bottom side of the package. The Y shows the year that the part was made, for example, Y = 5 means the part was in 2005. WW shows the work week that the part was made.

OUTLINE DIMENSIONS

EVALUATION BOARDS

Model[1]	Description
EVAL-AD5172SDZ	Evaluation Board

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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