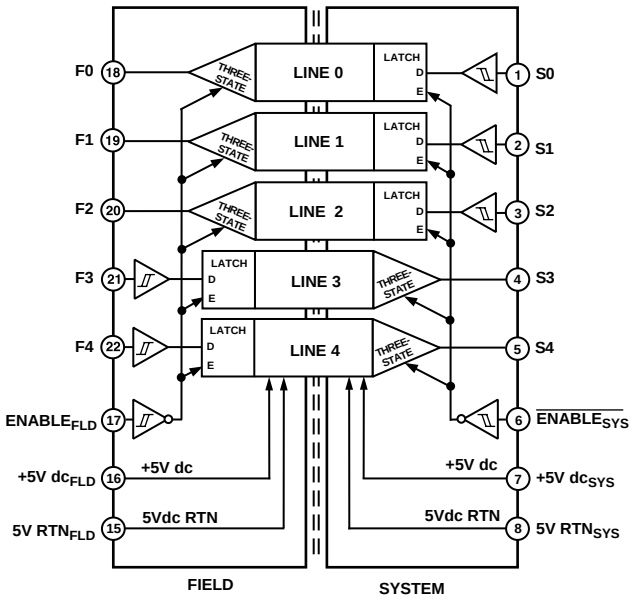
High Speed, Logic Isolator

AD261

FEATURES
Isolation Test Voltage: To 3.5 kV rms
Five Isolated Logic Lines: Available in Six I/O Configurations
Logic Signal Bandwidth: 20 MHz (min)
CMV Transient Immunity: 10 kV/μs min
Waveform Edge Transmission Symmetry: ±1 ns
Field and System Output Enable/Three-State Functions
Performance Rated Over –25°C to +85°C
UL1950, IEC950, EN60950 Certification (VDE, CE, Pending)

APPLICATIONS
PLC/DCS Analog Input and Output Cards
Communications Bus Isolation
General Data Acquisition Applications
IGBT Motor Drive Controls
High Speed Digital I/O Ports

FUNCTIONAL BLOCK DIAGRAM



TYPICAL MODEL
(AD261-2)

GENERAL DESCRIPTION

The AD261 is designed to isolate five digital control signals to/from a microcontroller and its related field I/O components. Six models allow all I/O combinations from five input lines to five output lines, including combinations in between. Every AD261 effectively replaces up to five opto-isolators.

Each line of the AD261 has a bandwidth of 20 MHz (min) with a propagation delay of only 14 ns, which allows for extremely fast data transmission. Output waveform symmetry is maintained to within ±1 ns of the input so the AD261 can be used to accurately isolate time-based PWM signals.

All field or system output pins of the AD261 can be set to a high resistance three-state level by use of the two enable pins. A field output three-stated offers a convenient method of presetting logic levels at power-up by use of pull-up/down resistors. System side outputs being three-stated allows for easy multiplexing of multiple AD261s.

The isolation barrier of the AD261 B Grade is 100% tested as high as 3.5 kV rms (system to field). The barrier design also provides excellent common-mode transient immunity from 10 kV/μs common-mode voltage excursions of field side terminals relative to the system side, with no false output triggering on either side.

Each output is updated within nanoseconds by input logic transitions, the AD261 also has a continuous output update feature that automatically updates each output based on the dc level of the input. This guarantees the output is always valid 10 μs after a fault condition or after the power-up reset interval.

PRODUCT HIGHLIGHTS

Six Isolated Logic Line I/O Configurations Available: The AD261 is available in six pin-compatible versions of I/O configurations to meet a wide variety of requirements**.**

Wide Bandwidth with Minimal Edge Error: The AD261 affords extremely fast isolation of logic signals due to its 20 MHz bandwidth and 14 ns propagation delay. It maintains a waveform input-to-output edge transition error of typically less than ±1 ns (total) for positive vs. negative transition.

3.5 kV rms Test Voltage Isolation Rating: The AD261 B Grade is rated to operate at 1.25 kV rms and is 100% production tested at 3.5 kV rms, using a standard ADI test method.

High Transient Immunity: The AD261 rejects common-mode transients slewing at up to 10 kV/μs without false triggering or damage to the device.

(*Continued on page* 5)

REV. 0

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AD261–SPECIFICATIONS (Typical at T_A = +25°C, +5 V dc_{SYS}, +5 V dc_{FLD}, t_{RR} = 50 ns max unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS					
Threshold Voltage					
Positive Transition (V_{T+})	+5 V dc_{SYS} = 4.5 V	2.0	2.7	3.15	V
	+5 V dc_{SYS} = 5.5 V	3.0	3.2	4.2	V
Negative Transition (V_{T-})	+5 V dc_{SYS} = 4.5 V	0.9	1.8	2.2	V
	+5 V dc_{SYS} = 5.5 V	1.2	2.2	3.0	V
Hysteresis Voltage (V_H)	+5 V dc_{SYS} = 4.5 V	0.4	0.9	1.4	V
	+5 V dc_{SYS} = 5.5 V	0.5	1.0	1.5	V
Input Capacitance (C_{IN})			5		pF
Input Bias Current (I_{IN})	Per Input		0.5		µA
OUTPUT CHARACTERISTICS					
Output Voltage[1]					
High Level (V_{OH})	+5 V dc_{SYS} = 4.5 V, $\|I_O\|$ = 0.02 mA	4.4			V
	+5 V dc_{SYS} = 4.5 V, $\|I_O\|$ = 4 mA	3.7			V
Low Level (V_{OL})	+5 V dc_{SYS} = 4.5 V, $\|I_O\|$ = 0.02 mA			0.1	V
	+5 V dc_{SYS} = 4.5 V, $\|I_O\|$ = 4 mA			0.4	V
Output Three-State Leakage Current	$ENABLE_{SYS/FLD}$ @ Logic Low/High Level Respectively		0.5		µA
DYNAMIC RESPONSE[1] (Refer to Figure 2)					
Max Logic Signal Frequency (f_{MIN})	50% Duty Cycle, +5 V dc_{SYS} = 5 V	20			MHz
Waveform Edge Symmetry Error (t_{ERROR})	t_{PHL} vs. t_{PLH}		±1		ns
Logic Edge Propagation Delay (t_{PHL}, t_{PLH})			14	25	ns
Minimum Pulsewidth (t_{PWMIN})		25			ns
Max Output Update Delay on Fault or After Power-Up Reset Interval (≈ 30 µs)[2]			12		µs
ISOLATION BARRIER RATING[3]					
Operating Isolation Voltage (V_{CMV})	AD261A			375	V rms
	AD261B			1250	V rms
Isolation Rating Test Voltage ($V_{CMV\ TEST}$)[4]	AD261A	1750			V rms
	AD261B	3500			V rms
Transient Immunity ($V_{TRANSIENT}$)		10,000			V/µs
Isolation Mode Capacitance (C_{ISO})	Total Capacitance, All Lines		9	15	pF
Capacitive Leakage Current (I_{LEAD})	240 V rms @ 60 Hz			2	µA rms
POWER SUPPLY					
Supply Voltage (+5 V dc_{SYS} and +5 V dc_{FLD})	Rated Performance	4.5		5.5	V dc
	Operating	4.0		5.75	V dc
Power Dissipation Capacitance	Effective, per Input, Either Side		8		pF
	Effective per Output, Either Side—No Load		28		pF
Quiescent Supply Current	Each, +5 V $dc_{SYS\ \&\ FLD}$		4		mA
Supply Current	All Lines @ 10 MHz (Sum of +5 V $dc_{SYS\ \&\ FLD}$)		18		mA
TEMPERATURE RANGE					
Rated Performance (T_A)[5]		–25		+85	°C
Storage (T_{STG})		–40		+85	°C

NOTES

[1]For best performance, bypass +5 V dc supplies to com., at or near the device (0.01 µF). +5 V dc supplies are also internally bypassed with 0.05 µF.

[2]As the supply voltage is applied to either side of the AD261, the internal circuitry will go into a power-up reset mode (all lines disabled) for about 30 µs after the point where +5 V $dc_{SYS\ \&\ FLD}$ passes above 3.3 V.

[3]"Operating" isolation voltage is derived from the Isolation Test Voltage in accordance with such methods as found in VDE-0883 wherein a device will be "hi-pot" tested at twice the operating voltage, plus one thousand volts. Partial discharge testing, with an acceptance threshold of 80 pC of discharge may be considered the same as a hi-pot test (but nondestructive).

[4]Partial Discharge at 80 pC THLD.

[5]Supply Current will increase slightly, but otherwise the unit will function within specification to –40°C.

Specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage (+5 V $dc_{SYS\ \&\ FLD}$)		–0.5		+6.0	V
DC Input Voltage ($V_{IN\ MAX}$)	Referred to +5 V $dc_{SYS\ \&\ FLD}$ and 5 V $RTN_{SYS\ \&\ FLD}$ Respectively	–0.5		+0.5	V
DC Output Voltage ($V_{OUT\ MAX}$)	Referred to +5 V $RTN_{SYS\ \&\ FLD}$ and 5 V $dc_{SYS\ \&\ FLD}$ Respectively	–0.5		+0.5	V
Clamp Diode Input Current (I_{IK})	For V_I < –0.5 V or V_I > 5 V $RTN_{SYS\ \&\ FLD}$ +0.5 V	–25		+25	mA
Clamp Diode Output Current (I_{OK})	For V_O < –0.5 V or V_O > 5 V $RTN_{SYS\ \&\ FLD}$ +0.5 V	–25		+25	mA
Output DC Current, per Pin (I_{OUT})		–25		+25	mA
DC Current, V_{CC} or GND (I_{CC} or I_{GND})		–50		+50	mA
Storage Temperature (T_{STG})		–40		+85	°C
Lead Temperature (Soldering, 10 sec)				+300	°C
Electrostatic Protection (V_{ESD})	Per MIL-STD-883, Method 3015	4.5	5		kV

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

I/O CONFIGURATIONS AVAILABLE

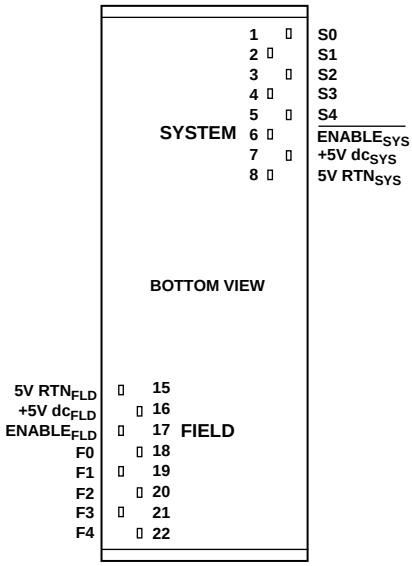
The AD261 is available in several configurations. The choice of model is determined by the desired number of input vs. output lines. All models have identical footprints with the power and enable pins always being in the same locations.

PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Function
1–5*	$\overline{S0\ Through\ S4}$	Digital Xmt or Rcv from F0 Through F4
6	$\overline{ENABLE}_{SYS}$	System Output Enable/Three-State
7	+5 V dc_{SYS}	System Power Supply (+5 V dc Input)
8	5 V RTN_{SYS}	System Power Supply Common
9–14		Not Present On Unit
15	5 V RTN_{FLD}	Field Power Supply Common
16	+5 V dc_{FLD}	Field Power Supply (+5 V Input)
17	$ENABLE_{FLD}$	Field Output Enable/Three-State
18–22*	F0 Through F4	Digital Xmt or Rcv from S0 Through S4

*Function of pin determined by model. Refer to Table I.

PIN CONFIGURATION



ORDERING GUIDE

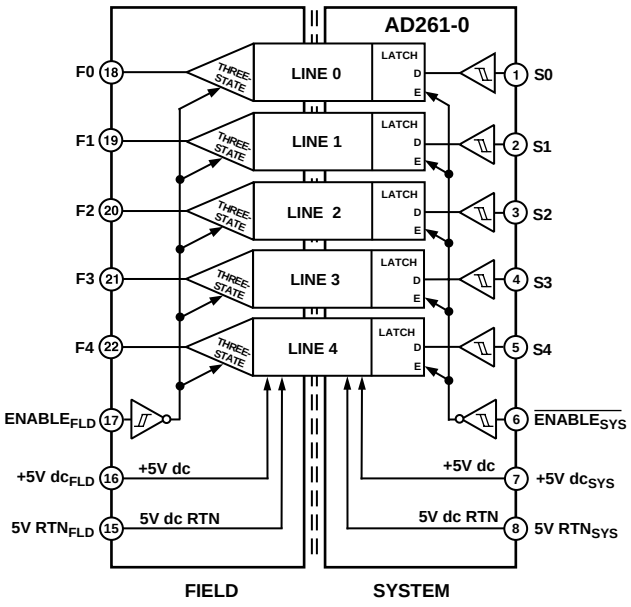
Model Number	Description	Isolation Ratings	Package Description	Package Option
AD261AND-0	0 Inputs, 5 Outputs	1.75 kV rms	Plastic DIP	ND-22A
AD261AND-1	1 Input, 4 Outputs	1.75 kV rms	Plastic DIP	ND-22A
AD261AND-2	2 Inputs, 3 Outputs	1.75 kV rms	Plastic DIP	ND-22A
AD261AND-3	3 Inputs, 2 Outputs	1.75 kV rms	Plastic DIP	ND-22A
AD261AND-4	4 Inputs, 1 Output	1.75 kV rms	Plastic DIP	ND-22A
AD261AND-5	5 Inputs, 0 Outputs	1.75 kV rms	Plastic DIP	ND-22A
AD261BND-0	0 Inputs, 5 Outputs	3.5 kV rms	Plastic DIP	ND-22A
AD261BND-1	1 Input, 4 Outputs	3.5 kV rms	Plastic DIP	ND-22A
AD261BND-2	2 Inputs, 3 Outputs	3.5 kV rms	Plastic DIP	ND-22A
AD261BND-3	3 Inputs, 2 Outputs	3.5 kV rms	Plastic DIP	ND-22A
AD261BND-4	4 Inputs, 1 Output	3.5 kV rms	Plastic DIP	ND-22A
AD261BND-5	5 Inputs, 0 Outputs	3.5 kV rms	Plastic DIP	ND-22A

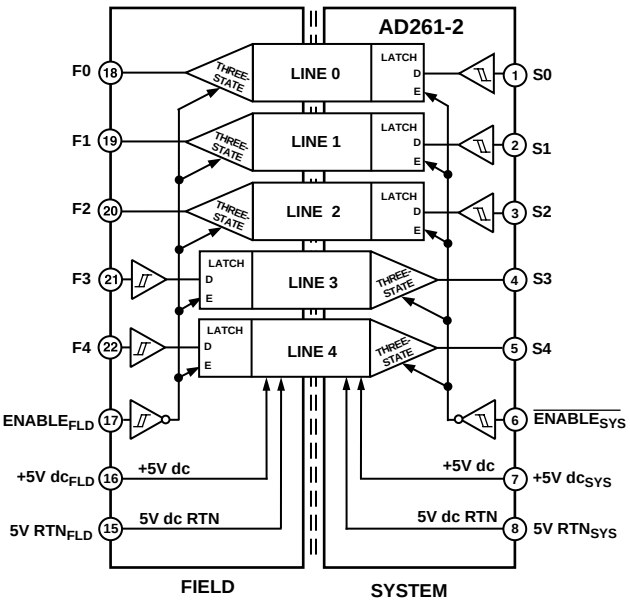
CAUTION

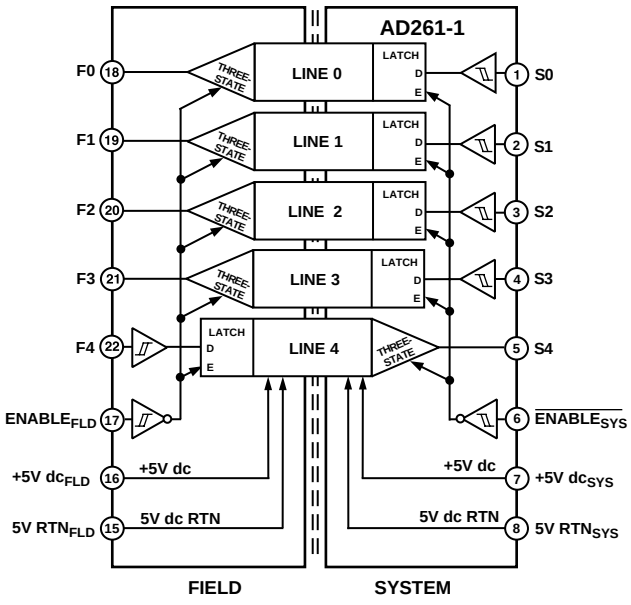
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD261 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

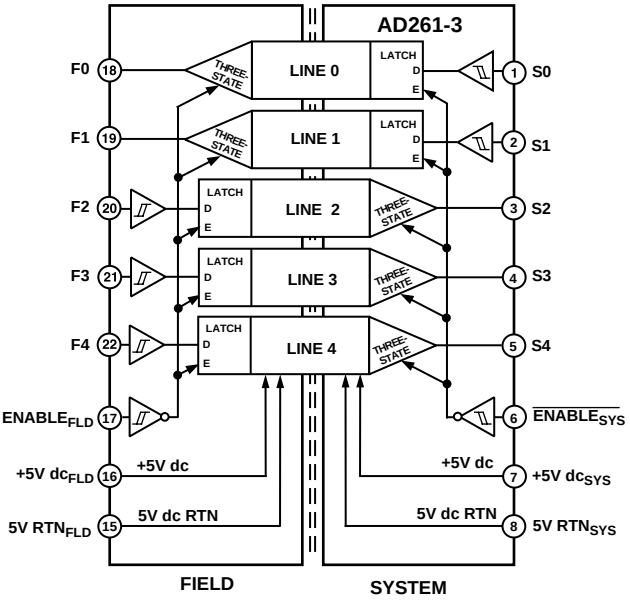


AD261 CONFIGURATIONS

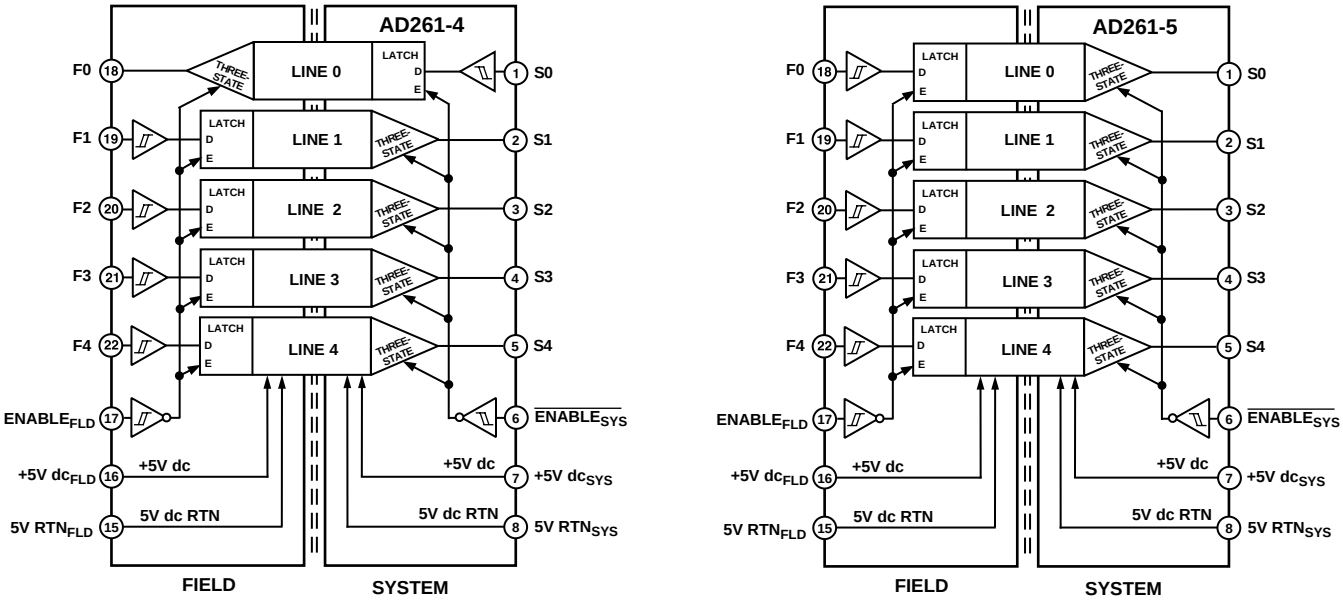








AD261 CONFIGURATIONS



(*Continued from page* 1)

Field and System Enable Functions: Both the isolated and nonisolated sides of the AD261 have ENABLE pins that three-state all outputs. Upon reenabling these pins, all outputs are updated to reflect the current input logic level.

CE Certifiable: Simply by adding the external bypass capacitors at the supply pins, the AD261 can attain CE certification in most applications (to the EMC directive) and conformance to the low voltage (safety) directive is assured by the EN60950 certification.

Table I. Model Number and Pinout Function

Pin	AD261-0	AD261-1	AD261-2	AD261-3	AD261-4	AD261-5
1	S0 (Xmt)	S0 (Xmt)	S0 (Xmt)	S0 (Xmt)	S0 (Xmt)	S0 (Rcv)
2	S1 (Xmt)	S1 (Xmt)	S1 (Xmt)	S1 (Xmt)	S1 (Rcv)	S1 (Rcv)
3	S2 (Xmt)	S2 (Xmt)	S2 (Xmt)	S2 (Rcv)	S2 (Rcv)	S2 (Rcv)
4	S3 (Xmt)	S3 (Xmt)	S3 (Rcv)	S3 (Rcv)	S3 (Rcv)	S3 (Rcv)
5	S4 (Xmt)	S4 (Rcv)	S4 (Rcv)	S4 (Rcv)	S4 (Rcv)	S4 (Rcv)
6	ENABLE$_{SYS}$	*	*	*	*	*
7	+5 V dc$_{SYS}$	*	*	*	*	*
8	5 V RTN$_{SYS}$	*	*	*	*	*
9–14		Not Present				
15	5 V RTN$_{FLD}$	*	*	*		*
16	+5 V dc$_{FLD}$	*	*	*	*	*
17	ENABLE$_{FLD}$	*	*	*	*	*
18	F0 (Rcv)	F0 (Rcv)	F0 (Rcv)	F0 (Rcv)	F0 (Rcv)	F0 (Xmt)
19	F1 (Rcv)	F1 (Rcv)	F1 (Rcv)	F1 (Rcv)	F1 (Xmt)	F1 (Xmt)
20	F2 (Rcv)	F2 (Rcv)	F2 (Rcv)	F2 (Xmt)	F2 (Xmt)	F2 (Xmt)
21	F3 (Rcv)	F3 (Rcv)	F3 (Xmt)	F3 (Xmt)	F3 (Xmt)	F3 (Xmt)
22	F4 (Rcv)	F4 (Xmt)	F4 (Xmt)	F4 (Xmt)	F4 (Xmt)	F4 (Xmt)

*Pin function is the same on all models, as shown in the AD261-0 column.

GENERAL ATTRIBUTES

The AD261 provides five HCMOS compatible isolated logic lines with ≥ 10 kV/μs common-mode transient immunity.

The case design and pin arrangement provides greater than 18 mm spacing between field and system side conductors, providing CSA/IS and IEC creepage spacing consistent with 750 V mains isolation.

The five unidirectional logic lines have six possible combinations of "ins" and "outs," or transmitter/receiver pairs; hence there are six AD261 part configurations (see Table I).

Each 20 MHz logic line has a Schmidt trigger input and a three-state output (on the other side of the isolation barrier) and 14 ns of propagation delay. A single enable pin on either side of the barrier causes all outputs on that side to go three-state and all inputs (driven pins) to ignore their inputs and retain their last known state.

Note: All unused logic inputs (1–5) should be tied either high or low, but not left floating.

Edge "fidelity," or the difference in propagation time for rising and falling edges, is typically less than ±1 ns.

Power consumption, unlike opto-isolators, is a function of operating frequency. Each logic line barrier driver requires about 160 μA per MHz and each receiver 40 μA per MHz plus, of course, 4 mA total idle current (each side). The supply current diminishes slightly with increasing temperature (about –0.03%/°C).

The total capacitance spanning the isolation barrier is less than 10 pF.

The minimum period of a pulse that can be accurately coupled across the barrier is about 25 ns. Therefore the maximum square-wave frequency of operation is 20 MHz.

Logic information is sent across the barrier as "set-hi/set-lo" data that is derived from logic level transitions of the input. At power-up or after a fault condition, an output might not represent the state of the respective channel input to the isolator. An internal circuit operates in the background which interrogates all inputs about every 5 µs and in the absence of logic transitions, sends appropriate "set-hi" or "set-lo" data across the barrier.

Recovery time from a fault condition or at power-up is thus between 5 µs and 10 µs.

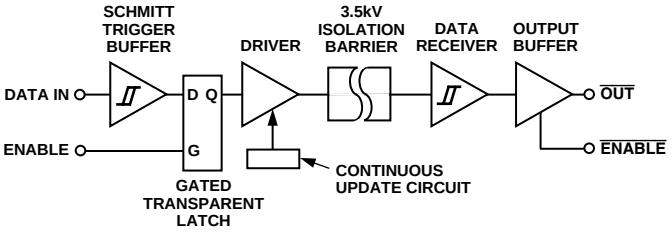


Figure 1. Simplified Block Diagram

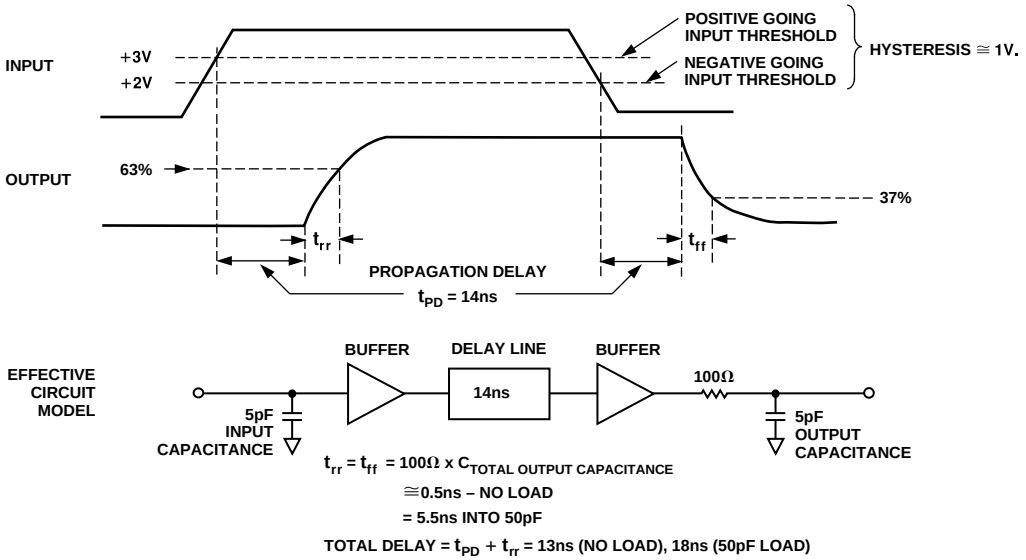
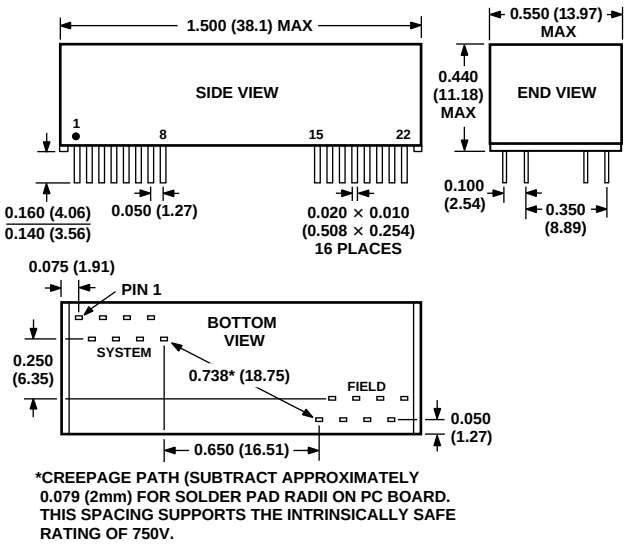


Figure 2. Typical Timing and Delay Models

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

22-Pin Plastic DIP
(ND-22A)



*CREEPAGE PATH (SUBTRACT APPROXIMATELY 0.079 (2mm) FOR SOLDER PAD RADII ON PC BOARD. THIS SPACING SUPPORTS THE INTRINSICALLY SAFE RATING OF 750V.

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