ACTT4X-800E

AC Thyristor Triac power switch

6 September 2018 **Product data sheet**

1. General description

Planar passivated AC Thyristor Triac power switch in a SOT186A (TO-220F) "full pack" plastic package with self-protective capabilities against low and high energy transients.

2. Features and benefits

- Clamping structure ensuring safe high over-voltage withstand capability
- Direct interfacing with low power drivers and microcontrollers
- Full cycle AC conduction
- Isolated mounting base package
- Over-voltage withstand capability to IEC 61000-4-5
- Pin compatible with standard triacs
- Planar passivated for voltage ruggedness and reliability
- Safe clamping capability for low energy over-voltage transients
- Self-protective turn-on during high energy voltage transients
- Sensitive gate for easy logic level triggering
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt

3. Applications

- AC fan, pump and compressor controls
- Highly inductive, resistive and safety loads
- Large and small appliances (White Goods)
- Reversing induction motor controls

4. Quick reference data

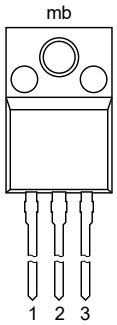
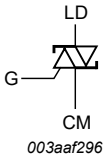
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 94$ °C; Fig. 1; Fig. 2; Fig. 3		-	-	4	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig. 4; Fig. 5		-	-	35	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms		-	-	39	A
T_j	junction temperature			-	-	125	°C
V_{PP}	peak pulse voltage	$T_j = 25$ °C; non-repetitive, off-state; Fig. 6		-	-	2	kV

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 100 mA; LD+ G+; T_j = 25 °C; Fig. 8		-	-	10	mA
		V_D = 12 V; I_T = 100 mA; LD+ G-; T_j = 25 °C; Fig. 8		-	-	10	mA
		V_D = 12 V; I_T = 100 mA; LD- G-; T_j = 25 °C; Fig. 8		-	-	10	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 10		-	-	20	mA
V_T	on-state voltage	I_T = 6 A; T_j = 25 °C; Fig. 11		-	-	1.7	V
V_{CL}	clamping voltage	I_{CL} = 0.1 mA; t_p = 1 ms; T_j = 25 °C		850	-	-	V
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 13		500	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 4 A; dV_{com}/dt = 20 V/µs; (snubberless condition); gate open circuit; Fig. 14; Fig. 15		4	-	-	A/ms
		V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 4 A; dV_{com}/dt = 10 V/µs; gate open circuit; Fig. 14; Fig. 15		5	-	-	A/ms
		V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 4 A; dV_{com}/dt = 1 V/µs; gate open circuit; Fig. 14; Fig. 15		8	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CM	common	 **TO-220F (SOT186A)**	
2	LD	load		
3	G	gate		
mb	n.c.	mounting base; isolated		

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6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
ACTT4X-800E	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

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7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq$ 94 °C; Fig. 1; Fig. 2; Fig. 3		-	4	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 4; Fig. 5		-	35	A
		full sine wave; $T_{j(init)}$ = 25 °C; t_p = 16.7 ms		-	39	A
I^2t	I^2t for fusing	t_p = 10 ms; sine-wave pulse		-	6	A^2s
dI_T/dt	rate of rise of on-state current	I_G = 20 mA		-	100	A/µs
I_{GM}	peak gate current	t = 20 µs		-	2	A
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_j	junction temperature			-	125	°C
V_{PP}	peak pulse voltage	T_j = 25 °C; non-repetitive, off-state; Fig. 6		-	2	kV

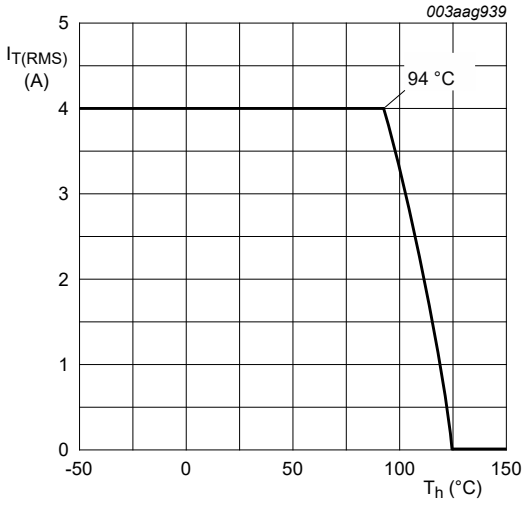
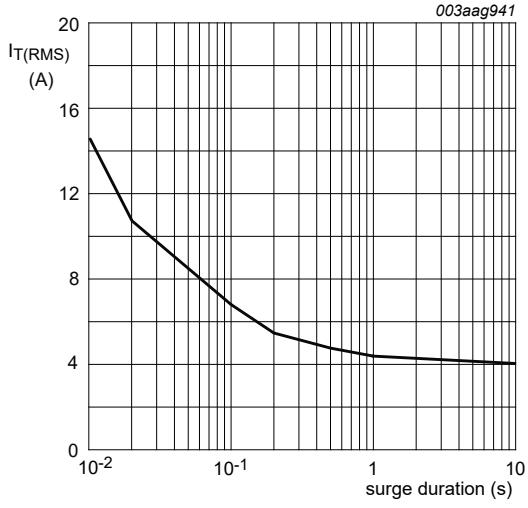


Fig. 1. RMS on-state current as a function of heatsink temperature; maximum values

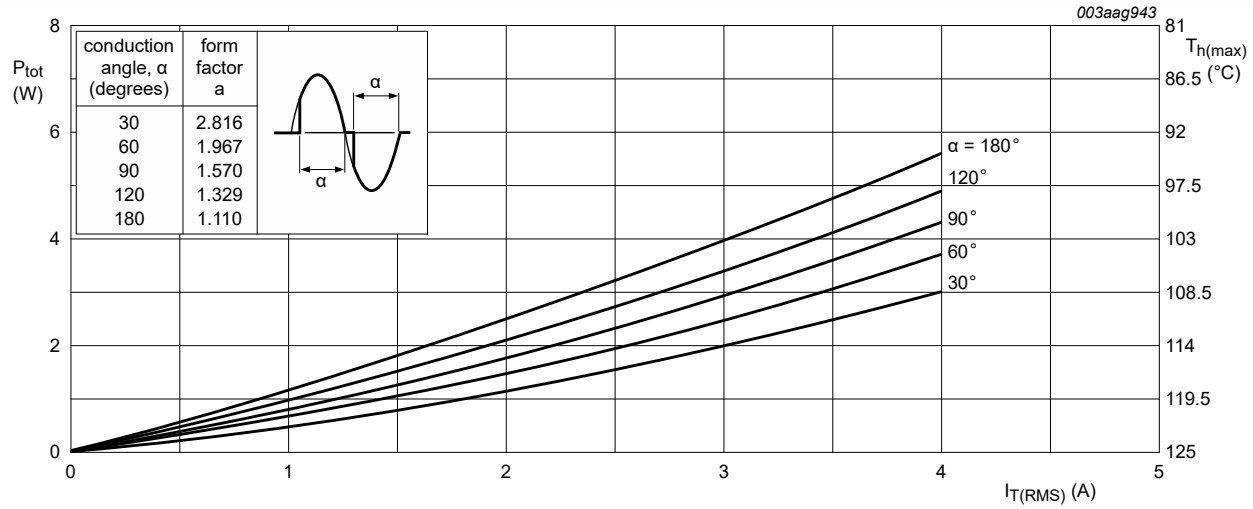


f = 50 Hz; T_h = 94 °C

Fig. 2. on-state current as a function of surge duration; maximum values

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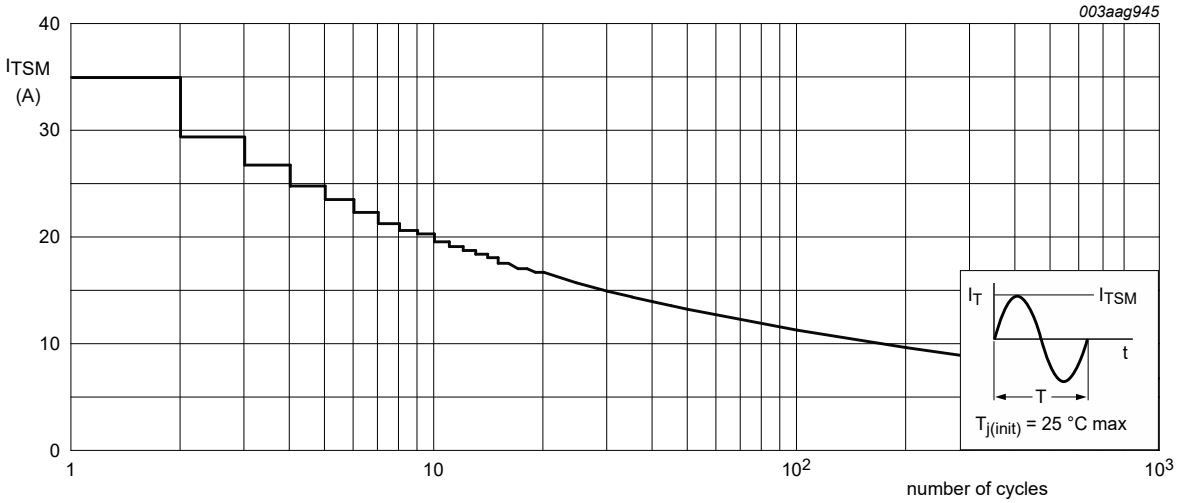
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α = conduction angle

a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

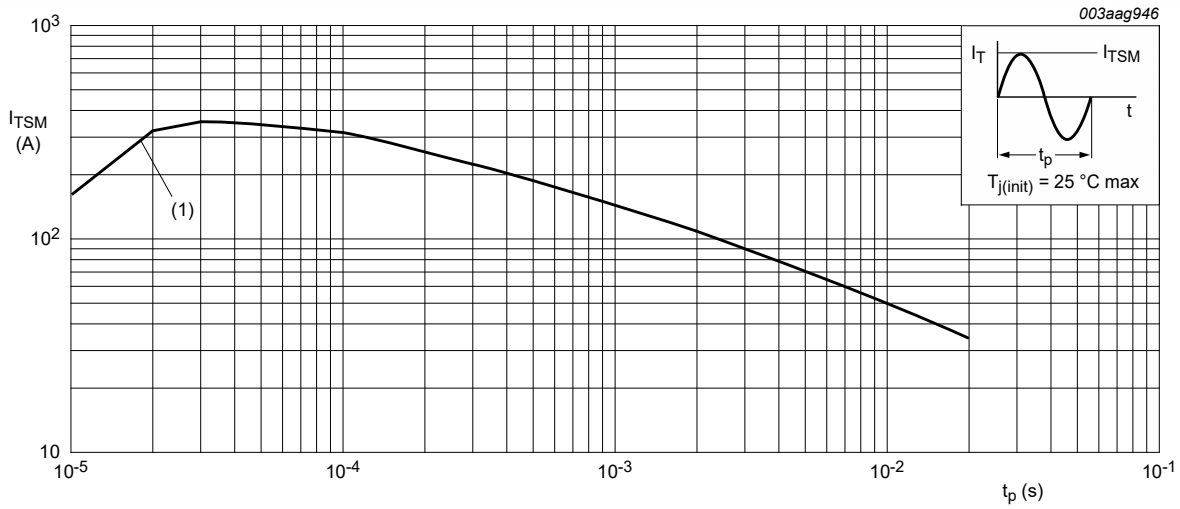


f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

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$t_p \leq 20$ ms

(1) dI_T/dt limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

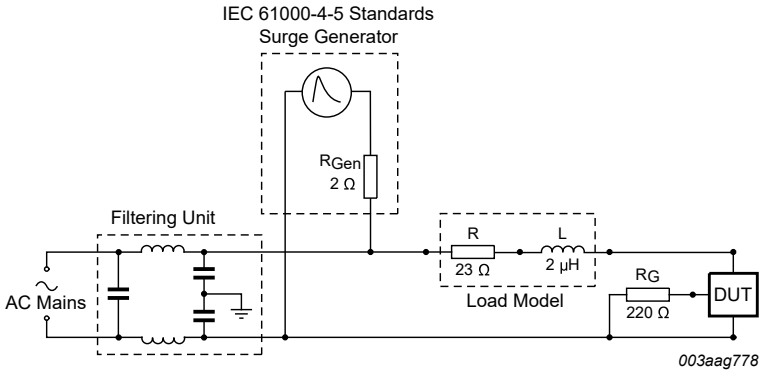


Fig. 6. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

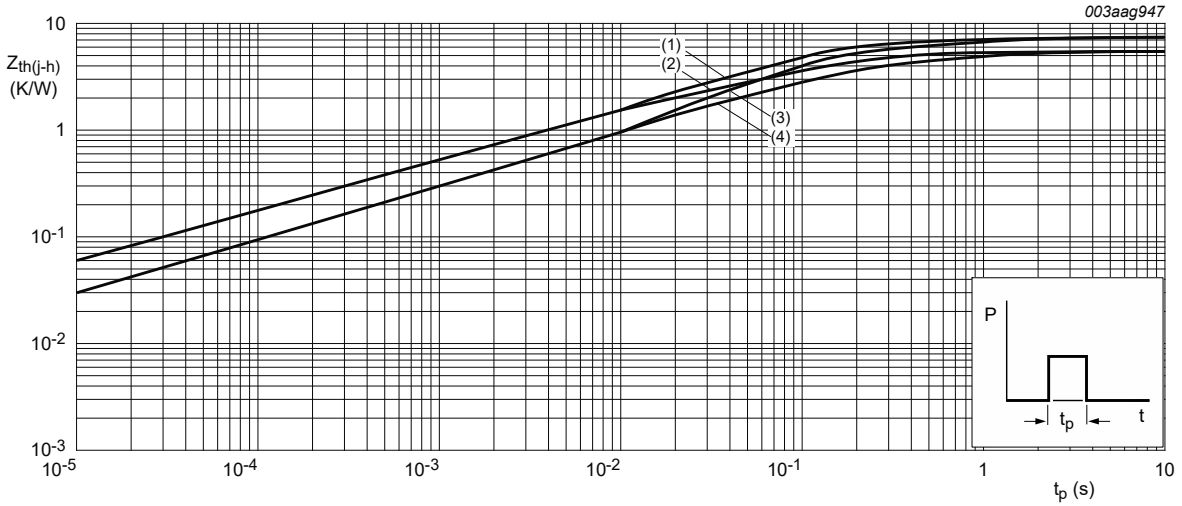
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8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	full cycle or half cycle; with heatsink compound; Fig. 7		-	-	5.5	K/W
		full cycle or half cycle; without heatsink compound; Fig. 7		-	-	7.2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air		-	55	-	K/W



(1) Unidirectional (half cycle) without heatsink compound
(2) Unidirectional (half cycle) with heatsink compound
(3) Bidirectional (full cycle) without heatsink compound
(4) Bidirectional (full cycle) with heatsink compound

Fig. 7. Transient thermal impedance from junction to heatsink as a function of pulse width

9. Isolation characteristics

Table 6. Isolation characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz ≤ f ≤ 60 Hz; T_h = 25 °C		-	-	2500	V
C_{isol}	isolation capacitance	from main terminal 2 to external heatsink; f = 1 MHz; T_h = 25 °C		-	10	-	pF

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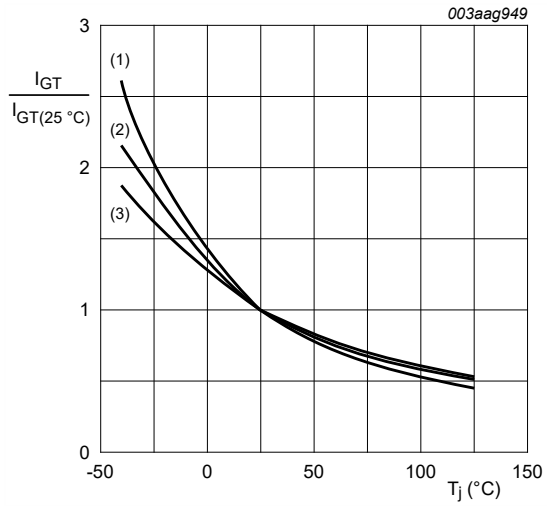
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 100 mA; LD+ G+; T_j = 25 °C; Fig. 8		-	-	10	mA
		V_D = 12 V; I_T = 100 mA; LD+ G-; T_j = 25 °C; Fig. 8		-	-	10	mA
		V_D = 12 V; I_T = 100 mA; LD- G-; T_j = 25 °C; Fig. 8		-	-	10	mA
I_L	latching current	V_D = 12 V; I_G = 100 mA; LD+ G+; T_j = 25 °C; Fig. 9		-	-	30	mA
		V_D = 12 V; I_G = 100 mA; LD+ G-; T_j = 25 °C; Fig. 9		-	-	40	mA
		V_D = 12 V; I_G = 100 mA; LD- G-; T_j = 25 °C; Fig. 9		-	-	30	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 10		-	-	20	mA
V_T	on-state voltage	I_T = 6 A; T_j = 25 °C; Fig. 11		-	-	1.7	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 100 mA; T_j = 25 °C; Fig. 12		-	0.8	1	V
		V_D = 400 V; I_T = 100 mA; T_j = 125 °C; Fig. 12		0.2	0.45	-	V
I_D	off-state current	V_D = 800 V; T_j = 25 °C		-	-	10	µA
		V_D = 800 V; T_j = 125 °C		-	-	0.5	mA
V_{CL}	clamping voltage	I_{CL} = 0.1 mA; t_p = 1 ms; T_j = 25 °C		850	-	-	V
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 13		500	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 4 A; dV_{com}/dt = 20 V/µs; (snubberless condition); gate open circuit; Fig. 14; Fig. 15		4	-	-	A/ms
		V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 4 A; dV_{com}/dt = 10 V/µs; gate open circuit; Fig. 14; Fig. 15		5	-	-	A/ms
		V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 4 A; dV_{com}/dt = 1 V/µs; gate open circuit; Fig. 14; Fig. 15		8	-	-	A/ms

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(1) LD- G-
(2) LD+ G+
(3) LD+ G-

Fig. 8. Normalized gate trigger current as a function of junction temperature

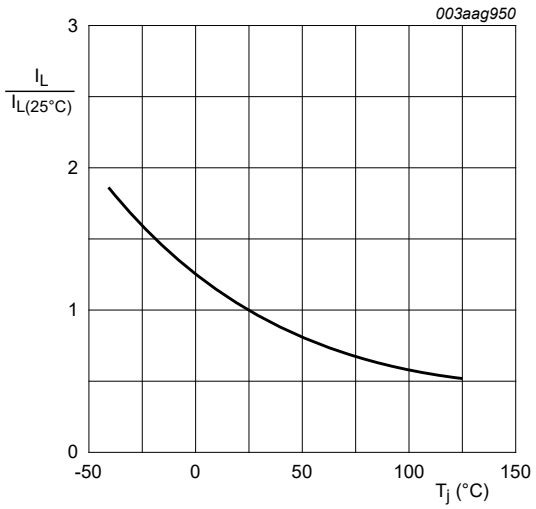


Fig. 9. Normalized latching current as a function of junction temperature

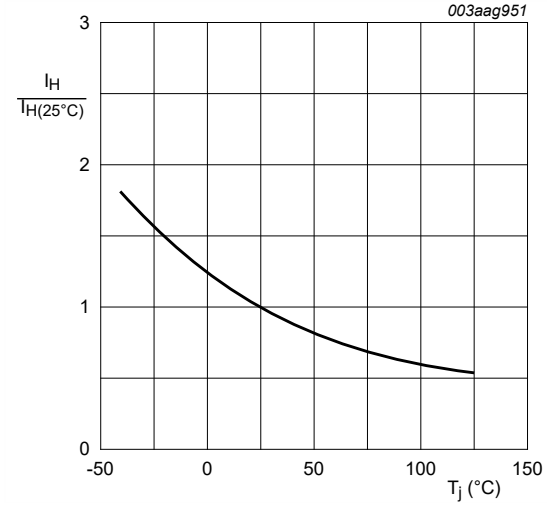
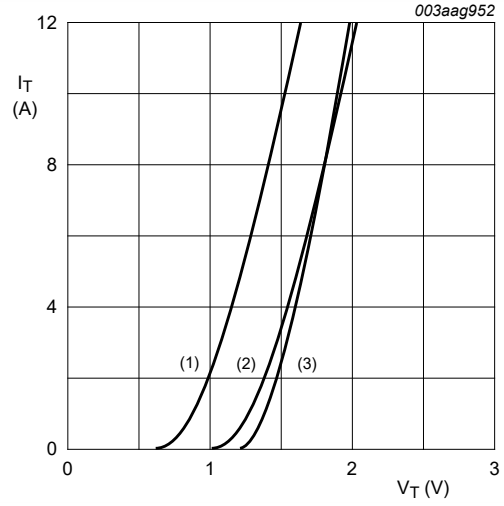


Fig. 10. Normalized holding current as a function of junction temperature



V_o = 1.242 V; R_s = 0.074 Ω
(1) T_j = 125 °C; typical values
(2) T_j = 125 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 11. On-state current as a function of on-state voltage

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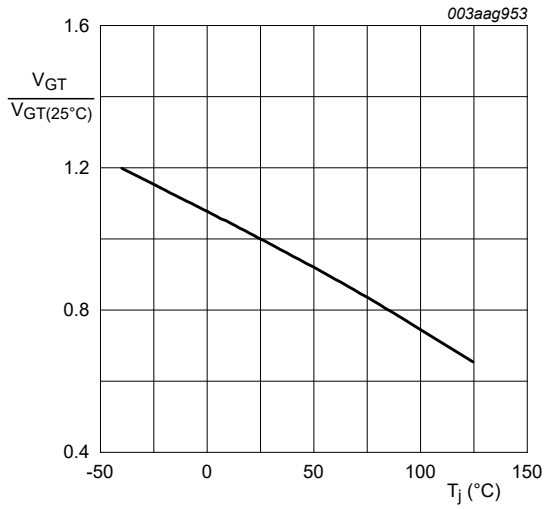
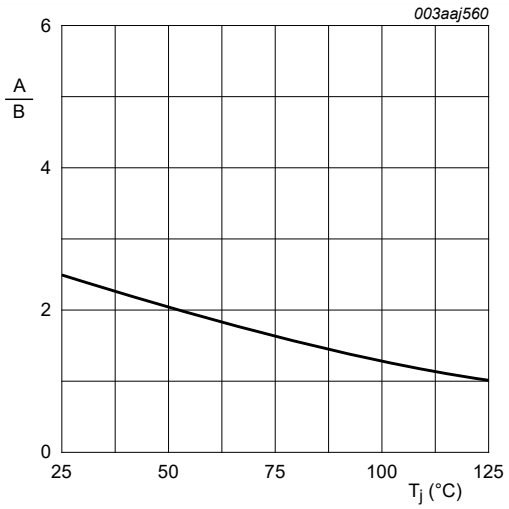
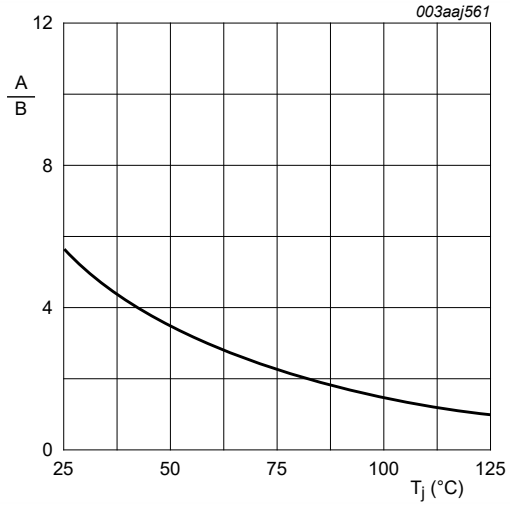


Fig. 12. Normalized gate trigger voltage as a function of junction temperature



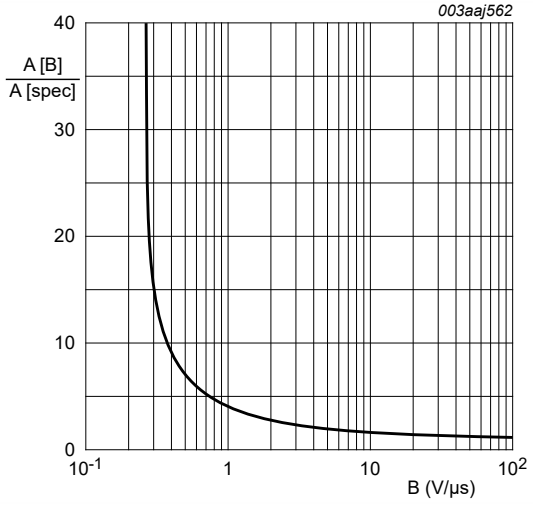
A = dV_D/dt at condition T_j °C
B = dV_D/dt at condition T_j [125] °C

Fig. 13. Normalized rate of rise of off-state voltage as a function of junction temperature



A = dI_{com}/dt at condition T_j °C
B = dI_{com}/dt at condition T_j [125] °C
V_D = 400 V

Fig. 14. Normalized critical rate of rise of commutating current as a function of junction temperature



A [B] is dI_{com}/dt at condition B, dV_{com}/dt
A [spec] is the specified data sheet value of dI_{com}/dt
turn-off time < 20 ms

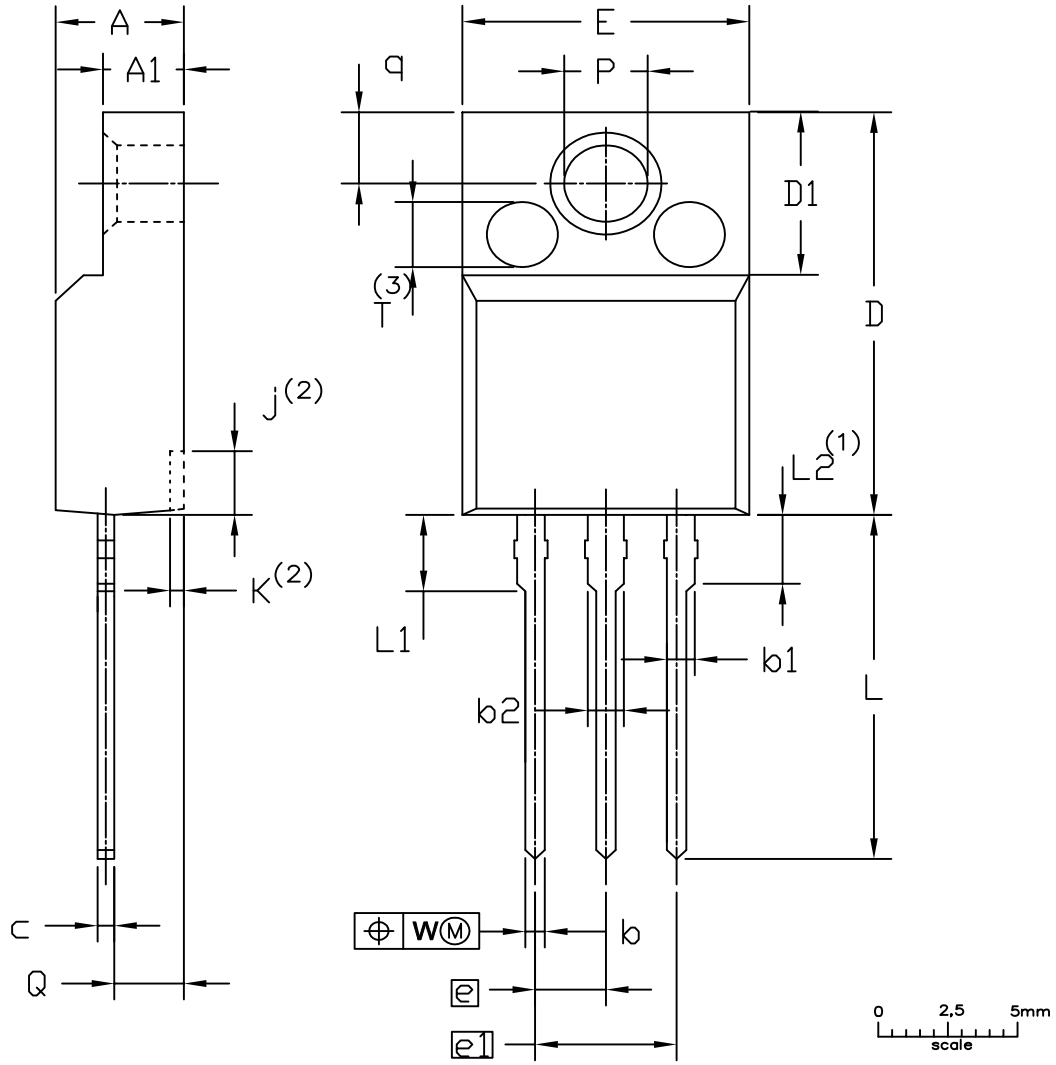
Fig. 15. Normalized critical rate of change of commutating current as a function of critical rate of change of commutating voltage; minimum values

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11. Package outline

Plastic single−ended package; isolated heatsink mounted; 1 mounting hole; 3−lead TO−220 "full pack" SOT186A



UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	j(2)	K(2)	L	L_1	L_2(1) max.	P	Q	q	W	T(3)
mm	4.6	2.9	0.9	1.1	1.4	0.7	15.8	6.5	10.3	2.54	5.08	2.7	0.6	14.4	3.30	3	3.2	2.6	3.0	0.4	2.5
	4.0	2.5	0.7	0.9	1.0	0.4	15.2	6.3	9.7			1.7	0.4	13.5	2.79		3.0	2.3	2.6		

Notes
1. Terminal dimensions within this zone are uncotrolled
2. Dot lines area designs may vary
3. Eject pin mark is for reference only

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3 LEADS TO220F				2013−11−14

Fig. 16. Package outline TO-220F (SOT186A)

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12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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