

RAD Tolerant ACT-RS128K32 High Speed 4 Megabit SRAM Multichip Module

Preliminary

Features

- 4 Low Power CMOS 128K x 8 SRAMs in one MCM
- Overall configuration as 128K x 32
- Tolerant to 30KRad (Si)
- Latch-up Immunity to 112MeV/(mg/cm²)
- Input and Output TTL Compatible
- 35 & 45ns Access Times
- Full Military (-55°C to +125°C) Temperature Range
- For Class K devices per MIL-PRF-38534 - Consult Factory
- +5V Power Supply
- Choice of 4 Hermetically sealed Co-fired Packages:
 - 68-Lead, Low Profile CQFP (F1), 1.56"SQ x .140"max
 - 68-Lead, Dual-Cavity CQFP (F2), .88"SQ x .20"max (.18"max thickness available, contact factory for details) (Drops into the 68 Lead JEDEC .99"SQ CQFJ footprint)
 - 66-Lead, PGA-Type (P1), 1.385"SQ x .245"max
- Internal Decoupling Capacitors

AEROFLEX
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www.aeroflex.com/act1.htm

General Description

The ACT-RS128K32 is a High Speed 4 megabit CMOS SRAM Multichip Module (MCM) designed for full temperature range, military, space, or high reliability mass memory and fast cache applications.

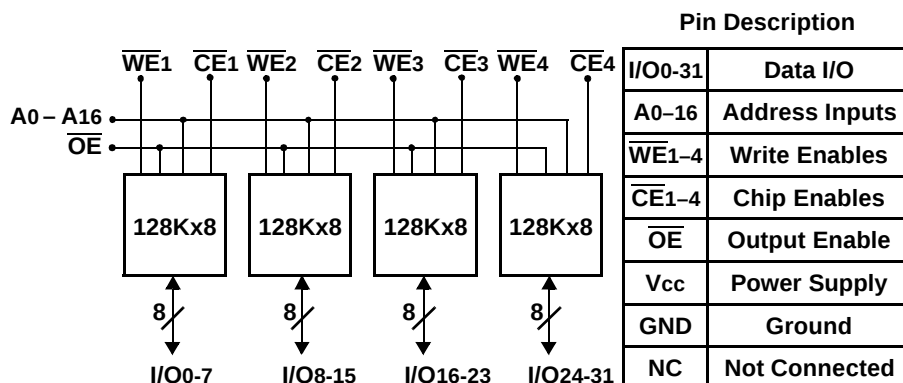
The MCM can be organized as a 128K x 32 bits, 256K x 16 bits or 512k x 8 bits device and is input and output TTL compatible. Writing is executed when the write enable (WE) and chip enable ($\overline{CE}$) inputs are low. Reading is accomplished when WE is high and CE and output enable ($\overline{OE}$) are both low. Access time grades of 35ns and 45ns maximum are standard.

The +5 Volt power supply version is standard.

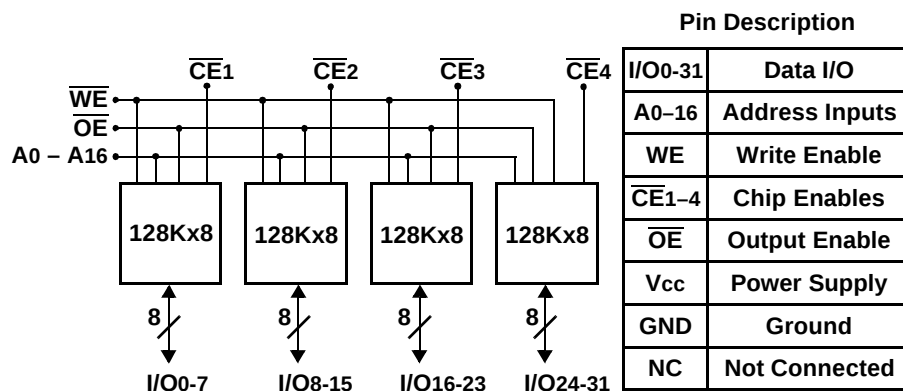
The products are designed for operation over the temperature range of -55°C to +125°C and screened under the full military environment. DESC Standard Military Drawing (SMD) part numbers are pending.

The ACT-RS128K32 is manufactured in Aeroflex's 80,000ft² MIL-PRF-38534 certified facility in Plainview, N.Y.

Block Diagram – PGA Type Package(P1) & CQFP(F2)



Block Diagram – CQFP(F1)



Absolute Maximum Ratings

Symbol	Rating	Range	Units
T_C	Case Operating Temperature	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_D	Maximum Package Power Dissipation		
	F1 & P1 Packages	4.4	W
	F2 Package	3.3	W
θ_{J-C}	Hottest Die, Max Thermal Resistance - Junction to Case		
	F1 & P1 Packages	2.0	°C/W
	F2 Package	8.0	°C/W
V_G	Maximum Signal Voltage to Ground	-0.5 to +7	V
T_L	Maximum Lead Temperature (10 seconds)	300	°C

Normal Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CC}	Power Supply Voltage	+4.5	+5.5	V
V_{IH}	Input High Voltage	+2.2	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	-0.5	+0.8	V

Truth Table

Mode	CE	OE	WE	Data I/O	Power
Standby	H	X	X	High Z	Standby (deselect/power down)
Read	L	L	H	Data Out	Active
Read	L	H	H	High Z	Active (deselected)
Write	L	X	L	Data In	Active

Capacitance

(f = 1MHz, $T_C = 25^\circ\text{C}$)

Symbol	Parameter	Maximum	Units
C_{AD}	$A_0 - A_{16}$ Capacitance	50	pF
C_{OE}	$\overline{OE}$ Capacitance	50	pF
C_{WE}	CQFP(F1) Package	50	pF
	PGA(P1) and CQFP(F2) Packages	20	pF
C_{CE}	Chip Enable Capacitance	20	pF
$C_{I/O}$	I/O0 – I/O31 Capacitance	20	pF

Capacitance is guaranteed by design but not tested.

DC Characteristics

(4.5Vdc $\leq V_{CC} \leq 5.5V_{dc}$, $V_{SS} = 0V$, $T_C = -55^\circ\text{C}$ to $+125^\circ\text{C}$, Unless otherwise specified)

Parameter	Sym	Conditions	<u>-035</u>		<u>-045</u>		Units
			Min	Max	Min	Max	
Input Leakage Current	I_{LI}	$V_{CC} = \text{Max}$, $V_{IN} = 0$ or V_{CC}		10		10	μA
Output Leakage Current	I_{LO}	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IH}$, $V_{OUT} = 0$ or V_{CC}		10		10	μA
Operating Supply Current 32 Bit Mode	$I_{CC} \times 32$	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, f = 5 MHz, $V_{CC} = \text{Max}$, CMOS Compatible		500		600	mA

DC Characteristics (Continued)

(4.5Vdc ≤ V_{CC} ≤ 5.5Vdc, V_{SS} = 0V, T_C = -55°C to +125°C, Unless otherwise specified)

Parameter	Sym	Conditions	-035		-045		Units
			Min	Max	Min	Max	
Standby Current	I _{SB}	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IH}$, f = 5 MHz, V _{CC} = Max, CMOS Compatible		30		30	mA
Output Low Voltage	V _{OL}	I _{OL} = 8 mA, V _{CC} = Min		0.4		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0 mA, V _{CC} = Min	2.4		2.4		V

AC Characteristics

(V_{CC} = 5.0V, V_{SS} = 0V, T_C = -55°C to +125°C)

Read Cycle

Parameter	Sym	-035		-045		Units
		Min	Max	Min	Max	
Read Cycle Time	t _{RC}	35		45		ns
Address Access Time	t _{AA}		35		45	ns
Chip Enable Access Time	t _{ACE}		35		45	ns
Chip Enable to Output in Low Z*	t _{CLZ}	3		3		ns
Output Enable to Output in Low Z*	t _{OLZ}	0		0		ns
Chip Deselect to Output in High Z*	t _{CHZ}		20		20	ns
Output Disable to Output in High Z*	t _{OHZ}		10		15	ns

* Parameters guaranteed by design but not tested

Write Cycle

Parameter	Sym	-035		-045		Units
		Min	Max	Min	Max	
Write Cycle Time	t _{WC}	35		45		ns
Chip Enable to End of Write	t _{CW}	25		35		ns
Address Valid to End of Write	t _{AW}	25		35		ns
Data Valid to End of Write	t _{DW}	18		20		ns
Write Pulse Width	t _{WP}	25		35		ns
Address Setup Time	t _{AS}	0		0		ns
Write to Output in High Z *	t _{WHZ}		10		15	ns
Data Hold from Write Time	t _{DH}	0		0		ns
Address Hold Time	t _{AH}	0		0		ns

* Parameters guaranteed by design but not tested

Data Retention Electrical Characteristics (Special Order Only)

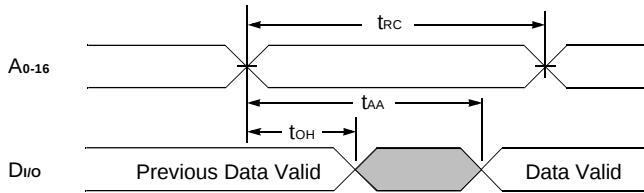
(T_C = -55°C to +125°C)

Parameter	Sym	Test Conditions	All Speeds		Units
			Min	Max	
V _{CC} for Data Retention	V _{DR}	$\overline{CE} \geq V_{CC} - 0.2V$	2	5.5	V
Data Retention Current	I _{CCDR1}	V _{CC} = 3V, 35 & 45ns		4	mA

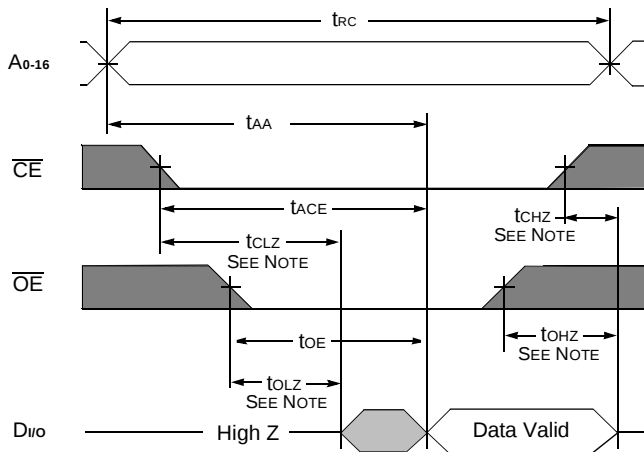
Timing Diagrams

Read Cycle Timing Diagrams

Read Cycle 1 ($\overline{\text{CE}} = \overline{\text{OE}} = \text{V}_{\text{IL}}$, $\overline{\text{WE}} = \text{V}_{\text{IH}}$)



Read Cycle 2 ($\overline{WE} = V_{IH}$)



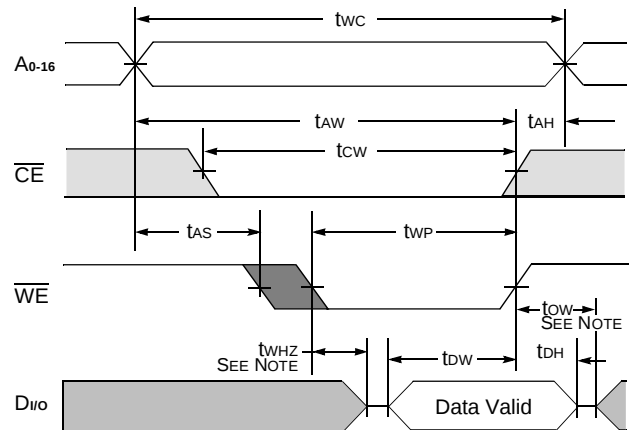
UNDEFINED

DON'T CARE

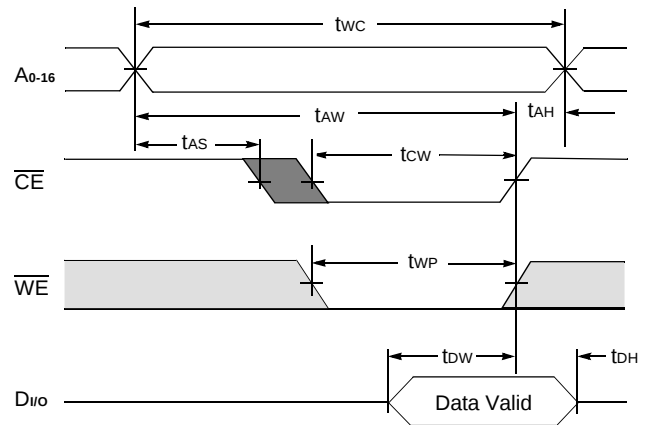
Note: Guaranteed by design, but not tested.

Write Cycle Timing Diagrams

Write Cycle 1 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}} = \text{VIL}$)

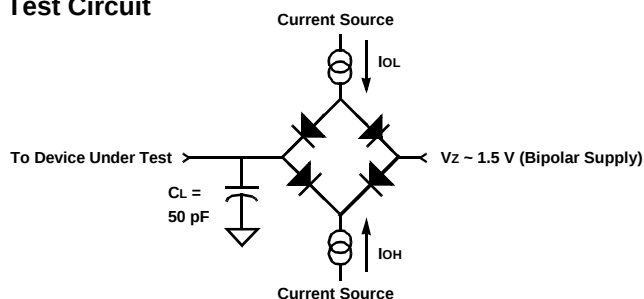


Write Cycle 2 ($\overline{\text{CE}}$ Controlled, $\overline{\text{OE}} = V_{\text{IH}}$)



Note: Guaranteed by design, but not tested.

AC Test Circuit



Notes:

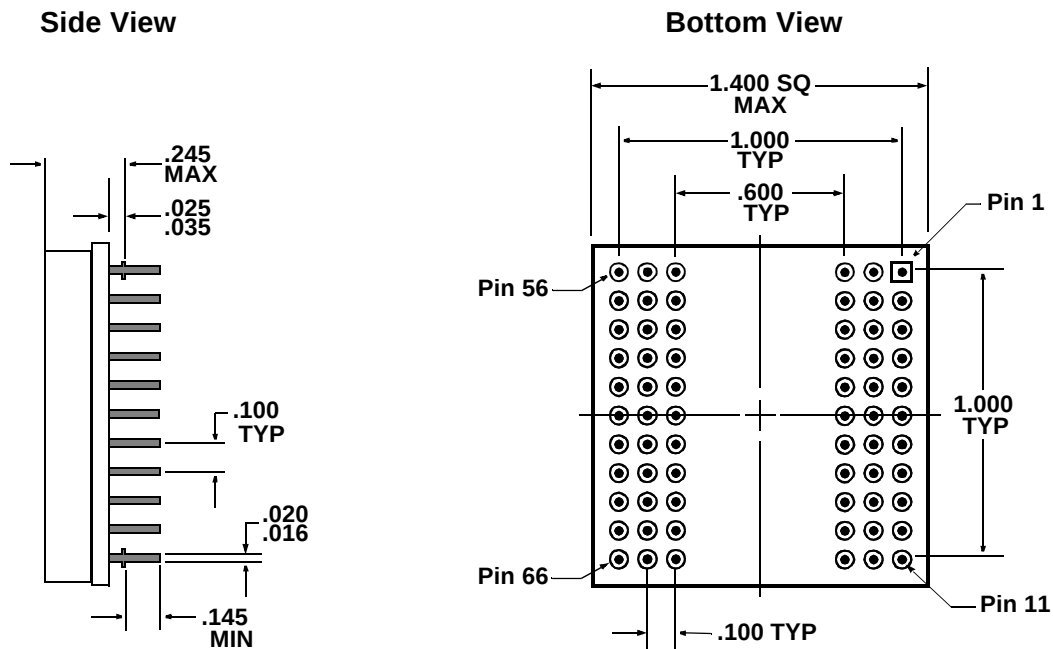
1) V_Z is programmable from -2V to +7V. 2) I_{OL} and I_{OH} programmable from 0 to 16 mA. 3) Tester Impedance Z_o = 75Ω. 4) V_Z is typically the midpoint of V_{OH} and V_{OL}. 5) I_{OL} and I_{OH} are adjusted to simulate a typical resistance load circuit. 6) ATE Tester includes jig capacitance.

Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	ns
Input and Output Timing Reference Level	1.5	V
Output Lead Capacitance	50	pF

Pin Numbers & Functions

66 Pins — PGA-Type							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	I/O8	18	A12	35	I/O25	52	$\overline{WE}_3$
2	I/O9	19	V _{CC}	36	I/O26	53	$\overline{CE}_3$
3	I/O10	20	$\overline{CE}_1$	37	A6	54	GND
4	A13	21	NC	38	A7	55	I/O19
5	A14	22	I/O3	39	NC	56	I/O31
6	A15	23	I/O15	40	A8	57	I/O30
7	A16	24	I/O14	41	A9	58	I/O29
8	NC	25	I/O13	42	I/O16	59	I/O28
9	I/O0	26	I/O12	43	I/O17	60	A0
10	I/O1	27	$\overline{OE}$	44	I/O18	61	A1
11	I/O2	28	NC	45	V _{CC}	62	A2
12	$\overline{WE}_2$	29	$\overline{WE}_1$	46	$\overline{CE}_4$	63	I/O23
13	$\overline{CE}_2$	30	I/O7	47	$\overline{WE}_4$	64	I/O22
14	GND	31	I/O6	48	I/O27	65	I/O21
15	I/O11	32	I/O5	49	A3	66	I/O20
16	A10	33	I/O4	50	A4		
17	A11	34	I/O24	51	A5		

"P1" — 1.385" SQ PGA Type Package Standard

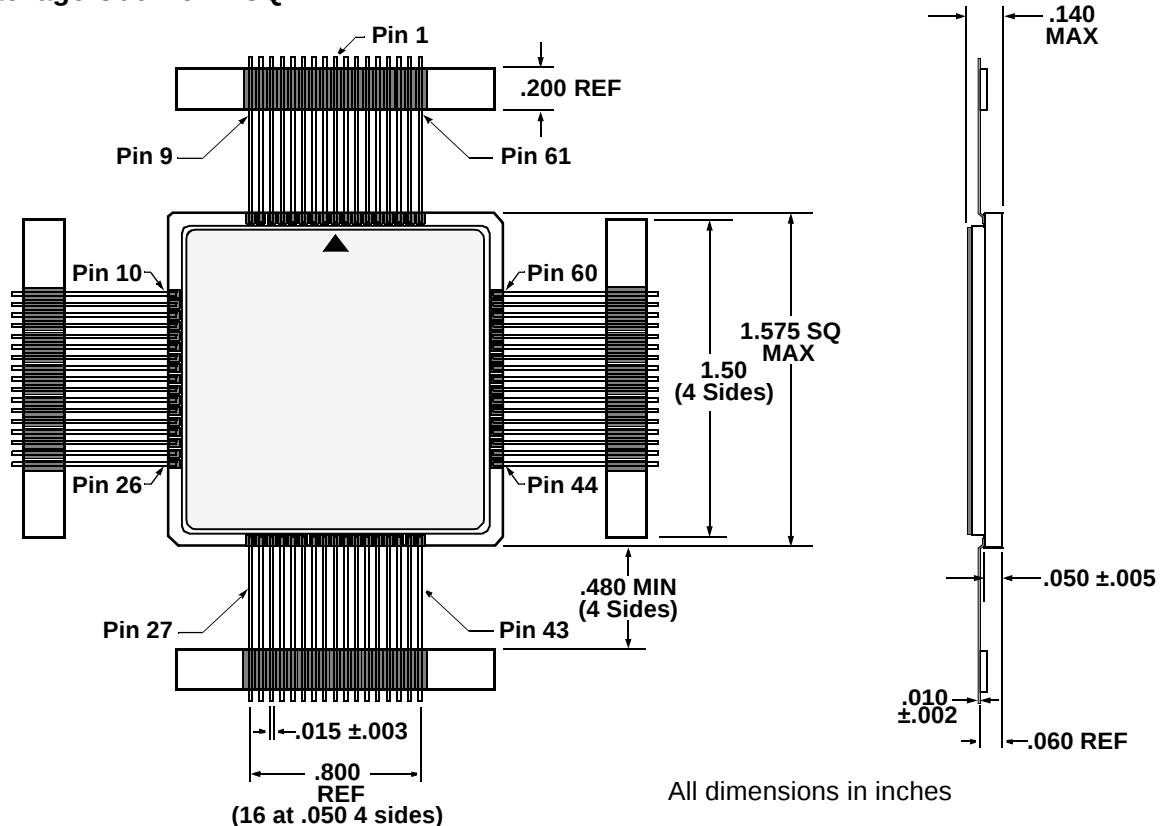


All dimensions in inches

Pin Numbers & Functions

68 Pins — CQFP							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CE}_1$	19	I/O ₈	36	$\overline{CE}_4$	53	I/O ₂₃
3	A ₅	20	I/O ₉	37	NC	54	I/O ₂₂
4	A ₄	21	I/O ₁₀	38	NC	55	I/O ₂₁
5	A ₃	22	I/O ₁₁	39	NC	56	I/O ₂₀
6	A ₂	23	I/O ₁₂	40	NC	57	I/O ₁₉
7	A ₁	24	I/O ₁₃	41	NC	58	I/O ₁₈
8	A ₀	25	I/O ₁₄	42	NC	59	I/O ₁₇
9	NC	26	I/O ₁₅	43	NC	60	I/O ₁₆
10	I/O ₀	27	V _{CC}	44	I/O ₃₁	61	V _{CC}
11	I/O ₁	28	A ₁₁	45	I/O ₃₀	62	A ₁₀
12	I/O ₂	29	A ₁₂	46	I/O ₂₉	63	A ₉
13	I/O ₃	30	A ₁₃	47	I/O ₂₈	64	A ₈
14	I/O ₄	31	A ₁₄	48	I/O ₂₇	65	A ₇
15	I/O ₅	32	A ₁₅	49	I/O ₂₆	66	A ₆
16	I/O ₆	33	A ₁₆	50	I/O ₂₅	67	$\overline{WE}$
17	I/O ₇	34	$\overline{CE}_2$	51	I/O ₂₄	68	$\overline{CE}_3$

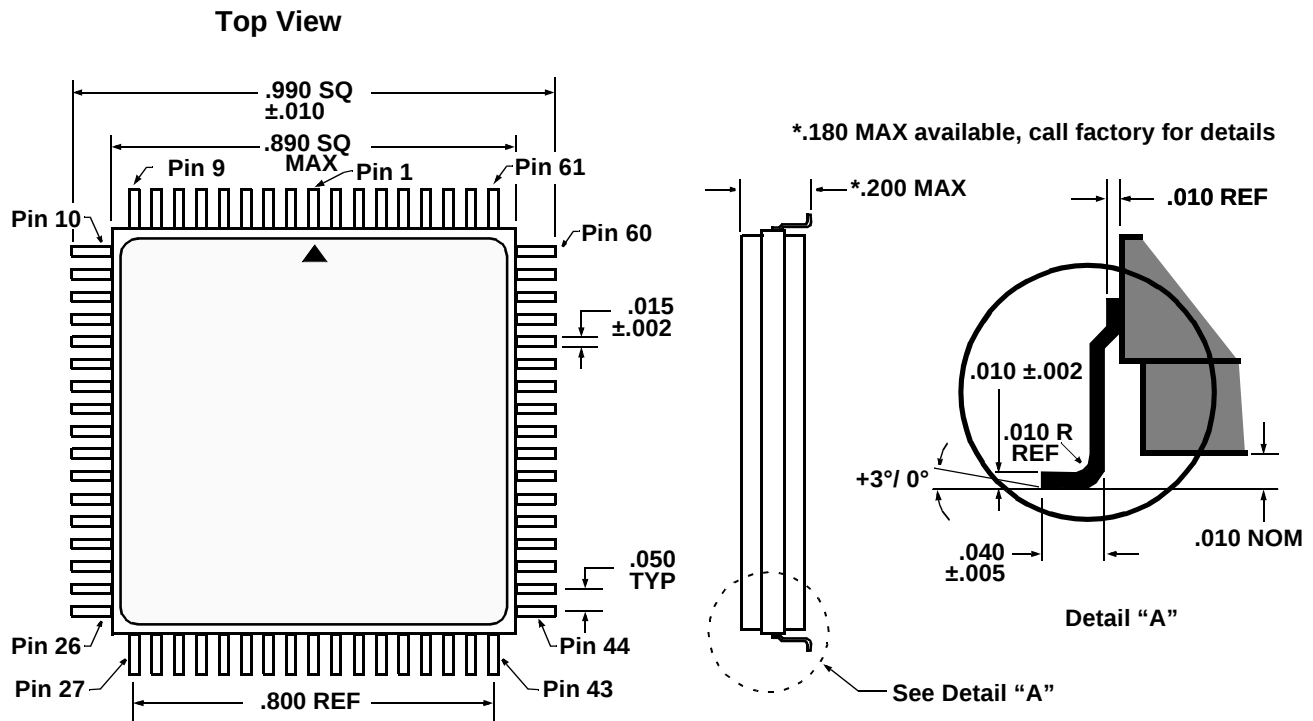
Package Outline — CQFP "F1"



Pin Numbers & Functions

68 Pins — Dual-Cavity CQFP							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CE}_3$	19	I/O ₈	36	$\overline{CE}_2$	53	I/O ₂₃
3	A ₅	20	I/O ₉	37	NC	54	I/O ₂₂
4	A ₄	21	I/O ₁₀	38	$\overline{WE}_2$	55	I/O ₂₁
5	A ₃	22	I/O ₁₁	39	$\overline{WE}_3$	56	I/O ₂₀
6	A ₂	23	I/O ₁₂	40	$\overline{WE}_4$	57	I/O ₁₉
7	A ₁	24	I/O ₁₃	41	NC	58	I/O ₁₈
8	A ₀	25	I/O ₁₄	42	NC	59	I/O ₁₇
9	NC	26	I/O ₁₅	43	NC	60	I/O ₁₆
10	I/O ₀	27	V _{CC}	44	I/O ₃₁	61	V _{CC}
11	I/O ₁	28	A ₁₁	45	I/O ₃₀	62	A ₁₀
12	I/O ₂	29	A ₁₂	46	I/O ₂₉	63	A ₉
13	I/O ₃	30	A ₁₃	47	I/O ₂₈	64	A ₈
14	I/O ₄	31	A ₁₄	48	I/O ₂₇	65	A ₇
15	I/O ₅	32	A ₁₅	49	I/O ₂₆	66	A ₆
16	I/O ₆	33	A ₁₆	50	I/O ₂₅	67	$\overline{WE}_1$
17	I/O ₇	34	$\overline{CE}_1$	51	I/O ₂₄	68	$\overline{CE}_4$

Package Outline — Dual-Cavity CQFP "F2"



All dimensions in inches

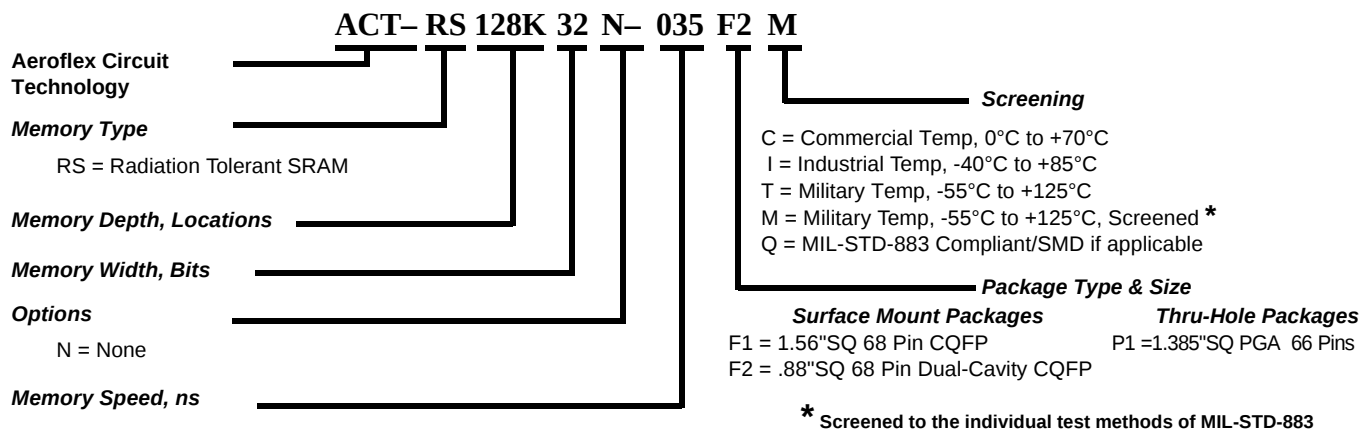
Note: Metallic lids and walls – both sides



Ordering Information

Model Number	DESC Part Number	Speed	Package
ACT-RS128K32N-035F1Q	5962-TBD	35ns	1.56"sq CQFP
ACT-RS128K32N-035F2Q	5962-TBD		.88"sq CQFP
ACT-RS128K32N-035P1Q	5962-TBD		1.385"sq PGA-Type
ACT-RS128K32N-045F1Q	5962-TBD	45ns	1.56"sq CQFP
ACT-RS128K32N-045F2Q	5962-TBD		.88"sq CQFP
ACT-RS128K32N-045P1Q	5962-TBD		1.385"sq PGA-Type

Model Number Breakdown



Specifications subject to change without notice

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