ACT-SF128K32 High Speed 128Kx32 SRAM / 128Kx32 Flash Multichip Module

AEROFLEX CIRCUIT TECHNOLOGY
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FEATURES

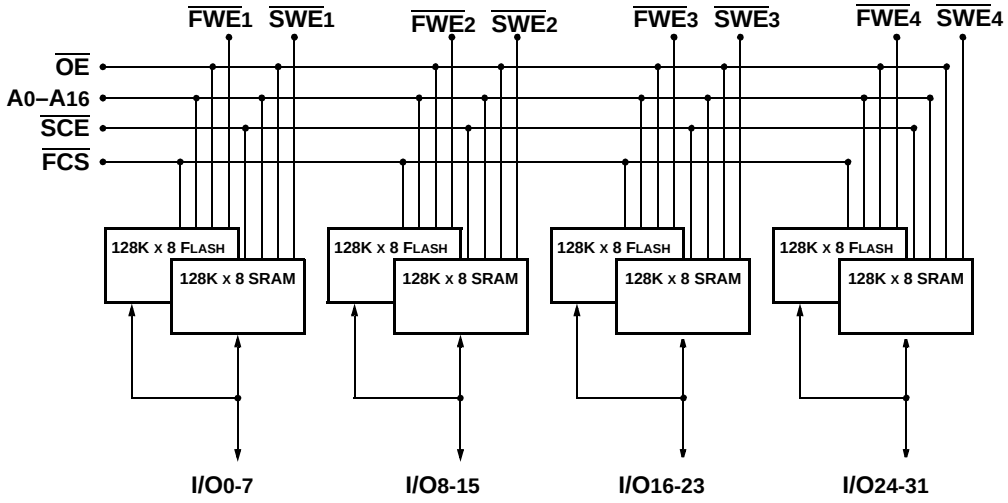
- 4 – 128K x 8 SRAMs & 4 – 128K x 8 Flash Die in One MCM
- Access Times of 25ns (SRAM) and 60ns (Flash) or 35ns (SRAM) and 70ns or 90ns (Flash)
- Organized as 128K x 32 of SRAM and 128K x 32 of Flash Memory with Common Data Bus
- Low Power CMOS
- Input and Output TTL Compatible Design
- MIL-PRF-38534 Compliant MCMs Available
- Decoupling Capacitors and Multiple Grounds for Low Noise
- Commercial, Industrial and Military Temperature Ranges
- Industry Standard Pinouts
- TTL Compatible Inputs and Outputs
- Packaging – Hermetic Ceramic
  - 66–Lead, PGA-Type, 1.385"SQ x 0.245"max, Aeroflex code# P3,P7 without/with shoulders

FLASH MEMORY FEATURES

- Sector Architecture (Each Die)
  - 8 Equal Sectors of 16K bytes each
  - Any combination of sectors can be erased with one command sequence.
- +5V Programing, +5V Supply
- Embedded Erase and Program Algorithms
- Hardware and Software Write Protection
- Page Program Operation and Internal Program Control Time.
- 10,000 Erase/Program Cycles

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Block Diagram – PGA Type Package (P3 & P7)



PIN DESCRIPTION

I/O0-31	Data I/O
A0–16	Address Inputs
$\overline{FWE}$1-4	Flash Write Enables
$\overline{SWE}$1-4	SRAM Write Enables
$\overline{FCE}$	Flash Chip Enable
$\overline{SCE}$	SRAM Chip Enable
$\overline{OE}$	Output Enable
NC	Not Connected
VCC	Power Supply
GND	Ground

Absolute Maximum Ratings

Symbol	Rating	Range	Units
T_C	Operating Temperature	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
V_G	Maximum Signal Voltage to Ground	-0.5 to +7	V
T_L	Maximum Lead Temperature (10 seconds)	300	°C

Parameter	
Flash Data Retention	10 Years
Flash Endurance (Write/Erase Cycles)	10,000

Normal Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CC}	Power Supply Voltage	+4.5	+5.5	V
V_{IH}	Input High Voltage	+2.2	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	-0.5	+0.8	V

Capacitance

(V_{IN} = 0V, f = 1MHz, T_C = 25°C)

Symbol	Parameter	Maximum	Units
C_{AD}	A_0 – A_{18} Capacitance	80	pF
C_{OE}	$\overline{OE}$ Capacitance	80	pF
C_{WE1-4}	F/S Write Enable Capacitance	30	pF
C_{CE}	F/S Chip Enable Capacitance	50	pF
$C_{I/O}$	I/O_0 – I/O_{31} Capacitance	30	pF

This parameter is guaranteed by design but not tested

DC Characteristics

(V_{CC} = 5.0V, V_{SS} = 0V, T_C = -55°C to +125°C)

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = Max, V_{IN} = 0 to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{FCE}$ = $\overline{SCE}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = 0 to V_{CC}		10	µA
SRAM Operating Supply Current x 32 Mode	I_{CC}x32	$\overline{SCE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = Max, $\overline{FCE}$ = V_{IH}		550	mA
Standby Current	I_{SB}	$\overline{FCE}$ = $\overline{SCE}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = Max		80	mA
SRAM Output Low Voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min, $\overline{FCE}$ = V_{IH}		0.4	V
SRAM Output High Voltage	V_{OH}	I_{OH} = -4.0 mA, , V_{CC} = Min, $\overline{FCE}$ = V_{IH}	2.4		V
Flash Vcc Active Current for Read (1)	I_{CC1}	$\overline{FCE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, $\overline{SCE}$ = V_{IH}		220	mA
Flash Vcc Active Current for Program or Erase (2)	I_{CC2}	$\overline{FCE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, $\overline{SCE}$ = V_{IH}		280	mA
Flash Output Low Voltage	V_{OL}	I_{OL} = 12 mA, V_{CC} = Min, $\overline{SCE}$ = V_{IH}		0.45	V
Flash Output High Voltage	V_{OH1}	I_{OH} = -2.5 mA, , V_{CC} = Min, $\overline{SCE}$ = V_{IH}	0.85 x V_{CC}		V
Flash Low Vcc Lock Out Voltage	V_{LKO}		3.2	4.2	V

Notes: 1) The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5MHz). The frequency component typically is less than 2mA/MHz, with $\overline{OE}$ at V_{IH} 2) I_{CC} active while Embedded Algorithim (program or erase) is in progress 3) DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

SRAM AC Characteristics

(V_{CC} = 5.0V, V_{SS}= 0V, T_C = -55°C to +125°C)

Read Cycle

Parameter	Symbol	–025		–035		Units
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		ns
Address Access Time	t_{AA}		25		35	ns
Chip Select Access Time	t_{ACE}		25		35	ns
Output Hold from Address Change	t_{OH}	0		0		ns
Output Enable to Output Valid	t_{OE}		15		20	ns
Chip Select to Output in Low Z *	t_{CLZ}	3		3		ns
Output Enable to Output in Low Z *	t_{OLZ}	0		0		ns
Chip Deselect to Output in High Z *	t_{CHZ}		12		20	ns
Output Disable to Output in High Z *	t_{OHZ}		12		20	ns

* Parameters guaranteed by design but not tested

Write Cycle

Parameter	Symbol	–025		–035		Units
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	25		35		ns
Chip Select to End of Write	t_{CW}	20		25		ns
Address Valid to End of Write	t_{AW}	20		25		ns
Data Valid to End of Write	t_{DW}	15		20		ns
Write Pulse Width	t_{WP}	20		25		ns
Address Setup Time	t_{AS}	0		0		ns
Output Active from End of Write *	t_{OW}	0		0		ns
Write to Output in High Z *	t_{WHZ}		10		20	ns
Data Hold from Write Time	t_{DH}	0		0		ns
Address Hold Time	t_{AH}	0		0		ns

* Parameters guaranteed by design but not tested

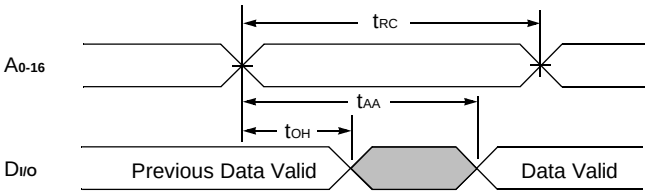
SRAM Truth Table

Mode	$\overline{SCE}$	$\overline{OE}$	$\overline{SWE}$	Data I/O	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	Data Out	Active
Output Disable	L	H	H	High Z	Active
Write	L	X	L	Data In	Active

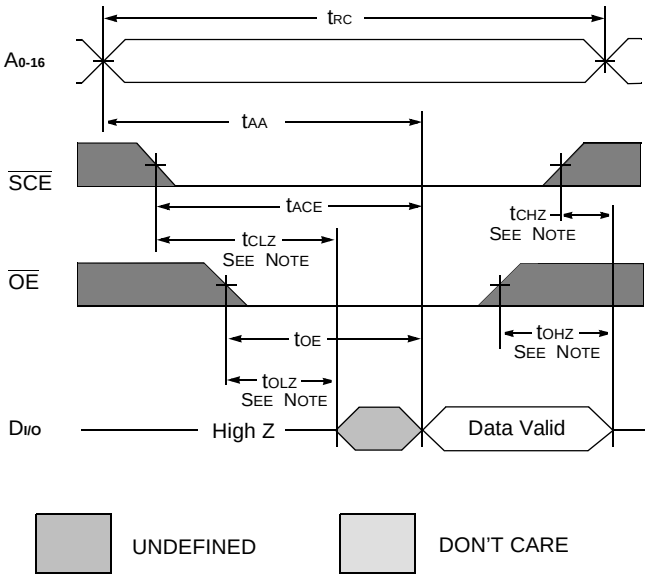
Timing Diagrams — SRAM

Read Cycle Timing Diagrams

Read Cycle 1 ($\overline{SCE}$ = $\overline{OE}$ = V_{IL}, $\overline{SWE}$ = V_{IH})



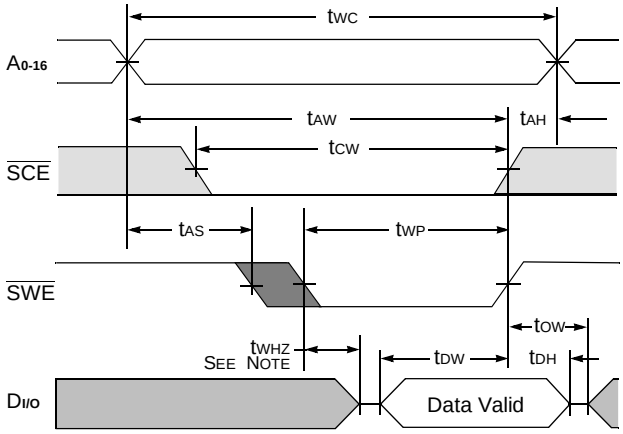
Read Cycle 2 ($\overline{SWE}$ = V_{IH})



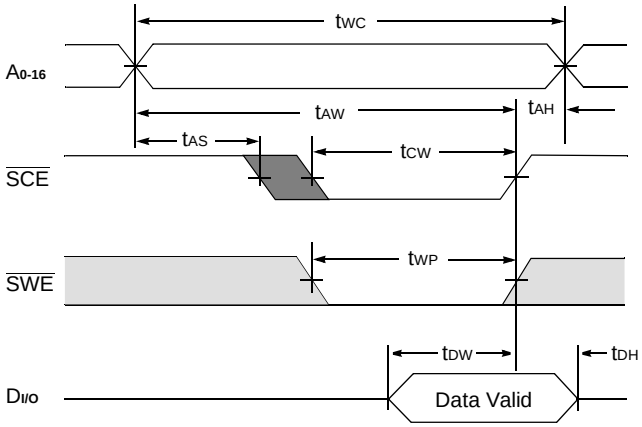
UNDEFINED DON'T CARE

Write Cycle Timing Diagrams

Write Cycle ($\overline{SWE}$ Controlled, $\overline{OE}$ = V_{IH})

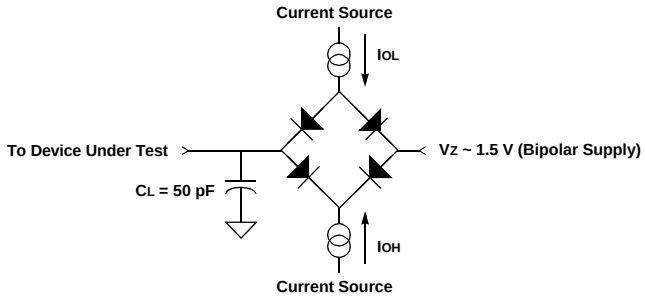


Write Cycle ($\overline{SCE}$ Controlled, $\overline{OE}$ = V_{IH})



Note: Guaranteed by design, but not tested.

AC Test Circuit



AC Test Conditions

Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	ns
Input and Output Timing Reference Level	1.5	V

Notes:
1) V_Z is programmable from -2V to +7V. 2) I_{OL} and I_{OH} programmable from 0 to 16 mA. 3) Tester Impedance Z_O = 75Ω. 4) V_Z is typically the midpoint of V_{OH} and V_{OL}. 5) I_{OL} and I_{OH} are adjusted to simulate a typical resistance load circuit. 6) ATE Tester includes jig capacitance.

Flash AC Characteristics – Read Only Operations

(Vcc = 5.0V, Vss = 0V, TC = -55°C to +125°C)

Parameter	Symbol		–60		–70		–90		Units
	JEDEC	Stand'd	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	60		70		90		ns
Address Access Time	t_{AVQV}	t_{ACC}		60		70		90	ns
Chip Enable Access Time	t_{ELQV}	t_{CE}		60		70		90	ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		30		35		40	ns
Chip Enable to Output High Z (1)	t_{EHQZ}	t_{DF}		20		20		25	ns
Output Enable High to Output High Z(1)	t_{GHQZ}	t_{DF}		20		20		25	ns
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Change, Whichever is First	t_{AXQX}	t_{OH}	0		0		0		ns

Note 1. Guaranteed by design, but not tested

Flash AC Characteristics – Write/Erase/Program Operations, $\overline{FWE}$ Controlled

(Vcc = 5.0V, Vss = 0V, TC = -55°C to +125°C)

Parameter	Symbol		–60		–70		–90		Units
	JEDEC	Stand'd	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAC}	t_{WC}	60		70		90		ns
Chip Enable Setup Time	t_{ELWL}	t_{CE}	0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	30		35		45		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	30		30		45		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	45		45		45		ns
Chip Enable Hold Time	t_{WHEH}	t_{CH}	0		0		0		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		20		ns
Duration of Byte Programming Operation	t_{WHWH1}		14	TYP	14	TYP	14	TYP	µs
Sector Erase Time	t_{WHWH2}			60		60		60	Sec
Chip Erase Time	t_{WHWH3}			120		120		120	Sec
Read Recovery Time before Write	t_{GHWL}		0		0		0		µs
Vcc Setup Time		t_{VCE}	50		50		50		µs
Output Enable Setup Time		t_{OES}		12.5		12.5		12.5	Sec
Output Enable Hold Time[1]		t_{OEH}	10		10		10		ns

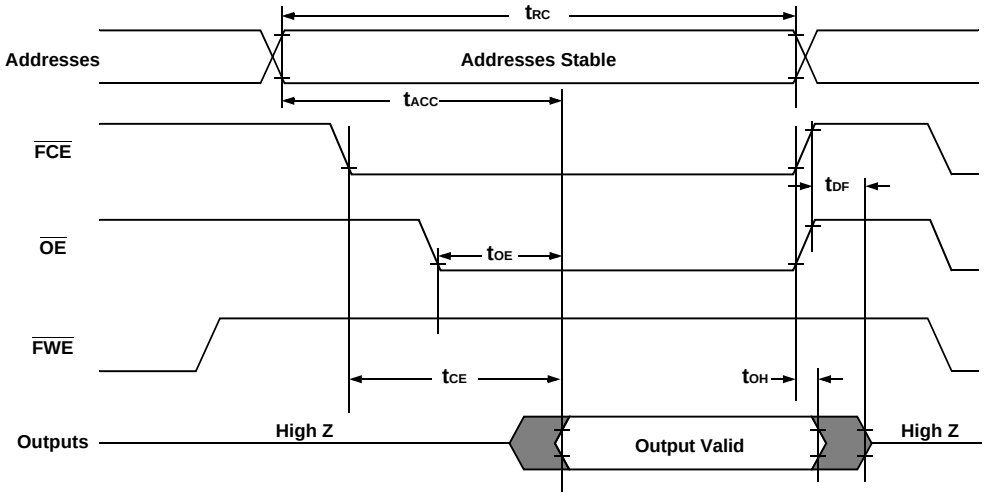
Note: 1. For Toggle and Data Polling.

Flash AC Characteristics – Write/Erase/Program Operations, $\overline{FCE}$ Controlled

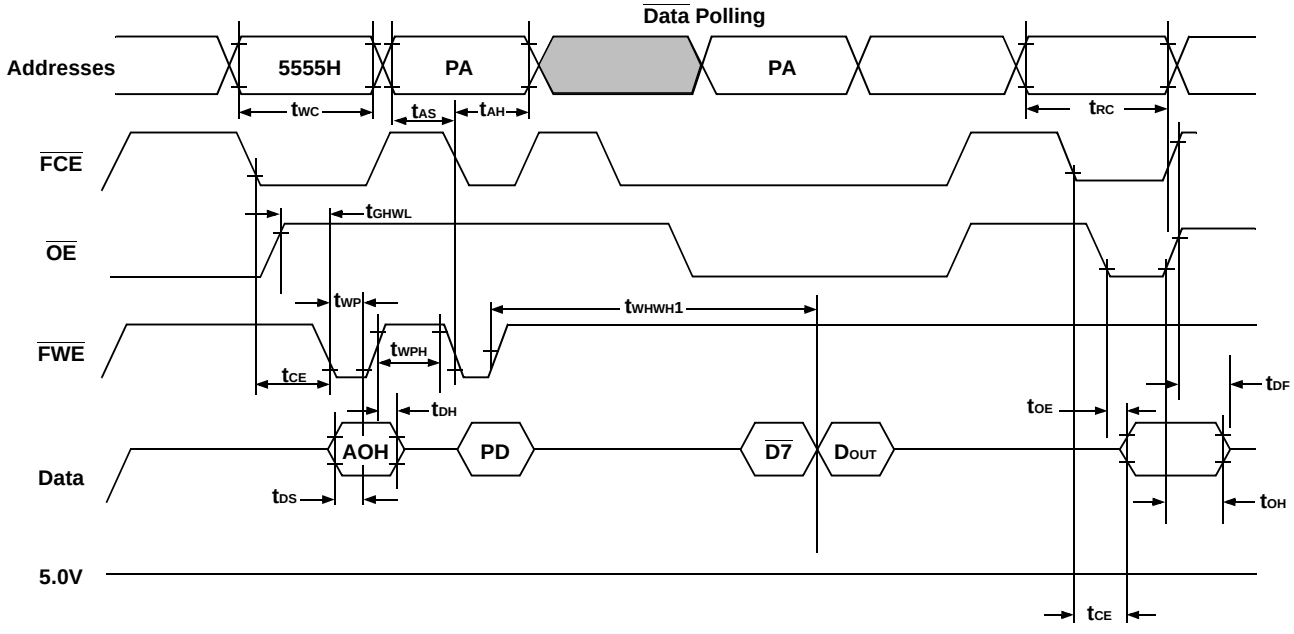
(Vcc = 5.0V, Vss = 0V, TC = -55°C to +125°C)

Parameter	Symbol		–60		–70		–90		Units
	JEDEC	Stand'd	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAC}	t_{WC}	60		70		90		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		ns
Chip Enable Pulse Width	t_{ELEH}	t_{CP}	35		35		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	30		30		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		45		50		ns
Write Enable Hold from Write Enable High	t_{EHWH}	t_{WH}	0		0		0		ns
Chip Enable Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		ns
Duration of Byte Programming	t_{WHWH1}		14	TYP	14	TYP	14	TYP	µs
Sector Erase Time	t_{WHWH2}			60		60		60	Sec
Chip Erase Time	t_{WHWH3}			120		120		120	Sec
Read Recovery Time	t_{GHEL}		0		0		0		ns
Chip Programming Time				12.5		12.5		12.5	Sec

AC Waveforms for Flash Memory Read Operations

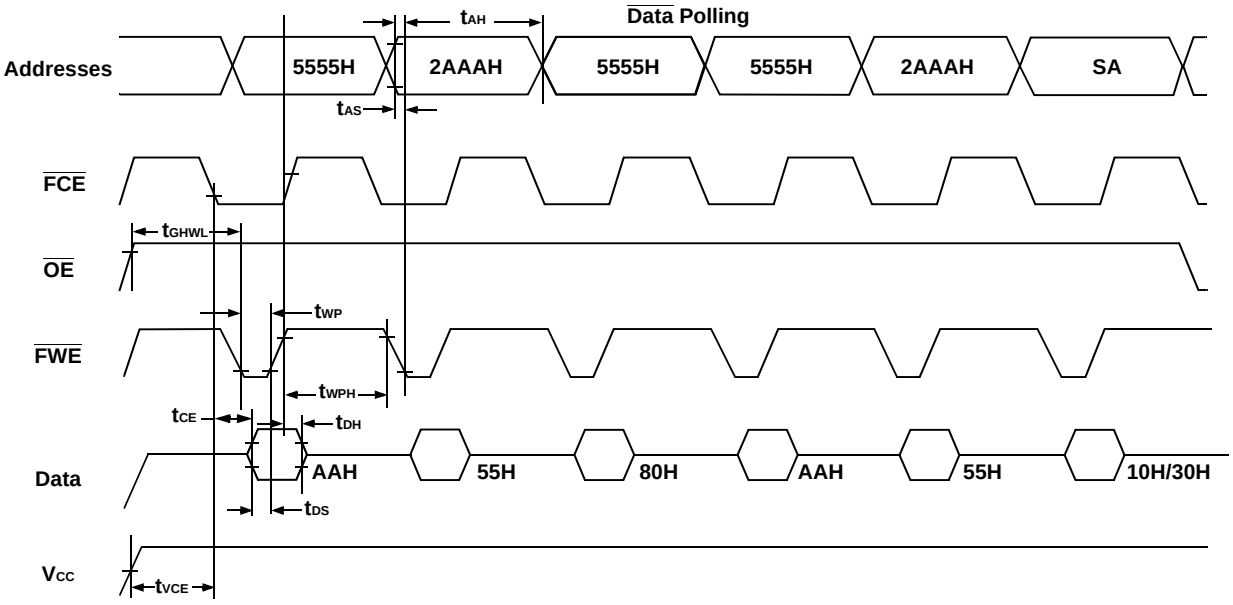


Write/Erase/Program Operation for Flash Memory, FWE Controlled



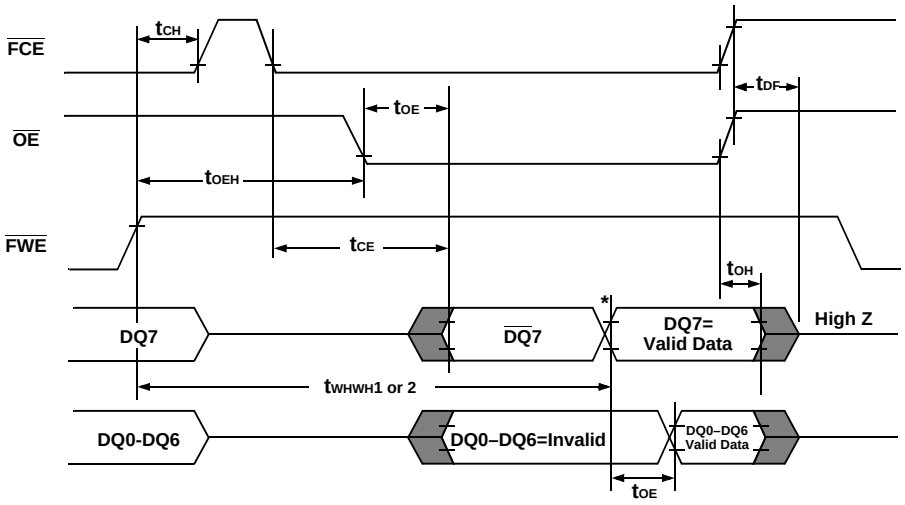
Notes:
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D7 is the 0utput of the complement of the data written to the deviced.
4. Dout is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

AC Waveforms Chip/Sector Erase Operations for Flash Memory



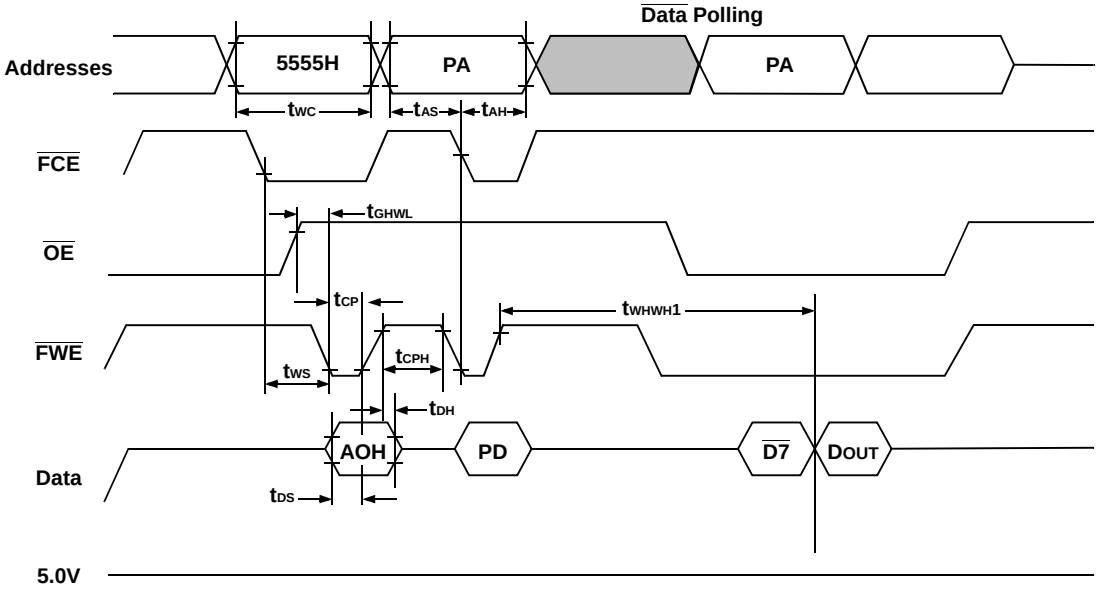
Notes:
1. SA is the sector address for sector erase.

AC Waveforms for Data Polling During Embedded Algorithm Operations for Flash Memory



** DQ7=Valid Data (The device has completed the Embedded operation).*

Write/Erase/Program Operation for Flash Memory, $\overline{FCE}$ Controlled

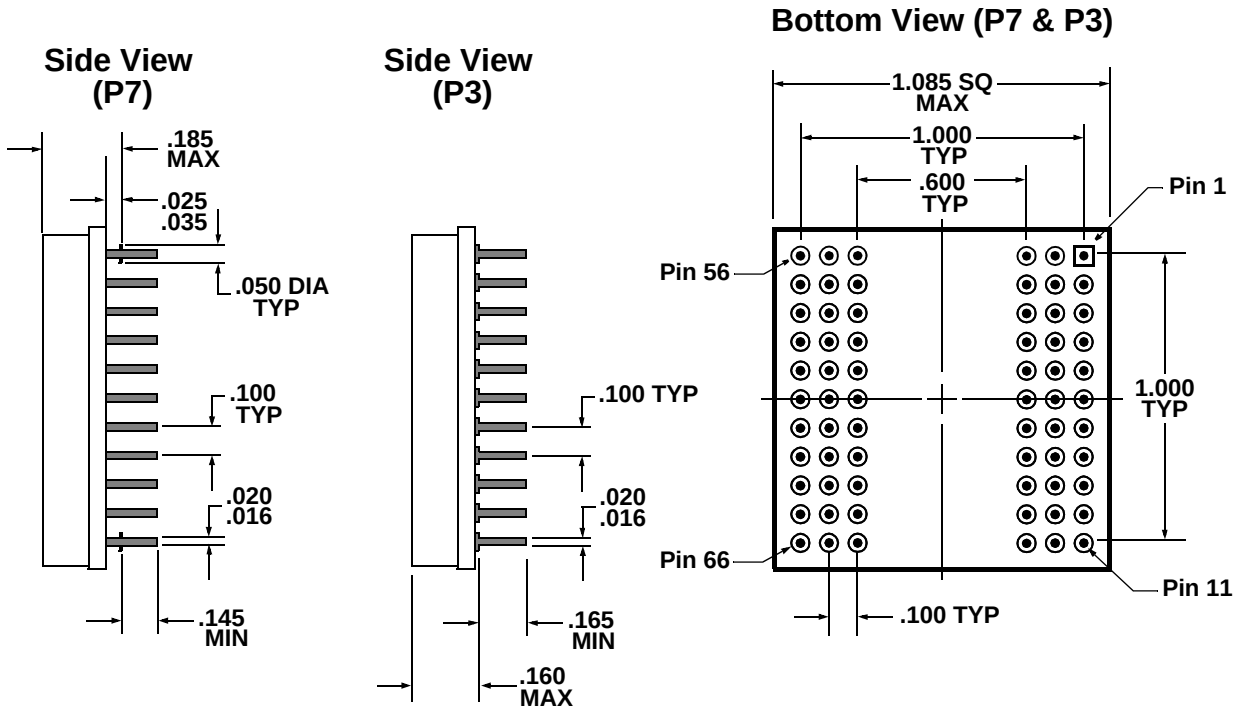


Notes:
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. $\overline{D7}$ is the 0utput of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

Pin Numbers & Functions

66 Pins — PGA-Type							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	I/O_8	18	A_{15}	35	I/O_{25}	52	$\overline{FWE}_3$
2	I/O_9	19	Vcc	36	I/O_{26}	53	$\overline{SWE}_3$
3	I/O_{10}	20	$\overline{FCE}$	37	A_7	54	GND
4	A_{14}	21	$\overline{SCE}$	38	A_{12}	55	I/O_{19}
5	A_{16}	22	I/O_3	39	$\overline{SWE}_1$	56	I/O_{31}
6	A_{11}	23	I/O_{15}	40	A_{13}	57	I/O_{30}
7	A_0	24	I/O_{14}	41	A_8	58	I/O_{29}
8	NC	25	I/O_{13}	42	I/O_{16}	59	I/O_{28}
9	I/O_0	26	I/O_{12}	43	I/O_{17}	60	A_1
10	I/O_1	27	$\overline{OE}$	44	I/O_{18}	61	A_2
11	I/O_2	28	NC	45	V_{CC}	62	A_3
12	$\overline{FWE}_2$	29	$\overline{FWE}_1$	46	$\overline{SWE}_4$	63	I/O_{23}
13	$\overline{SCE}_2$	30	I/O_7	47	$\overline{FWE}_4$	64	I/O_{22}
14	GND	31	I/O_6	48	I/O_{27}	65	I/O_{21}
15	I/O_{11}	32	I/O_5	49	A_4	66	I/O_{20}
16	A_{10}	33	I/O_4	50	A_5		
17	A_9	34	I/O_{24}	51	A_6		

"P3" — 1.08" SQ PGA Type Package Standard (without shoulders)
"P7" — 1.08" SQ PGA Type Package (with shoulders on Pins 1, 11, 56 & 66)



All dimensions in inches

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Ordering Information

Model Number	DESC Part Number	Speed	Package
ACT-SF128K32N–26P1X	TBD	25(S) / 60(F) ns	1.08"sq PGA-Type
ACT-SF128K32N–37P1X	TBD	35(S) / 70(F) ns	1.08"sq PGA-Type
ACT-SF128K32N–39P1X	TBD	35(S) / 90(F) ns	1.08"sq PGA-Type

Note: (S) = Speed for SRAM, (F) = Speed for FLASH

Part Number Breakdown

ACT– SF 128K 32 N– 26 P1 M

Aeroflex Circuit Technology

Memory Type
SF = SRAM Flash Combo Module

Memory Depth, Locations

Memory Width, Bits

Pinout Options
N = none

Memory Speed (Code)
26 = 25ns SRAM / 60ns FLASH
37 = 35ns SRAM / 70ns FLASH
39 = 35ns SRAM / 90ns FLASH

Screening
C = Commercial Temp, 0°C to +70°C
I = Industrial Temp, -40°C to +85°C
T = Military Temp, -55°C to +125°C
M = Military Temp, -55°C to +125°C Screened *
Q = MIL-PRF-38534 Compliant/SMD

Package Types & Sizes

Thru-Hole Packages
P3 = 1.08"SQ PGA 66 Pins WO/Shoulder
P7 = 1.08"SQ PGA 66 Pins W/Shoulder

* **Screened to the individual test methods of MIL-STD-883**

Specifications subject to change without notice.

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