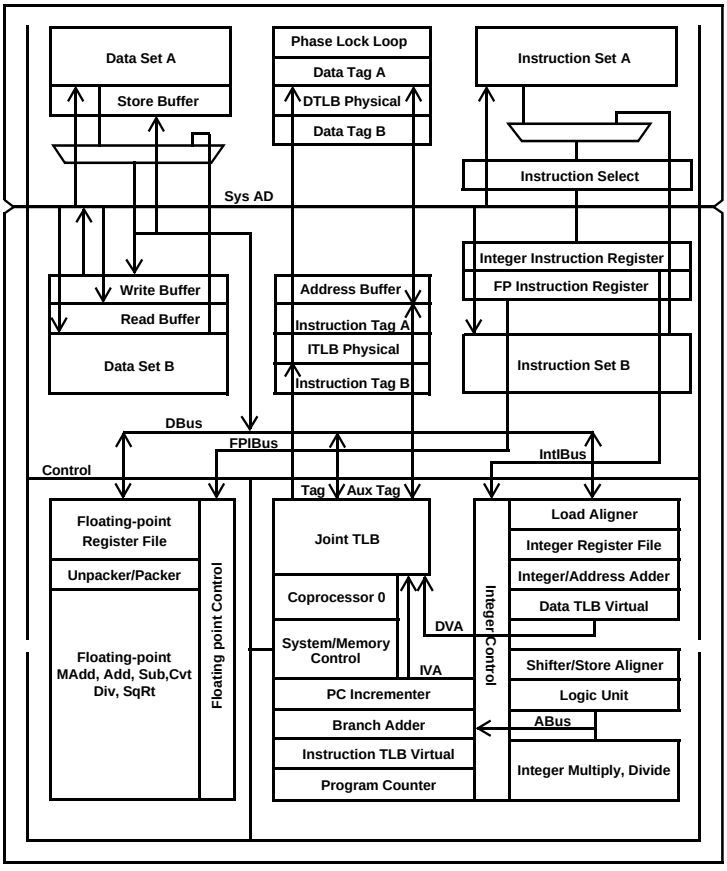
ACT5260
64-Bit Superscaler Microprocessor

Features

- Full militarized QED RM5260 microprocessor
- Dual Issue superscalar QED RISCMark™ - can issue one integer and one floating-point instruction per cycle microprocessor - can issue one integer and one floating-point instruction per cycle
  - 100, 133 and 150MHz frequency (200MHz future option) Consult Factory for latest speeds
  - 260 Dhrystone2.1 MIPS
  - SPECInt95 4.8. SPECfp95 5.1
- High performance system interface compatible with R4600, R4700 and R5000
  - 64-bit multiplexed system address/data bus for optimum price/performance up to 100 MHz operating frequency
  - High performance write protocols maximize uncached write bandwidth
  - Operates at input system clock multipliers of 2 through 8
  - 5V tolerant I/O's
  - IEEE 1149.1 JTAG boundary scan
- Integrated on-chip caches - up to 3.2GBps internal data rate
  - 16KB instruction - 2 way set associative
  - 16KB data - 2 way set associative
  - Virtually indexed, physically tagged
  - Write-back and write-through on per page basis
  - Pipeline restart on first double for data cache misses
- Integrated memory management unit
  - Fully associative joint TLB (shared by I and D translations)
  - 48 dual entries map 96 pages
  - Variable page size (4KB to 16MB in 4x increments)
- Embedded supply de-coupling capacitors and Pll filter components
- High-performance floating point unit - up to 400 MFLOPS
  - Single cycle repeat rate for common single precision operations and some double precision operations
  - Two cycle repeat rate for double precision multiply and double precision combined multiply-add operations
  - Single cycle repeat rate for single precision combined multiply-add operation
- MIPS IV instruction set
  - Floating point multiply-add instruction increases performance in signal processing and graphics applications
  - Conditional moves to reduce branch frequency
  - Index address modes (register + register)
- Embedded application enhancements
  - Specialized DSP integer Multiply-Accumulate instruction and 3 operand multiply instruction
  - I and D cache locking by set
  - Optional dedicated exception vector for interrupts
- Fully static CMOS design with power down logic
  - Standby reduced power mode with WAIT instruction
  - 5 Watts typical at 3.3V, less than 175 mwatts in Standby
- 208-lead CQFP, cavity-up package (F17)
- 208-lead CQFP, inverted footprint (F24), Intended to duplicate the commercial QED footprint *(Consult Factory)*
- 179-pin PGA package (*Future Product*) (P10)

BLOCK DIAGRAM



DESCRIPTION:

The ACT5260 is a highly integrated superscalar microprocessor that implements a superset of the MIPS IV Instruction Set Architecture(ISA). It has a high performance 64-bit integer unit, a high throughput, fully pipelined 64-bit floating point unit, an operating system friendly memory management unit with a 48-entry fully associative TLB, a 16 KByte 2-way set associative instruction cache, a 16 KByte 2-way set associative data cache, and a high-performance 64-bit system interface. The ACT5260 can issue both an integer and a floating point instruction in the same cycle.

The ACT5260 is ideally suited for high-end embedded control applications such as internetworking, high performance image manipulation, high speed printing, and 3-D visualization.

HARDWARE OVERVIEW

The ACT5260 offers a high-level of integration targeted at high-performance embedded applications. Some of the key elements of the ACT5260 are briefly described below.

Superscalar Dispatch

The ACT5260 has an efficient asymmetric superscalar dispatch unit which allows it to issue an integer instruction and a floating-point computation instruction simultaneously. With respect to superscalar issue, integer instructions include alu, branch, load/store, and floating-point load/store, while floating-point computation instructions include floating-point add, subtract, combined multiply-add, converts, etc. In combination with its high throughput fully pipelined floating-point execution unit, the superscalar capability of the ACT5260 provides unparalleled price/performance in computationally intensive embedded applications.

CPU Registers

Like all MIPS ISA processors, the ACT5260 CPU has a simple, clean user visible state consisting of 32 general purpose registers, two special purpose registers for integer multiplication and division, a program counter, and no condition code bits.

Pipeline

For integer operations, loads, stores, and other non-floating-point operations, the ACT5260 uses the simple 5-stage pipeline also found in the circuits R4600, R4700, and R5000. In addition to this standard pipeline, the ACT5260 uses an extended seven stage pipeline for floating-point operations. Like the R5000, the ACT5260 does virtual to physical translation in parallel with cache access.

Integer Unit

Like the R5000, the ACT5260 implements the MIPS IV Instruction Set Architecture, and is therefore fully upward compatible with applications that run on processors implementing the earlier generation MIPS I-III instruction sets. Additionally, the ACT5260 includes two implementation specific instructions not found in the baseline MIPS IV ISA but that are useful in the embedded market place. Described in detail in the QED RM5260 datasheet, these instructions are integer multiply-accumulate and 3-operand integer multiply.

The ACT5260 integer unit includes thirty-two general purpose 64-bit registers, a load/store architecture with single cycle ALU operations (add, sub, logical, shift) and an autonomous multiply/divide unit. Additional register resources include: the HI/LO result registers for the two-operand integer multiply/ divide operations, and the program counter(PC).

Register File

The ACT5260 has thirty-two general purpose registers with register location 0 hard wired to zero. These registers are used for scalar integer operations and address calculation. The register file has two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

ALU

The ACT5260 ALU consists of the integer adder/ subtractor, the logic unit, and the shifter. The adder performs address calculations in addition to arithmetic operations, the logic unit performs all logical and zero shift data moves, and the shifter performs shifts and store alignment operations. Each of these units is optimized to perform all operations in a single processor cycle

For additional Detail Information regarding the operation of the Quantum Effect Design (QED) RISCMark™ RM5260™, 64-Bit Superscalar Microprocessor see the latest QED datasheet (Revision 1.1 July 1998).

Absolute Maximum Ratings[1]

Symbol	Rating	Range	Units
V_{TERM}	Terminal Voltage with respect to GND	-0.5[2] to 4.6	V
Tc	Operating Temperature	-55 to +125	°C
T_{BIAS}	Case Temperature under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{IN}	DC Input Current	20[3]	mA
I_{OUT}	DC Output Current	50	mA

Notes:
1. Stresses above those listed under "AbsoluteMaximums Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. VIN minimum = -2.0V for pulse width less than 15nS. VIN maximum should not exceed +5.5 Volts.
3. When VIN < 0V or VIN > Vcc.
4. No more than one output should be shorted at one time. Duration of the short should not exceed more than 30 second.

Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CC}	Power Supply Voltage	+3.135	+3.465	V
V_{IH}	Input High Voltage	$0.7V_{CC}$	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage	-0.5	$0.2V_{CC}$	V
T_C	Operating Temperature Case	-55	+125	°C
	For 133MHz Parts only	-40	+125	°C

DC Characteristics

(VCC = 3.3V ±5%; 133MHz parts: Tc =-40°C to +125°C, All other parts Tc =-55°C to +125°C)

Parameter	Sym	Conditions	100 / 133 / 150MHz		Units
			Min	Max	
Output Low Voltage	V_{OL1}	I_{OL} = 20 µA	-	0.1	V
Output High Voltage	V_{OH1}	I_{OL} = 20 µA	Vcc - 0.1	-	V
Output Low Voltage	V_{OL2}	I_{OL} = 4 mA	-	0.4	V
Output High Voltage	V_{OH2}	I_{OL} = 4 mA	2.4	-	V
Input High Voltage	V_{IH}		$0.7V_{CC}$	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}		-0.5	$0.2V_{CC}$	V
Input Current	I_{IN1}	V_{IN} = 0V	-20	+20	µA
Input Current	I_{IN2}	V_{IN} = V_{CC}	-20	+20	µA
Input Current	I_{IN3}	V_{IN} = 5.5V	-250	+250	µA
Input Capacitance	C_{IN}		-	10	pF
Output Capacitance	C_{OUT}		-	10	pF

Power Consumption

Parameter	Symbol	Conditions	100MHz, 3.3V		133MHz, 3.3V		150MHz, 3.3V		Units
			Typ[5]	Max	Typ[5]	Max	Typ[5]	Max	
Active Operating Supply Current	I_{CC1}	C_L = 0pF, No SysAD activity	800	1550	800	1550	1000	1750	mA
	I_{CC2}	C_L = 50pF, R4000 write protocol without FPU operation	1000	1750	1000	1750	1150	1950	mA
	I_{CC3}	C_L = 50pF, write re-issue or pipelined writes	1100	2000	1100	2000	1250	2250	mA
Standby Current	I_{SB1}	C_L = 0pF	75	150	75	150	100	175	mA
	I_{SB1}	C_L = 50pF	75	150	75	150	100	175	mA

Notes:
5. Typical integer instruction mix and cache miss rates.

AC Characteristics

(V_{CC} = 3.3V ±5%; 133MHz parts: Tc =-40°C to +125°C, All other parts Tc =-55°C to +125°C)

Capacitive Load Deration

Symbol	Parameter	100 / 133 / 150MHz		Units
		Minimum	Maximum	
C_{LD}	Load Derate	-	2	ns/25pF

Clock Parameters

Parameter	Symbol	Test Conditions	100/133/150MHz		Units
			Min	Max	
SysClock High	t_{SCHigh}	Transition ≤ 5ns	4	-	ns
SysClock Low	t_{SCLow}	Transition ≤ 5ns	4	-	ns
SysClock Frequency[6]			33	75	MHz
SysClock Period	t_{SCP}		-	30	ns
Clock Jitter for SysClock	$t_{JitterIn}$		-	±250	ps
SysClock Rise Time	t_{SCRise}		-	5	ns
SysClock Fall Time	t_{SCFall}		-	5	ns
ModeClock Period	$t_{ModeCKP}$		-	$256*t_{SCP}$	ns
JTAG Clock Period	$t_{JTAGCKP}$		-	$4*t_{SCP}$	ns

Notes:
6. Operation of the ACT5260 is only guaranteed with the Phase Loop enabled.

System Interface Parameters[7]

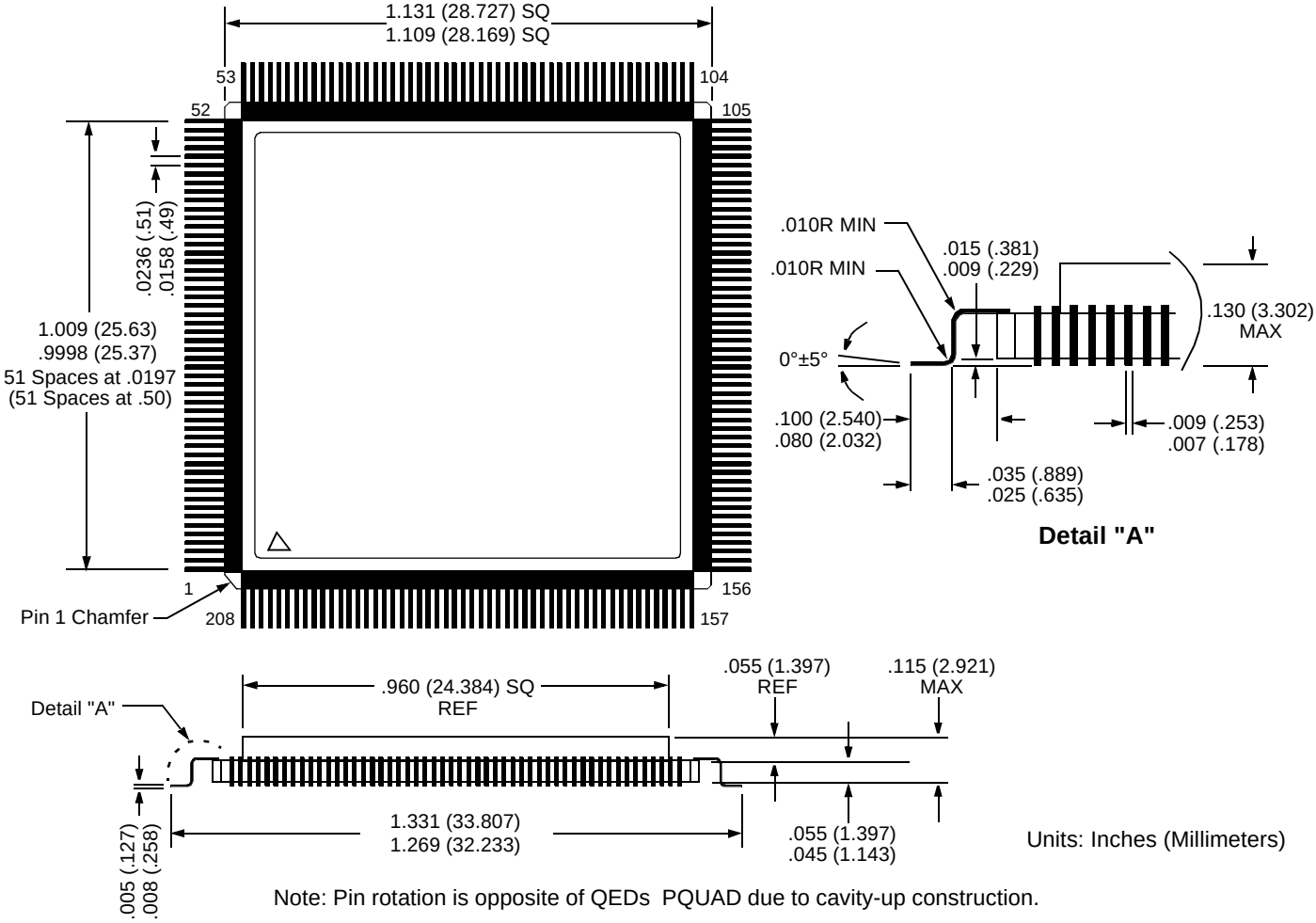
Parameter	Symbol	Test Conditions	100MHz		133MHz		150MHz		Units
			Min	Max	Min	Max	Min	Max	
Data Output[8]	t_{DO}	$mode_{14...13}$ = 10 (fastest)	1.0	7.0	1.0	7.0	1.0	7.0	ns
		$mode_{14...13}$ = 11	1.0	7.5	1.0	7.5	1.0	7.5	ns
		$mode_{14...13}$ = 00	1.0	8.0	1.0	8.0	1.0	8.0	ns
		$mode_{14...13}$ = 01 (slowest)	1.0	8.5	1.0	8.5	1.0	8.5	ns
Data Setup	t_{DS}	t_{RISE} = 5ns	5.0	-	5.0	-	5.0	-	ns
Data Hold	t_{DH}	t_{FALL}= 5ns	2.0	-	2.0	-	2.0	-	ns

Notes: -
7. Timmings are are measured from from 1.5V of the clock to 1.5V of the signal.
8. Capacitive load for all output timing is 50pF.

Boot Time Interface Parameters

Parameter	Symbol	Test Conditions	100/133/150MHz		Units
			Min	Max	
Mode Data Setup	t_{DS}		4	-	SysClock cycles
Mode Data Hold	t_{DH}		0	-	SysClock cycles

Package Information – "F17" – CQFP 208 Leads

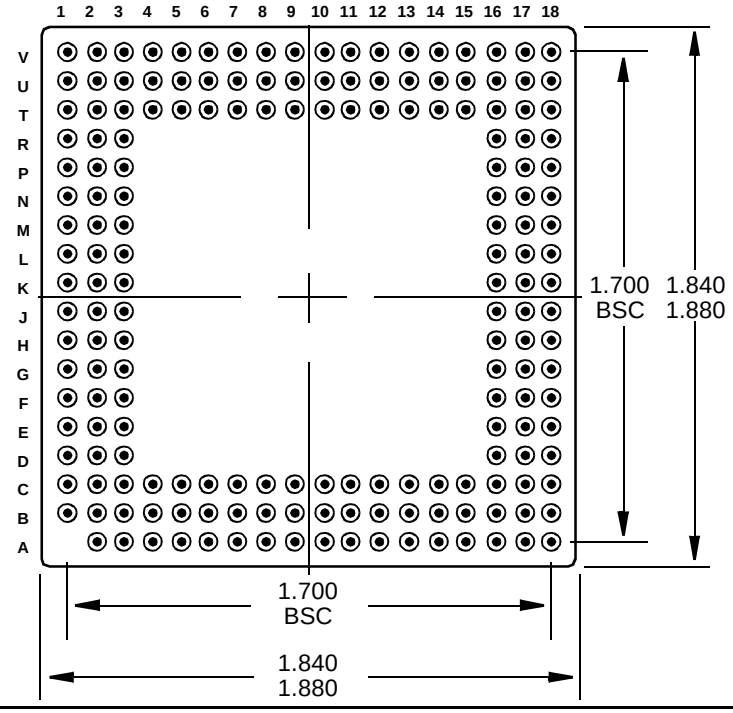


Units: Inches (Millimeters)

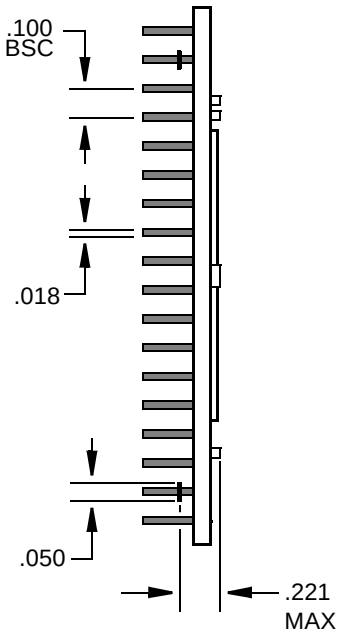
Note: Pin rotation is opposite of QEDs PQUAD due to cavity-up construction.

Future Package – "P10" – PGA 179 Pins *(Advanced)*

Bottom View



Side View



ACT5260 Microprocessor CQFP Pinouts – "F17"

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	Vcc (3.3V)	53	NC	105	Vcc (3.3V)	157	NC
2	NC	54	NC	106	NMI*	158	NC
3	NC	55	NC	107	ExtRqst*	159	NC
4	Vcc (3.3V)	56	Vcc (3.3V)	108	Reset*	160	NC
5	Vss	57	Vss	109	ColdReset*	161	Vcc (3.3V)
6	SysAD4	58	ModeIn	110	VccOK	162	Vss
7	SysAD36	59	RdRdy*	111	BigEndian	163	SysAD28
8	SysAD5	60	WrRdy*	112	Vcc (3.3V)	164	SysAD60
9	SysAD37	61	ValidIn*	113	Vss	165	SysAD29
10	Vcc (3.3V)	62	ValidOut*	114	SysAD16	166	SysAD61
11	Vss	63	Release*	115	SysAD48	167	Vcc (3.3V)
12	SysAD6	64	VccP	116	Vcc (3.3V)	168	Vss
13	SysAD38	65	VssP	117	Vss	169	SysAD30
14	Vcc (3.3V)	66	SysClock	118	SysAD17	170	SysAD62
15	Vss	67	Vcc (3.3V)	119	SysAD49	171	Vcc (3.3V)
16	SysAD7	68	Vss	120	SysAD18	172	Vss
17	SysAD39	69	Vcc (3.3V)	121	SysAD50	173	SysAD31
18	SysAD8	70	Vss	122	Vcc (3.3V)	174	SysAD63
19	SysAD40	71	Vcc (3.3V)	123	Vss	175	SysADC2
20	Vcc (3.3V)	72	Vss	124	SysAD19	176	SysADC6
21	Vss	73	SysCmd0	125	SysAD51	177	Vcc (3.3V)
22	SysAD9	74	SysCmd1	126	Vcc (3.3V)	178	Vss
23	SysAD41	75	SysCmd2	127	Vss	179	SysADC3
24	Vcc (3.3V)	76	SysCmd3	128	SysAD20	180	SysADC7
25	Vss	77	Vcc (3.3V)	129	SysAD52	181	Vcc (3.3V)
26	SysAD10	78	Vss	130	SysAD21	182	Vss
27	SysAD42	79	SysCmd4	131	SysAD53	183	SysADC0
28	SysAD11	80	SysCmd5	132	Vcc (3.3V)	184	SysADC4
29	SysAD43	81	Vcc (3.3V)	133	Vss	185	Vcc (3.3V)
30	Vcc (3.3V)	82	Vss	134	SysAD22	186	Vss
31	Vss	83	SysCmd6	135	SysAD54	187	SysADC1
32	SysAD12	84	SysCmd7	136	Vcc (3.3V)	188	SysADC5
33	SysAD44	85	SysCmd8	137	Vss	189	SysAD0
34	Vcc (3.3V)	86	SysCmdP	138	SysAD23	190	SysAD32
35	Vss	87	Vcc (3.3V)	139	SysAD55	191	Vcc (3.3V)
36	SysAD13	88	Vss	140	SysAD24	192	Vss
37	SysAD45	89	Vcc (3.3V)	141	SysAD56	193	SysAD1
38	SysAD14	90	Vss	142	Vcc (3.3V)	194	SysAD33
39	SysAD46	91	Vcc (3.3V)	143	Vss	195	Vcc (3.3V)
40	Vcc (3.3V)	92	Vss	144	SysAD25	196	Vss
41	Vss	93	Int0*	145	SysAD57	197	SysAD2
42	SysAD15	94	Int1*	146	Vcc (3.3V)	198	SysAD34
43	SysAD47	95	Int2*	147	Vss	199	SysAD3
44	Vcc (3.3V)	96	Int3*	148	SysAD26	200	SysAD35
45	Vss	97	Int4*	149	SysAD58	201	Vcc (3.3V)
46	ModeClock	98	Int5*	150	SysAD27	202	Vss
47	JTDO	99	Vcc (3.3V)	151	SysAD59	203	NC
48	JTDI	100	Vss	152	Vcc (3.3V)	204	NC
49	JTCK	101	NC	153	Vss	205	NC
50	JTMS	102	NC	154	NC	206	NC
51	Vcc (3.3V)	103	NC	155	NC	207	Vcc (3.3V)
52	Vss	104	NC	156	Vss	208	Vss

AEROFLEX
CIRCUIT TECHNOLOGY

Ordering Information

Part Number	Screening	Speed (MHz)	Package
ACT-5260PC-100F17C	Commercial Temperature (0°C to +70°C)	100	208 Lead CQFP
ACT-5260PC-133F17C	Commercial Temperature (0°C to +70°C)	133	208 Lead CQFP
ACT-5260PC-150F17C	Commercial Temperature (0°C to +70°C)	150	208 Lead CQFP
ACT-5260PC-100F17I	Industrial Temperature (-40°C to +85°C)	100	208 Lead CQFP
ACT-5260PC-133F17I	Industrial Temperature (-40°C to +85°C)	133	208 Lead CQFP
ACT-5260PC-150F17I	Industrial Temperature (-40°C to +85°C)	150	208 Lead CQFP
ACT-5260PC-100F17T	Military Temperature (-55°C to +125°C)	100	208 Lead CQFP
ACT-5260PC-133F17T	Reduced Military Temperature (-40°C to +125°C)	133	208 Lead CQFP
ACT-5260PC-150F17T	Military Temperature (-55°C to +125°C)	150	208 Lead CQFP
ACT-5260PC-100F17M	Military Temperature, Screened* (-55°C to +125°C)	100	208 Lead CQFP
ACT-5260PC-133F17M	Reduced Military Temperature, Screened* (-40°C to +125°C)	133	208 Lead CQFP
ACT-5260PC-150F17M	Military Temperature, Screened* (-55°C to +125°C)	150	208 Lead CQFP

Part Number Breakdown

ACT– 5260 PC – 100 F17 M

Aeroflex Circuit Technology

Base Processor Type

Cache Style

PC = Primary Cache

Maximum Pipeline Freq.

100 = 100MHz
133 = 133MHz (Screening: T & M -40°C to +125°C only)
150 = 150MHz
200 = 200MHZ (Future option)

Screening

C = Commercial Temp, 0°C to +70°C
I = Industrial Temp, -40°C to +85°C
T = Military Temp, -55°C to +125°C
M = Military Temp, -55°C to +125°C, Screened *
Q = MIL-PRF-38534 Compliant/SMD if applicable

Package Type & Size

Surface Mount Package

F17 = 1.120" SQ 208 Lead CQFP
F24 = 1.120" SQ Inverted 208 Lead CQFP
(Consult Factory)

Thru-Hole Package

P10 = 1.86"SQ PGA 179 pins with shoulder
Future Product

*** Screened to the individual test methods of MIL-STD-883**

Specifications subject to change without notice.

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