ACS70310

Very High Precision, Programmable Linear Hall-Effect Sensor IC
with Reverse Battery Protection and High-Bandwidth (240 kHz) Analog Output for Core-Based Current Sensing

FEATURES AND BENEFITS

- Factory-programmed segmented linear temperature compensation (TC) provides ultralow thermal drift
  - □ Sensitivity ±1%
  - □ Offset ±5 mV
- On-board supply regulator with reverse-battery protection provides high immunity to Electrical Overstress (EOS)
- Very fast response time (2 µs)
- High operating bandwidth: DC to 240 kHz
- AEC-Q100 Grade 0, automotive qualified
- Customer-programmable, high-resolution offset, and sensitivity trim

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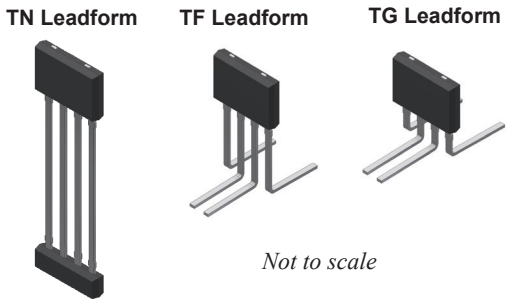
PACKAGE: 4-pin SIP (suffix KT)



Not to scale

DESCRIPTION

The Allegro ACS70310 IC incorporates a Hall element with BiCMOS integrated circuitry to provide a fully monolithic linear current sensor IC. The IC is sensitive to magnetic flux density orthogonal to the IC package surface and the output is an analog voltage proportional to the applied flux density. The ACS70310 is designed to be used in conjunction with a ferromagnetic core to provide highly accurate current sensing. The gain and offset drift over temperature is factory programmed at Allegro and delivers a solution with 1% sensitivity and 5 mV offset error from 25°C to 150°C.

The ACS70310 is customer programmable. The absolute value of gain and offset can be programmed after manufacturing to provide customers industry-leading current sensor accuracy. The sensor has a high operating bandwidth from DC to 240 kHz and a fast 2 µs response time. It is ideal for use in high frequency automotive inverters and DC/DC converters where fast switching is required.

Broken ground wire detection, clamps, power-on reset, and overvoltage detection provide the required diagnostics for safety-critical automotive applications.

The on-board supply regulator enables the supply pin to survive voltages of ±18 V and the output pin to survive voltages of +16 to –6 V for added robustness in the harsh automotive

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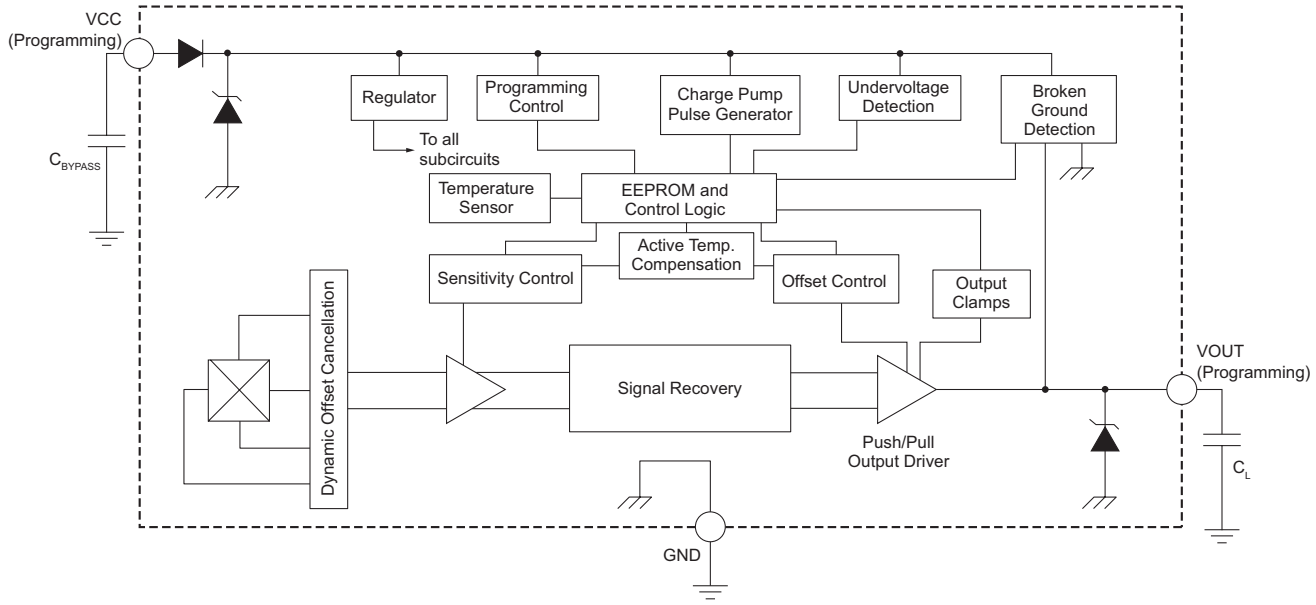


Figure 1: Functional Block Diagram

FEATURES AND BENEFITS (continued)

- Extremely low noise and high resolution achieved via proprietary Hall element and low-noise amplifier circuits
- Patented circuits suppress IC output spiking during fast current step inputs
- Wide selectable sensitivity range between 0.5 and 11.5 mV/G
- User-selectable ratiometric behavior of sensitivity, quiescent voltage, and clamps (ratiometry can be disabled), for simple interface with application A-to-D converter (ADC)
- Precise recoverability after temperature cycling
- Open circuit detection on ground pin (broken wire)
- Customer programmable Output Voltage Clamps provide short-circuit diagnostic capabilities
- Wide ambient temperature range: –40°C to 150°C
- Immune to mechanical stress
- Extremely thin package: 1 mm case thickness

DESCRIPTION (continued)

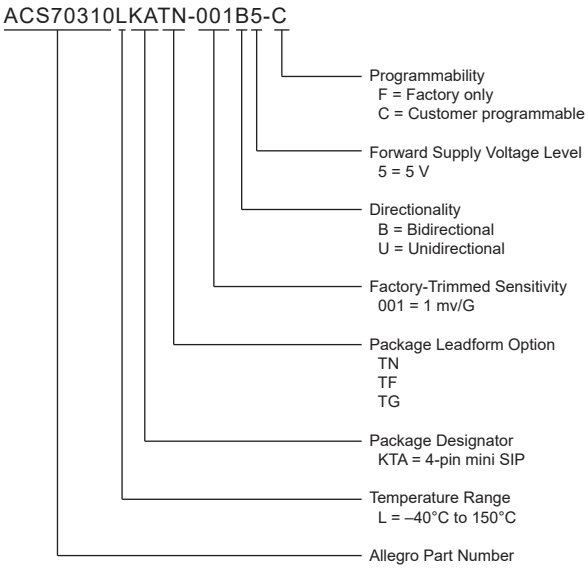
environment.

Device parameters are specified across an extended ambient automotive temperature range: –40°C to 150°C. The ACS70310 sensor IC is provided in an extremely thin case (1 mm thick), 4-pin SIP (single in-line package, suffix KT) that is lead (Pb) free, with 100% matte-tin leadframe plating.

SELECTION GUIDE

Part Number [1]	Factory-Programmed Sensitivity (mV/G)	Programmable Sens Range (mV/G)	T_A (°C)	Package [2]	Packing [3]
ACS70310LKTATN-001B5-C	1	0.5 to 1.2	–40 to 150	4-pin SIP, TN leadform	4000 pieces per 13-inch reel
ACS70310LKTATN-2P5B5-C	2.5	1.2 to 2.5			
ACS70310LKTATN-005B5-C	5	2.5 to 5.5			
ACS70310LKTATN-010B5-C	10	5.5 to 11.5			

[1] Characteristics are guaranteed within the sense programmable range of the corresponding part number.
[2] TN, TG and TF package leadform options available.
[3] Contact Allegro for additional packing options.



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ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		18	V
Reverse Supply Voltage	V_{RCC}	$T_{J(max)}$ should not be exceeded	–18	V
Forward Output Voltage	V_{OUT}	$V_{OUT} < V_{CC} + 2$ V	16	V
Reverse Output Voltage	V_{ROUT}	Difference between V_{CC} and output should not exceed 20 V	–6	V
Output Current	I_{OUT}	Maximum survivable sink or source current on the output	10	mA
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	°C
Storage Temperature	T_{stg}		–65 to 165	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions [2]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 1-layer PCB with exposed copper limited to solder pads	174	°C/W

[2] Additional thermal information available on the Allegro website

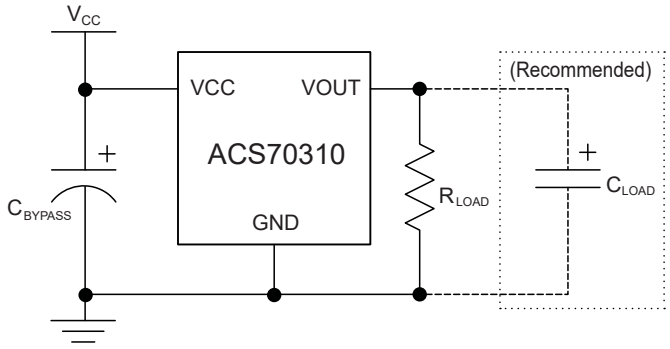
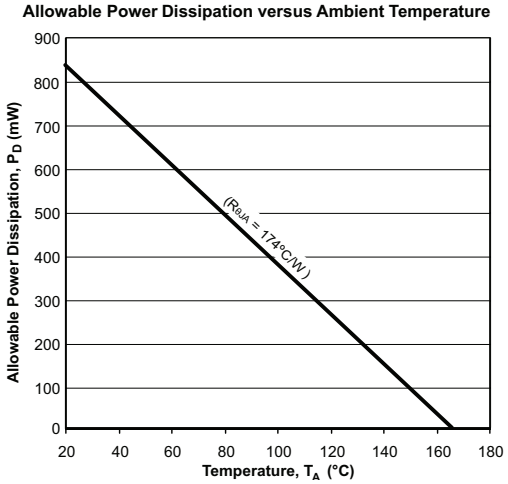


Figure 2: Typical Application Drawing



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PINOUT DIAGRAM AND TERMINAL LIST TABLE

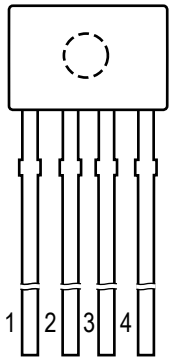

Figure 3: KT Package Pinout Diagram

(Ejector pin mark on opposite side)

Terminal List Table

Number	Name	Function
1	VCC	Input Power Supply; also used for programming
2	VOUT	Output Signal, also used for programming
3	NC/GND	Connect to GND for optimal ESD performance
4	GND	Ground

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OPERATING CHARACTERISTICS: Valid over full operating temperature range of T_A, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		4.5	5	5.5	V
Supply Current	I_{CC}	No load on VOUT; V_{CC} @ 4.5, 5, and 5.5 V	–	13	15	mA
Power-On Reset Voltage	$V_{POR(H)}$	T_A = 25°C, V_{CC} rising	3.7	3.9	4.3	V
	$V_{POR(L)}$	T_A = 25°C, V_{CC} falling	3.2	3.4	3.75	V
Power-On Reset Hysteresis	$V_{POR(HYS)}$	T_A = 25°C	440	500	560	mV
Power-On Reset Release Time	$t_{POR(R)}$	T_A = 25°C, V_{CC} rising	–	32	–	µs
Power-On Delay Time	t_{PO}	T_A = 25°C, C_{BYPASS} = open, C_L = 1 nF	–	80	–	µs
Temperature Compensation Power-On Time	t_{TC}	T_A = 150°C, C_{BYPASS} = open, C_L = 1 nF, Sens = 1 and 10 mV/G	–	146	–	µs
Supply Zener Clamp Voltage	V_z	T_A = 25°C, I_{CC} = 30 mA	18	20	–	V
OUTPUT CHARACTERISTICS						
DC Output Resistance	R_{OUT}	T_A = 25°C	2	4	8	Ω
Output Load Resistance [1]	R_L	VOUT to GND or VCC	4.7	10	–	kΩ
Output Load Capacitance	C_L	VOUT to GND	–	–	5	nF
Output Voltage Saturation	$V_{OUT(SATH)}$	T_A = 25°C, R_L = 10 kΩ to GND, Bias = 400 G	4.75	4.8	–	V
	$V_{OUT(SATL)}$	T_A = 25°C, R_L = 10 kΩ to VCC, Bias = 400 G	–	0.2	0.25	V
Output Voltage Clamp	$V_{CLP(HIGH)}$	T_A = 25°C, R_L = 10 kΩ to GND, Bias = 400 G	4.65	4.7	4.75	V
	$V_{CLP(LOW)}$	T_A = 25°C, R_L = 10 kΩ to VCC, Bias = 400 G	0.25	0.3	0.36	V
Output Voltage with Broken GND	V_{BRK_DN}	T_A = 25°C, R_L = 10 kΩ to GND, Pin 3 = NC	0	100	200	mV
	V_{BRK_UP}	T_A = 25°C, R_L = 10 kΩ to VCC (5 V), Pin 3 = NC	4.8	4.9	5	V
Overvoltage Detection [2]	$V_{OVD(EN)}$	T_A = 25°C	–	6.5	–	V
	$V_{OVD(DIS)}$	T_A = 25°C	–	6	–	V
Noise	V_{IN}	T_A = 25°C, C_L = 1 nF, Sens = 5 mV/G	–	1.4	–	mG/√(Hz)
	V_{ON}	T_A = 25°C, Sens = 5 mV/G	–	3.5	–	mV_{RMS}
Propagation Delay Time	t_{pd}	T_A = 25°C, 0.5 Fullscale = 1 V/(t < 750 ns), C_L = 0 nF, no R_L	–	1.2	1.65	µs
Response Time	$t_{RESPONSE}$	T_A = 25°C, 0.5 Fullscale = 1 V/(t < 750 ns), C_L = 0 nF, no R_L	–	2.1	3	µs
Rise Time	t_r	T_A = 25°C, 0.5 Fullscale = 1 V/(t < 750 ns), C_L = 0 nF, no R_L	–	1.9	–	µs
Output Slew Rate	SR	T_A = 25°C, 0.5 Fullscale = 1 V/(t < 750 ns), C_L = 0 nF, no R_L	410	480	550	V/ms
Internal Bandwidth	BW_i	Small signal –3 dB, C_L = 1 nF, T_A = 25°C; Sens = 10 mV/G	–	240	–	kHz

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OPERATING CHARACTERISTICS (continued): Valid over full operating temperature range of T_A, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
QUIESCENT OUTPUT VOLTAGE ($V_{OUT(Q)}$)						
Number of Fine QVO Programming Bits	QVO_FINE		–	9	–	bit
Quiescent Output Voltage [3]	$V_{OUT(QU)}$	Unidirectional, T_A = 25°C	0.495	0.5	0.505	V
	$V_{OUT(QBI)}$	Bidirectional, T_A = 25°C	2.495	2.5	2.505	V
Average Quiescent Voltage Output Programming Step Size [4]	$V_{OUT(Q)Step}$	T_A = 25°C	–	1.18	–	mV
Average Quiescent Voltage Output Temperature Compensation Step Size	$V_{OUT(Q)TCStep}$		–	$V_{OUT(Q)Step}$	–	mV
SENSITIVITY (Sens)						
Coarse Sensitivity Programming Bits [5]	SENS_COARSE	Readable by customer	–	2	–	bit
Fine Sensitivity Programming Bits	SENS_FINE		–	9	–	bit
Sensitivity Programming Range [6]	$Sens_{PR}$	SENS_COARSE = 0	0.5	–	1.2	mV/G
		SENS_COARSE = 1	1.2	–	2.5	mV/G
		SENS_COARSE = 2	2.5	–	5.5	mV/G
		SENS_COARSE = 3	5.5	–	11.5	mV/G
Average Sensitivity Programming Step Size	$Step_{SENS}$	SENS_COARSE = 0	–	2.87	–	µV/G
		SENS_COARSE = 1	–	6.06	–	µV/G
		SENS_COARSE = 2	–	13.06	–	µV/G
		SENS_COARSE = 3	–	27.1	–	µV/G
Average Sensitivity Temperature Compensation Step Size	$Step_{SENSTC}$	T_A = –40°C to 150°C	–	$Step_{SENS}$	–	µV/G
SENSITIVITY ERROR						
Factory Sensitivity Error	$Sens_{ERR}$	T_A = 25°C	–1	–	1	%
Sensitivity Drift Over Temperature	$\Delta Sens_{TC}$	T_A = 25°C to 150°C	–1	–	1	%
		T_A = –40°C to 25°C	–1.2	–	1.2	%
Sensitvity Non-Linearity Error [7]	Lin_{ERR}	Measured at 400 G (1, 2.5, and 5 mV/G) or 200 G (10 mV/G)	–0.5	–	0.5	%
Sensitivity Ratiometry Error	$Rat_{ERRSENS}$	V_{CC} = 4.85 to 5.15 V	–0.55	–	0.55	%
QUIESCENT VOLTAGE OUTPUT ERROR						
Factory Quiescent Voltage Output Error	V_{QVOERR}	T_A = 25°C	–5	–	5	mV
Quiescent Voltage Output Temperature Error	$V_{OUT(Q)TC}$	T_A = 25°C to 150°C	–5	–	5	mV
		T_A = –40°C to 25°C	–5	–	5	mV
Quiescent Voltage Output Ratiometry Error	$V_{RatERRVOUT(Q)}$	V_{CC} = 4.85 to 5.15 V	–5	–	5	mV
LIFETIME						
QVO Lifetime Drift	$V_{QVOLife}$	T_A = 25°C	–	0.8	–	mV
Sens Lifetime Drift	$Sens_{ERR_Life}$	T_A = 25°C	–	0.5	–	%

[1] Using small R_L will increase output error; this error scales with output causing offset and symmetry error, i.e. using a R_L = 4.7 kΩ will cause a 4 mV error due to the resistor divider between the $R_{L(pulldown)}$ and the internal resistance of 4 Ω at 5 V output. Keep this in mind when sizing R_L.
[2] Overvoltage Detection was characterized on the bench.
[3] Devices programed to the typical values are guaranteed to meet the $V_{OUT(Q)TC}$ spec.
[4] This is an average and actual step can vary. For best results, check QVO after every retrim. Refer to the Quiescent Voltage Output Programming Resolution in the definition section.
[5] Allegro guarantees limits of devices that remains within their factory programed SEN_COARSE and the corresponding $SENS_{PR}$ during customer programing.
[6] Device performance is guaranteed within these ranges.
[7] LinErr valid from 0 to ±2000 G, validated by characterization and design.

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CHARACTERISTIC DEFINITIONS

Power-On Time (t_{PO})

When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field.

Power-On Time (t_{PO}) is defined as: the time it takes for the output voltage to settle within ±10% of its steady-state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage ($V_{CC(min)}$) as shown in Figure 4.

Temperature Compensation Power-On Time (t_{TC})

After Power-On Time (t_{PO}) elapses, t_{TC} is also required before a valid temperature compensated output.

Propagation Delay (t_{pd})

The time interval between a) when the applied magnetic field reaches 20% of its final value, and b) when the output reaches 20% of its final value (see Figure 5).

Rise Time (t_r)

The time interval between a) when the sensor IC reaches 10% of its final value, and b) when it reaches 90% of its final value (see Figure 2).

Response Time ($t_{RESPONSE}$)

The time interval between a) when the applied magnetic field reaches 90% of its final value, and b) when the sensor reaches 90% of its output corresponding to the applied magnetic field (see Figure 6). The 90%-90% is also shown in the Electrical Characteristics table and in the performance data.

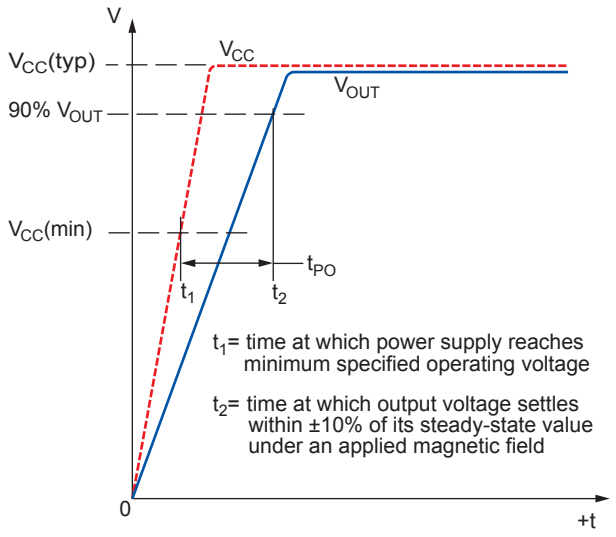

Figure 4: Power-On Time Definition

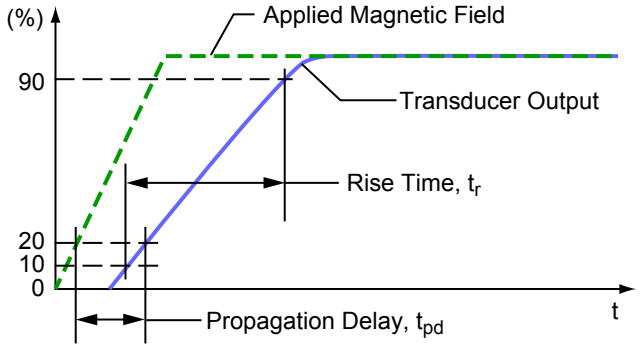

Figure 5: Propagation Delay and Rise Time Definitions

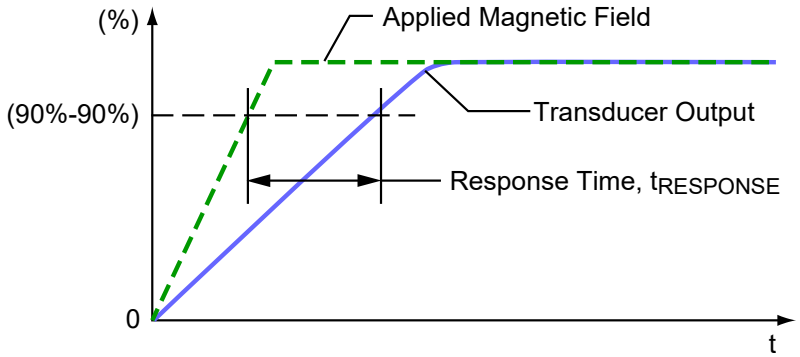

Figure 6: Response Time Definition

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Quiescent Voltage Output ($V_{OUT(QU/BI)}$)

In the quiescent state (no significant magnetic field: B = 0 G), the output ($V_{OUT(QU/BI)}$) has a constant ratio to the supply voltage (V_{CC}) throughout the entire operating ranges of V_{CC} and ambient temperature (T_A). *U* and *BI* correspond to unidirectional or bidirectional mode.

Before any programming, the Quiescent Voltage Output ($V_{OUT(Q)}$) has a nominal value of V_{CC} / 2 for a bidirectional device and 0.5 V for unidirectional parts with a V_{CC} of 5 V.

Quiescent Voltage Output Programming Range

The Quiescent Voltage Output ($V_{OUT(Q)}$) can be programmed within the Quiescent Voltage Output limits. Exceeding the specified Quiescent Voltage Output limits will cause Quiescent Voltage Output Drift Through Temperature Range ($\Delta V_{OUT(Q)TC}$) to deteriorate beyond the specified values.

Average Quiescent Voltage Output Programming Step Size ($Step_{VOUT(Q)}$)

The Average Quiescent Voltage Output Progamming Step Size ($Step_{VOUT(Q)}$) is determined using the following calculation:

$$V_{OUT(Q)Step} = \frac{V_{OUT(Q)maxcode} - V_{OUT(Q)mincode}}{2^n - 1}, \quad (1)$$

where *n* is the number of available programming bits in the trim range, 9 bits, $V_{OUT(Q)maxcode}$ is at decimal code 255, and $V_{OUT(Q)mincode}$ is at decimal code 256.

Quiescent Voltage Output Programming Resolution

The programming resolution for any device is half of its programming step size.

The step size of each bit can vary. For best accuracy, check V_{OUT} after every trim. The devices DAC performance is screened and accounted in the factory-standard trim, but becomes a possible source of error if the devices is reprogramed beyond the Quiescent Voltage Output; programming beyond this range causes $V_{OUT(Q)TC}$ to be invalid.

Quiescent Voltage Output Drift Through Temperature Range ($V_{OUT(Q)TC}$)

Due to internal component tolerances and thermal considerations, the Quiescent Voltage Output ($V_{OUT(Q)}$) may drift from its nominal value through the operating ambient temperature (T_A). The Quiescent Voltage Output Drift Through Temperature Range ($\Delta_{VOUT(Q)TC}$) is defined as:

$$D_{VOUT(Q)TC} = V_{OUT(Q)(TA)} - V_{OUT(Q)EXPECTED(TA)} \quad (2)$$

$\Delta V_{OUT(Q)TC}$ should be calculated using the actual measured values of $\Delta V_{OUT(Q)(TA)}$ and $\Delta V_{OUT(Q)EXPECTED(TA)}$ rather than programming target values.

Sensitivity (Sens)

The presence of a south polarity magnetic field, perpendicular to the branded surface of the package face, increases the output voltage from its quiescent value toward the supply voltage rail. The amount of the output voltage increase is proportional to the magnitude of the magnetic field applied.

Conversely, the application of a north polarity field decreases the output voltage from its quiescent value. This proportionality is specified as the magnetic sensitivity, Sens (mv/G), of the device, and it is defined as:

$$Sens = \frac{V_{OUT(BPOS)} - V_{OUT(BNEG)}}{BPOS - BNEG}, \quad (3)$$

where BPOS and BNEG are two magnetic fields with opposite polarities.

Initial Factory-Programmed Sensitivity

Before any programming, Sensitivity has a nominal value that depends on the SENS_COARSE bits setting. Each ACS70310 variant has a different SENS_COARSE setting. The parts TC performance is guaranteed if the SENS_COARSE bit is in its default factory value and within the Sensitivity Programing Range corresponding to the SENS_COARSE bit.

Sensitivity Programming Range ($Sens_{PR}$)

The magnetic sensitivity (Sens) can be programmed around its initial value within the sensitivity range limits: $Sens_{PR}$(min) and $Sens_{PR}$(max). Exceeding the specified Sensitivity Range will cause Sensitivity Drift Through Temperature Range ($\Delta Sens_{TC}$) to deteriorate beyond the specified values.

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Average Fine Sensitivity Programming Step Size ($Step_{SENS}$)

This the change is the fine sensitivity parameter per code of sensf DAC. This value changes depending on SENS_COARSE. Keep in mind that the over temperature performance of the device is guaranteed only for the factory programed SENS_COARSE and its associated SENSPR.

Sensitivity Programming Resolution

This resolution is equal to or less than 1/2 × $Step_{SENS}$. If the device is more than 1/2 × $Step_{SENS}$ but less than one $Step_{SENS}$ away from a desired trim, then an additional step in the correct direction will yield a resolution less than 1/2 × $Step_{SENS}$.

Sensitivity Drift Through Temperature Range ($\Delta Sens_{TC}$)

Second-order sensitivity temperature coefficient effects cause the magnetic sensitivity, Sens, to drift from its expected value over the operating ambient temperature range (T_A). The Sensitivity Drift Through Temperature Range ($\Delta Sens_{TC}$) is defined as:

$$\Delta Sens_{TC} = \frac{Sens_{TA} - Sens_{EXPECTED(TA)}}{Sens_{EXPECTED(TA)}} \times 100\% \quad . \qquad (4)$$

Output Voltage Operating Range

The functional range for optimal performance of the device is between 4.5 to 0.5 V output voltage while V_{CC} = 5 V. The device can respond to magnetic fields that cause the output to go beyond these voltages, but parameters may not meet datasheet limits.

Sensitivity Non-Linearity Error (Lin_{ERR})

The ACS70310 is designed to provide a linear output in response to a ramping applied magnetic field. LinERR is valid from 0 G to ±2000 G input field while within the Output Voltage Operating Range. Consider two magnetic fields, B1 and B2. Ideally, the sensitivity of a device is the same for both fields, for a given supply voltage and temperature. Linearity error is present when there is a difference between the sensitivities measured at B1 and B2.

Linearity error is calculated separately for the positive $SensB_{POS2}$ (Lin_{ERRPOS}) and negative (Lin_{ERRNEG}) applied magnetic fields. Linearity Error (%) is measured and defined as:

$$Lin_{ERR(POS,NEG)} = \left(1 - \frac{Sens_{B(POS,NEG)2}}{Sens_{B(POS,NEG)1}}\right) \times 100\% \qquad (5)$$

where:

$$Sens_{Bx} = \frac{|V_{OUT(Bx)} - V_{OUT(Q)}|}{B_x} \quad , \qquad (6)$$

and BPOS*x* and BNEG*x* are positive and negative magnetic fields, with respect to the quiescent voltage output such that |BPOS2| = 2 × |BPOS1| and |BNEG2| = 2 × |BNEG1|.

Then:

$$Lin_{ERR} = \max(Lin_{ERRPOS}, Lin_{ERRNEG}) \quad . \qquad (7)$$

Ratiometry Error (Rat_{ERR})

The ACS70310 device features a ratiometric output. This means that the Quiescent Voltage Output ($V_{OUT(Q)}$), magnetic sensitivity, Sens, and Output Voltage Clamp ($V_{CLP(HIGH)}$ and $V_{CLP(LOW)}$) are proportional to the Supply Voltage (V_{CC}). In other words, when the supply voltage increases or decreases by a certain percentage, each characteristic also increases or decreases by the same percentage. Ratiometry Error is the difference between the measured change in the supply voltage relative to 5 V, and the measured change in each characteristic.

The ratiometric error in Quiescent Voltage Output, $Rat_{ERRVOUT(Q)}$ (%), for a given supply voltage (V_{CC}) is defined as:

$$Rat_{ERRVOUT(QBI)} = \left[1 - \frac{\left(\frac{V_{OUT(QBI)(VCC)}}{V_{OUT(QBI)(5V)}}\right)}{\frac{V_{CC}}{5\ V}}\right] \times 100\% \qquad (8)$$

$Rat_{ERRVOUT(QU)}$ is defined in the same way as $Rat_{ERRVOUT(QBI)}$ with a factor of 1/5 multiplied.

This is to scale the ratiometry error of the unidirectional device so that it can be compared with the bidirectional device.

The ratiometric error in magnetic sensitivity, $Rat_{ERRSens}$ (%), for a given Supply Voltage (V_{CC}) is defined as:

$$Rat_{ERRSens} = \left(1 - \frac{Sens_{(VCC)} / Sens_{(5V)}}{V_{CC} / 5\ V}\right) \times 100\% \quad . \qquad (9)$$

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Power-On Reset Voltage (V_{POR})

On power-up, to initialize to a known state and avoid current spikes, the ACS70310 is held in a reset state. The reset signal is disabled when V_{CC} reaches V_{PORH} and time t_{PORR} has elapsed, allowing the output voltage to go from a high-impedance state into normal operation. During power-down, the reset signal is enabled when V_{CC} reaches V_{PORL}, causing the output voltage to go into a high-impedance state. (Note that a detailed description of POR can be found in the Functional Description section).

Power-On Reset Release Time (t_{PORR})

When V_{CC} rises to V_{PORH}, the Power-On Reset counter starts. The ACS70310 output voltage will transition from a high-impedance state to normal operation only when the Power-On Reset Counter has reached t_{PORR} and V_{CC} has been maintained above V_{PORH}.

Output Saturation Voltage (V_{SAT})

When output voltage clamps are disabled, the output voltage can swing to a maximum of $V_{SAT(HIGH)}$ and to a minimum of $V_{SAT(LOW)}$.

Broken Wire Voltage (V_{BRK})

If the GND pin is disconnected (broken wire event), the output voltage will go to $V_{BRK(HIGH)}$ (if a load resistor is connected to VCC) or to $V_{BRK(LOW)}$ (if a load resistor is connected to GND).

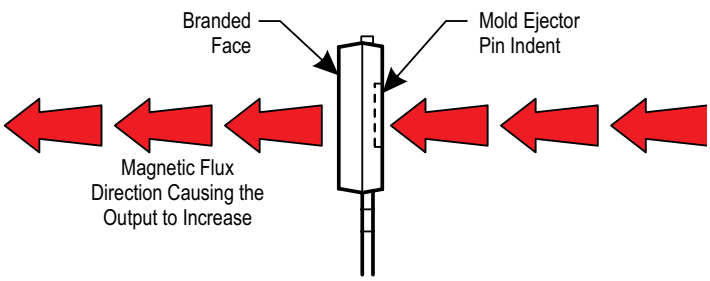

Figure 7: Magnetic Flux Polarity

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FUNCTIONAL DESCRIPTIONS

Power-On Reset (POR)

The descriptions in this section assume: Temperature = 25°C, no output load (R_L, C_L), and no significant magnetic field is present. When the device is off, the output will be in a high-impedance state.

Power-On

As V_{CC} ramps up, the device output is in high impedance until V_{CC} reaches $V_{POR(H)}$. As V_{CC} rises above $V_{POR(H)}$, the device's output leaves the high impedance state and enters normal operating mode.

Overvoltage Detection (V_{OVD})

When V_{CC} is raised above the Overvoltage Detection enable voltage ($V_{OVD(EN)}$), the ACS70310 output stage enters high impedance. V_{OUT} will float: to V_{CC} with a pull-up R_L, or to GND with a pull-down R_L, when $V_{OVD(EN)}$ is reached. When programing the ACS70310, Overvoltage Detection must be active for communication. The ACS70310 output will resume normal operation after V_{CC} is below the Overvoltage Detection disable voltage $V_{OVD(DIS)}$. Note that Supply Voltage limits still apply for operating characteristic.

Power-Down

As V_{CC} ramps down, the device output is active until V_{CC} falls below $V_{POR(L)}$. As V_{CC} falls below $V_{POR(L)}$, the device's output will enter a high impedance state.

Power On/Off Profile

Figure 8 shows the analog output of a device at power on and power off.

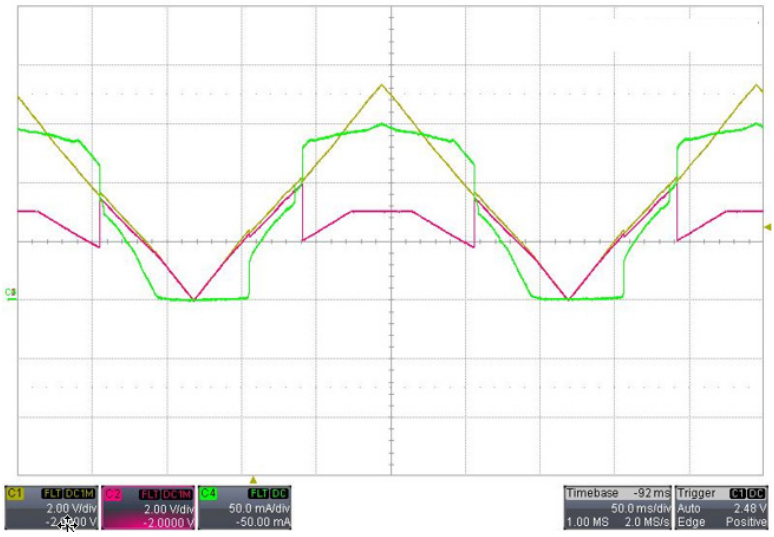

Figure 8: Power On/Off and Overvoltage Detection (OVD), no R_L
V_{CC} = C1 (yellow), V_{OUT} = C2 (red), I_{CC} = C4/10 (green)

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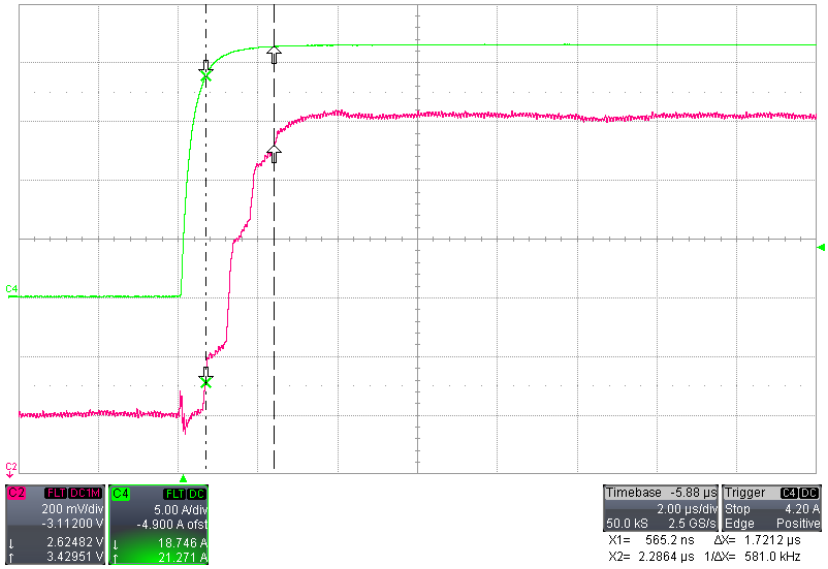

Figure 9: Rise Time: 110 G excitation signal with 10%-90% rise time = 700 ns, Input = C4 × 5 G/A (green), V_{OUT} = C2 (red), no C_L or R_L, C_{BY} = 0.1 µF

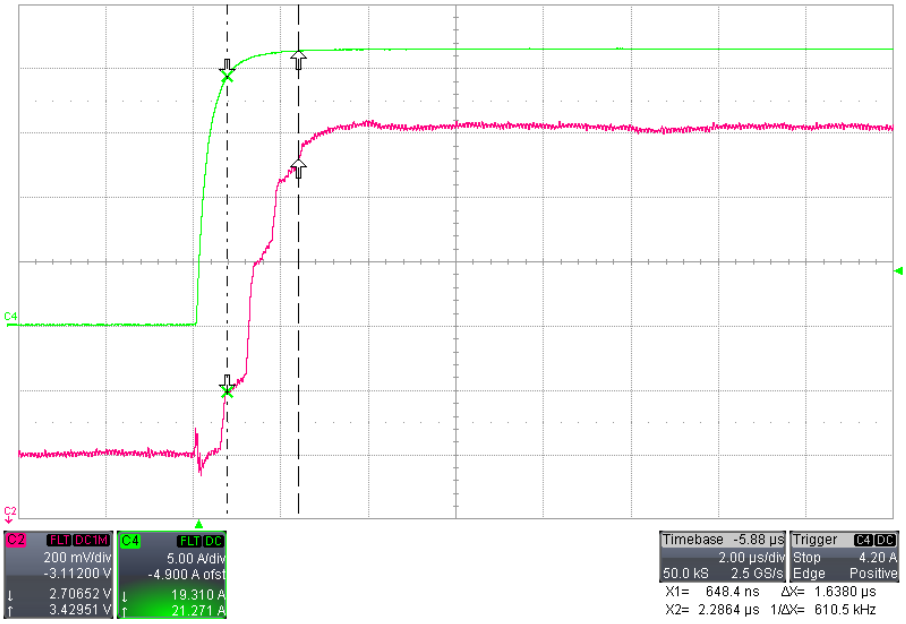

Figure 10: Response Time plot of 90%-90% (input to output): 110 G excitation signal with rise time 10%-90% = 700 ns, Input = C4 × 5 G/A (green), V_{OUT} = C2 (red), no C_L or R_L, C_{BY} = 0.1 µF

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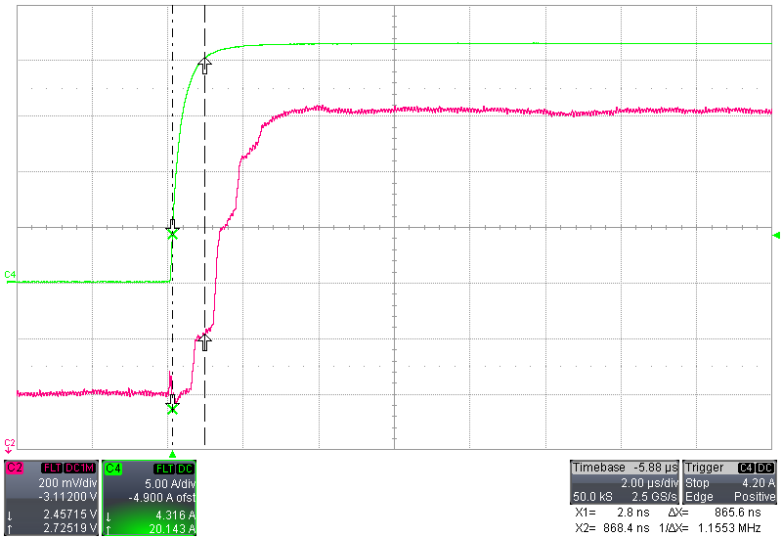

Figure 11: Propagation Delay from 20%-20% (input to output): 110 G excitation signal with rise time 10%-90% = 700 ns, Input = C4 × 5 G/A (green), V_{OUT} = C2 (red), no C_L or R_L, C_{BY} = 0.1 µF

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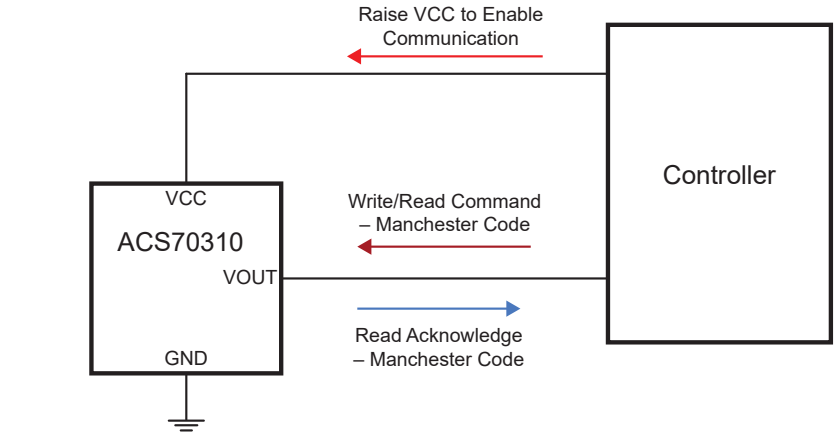
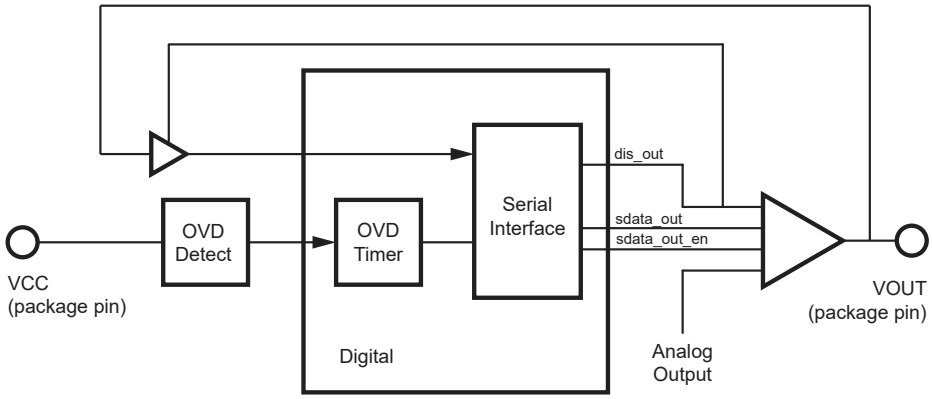
PROGRAMMING GUIDELINES

The serial interface uses a bidirectional communication on VOUT. When the voltage on the VCC pin is increased beyond the programming threshold, the device will enter programming mode.

The device has an internal charge pump to generate the EEPROM pulses.

Recommended programing kits/subkits and software can be found under the Technical Docs on the ACS70310 product page at the www.allegromicro.com website.





sdata_out_en	out_dis	VOUT
0	0	Analog output
0	1	High-Z
1	X	sdata_out

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Memory-Locking Mechanisms

The ACS70310 is equipped with two distinct memory-locking mechanisms:

- ***Default Lock:*** At power-up, all registers of the ACS70310 are locked by default. EEPROM and volatile memory cannot be read or written. To disable Default Lock, a specific 32-bit customer access code has to be written to address 0x36 within Access Code Timeout (t_{ACC} = 10 ms) from power-up. After doing so, registers can be accessed. If VCC is power-cycled, the Default Lock will automatically be re-enabled. This ensures that during normal operation, memory content will not be altered due to unwanted glitches on VCC or the output pin.
- ***Lock Bit:*** After EEPROM has been programmed by the user, the EELOCK bit can be set high and VCC power-cycled to permanently disable the ability to read or write any register. This will prevent the ability to disable Default Lock using the method described above. Note that after the EELOCK bit is set high and the VCC pin has been power-cycled, the EELOCK bit can no longer be cleared and registers can no longer be written to.

Serial Communication

The serial interface allows an external controller to read and write registers, including EEPROM, in the ACS70310 using a point-to-point command/acknowledge protocol. The ACS70310 does not initiate communication; it only responds to commands from the external controller. Each transaction consists of a command from the controller. If the command is a write, there is no acknowledging from the ACS70310. If the command is a read, the ACS70310 responds by transmitting the requested data.

Serial interface timing parameters can be found in the Programming Levels table (Table 1). Note that the external controller must avoid sending a Command frame that overlaps a Read Acknowledge frame.

The serial interface uses a Manchester-encoding-based protocol per G.E. Thomas (0 = rising edge, 1 = falling edge), with address and data transmitted MSB first. Four commands are recognized by the ACS70310: Write Access Code, Write to Volatile Memory, Write to Non-Volatile Memory (EEPROM) and Read. One frame type, Read Acknowledge, is sent by the ACS70310 in response to a Read command.

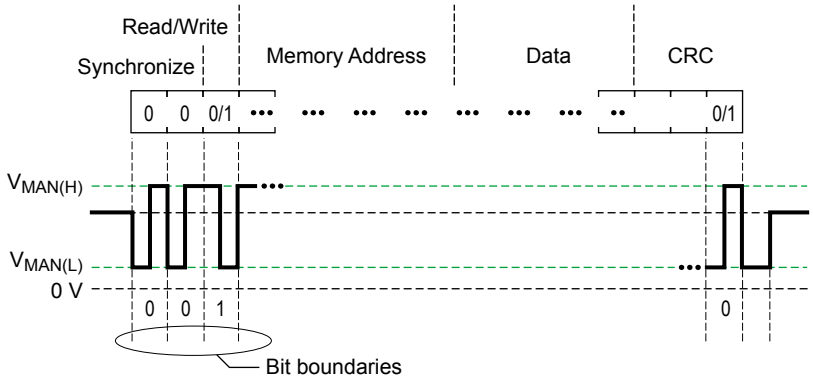

Figure 12: General Format for Serial Interface Commands

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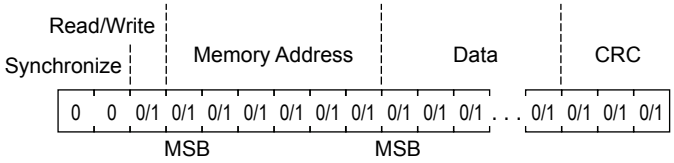
The ACS70310 device uses a three-wire programming interface, where VCC is used to control the program enable signal, data is transmitted on VOUT, and all signals are referenced to GND. This three-wire interface makes it possible to communicate with multiple devices with shared VCC and GND lines.

The four transactions (Write Access, Write to EEPROM, Write to Volatile Memory, and Read) are show in the figures on the following pages. To initialize any communication, V_{CC} should be increased to a level above V_{prgH}(min) without exceeding V_{prgH}(max). At this time, VOUT is disabled and acts as an input.

After program enable is asserted, the external controller must drive the output low in a time less than t_d. This prevents the device interpreting any false transients on VOUT as data pulses. After the command is completed, V_{CC} is reduced below V_{prgL}, back to normal operating level. Also, the output is enabled and responds to magnetic input.

When performing a Write to EEPROM transaction, the ACS70310 requires a delay of t_w to store the data into the EEPROM. The device will respond with a high-to-low transition on VOUT to indicate the Write to EEPROM sequence is complete.

When sending multiple command frames, it is not necessary to toggle the program enable signal on VCC. After the first command frame is completed, and V_{CC} remains at V_{prgH}, the device will ignore any subsequent pulses on the output. When the program enable signal is brought below $V_{prgL(max)}$, the output will respond to the magnetic input.



Quantity of Bits	Name	Values	Description
2	Synchronization	00	Used to identify the beginning of a serial interface command
1	Read / Write	0	[As required] Write operation
		1	[As required] Read operation
6	Address	0/1	[Read/Write] Register address (volatile memory or EEPROM)
32	Data	0/1	26 data bits and 6 ECC bits. For a read command frame the data consists of 32 bits: [31:28] Don't Care, [27:26] ECC Pass/Fail, and [25:0] Data. Where bit 0 is the LSB. For a write command frame the data consists of 32 bits: [31:26] Don't Care and [25:0] Data. Where bit 0 is the LSB.
3	CRC	0/1	Bits to check the validity of frame.

Figure 13: Command Frame General Format

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Table 1: Programming Parameters, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V

Characteristics	Symbol	Note	Min.	Typ.	Max.	Unit
Program Enable Voltage (High)	V_{prgH}	Program enable signal high level on VCC	–	9.2	–	V
Program Enable Voltage (Low)	V_{prgL}	Program enable signal low level on VCC	–	6.5	–	V
Output Enable Delay	t_e	External capacitance (C_{LX}) on VOUT may increase the Output Enable Delay	–	125	–	µs
Program Time Delay	t_d		–	74	–	µs
Program Write Delay	t_w		–	20	–	ms
Manchester High Voltage	$V_{MAN(H)}$	Data pulses on VOUT	4	5	V_{CC}	V
Manchester Low Voltage	$V_{MAN(L)}$	Data pulses on VOUT	0	–	1	V
Bit Rate	t_{BITR}	Communication rate	1	30	100	kbps
Bit Time	t_{BIT}	Data bit pulse width at 30 kbps	–	(33)	–	µs
Access Code Timeout	t_{ACC}			10		ms

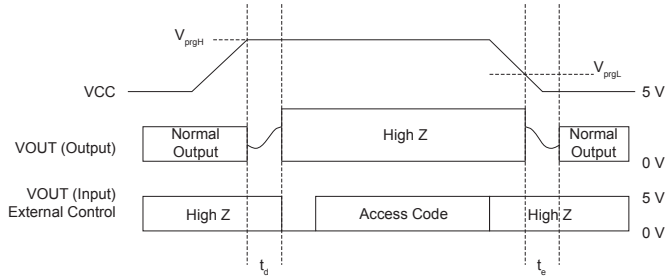

Figure 14: Write Access Code

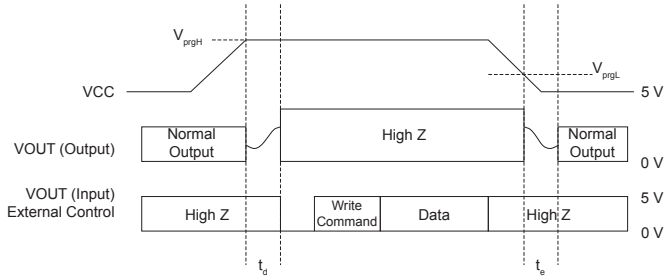

Figure 15: Write Volatile Memory

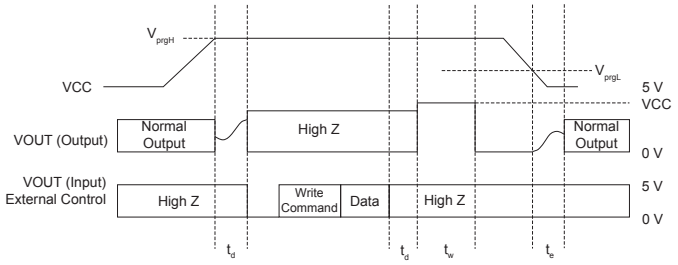

Figure 16: Write Non-Volatile Memory

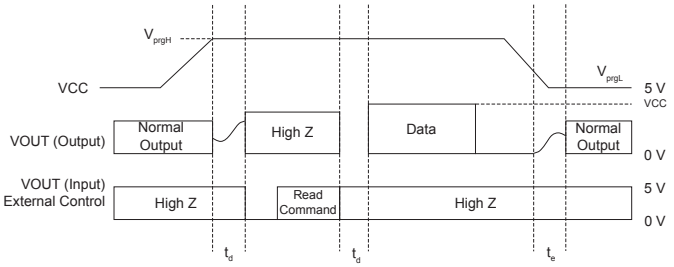

Figure 17: Read

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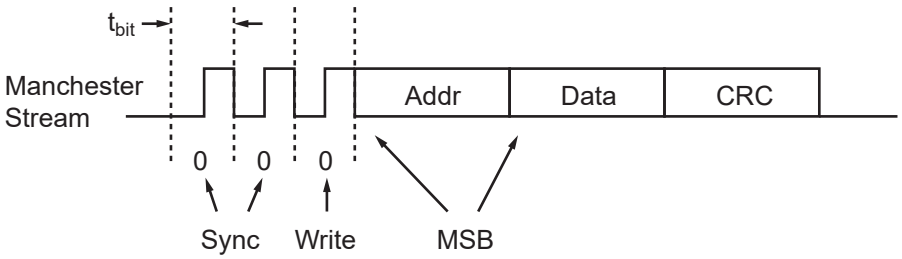
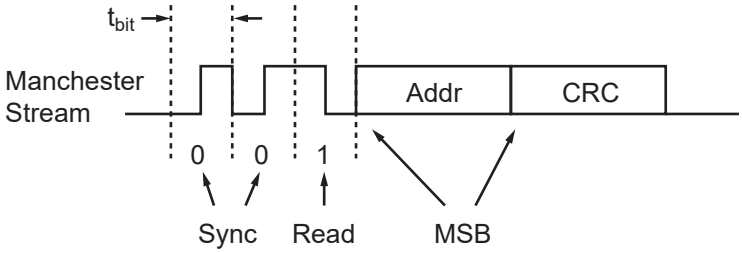
MANCHESTER COMMUNICATION

Command Format

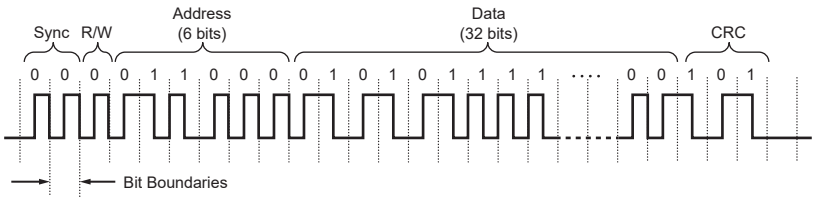


Manchester Write Command

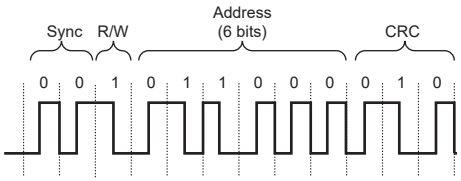


Manchester Read Command

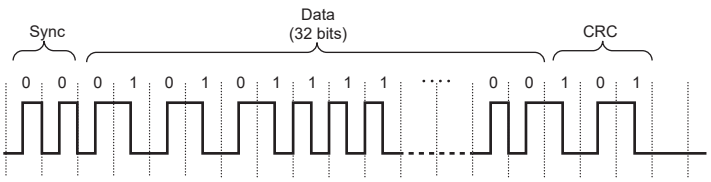
Write Command



Read Command



Read Acknowledge



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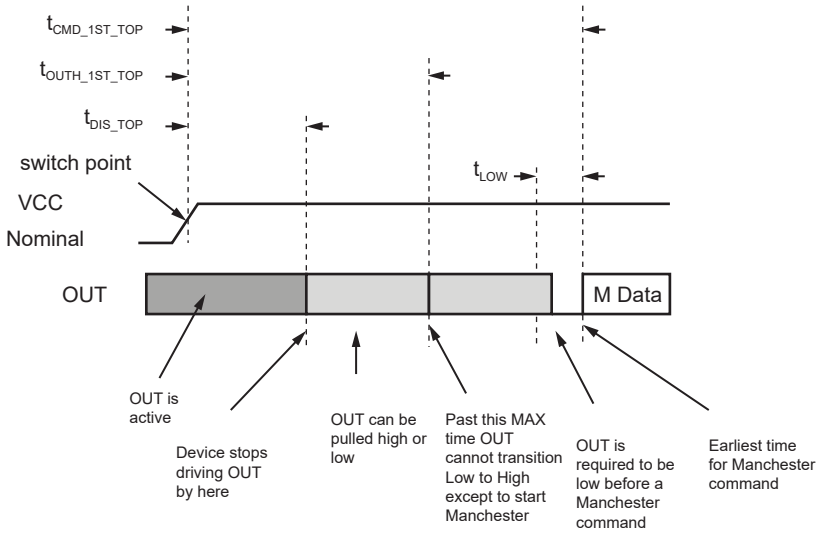
Generic Timing

For initial portion of Manchester command



Parameter	Description	Min.	Max.
t_{sclk}	System clock period after trimming.	133 ns (7.5 MHz)	167 ns (6 MHz)
t_{bit}	Bit time.	1 µs (1 MBd)	1 ms (1 kBd)
t_{DIS_TOP}	OUT pin is disabled after raising VCC.	56 µs (512 × t_{sclk})	73.5 µs (514 × t_{sclk})
$t_{OUTH_1ST_TOP}$	The OUT pin is either pulled high or low. No low-to-high transitions are allowed after this MAX time except to start the Manchester command. This is for the 1st Manchester command after raising VCC.	73.5 µs	123 µs
$t_{CMD_1ST_TOP}$	Time required before the 1st Manchester command can be sent after raising VCC.	144 µs	n/a
t_{LOW}	Time required to hold output low before the 1st Manchester edge.	1 µs	n/a

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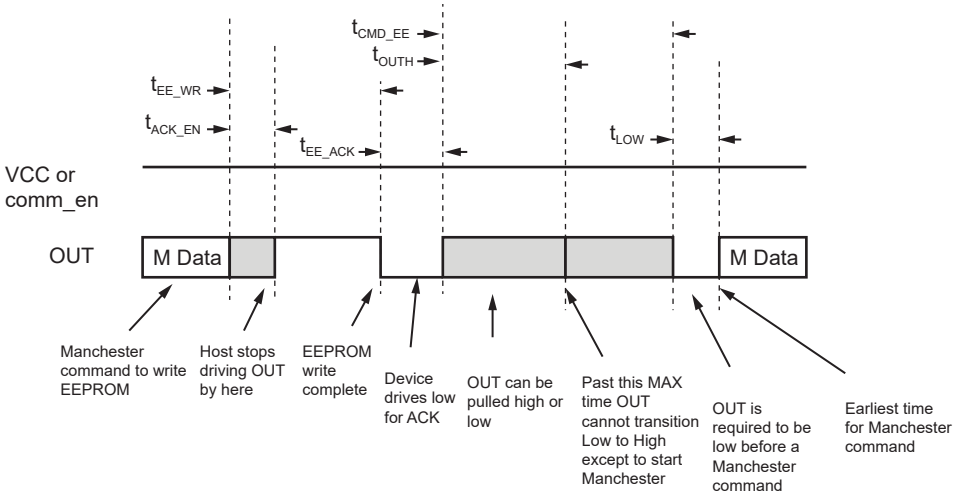
Write to EEPROM

If VCC is held up at the programming voltage, multiple Manchester commands can be executed.



Parameter	Description	Min.	Max.
t_{sclk}	System clock period after trimming.	133 ns (7.5 MHz)	167 ns (6 MHz)
t_{bit}	Bit time.	1 µs (1 MBd)	1 ms (1 kBd)
t_{ACK_EN}	Time for the device to drive OUT after Manchester command. Host must stop driving OUT within this time.	2 × t_{bit}	2 × t_{bit}
t_{EE_WR}	During this time the device is writing the EEPROM	–	–
t_{EE_ACK}	Device will drive OUT low during this time	1 × t_{bit}	1 × t_{bit}
t_{OUTH}	The OUT pin is either pulled high or low. No low-to-high transitions are allowed after this MAX time except to start the next Manchester command.	0	1.8 × t_{bit}
t_{CMD_EE}	Time before the next Manchester command may be given following a write to EEPROM.	2.2 × t_{bit}	n/a
t_{LOW}	Time required to hold output low before the 1st Manchester edge.	1 µs	n/a

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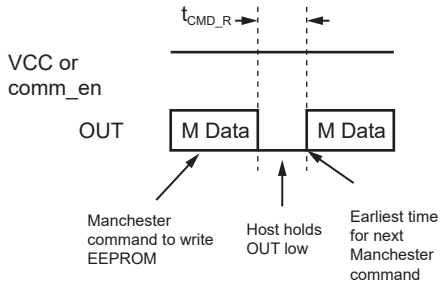
Write to Register (Not EEPROM)



Parameter	Description	Min.	Max.
t_{sclk}	System clock period after trimming.	133 ns (7.5 MHz)	167 ns (6 MHz)
t_{bit}	Bit time.	1 µs (1 MBd)	1 ms (1 kBd)
t_{CMD_R}	Time before the next Manchester command may be given following a write to a Register.	2 µs	n/a

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Read (Controller to ACS70310)

The fields for the Read command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 1 for read)
- CRC (3 bits)

Figure 18 shows the sequence for a Read command.

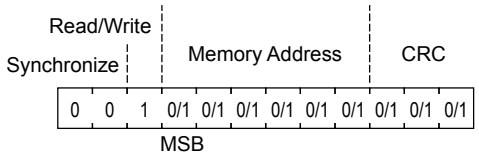

Figure 18: Read Sequence

Read Acknowledge (ACS70310 to Controller)

The fields for the data return frame are:

- Sync (2 zero bits)
- Data (32 bits):
  - □ [31:28] Don't Care
  - □ [27:26] ECC Pass/Fail
  - □ [25:0] Data

Figure 19 shows the sequence for a Read Acknowledge. Refer to the Detecting ECC Error section for instructions on how to detect Read/Write Synchronize Memory Address Data (32 bits) and ECC failure.

Figure 19: Read Acknowledgement Sequence

Write (Controller to ACS70310)

The fields for the Write command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 0 for write)
- Address (6 bits)
- Data (32 bits):
  - □ [31:26] Don't Care
  - □ [25:0] Data
- CRC (3 bits)

Figure 20 shows the sequence for a Write command. Bits [31:26] are Don't Care because the ACS70310 automatically generates 6 ECC bits based on the content of bits [25:0]. These ECC bits will be stored in EEPROM at locations [31:26].

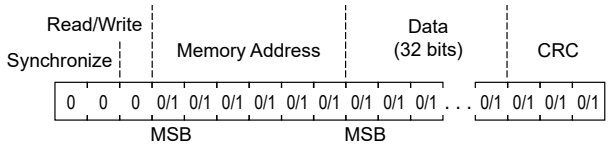

Figure 20: Write Sequence

Write Access Code (Controller to ACS70310)

The fields for the Access Code command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 0 for write)
- Address (6 bits, address 0x36 for Customer Access)
- Data (32 bits, 0xC4136737 for Customer Access)
- CRC (3 bits)

Figure 21 shows the sequence for an Access Code command.

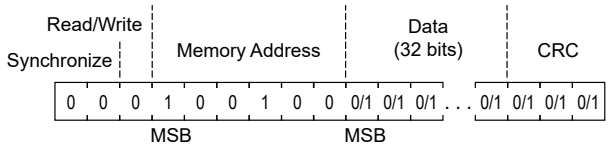

Figure 21: Write Access Code

The controller must open the serial communication with the ACS70310 device by sending an Access Code. It must be sent within Access Code Timeout, t_{ACC}, from power-up, or the device will be disabled for read and write access.

Access Codes Information

Name	Serial Interface Format	
	Register Address (Hex)	Data (Hex)
Customer	0x36	0xC4136737

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EEPROM Error Checking and Correction (ECC)

Hamming code methodology is implemented for EEPROM checking and correction. The device has ECC enabled after power-up.

The device always returns 32 bits.

The message received from controller is analyzed by the device EEPROM driver and ECC bits are added. The first 6 received bits from device to controller are dedicated to ECC.

Detecting ECC Error

If an uncorrectable error has occurred, bits 27:26 are set to 10, the VOUT pin will go to a high-impedance state, and the device will not respond to the applied magnetic field.

EEPROM ECC Errors

Bits	Name	Description
31:28	–	No meaning
27:26	ECC	00 = No Error 01 = Error detected and message corrected 10 = Uncorrectable error 11 = No meaning
25:0	D[25:0]	EEPROM data

Table 2: Customer Memory Map

Address	Register Name	Parameter Name	Description	r/w	Bits	Location
0x4	scratch_c	customer_scratch	Unused area	RW	26	25:0
0x5	cust0_c	sensf	Sensitivity, fine adjustment	RW	9	8:0
		qvof	Quiescent Output Voltage (QVO), fine adjustment	RW	9	17:9
		sensc	Coarse Sensitivity	RW [1]	2	19:18
0x6	cust1_c	rat_dis	Ratiometry disable. Sens and $V_{OUT(Q)}$ are not guaranteed if ratiometry is disabled.	RW	1	2
		uni_en	Enables Unidirectional Output	RW	1	4
		clamp_en	Clamp enable	RW	1	5
		pol	Reverses output polarity	RW	1	6
		dev_lock	Bit to lock the serial interface from receiving data	RW	1	7
0x29	status_c	customer_access	Customer write access enabled	RO	1	0

[1] Overtemperature performance is no longer valid if this register is changed from factory default.

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PACKAGE OUTLINE DRAWING

For Reference Only - Not for Tooling Use

(Reference DWG-9202)
Dimensions in millimeters - NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

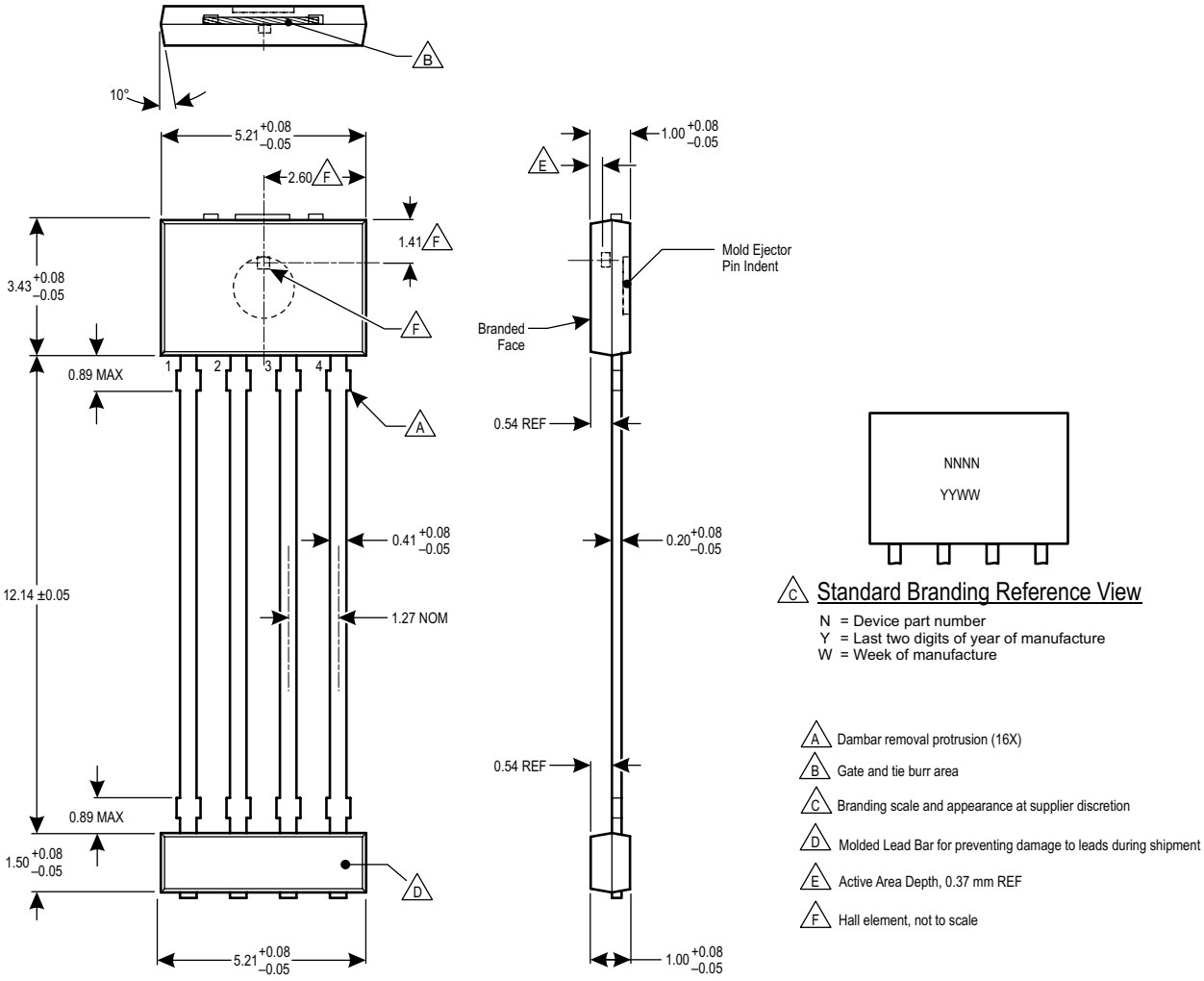

Figure 22: Package KT, 4-Pin SIP, TN Leadform

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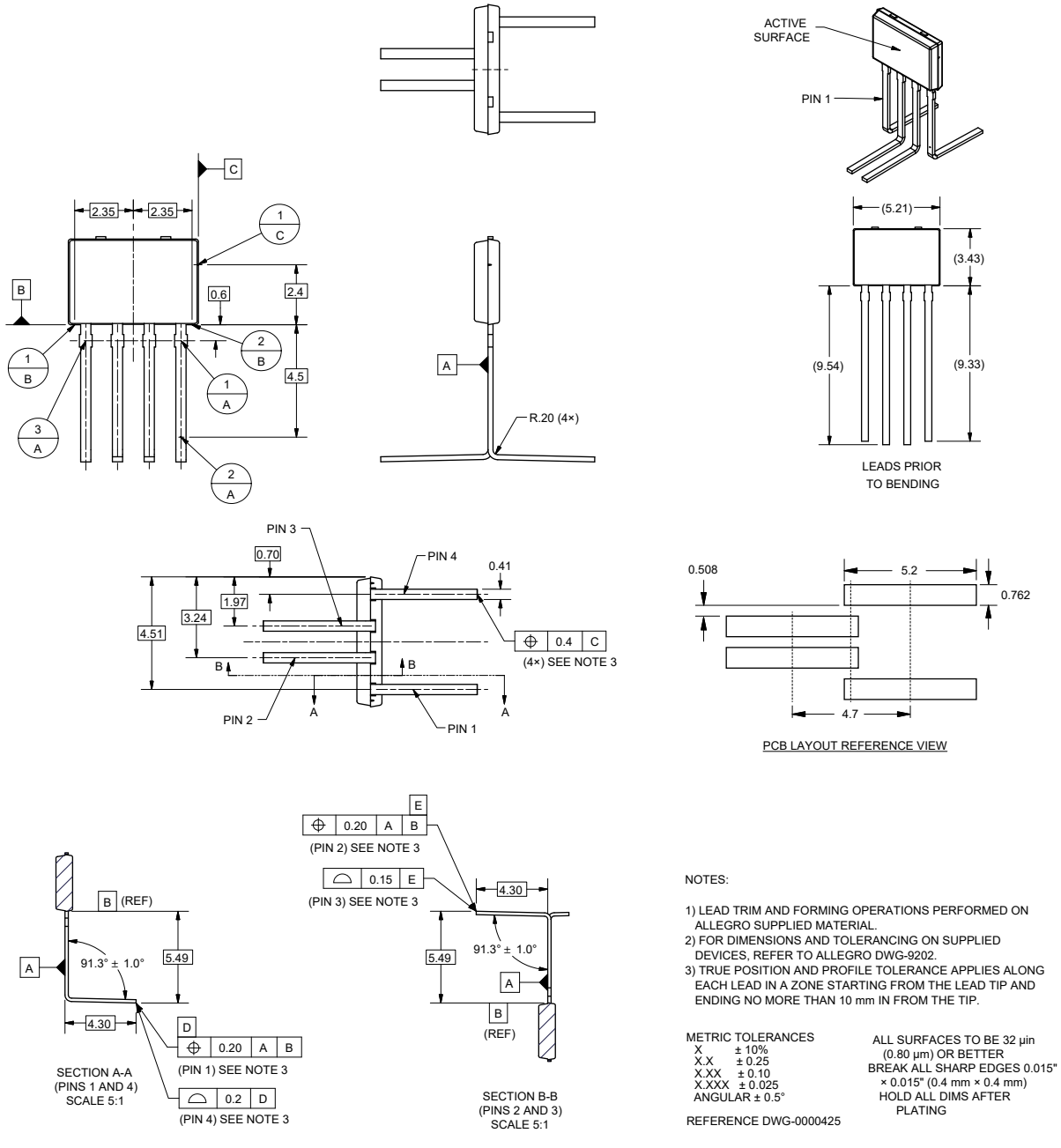

Figure 23: Package KT, 4-Pin SIP, TF Leadform

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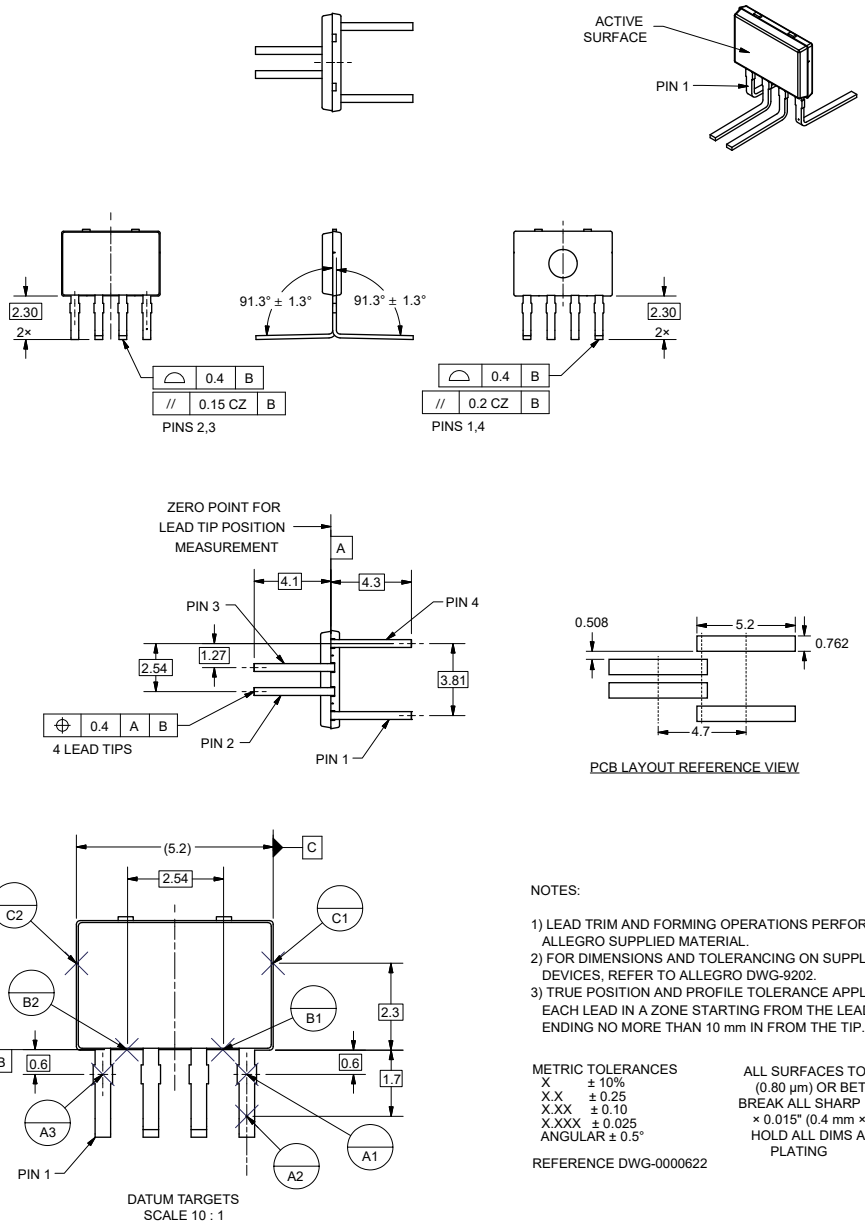

Figure 24: Package KT, 4-Pin SIP, TG Leadform

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Revision History

Number	Date	Description
–	February 27, 2019	Initial release
1	April 10, 2019	Removed Internal Bandwidth min/max values (page 5) and added TF/TG leadform footprints (pages 25-26)

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