ACPL-3130/J313, ACNW3130

Very High CMR 2.5 Amp Output Current IGBT Gate Driver Optocoupler

AVAGO TECHNOLOGIES

Data Sheet

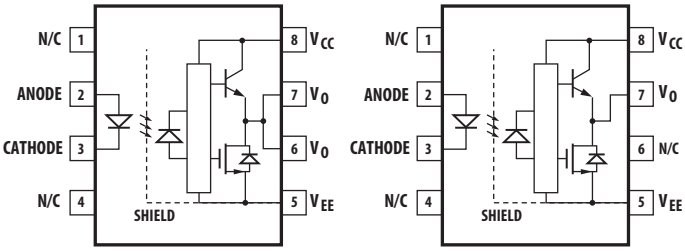
Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

The ACPL-3130 contains a GaAsP LED while the ACPL-J313 and the ANCW3130 contain an AlGaAs LED. The LED is optically coupled to an integrated circuit with a power output stage. These optocouplers are ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and current supplied by these optocouplers make them ideally suited for directly driving IGBTs with ratings up to 1200 V/100 A. For IGBTs with higher ratings, the ACPL-3130 series can be used to drive a discrete power stage which drives the IGBT gate. The ANCW3130 has the highest insulation voltage of V_{IORM} = 1414 V_{peak} in the IEC/EN/DIN EN 60747-5-5. The ACPL-J313 has an insulation voltage of V_{IORM} = 1230 V_{peak} and the V_{IORM} = 630 V_{peak} is also available with the ACPL-3130 (Option 060).

Functional Diagram



ACPL-3130 and ACPL-J313 **ACNW3130**

Truth Table

LED	$V_{CC} - V_{EE}$ "POSITIVE GOING" (i.e., TURN-ON)	$V_{CC} - V_{EE}$ "NEGATIVE GOING" (i.e., TURN-OFF)	VO
OFF	0 - 30 V	0 - 30 V	LOW
ON	0 - 11 V	0 - 9.5 V	LOW
ON	11 - 13.5 V	9.5 - 12 V	TRANSITION
ON	13.5 - 30 V	12 - 30 V	HIGH

Note: A 0.1 µF bypass capacitor must be connected between pins V_{CC} and V_{EE}.

Features

- High speed response.
- Very high CMR.
- Bootstrappable supply current.
- Safety Approval:

  UL Recognized
  - 3750 V_{rms} for 1 min. for ACPL-3130/ACPL-J313
  - 5000 V_{rms} for 1 min. for ACNW3130

  CSA Approval

  IEC/EN/DIN EN 60747-5-5 Approved
  - V_{IORM} = 630 V_{peak} for ACPL-3130 (Option 060)
  - V_{IORM} = 1230 V_{peak} for ACPL-J313
  - V_{IORM} = 1414 V_{peak} for ACNW3130

Specifications

- 2.5 A maximum peak output current.
- 2.0 A minimum peak output current.
- 40 kV/µs minimum Common Mode Rejection (CMR) at V_{CM} = 1500 V
- 0.5 V maximum low level output voltage (V_{OL}) eliminates need for negative gate drive
- I_{CC} = 5 mA maximum supply current
- Under Voltage Lock-Out protection (UVLO) with hysteresis
- Wide operating V_{CC} range: 15 to 30 Volts
- 500 ns maximum switching speeds
- Industrial temperature range: -40°C to 100°C

Applications

- IGBT/MOSFET gate drive
- AC/Brushless DC motor drives
- Industrial inverters
- Switching Power Supplies (SPS)

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Ordering Information

ACPL-3130 and ACPL-J313 are UL Recognized with 3750 Vrms for 1 minute per UL1577. ACNW3130 is UL Recognized with 5000Vrms for 1 minute per UL1577.

Part number	Option RoHS Compliant	Package	Surface Mount	Gull Wing	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-3130	-000E	300mil DIP-8					50 per tube
	-300E		X	X			50 per tube
	-500E		X	X	X		1000 per reel
	-060E					X	50 per tube
	-360E		X	X		X	50 per tube
	-560E		X	X	X	X	1000 per reel
ACPL-J313	-000E	300mil DIP-8				X	50 per tube
	-300E		X	X		X	50 per tube
	-500E		X	X	X	X	1000 per reel
ACNW3130	-000E	400mil DIP-8				X	42 per tube
	-300E		X	X		X	42 per tube
	-500E		X	X	X	X	750 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-3130-560E to order product of 300mil DIP Gull Wing Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Example 2:

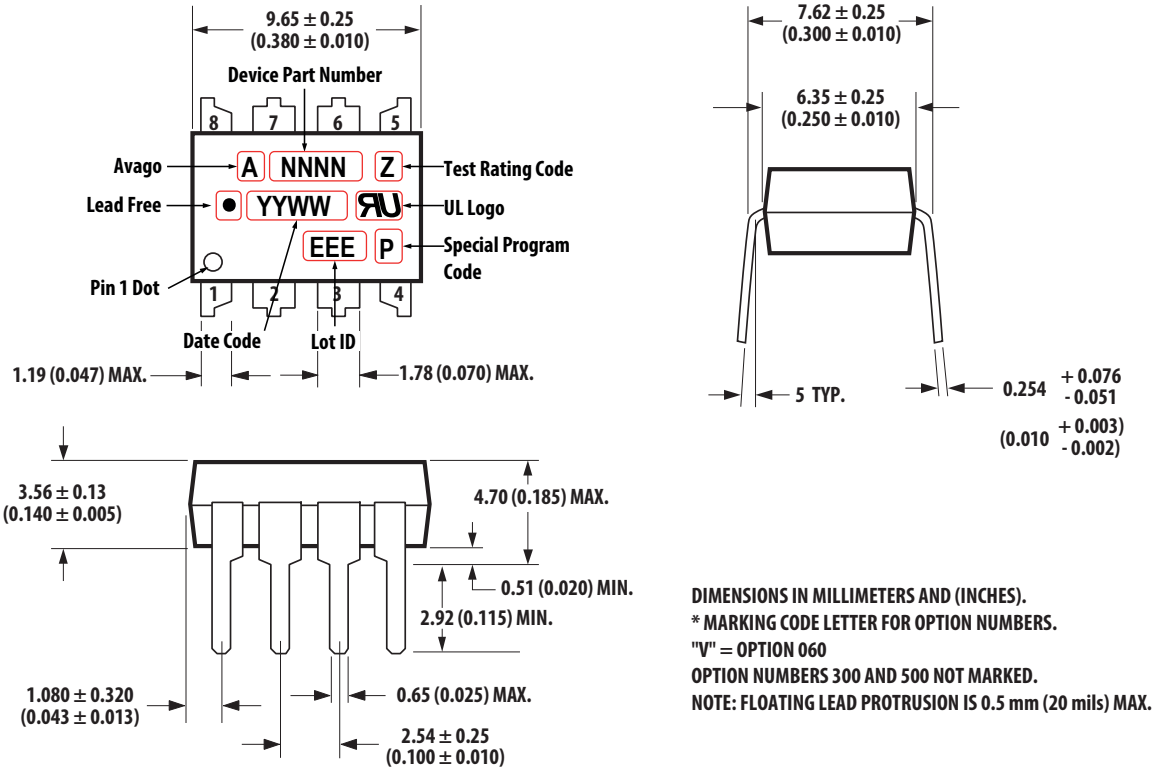
ACPL-3130-000E to order product of 300mil DIP package in tube packaging and RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, while (new) products launched since 15th July 2001 and RoHS compliant option will use '-XXXE'.

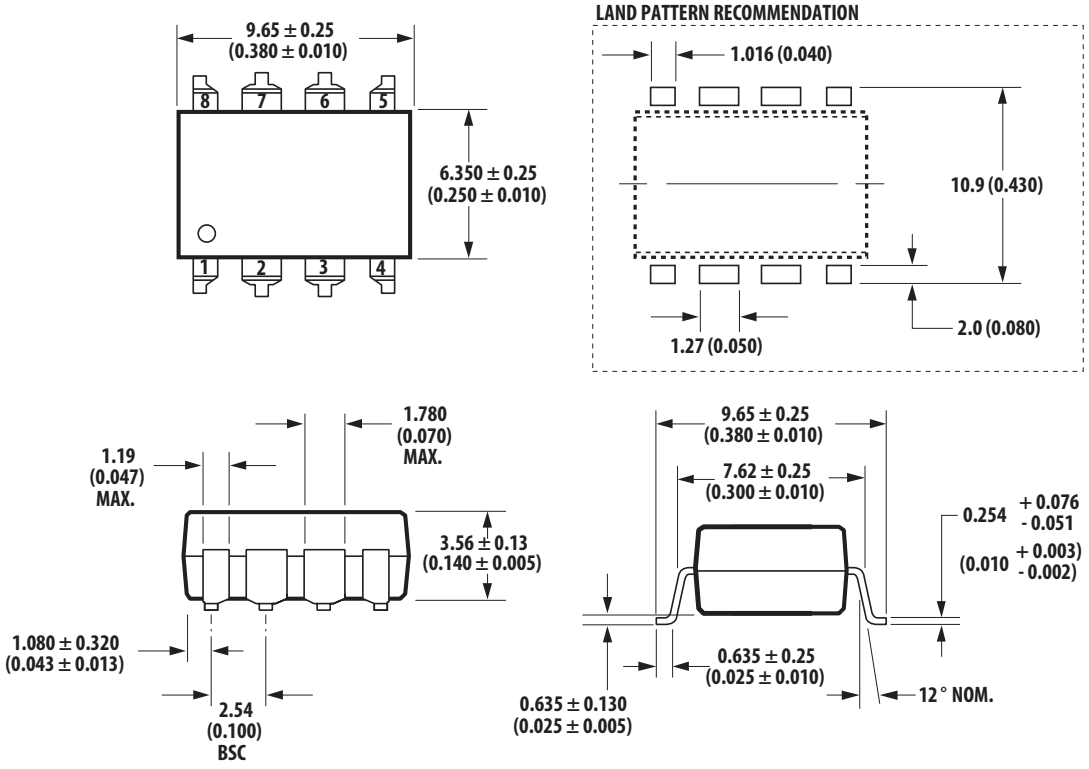
Package Outline Drawings

ACPL-3130 Outline Drawing (Standard DIP Package / 300mil DIP)



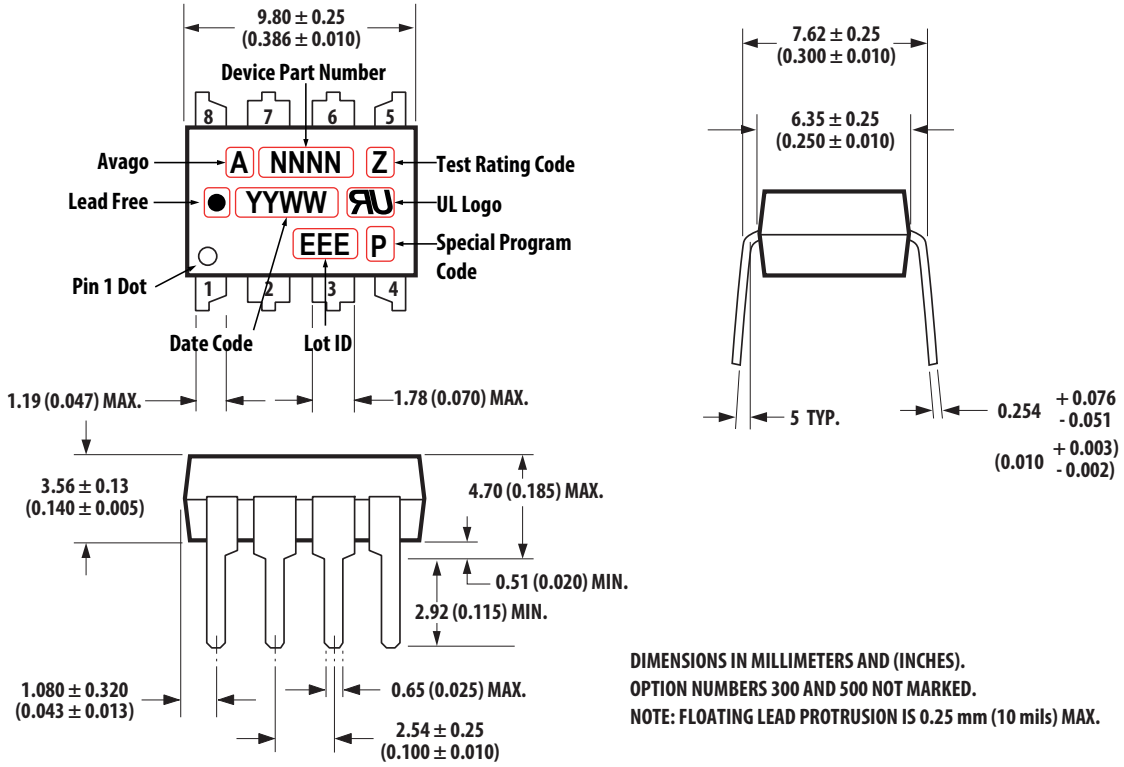
DIMENSIONS IN MILLIMETERS AND (INCHES).
* MARKING CODE LETTER FOR OPTION NUMBERS.
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.
NOTE: FLOATING LEAD PROTRUSION IS 0.5 mm (20 mils) MAX.

ACPL-3130 Gull Wing Surface Mount Option 300 Outline Drawing



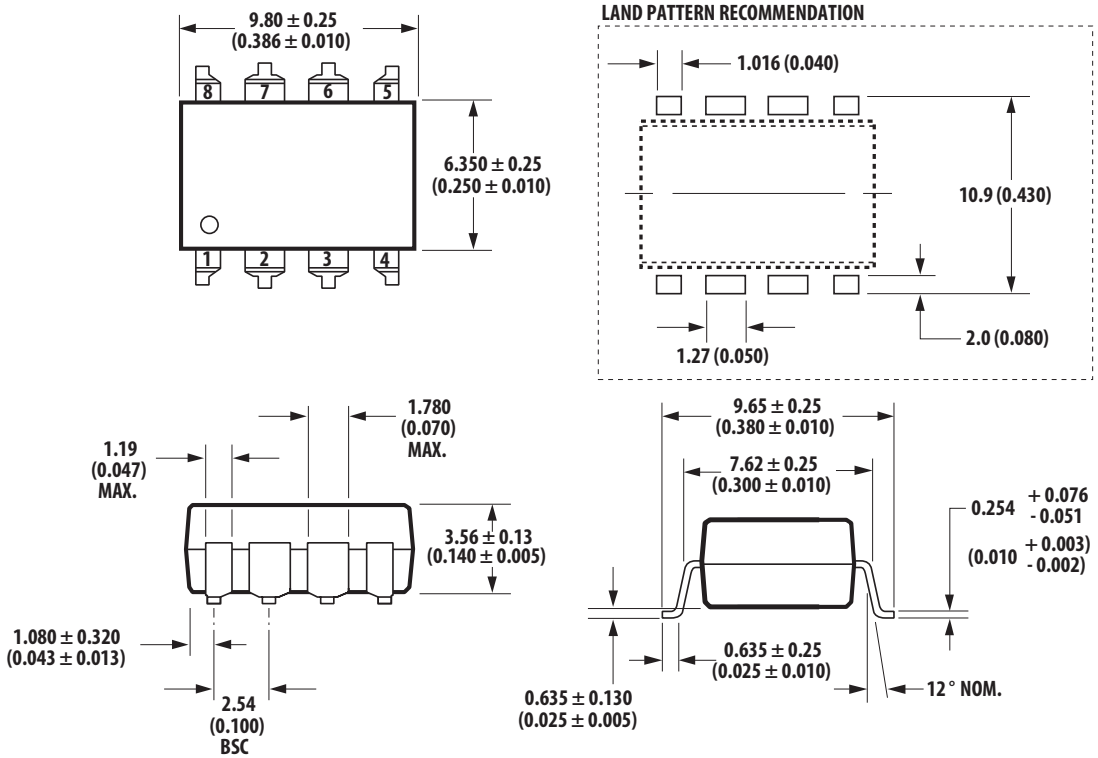
DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).
NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

ACPL-J313 Outline Drawing (300mil DIP)



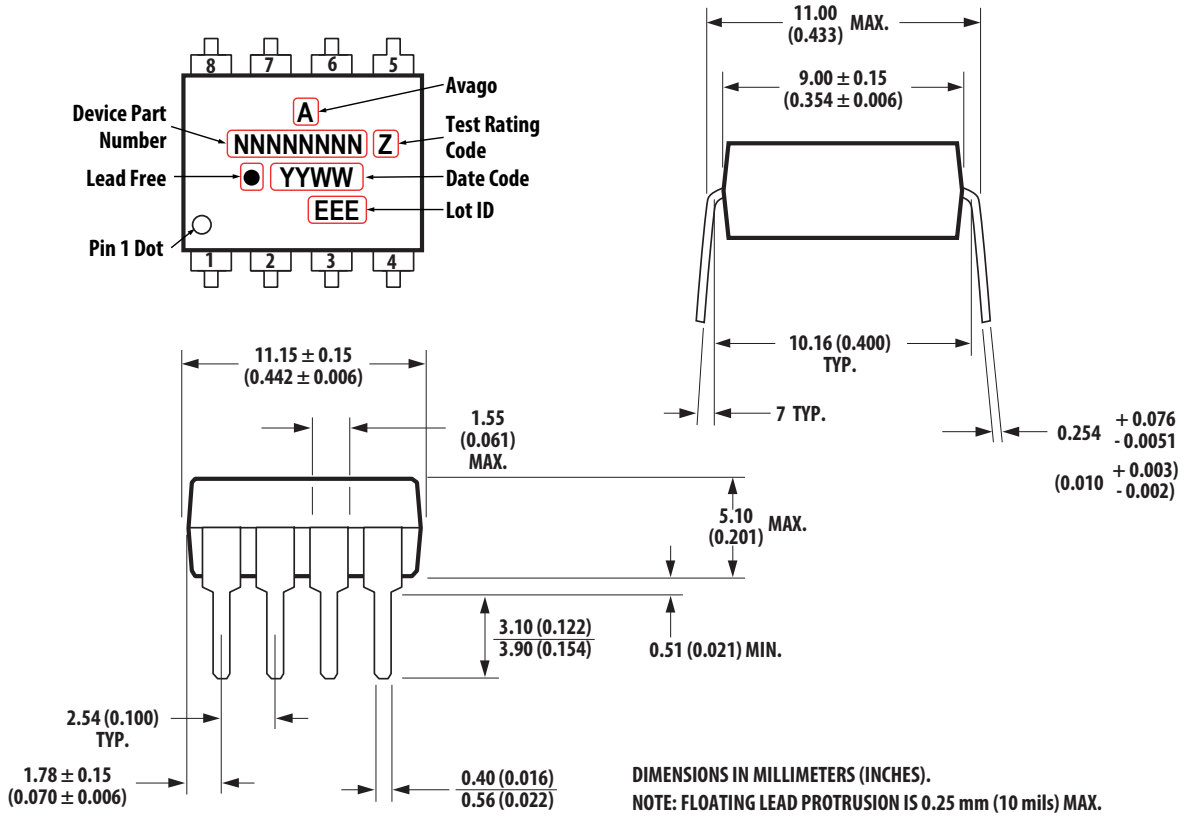
DIMENSIONS IN MILLIMETERS AND (INCHES).
OPTION NUMBERS 300 AND 500 NOT MARKED.
NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

ACPL-J313 Gull Wing Surface Mount Option 300 Outline Drawing



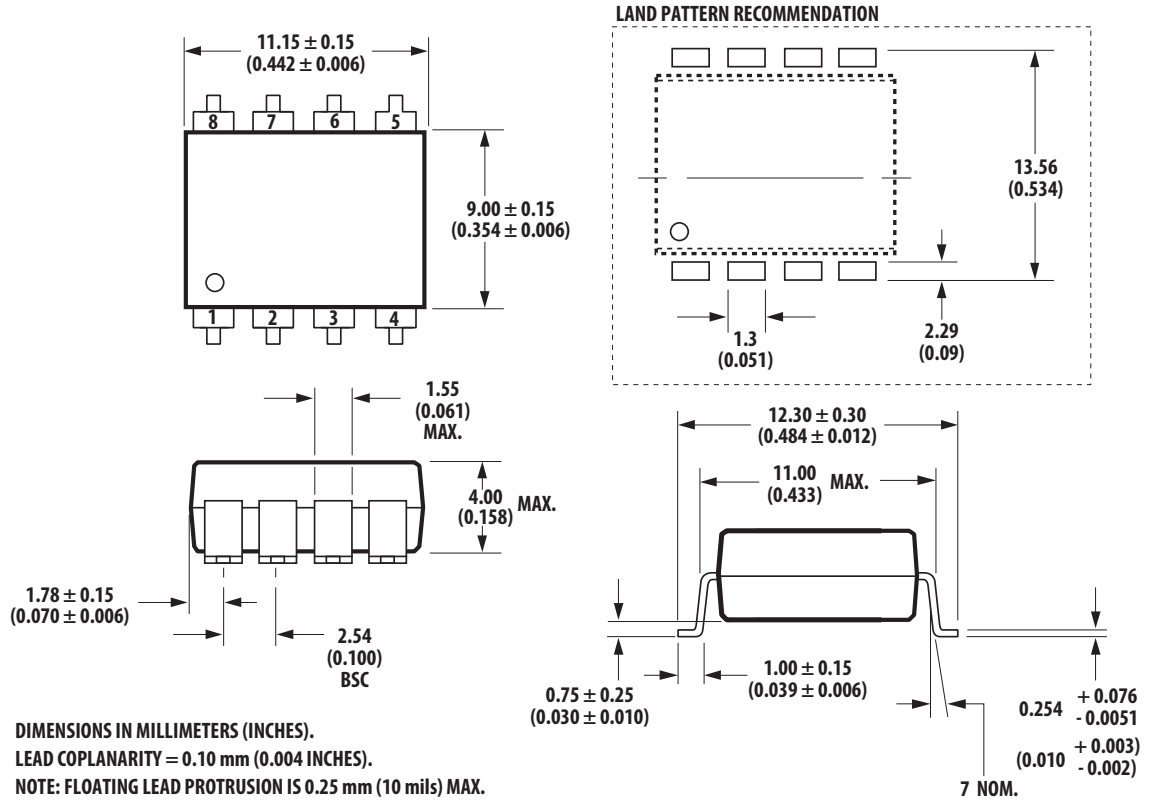
DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).
NOTE: FLOATING LEAD PROTRUSION IS 0.5 mm (20 mils) MAX.

ACNW3130 Outline Drawing (8-Pin Wide Body Package / 400mil DIP)



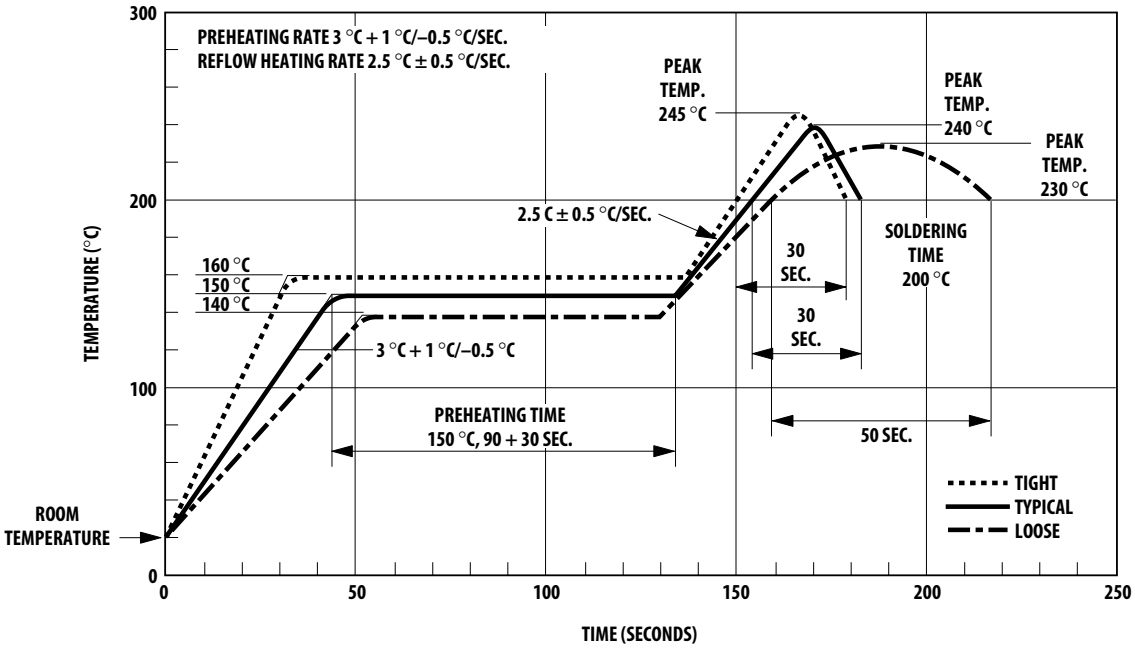
DIMENSIONS IN MILLIMETERS (INCHES).
NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

ACNW3130 Gull Wing Surface Mount Option 300 Outline Drawing



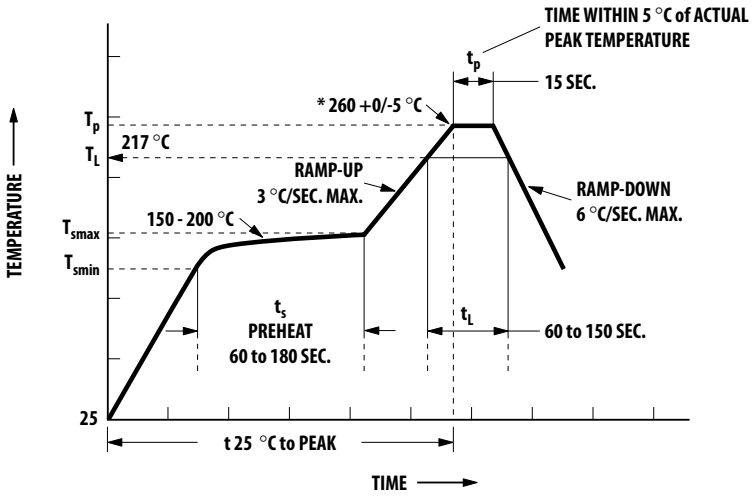
DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).
NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

Recommended Solder Reflow Temperature Profile



NOTE: NON-HALIDE FLUX SHOULD BE USED.

Recommended Pb-Free IR Profile



NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200 °C, T_{smin} = 150 °C

NOTE: NON-HALIDE FLUX SHOULD BE USED.

* RECOMMENDED PEAK TEMPERATURE FOR WIDEBODY 400mils PACKAGE IS 245 °C

Regulatory Information

The ACPL-3130/J313 and ACNW3130 are approved by the following organizations:

IEC/EN/DIN EN 60747-5-5
(ACPL-3130 Option 060 only, ACPL-J313 and ACNW3130)
Approval under:
IEC 60747-5-5
EN 60747-5-5:2011
DIN EN 60747-5-5 (VDE 0884-5):2011-11

UL
Approval under UL 1577, component recognition program, File E55361.

CSA
Approval under CSA Component Acceptance Notice #5, File CA 88324.

Table 1. IEC/EN/DIN EN 60747-5-5 Insulation Characteristics*

Description	Symbol	ACPL-3130 Option 060	ACPL-J313	ACNW3130	Unit
Installation classification per DIN VDE 0110/1.89, Table 1					
for rated mains voltage ≤ 150 V_{rms}		I – IV	I – IV	I – IV	
for rated mains voltage ≤ 300 V_{rms}		I – IV	I – IV	I – IV	
for rated mains voltage ≤ 450 V_{rms}		I – III	I – III	I – IV	
for rated mains voltage ≤ 600 V_{rms}			I – III	I – IV	
for rated mains voltage ≤ 1000 V_{rms}				I – III	
Climatic Classification		55/100/21	55/100/21	55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	2	2	
Maximum Working Insulation Voltage	V_{IORM}	630	1230	1414	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875=V_{PR}, 100% Production Test with t_m=1 sec, Partial discharge < 5 pC	V_{PR}	1181	1670	2652	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.6=V_{PR}, Type and Sample Test, t_m=10 sec, Partial discharge < 5 pC	V_{PR}	1008	1968	2262	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage tini = 60 sec)	V_{IOTM}	6000	8000	8000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure, also see Figure 41 and 42.					
Case Temperature	T_S	175	175	150	°C
Input Current	$I_{S, INPUT}$	230	400	400	mA
Output Power	$P_{S, OUTPUT}$	600	600	700	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	$>10^9$	$>10^9$	Ω

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.
Note: These optocouplers are suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits. Surface mount classification is Class A in accordance with CECC 00802.

Table 2. Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-3130	ACPL-J313	ACNW3130	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	7.1	7.4	9.6	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	7.4	8.0	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.5	1.0	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	> 175	> 175	> 200	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

All Avago data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered. There are recommended techniques such as grooves and ribs which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

Table 3. Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Note
Storage Temperature		T_S	-55	125	°C	
Operating Temperature		T_A	-40	100	°C	
Average Input Current		$I_{F(AVG)}$		25	mA	1
Peak Transient Input Current (<1 µs pulse width, 300pps)		$I_{F(TRAN)}$		1.0	A	
Reverse Input Voltage	ACPL-3130	V_R		5	V	
	ACPL-J313			5	V	
	ACNW3130			5	V	
"High" Peak Output Current		$I_{OH(PEAK)}$		2.5	A	2
"Low" Peak Output Current		$I_{OL(PEAK)}$		2.5	A	2
Supply Voltage		$V_{CC} – V_{EE}$	0	35	V	
Input Current (Rise/Fall Time)		$t_{r(IN)} / t_{f(IN)}$		500	ns	
Output Voltage		$V_{O(PEAK)}$	0	V_{CC}	V	
Output Power Dissipation		P_O		250	mW	3
Total Power Dissipation		P_T		295	mW	4
Lead Solder Temperature	ACPL-3130	260°C for 10 sec., 1.6 mm below seating plane				
	ACPL-J313					
	ACNW3130	260°C for 10 sec., up to seating plane				
Solder Reflow Temperature Profile		See Package Outline Drawings section				

Table 4. Recommended Operating Conditions

Parameter		Symbol	Min.	Max.	Units	Note
Power Supply		V_{CC} - V_{EE}	15	30	V	
Input Current (ON)	ACPL-3130	$I_{F(ON)}$	7	16	mA	
	ACPL-J313					
	ACNW3130		10	16	mA	
Input Voltage (OFF)		$V_{F(OFF)}$	- 3.6	0.8	V	
Operating Temperature		T_A	- 40	100	°C	

Table 5. Electrical Specifications (DC)

Over recommended operating conditions (T_A = -40 to 100°C, for ACPL-3130,ACPL-J313 $I_{F(ON)}$ = 7 to 16mA, for ACNW3130 $I_{F(ON)}$ = 10 to 16mA, $V_{F(OFF)}$ = -3.6 to 0.8 V, V_{CC} = 15 to 30 V, V_{EE} = Ground) unless otherwise specified. All typical values at T_A = 25°C and V_{CC} - V_{EE} = 30 V, unless otherwise noted.

Parameter	Symbol	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}		0.5	1.5		A	$V_O = V_{CC} - 4$	2, 3, 21	5
			2.0			A	$V_O = V_{CC} - 15$		2
Low Level Output Current	I_{OL}		0.5	2.0		A	$V_O = V_{EE} + 2.5$	5, 6, 22	5
			2.0			A	$V_O = V_{EE} + 15$		2
High Level Output Voltage	V_{OH}		V_{CC}-4	V_{CC}-3		V	I_O = -100 mA	1, 3, 23	6, 7
Low Level Output Voltage	V_{OL}			0.1	0.5	V	I_O = 100 mA	4, 6, 24	
High Level Supply Current	I_{CCH}			2.5	5.0	mA	Output open, I_F = 7 to 16 mA	7, 8	
Low Level Supply Current	I_{CCL}			2.5	5.0	mA	Output open, V_F = -3.0 to +0.8 V		
Threshold Input Current Low to High	I_{FLH}	ACPL-3130		2.3	5.0	mA	I_O = 0 mA, V_O > 5 V	9, 17, 25	
		ACPL-J313		1.0	5.0	mA	I_O = 0 mA, V_O > 5 V	10, 18, 25	
		ACNW3130		2.3	8.0	mA	I_O = 0 mA, V_O > 5 V	11, 17, 25	
Threshold Input Voltage High to Low	V_{FHL}		0.8			V	I_O = 0 mA, V_O > 5 V		
Input Forward Voltage	V_F	ACPL-3130	1.2	1.5	1.8	V	I_F = 10 mA	19	
		ACPL-J313	1.2	1.6	1.95	V	I_F = 10 mA	20	
		ACNW3130	1.2	1.6	1.95	V	I_F = 10 mA	20	
Temperature Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T_A$	ACPL-3130		-1.6		mV/°C	I_F = 10 mA		
		ACPL-J313		-1.3		mV/°C	I_F = 10 mA		
		ACNW3130		-1.3		mV/°C	I_F = 10 mA		
Input Reverse Breakdown Voltage	BV_R	ACPL-3130	5			V	I_R = 10 µA		
		ACPL-J313	3			V	I_R = 100 µA		
		ACNW3130	3			V	I_R = 100 µA		
Input Capacitance	C_{IN}	ACPL-3130		60		pF	f = 1 MHz, V_F = 0 V		
		ACPL-J313		70		pF	f = 1 MHz, V_F = 0 V		
		ACNW3130		70		pF	f = 1 MHz, V_F = 0 V		
UVLO Threshold	V_{UVLO+}		11.0	12.3	13.5	V	I_F = 10 mA, V_O > 5 V	26, 38	
	V_{UVLO-}		9.5	10.7	12.0	V	I_F = 10 mA, V_O > 5 V	26, 38	
UVLO Hysteresis	$UVLO_{HYS}$			1.6		V	I_F = 10 mA, V_O > 5 V	26, 38	

Table 6. Switching Specifications (AC)

Over recommended operating conditions (T_A = -40 to 100°C, for ACPL-3130,ACPL-J313 $I_{F(ON)}$ = 7 to 16mA, for ACNW3130 $I_{F(ON)}$ = 10 to 16mA, $V_{F(OFF)}$ = -3.6 to 0.8 V, V_{CC} = 15 to 30 V, V_{EE} = Ground) unless otherwise specified. All typical values at T_A = 25°C and V_{CC} - V_{EE} = 30 V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	0.10	0.30	0.50	µs	Rg = 10 Ω, Cg = 10 nF, f = 10 kHz, Duty Cycle = 50%	12,13, 14, 15, 16, 27	16
Propagation Delay Time to Low Output Level	t_{PHL}	0.10	0.30	0.50	µs			
Pulse Width Distortion	PWD			0.3	µs			17
Propagation Delay Difference Between Any Two Parts or Channels	PDD							
	(t_{PHL} – t_{PLH})	-0.35		0.35	µs		39, 40	12
Rise Time	t_R		0.1		µs		27	
Fall Time	t_F		0.1		µs			
UVLO Turn On Delay	$t_{UVLO\ ON}$		0.8		µs	I_F = 10 mA, V_O > 5 V	26	
UVLO Turn Off Delay	$t_{UVLO\ OFF}$		0.6		µs	I_F = 10 mA, V_O > 5 V	26	
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	40	50		kV/ µs	T_A = 25°C, I_F = 10 to 16 mA, V_{CM} = 1500 V, V_{CC} = 30 V	27	13, 14
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	40	50		kV/ µs	T_A = 25°C, V_F = 0 V, V_{CM} = 1500 V V_{CC} = 30 V	27	13, 15

Table 7. Package Characteristics

Over recommended temperature (T_A = -40 to 100°C) unless otherwise specified. All typicals at T_A = 25°C.

Parameter	Symbol	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage**	V_{ISO}	ACPL-3130	3750			V_{rms}	RH < 50%, t = 1 min., T_A = 25°C		8, 11
		ACPL-J313	3750			V_{rms}			9, 11
		ACNW3130	5000			V_{rms}			10, 11
Resistance (Input-Output)	R_{I-O}	ACPL-3130		10^{12}		Ω	V_{I-O} = 500 V		11
		ACPL-J313		10^{12}		Ω	V_{I-O} = 500 V		
		ACNW3130	10^{12}	10^{13}		Ω	V_{I-O} = 500 V, T_A = 25°C		
			10^{11}			Ω	V_{I-O} = 500 V, T_A = 100°C		
Capacitance (Input-Output)	C_{I-O}	ACPL-3130		0.6		pF	Freq=1 MHz		
		ACPL-J313		0.8		pF	Freq=1 MHz		
		ACNW3130		0.5	0.6	pF	Freq=1 MHz		
LED-to-Case Thermal Resistance	θ_{LC}			467		°C/W	Thermocouple located at center underside of package	32	
LED-to-Detector Thermal Resistance	θ_{LD}			442		°C/W		32	
Detector-to-Case Thermal Resistance	θ_{DC}			126		°C/W		32	

** The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to your equipment level safety specification or Avago Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Derate linearly above 70° C free-air temperature at a rate of 0.3 mA/°C.
2. Maximum pulse width = 10 µs, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with $I_{O\ peak}$ minimum = 2.0 A. See Applications section for additional details on limiting I_{OH} peak.
3. Derate linearly above 70° C free-air temperature at a rate of 4.8 mW/°C.
4. Derate linearly above 70° C free-air temperature at a rate of 5.4 mW/°C. The maximum LED junction temperature should not exceed 125°C.
5. Maximum pulse width = 50 µs, maximum duty cycle = 0.5%.
6. In this test V_{OH} is measured with a dc load current. When driving capacitive loads V_{OH} will approach V_{CC} as I_{OH} approaches zero amps.
7. Maximum pulse width = 1 ms, maximum duty cycle = 20%.
8. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V_{rms} for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ µA).
9. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V_{rms} for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ µA).
10. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{rms} for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ µA).
11. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
12. The difference between t_{PHL} and t_{PLH} between any two ACPL-3130, ACPL-J313 or ACNW3130 parts under the same test condition.
13. Pins 1 and 4 need to be connected to LED common.
14. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., $V_O > 15.0$ V).
15. Common mode transient immunity in a low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., $V_O < 1.0$ V).
16. This load condition approximates the gate load of a 1200 V/75A IGBT.
17. Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given device.

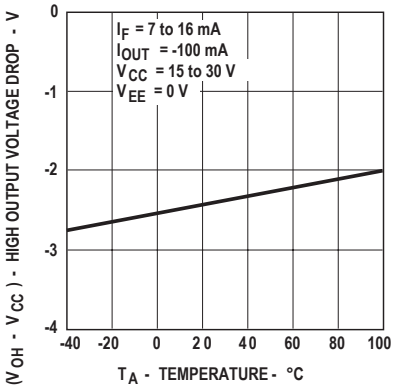


Figure 1. V_{OH} vs. Temperature.

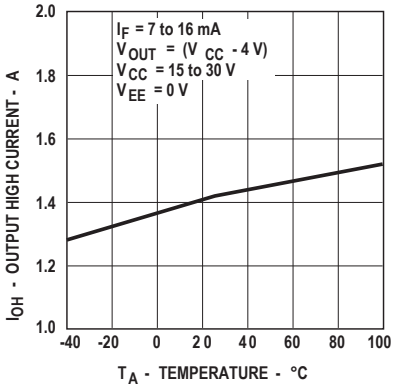


Figure 2. I_{OH} vs. Temperature.

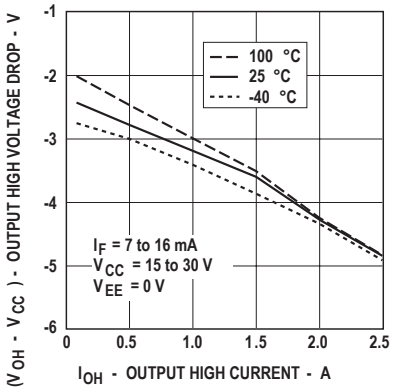


Figure 3. V_{OH} vs. I_{OH}.

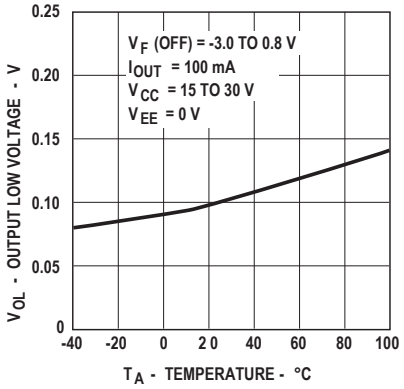


Figure 4. V_{OL} vs. Temperature.

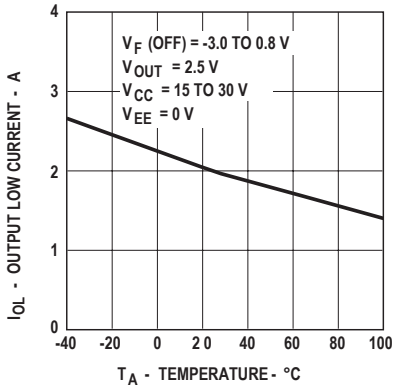


Figure 5. I_{OL} vs. Temperature.

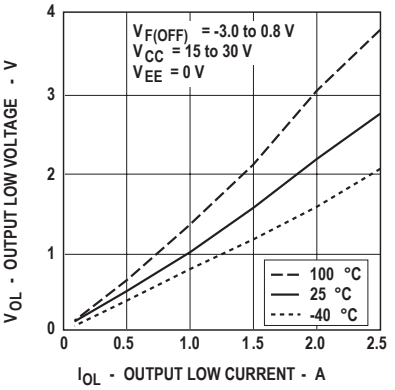


Figure 6. V_{OL} vs. I_{OL}.

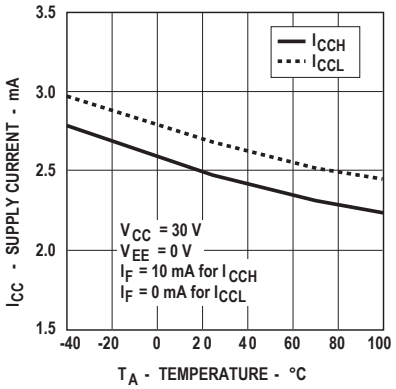


Figure 7. I_{CC} vs. Temperature.

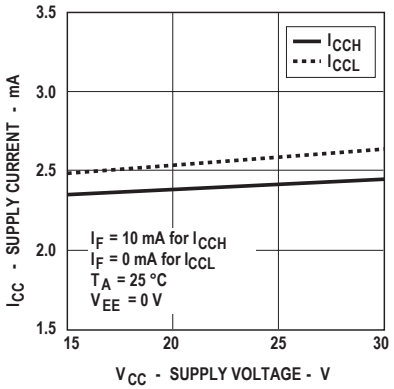


Figure 8. I_{CC} vs. V_{CC}.

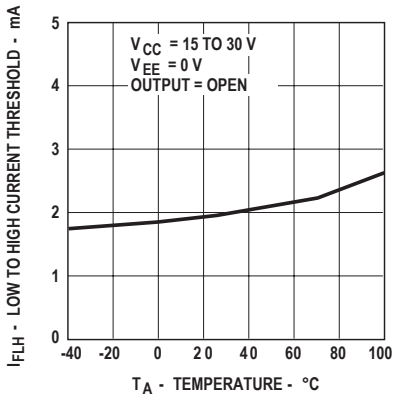


Figure 9. I_{FLH} vs. Temperature. (ACPL-3130)

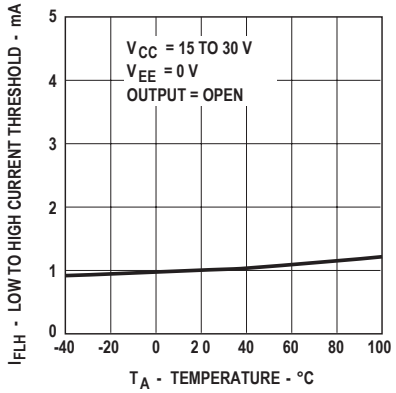


Figure 10. I_{FLH} vs. Temperature. (ACPL-J313)

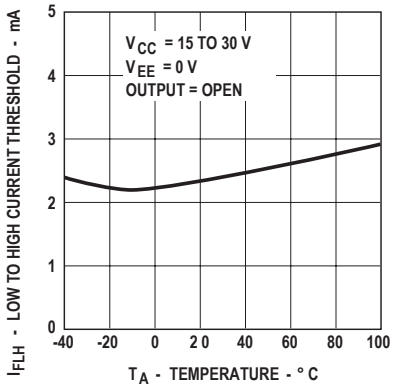


Figure 11. I_{FLH} vs. Temperature. (ACNW3130)

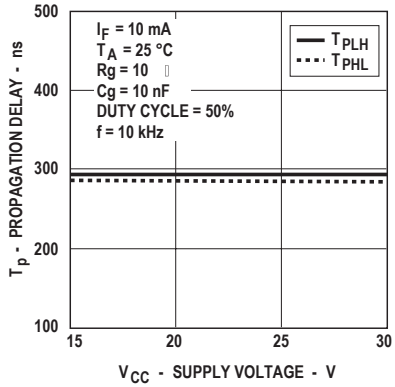


Figure 12. Propagation Delay vs. V_{CC}.

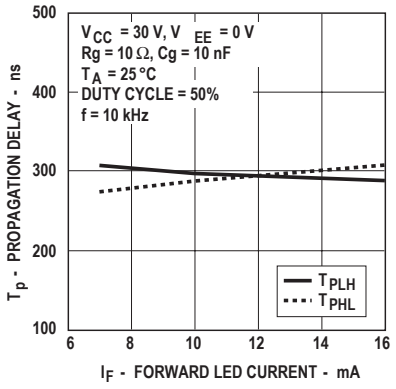


Figure 13. Propagation Delay vs. I_F.

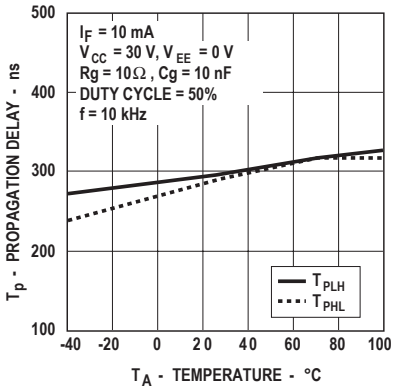


Figure 14. Propagation Delay vs. Temperature.

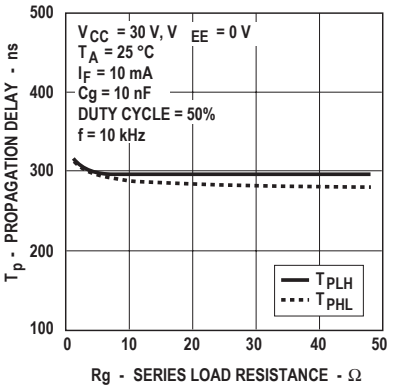


Figure 15. Propagation Delay vs. Rg.

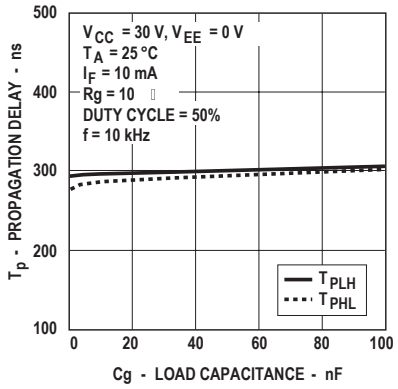


Figure 16. Propagation Delay vs. Cg.

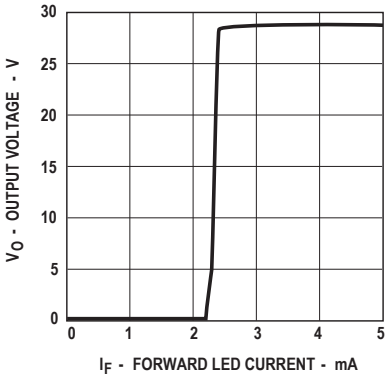


Figure 17. Transfer Characteristics (ACPL-3130 / ACNW3130)

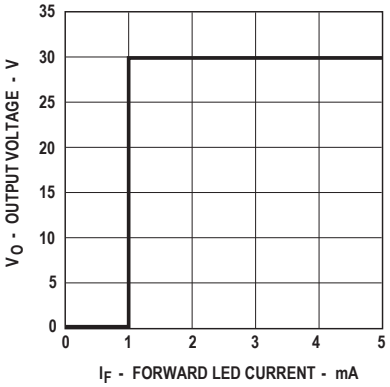


Figure 18. Transfer Characteristics (ACPL-J313)

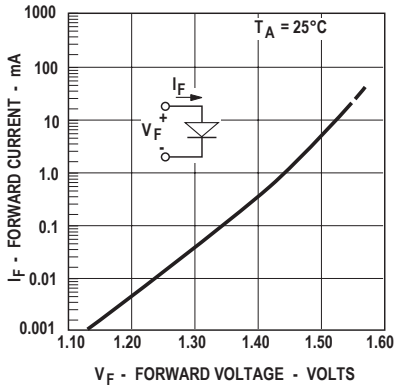


Figure 19. I_F vs. V_F. (ACPL-3130)

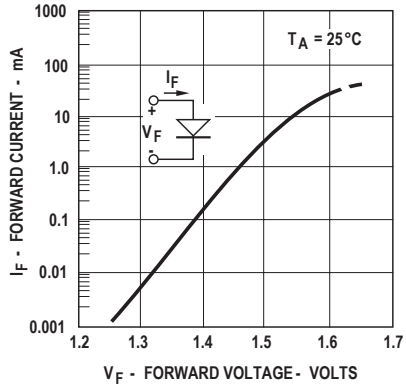


Figure 20. I_F vs. V_F. (ACPL-J313 / ACNW3130)

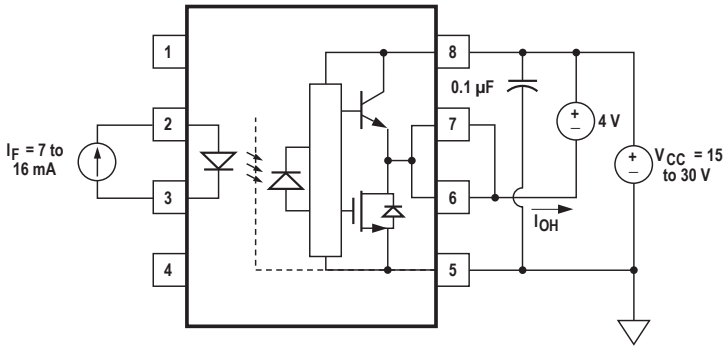


Figure 21. I_{OH} Test Circuit.

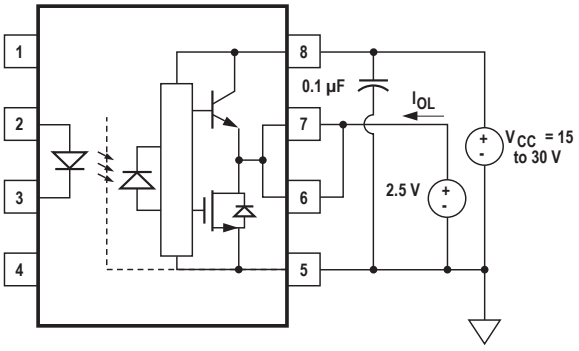


Figure 22. I_{OL} Test Circuit.

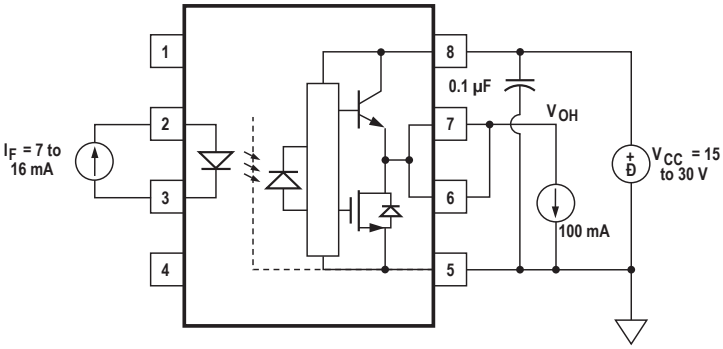


Figure 23. V_{OH} Test Circuit.

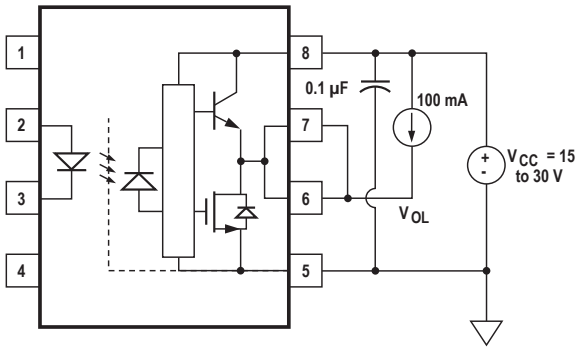


Figure 24. V_{OL} Test Circuit.

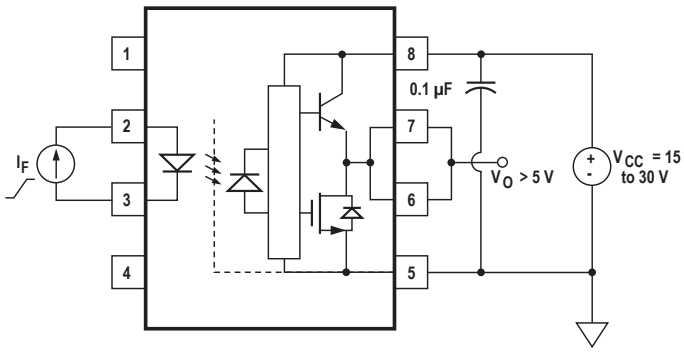


Figure 25. I_{FLH} Test Circuit.

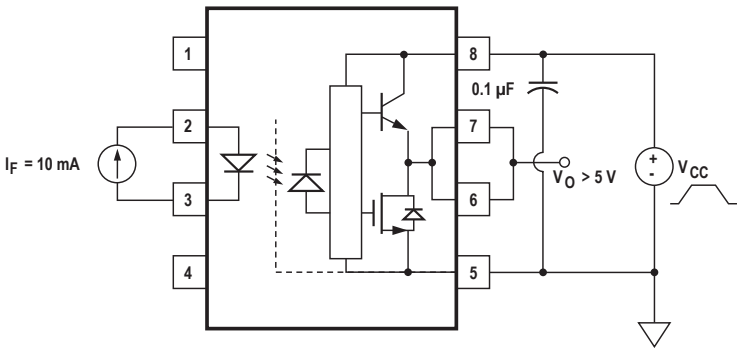
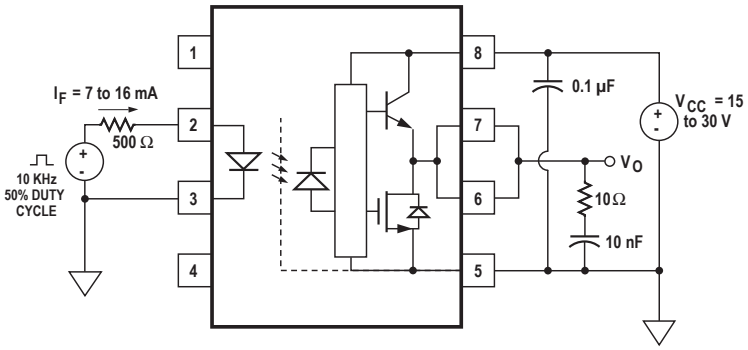


Figure 26. UVLO Test Circuit.



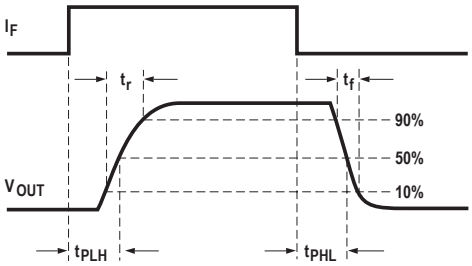
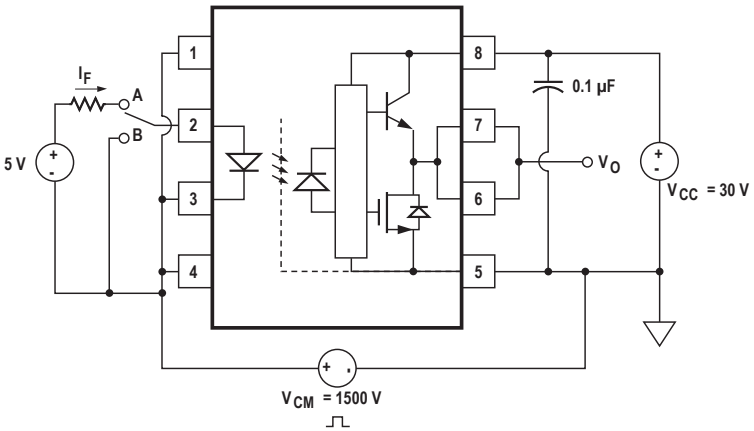


Figure 27. t_{PLH}, t_{PHL}, t_r, and t_f Test Circuit and Waveforms.



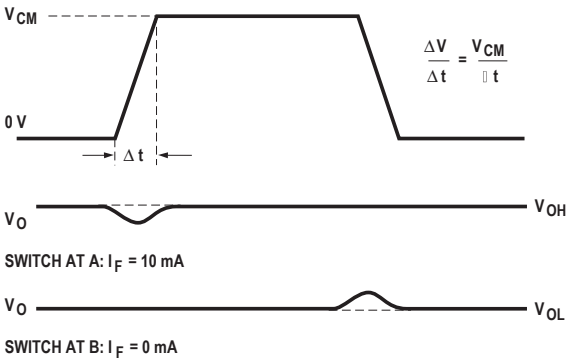


Figure 28. CMR Test Circuit and Waveforms.

Applications Information

Eliminating Negative IGBT Gate Drive (Discussion applies to ACPL-3130, ACPL-J313, and ACNW3130)

To keep the IGBT firmly off, the ACPL-3130 has a very low maximum VOL specification of 0.5 V. The ACPL-3130 realizes this very low V_{OL} by using a DMOS transistor with 1 Ω (typical) on resistance in its pull down circuit. When the ACPL-3130 is in the low state, the IGBT gate is shorted to the emitter by R_g + 1 Ω. Minimizing R_g and the lead inductance from the ACPL-3130 to the IGBT gate and emitter (possibly by mounting the ACPL-3130 on a small PC board directly above the IGBT) can eliminate the need for negative IGBT gate drive in many applications as shown in Figure 29. Care should be taken with such a PC board design to avoid routing the IGBT collector or emitter traces close to the ACPL-3130 input as this can result in unwanted coupling of transient signals into the ACPL-3130 and degrade performance. (If the IGBT drain must be routed near the ACPL-3130 input, then the LED should be reverse-biased when in the off state, to prevent the transient signals coupled from the IGBT drain from turning on the ACPL-3130.)

Selecting the Gate Resistor (R_g) to Minimize IGBT Switching Losses. (Discussion applies to ACPL-3130, ACPL-J313 and ACNW3130)

Step 1: Calculate Rg minimum from the I_{OL} peak specification. The IGBT and R_g in Figure 30 can be analyzed as a simple RC circuit with a voltage supplied by the ACPL-3130.

$$R_g \geq \frac{V_{CC} - V_{EE} - V_{OL}}{I_{OLPEAK}} = \frac{15 + 5 - 2}{2.5} = 7.2\Omega \cong 8\Omega$$

The V_{OL} value of 2 V in the previous equation is a conservative value of V_{OL} at the peak current of 2.5A (see Figure 6). At lower R_g values the voltage supplied by the ACPL-3130 is not an ideal voltage step. This results in lower peak currents (more margin) than predicted by this analysis. When negative gate drive is not used V_{EE} in the previous equation is equal to zero volts.

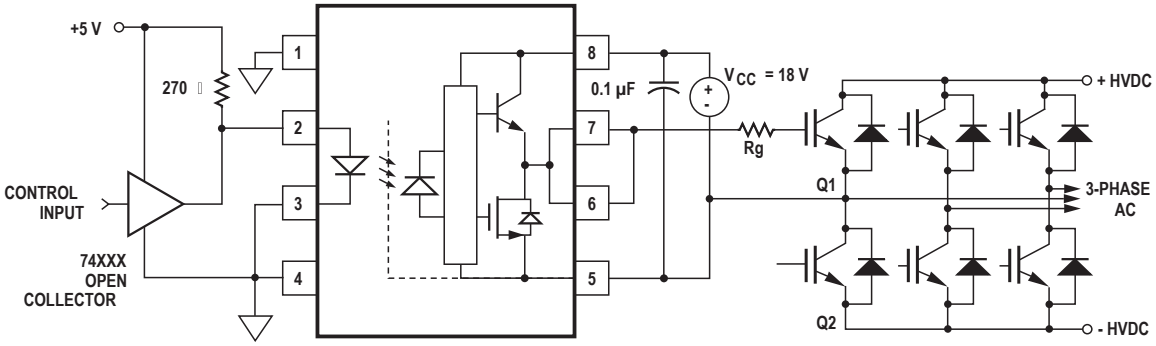


Figure 29. Recommended LED Drive and Application Circuit.

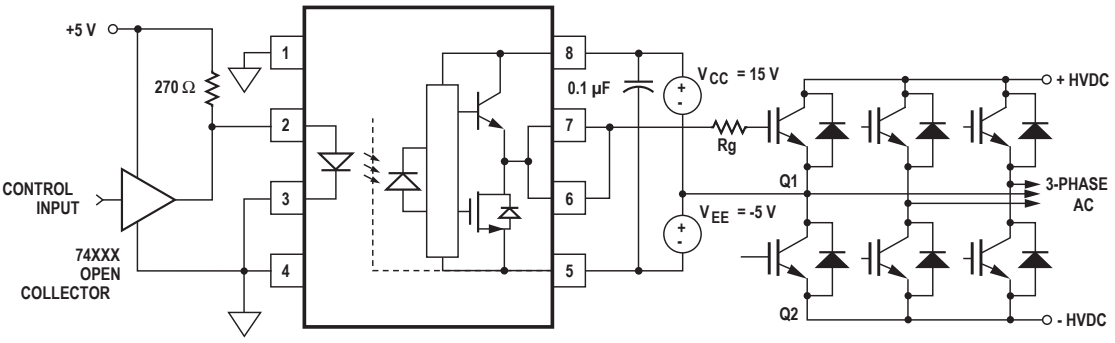


Figure 30. ACPL-3130 Typical Application Circuit with Negative IGBT Gate Drive.

Step 2: Check the ACPL-3130 Power Dissipation and Increase R_g if Necessary. The ACPL-3130 total power dissipation (P_T) is equal to the sum of the emitter power (P_E) and the output power (P_O):

$$P_T = P_E + P_O$$

$$P_E = I_F \bullet V_F \bullet \text{DutyCycle}$$

$$P_O = P_{O(BIAS)} + P_{O(SWITCHING)} = I_{CC} \bullet V_{CC} + E_{SW}(R_g; Q_g) \bullet f$$

PE Parameter	Description
I_F	LED Current
V_F	LED On Voltage
Duty Cycle	Maximum LED Duty Cycle
PO Parameter	**Description**
I_{CC}	Supply Current
V_{CC}	Positive Supply Voltage
V_{EE}	Negative Supply Voltage
$E_{SW(Rg,Qg)}$	Energy Dissipated in the ACPL-3130 for each IGBT Switching Cycle (See Figure 31)
f	Switching Frequency

For the circuit in Figure 30 with I_F (worst case) = 16 mA, R_g = 8 Ω, Max Duty Cycle = 80%, Q_g = 500 nC, f = 20 kHz and T_A max = 85°C:

$$P_E = 16\text{mA} \bullet 1.8\text{V} \bullet 0.8 = 23\text{mW}$$

$$P_O = 4.25\text{mA} \bullet 20\text{V} + 5.2\mu\text{J} \bullet 20\text{kHz}$$

$$= 85\text{mW} + 104\text{mW}$$

$$= 189\text{mW}$$

$$> 178\text{mW}\left(P_{O(MAX)} @ 85°C = 250\text{mW} - 15°C \bullet 4.8\text{mW}/°C\right)$$

The value of 4.25 mA for I_{CC} in the previous equation was obtained by derating the I_{CC} max of 5 mA (which occurs at -40°C) to I_{CC} max at 85°C (see Figure 7).

$$P_{O(SWITCHING\,MAX)} = P_{O(MAX)} - P_{O(BIAS)}$$

$$= 178\text{mW} - 85\text{mW}$$

$$= 93\text{mW}$$

$$E_{SW(MAX)} = \frac{P_{O(SWITCHING\,MAX)}}{f}$$

$$= \frac{93\text{mW}}{20\text{kHz}} = 4.65\mu\text{J}$$

Since P_O for this case is greater than $P_{O(MAX)}$, R_g must be increased to reduce the ACPL-3130 power dissipation.

For Q_g = 500 nC, from Figure 31, a value of E_{SW} = 4.65 µJ gives a R_g = 10.3 Ω.

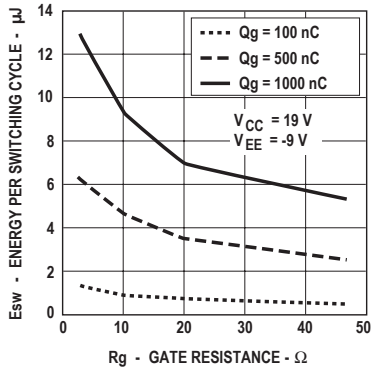
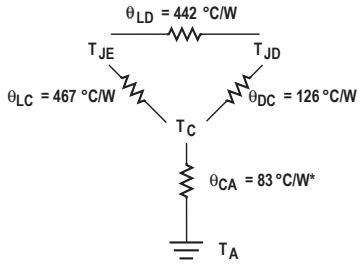


Figure 31. Energy Dissipated in the ACPL-3130 for Each IGBT Switching Cycle.

Thermal Model
(Discussion applies to ACPL-3130, ACPL-J313 and



ACNW3130)

T_{JE} = LED junction temperature

T_{JD} = detector IC junction temperature

T_C = case temperature measured at the center of the package bottom

θ_{LC} = LED-to-case thermal resistance

θ_{LD} = LED-to-detector thermal resistance

θ_{DC} = detector-to-case thermal resistance

θ_{CA} = case-to-ambient thermal resistance

*θ_{CA} will depend on the board design and the placement of the part.

Figure 32. Thermal Model.

The steady state thermal model for the ACPL-3130 is shown in Figure 32. The thermal resistance values given in this model can be used to calculate the temperatures at each node for a given operating condition. As shown by the model, all heat generated flows through θ_{CA} which raises the case temperature T_C accordingly. The value of θ_{CA} depends on the conditions of the board design and is, therefore, determined by the designer. The value of θ_{CA} = 83°C/W was obtained from thermal measurements using a 2.5 x 2.5 inch PC board, with small traces (no ground plane), a single ACPL-3130 soldered into the center of the board and still air. The absolute maximum power dissipation derating specifications assume a θ_{CA} value of 83°C/W.

From the thermal mode in Figure 32 the LED and detector IC junction temperatures can be expressed as:

$$T_{JE} = P_E \bullet \left(\theta_{LC} \,||\, \left(\theta_{LD} + \theta_{DC}\right) + \theta_{CA}\right) + P_D \bullet \left(\frac{\theta_{LC} \bullet \theta_{DC}}{\theta_{LC} + \theta_{DC} + \theta_{LD}} + \theta_{CA}\right) + T_A$$

$$T_{JD} = P_E \bullet \left(\frac{\theta_{LC} \bullet \theta_{DC}}{\theta_{LC} + \theta_{DC} + \theta_{LD}} + \theta_{CA}\right) + P_D \bullet \left(\theta_{DC} \,||\, \left(\theta_{LD} + \theta_{LC}\right) + \theta_{CA}\right) + T_A$$

Inserting the values for θ_{LC} and θ_{DC} shown in Figure 32 gives:

$$T_{JE} = P_E \bullet \left(256°C/W + \theta_{CA}\right) + P_D \bullet \left(57°C/W + \theta_{CA}\right) + T_A$$

$$T_{JD} = P_E \bullet \left(57°C/W + \theta_{CA}\right) + P_D \bullet \left(111°C/W + \theta_{CA}\right) + T_A$$

For example, given P_E = 45 mW, P_O = 250 mW, T_A = 70°C and θ_{CA} = 83°C/W:

$$T_{JE} = P_E \bullet 339°C/W + P_D \bullet 140°C/W + T_A$$
$$= 45mW \bullet 339°C/W + 250mW \bullet 140°C/W + 70°C = 120°C$$

$$T_{JD} = P_E \bullet 140°C/W + P_D \bullet 194°C/W + T_A$$
$$= 45mW \bullet 140°C/W + 250mW \bullet 194°C/W + 70°C$$

T_{JE} and T_{JD} should be limited to 125°C based on the board layout and part placement (θ_{CA}) specific to the application

LED Drive Circuit Considerations for Ultra High CMR Performance. (Discussion applies to ACPL-3130, ACPL-J313, and ACNW3130)

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 33. The ACPL-3130 improves CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and optocoupler pins 5-8 as shown in Figure 34. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 29), can achieve 40 kV/µs CMR while minimizing component complexity.

Techniques to keep the LED in the proper state are discussed in the next two sections.

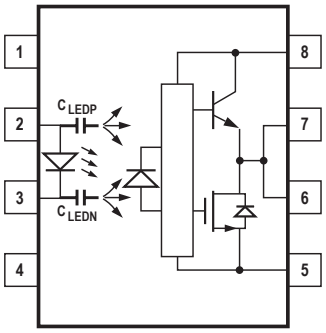


Figure 33. Optocoupler Input to Output Capacitance Model for Unshielded Optocouplers.

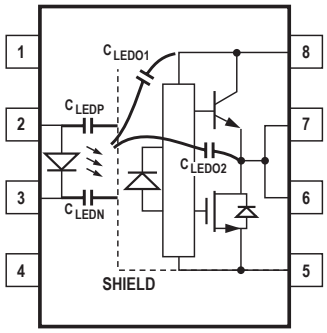


Figure 34. Optocoupler Input to Output Capacitance Model for Shielded Optocouplers.

CMR with the LED On (CMR_H)

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. A minimum LED current of 10 mA provides adequate margin over the maximum I_{FLH} of 5 mA to achieve 40 kV/µs CMR.

CMR with the LED Off (CMR_L)

A high CMR LED drive circuit must keep the LED off ($V_F \leq V_{F(OFF)}$) during common mode transients. For example, during a $-dV_{cm}/dt$ transient in Figure 35, the current flowing through C_{LEDP} also flows through the R_{SAT} and V_{SAT} of the logic gate. As long as the low state voltage developed across the logic gate is less than $V_{F(OFF)}$, the LED will remain off and no common mode failure will occur.

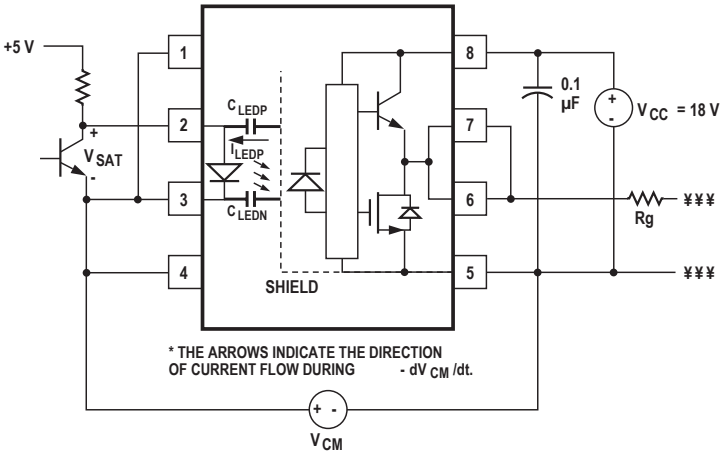


Figure 35. Equivalent Circuit for Figure 29 During Common Mode Transient.

The open collector drive circuit, shown in Figure 36, cannot keep the LED off during a $+dV_{cm}/dt$ transient, since all the current flowing through C_{LEDN} must be supplied by the LED, and it is not recommended for applications requiring ultra high CMR_L performance. Figure 37 is an alternative drive circuit which, like the recommended application circuit (Figure 29), does achieve ultra high CMR performance by shunting the LED in the off state.

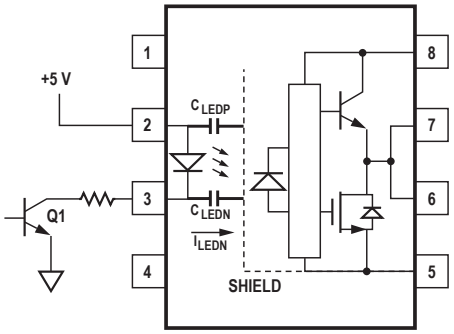


Figure 36. Not Recommended Open Collector Drive Circuit.

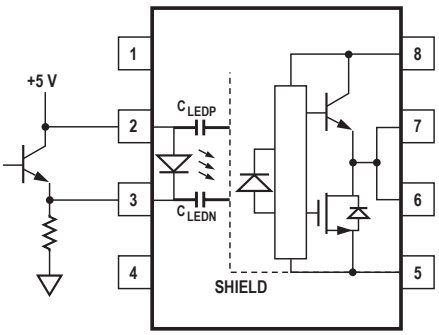


Figure 37. Recommended LED Drive Circuit for Ultra-High CMR.

Under Voltage Lockout Feature. (Discussion applies to ACPL-3130, ACPL-J313, and ACNW3130)

The ACPL-3130 contains an under voltage lockout (UVLO) feature that is designed to protect the IGBT under fault conditions which cause the ACPL-3130 supply voltage (equivalent to the fully-charged IGBT gate voltage) to drop below a level necessary to keep the IGBT in a low resistance state. When the ACPL-3130 output is in the high state and the supply voltage drops below the ACPL-3130 V_{UVLO-} threshold ($9.5 < V_{UVLO-} < 12.0$) the optocoupler output will go into the low state with a typical delay, UVLO Turn Off Delay, of 0.6 µs.

When the ACPL-3130 output is in the low state and the supply voltage rises above the ACPL-3130 V_{UVLO+} threshold ($11.0 < V_{UVLO+} < 13.5$) the optocoupler output will go into the high state (assumes LED is "ON") with a typical delay, UVLO Turn On Delay of 0.8 µs.

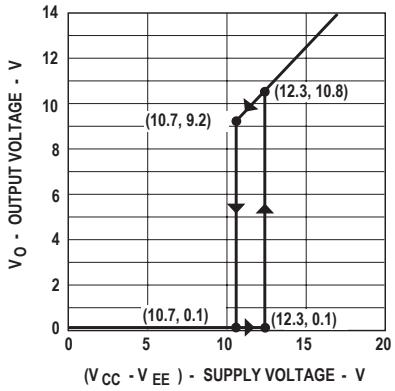


Figure 38. Under Voltage Lock Out.

Dead Time and Propagation Delay Specifications. (Discussion applies to ACPL-3130, ACPL-J313, and ACNW3130)

The ACPL-3130 includes a Propagation Delay Difference (PDD) specification intended to help designers minimize "dead time" in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 29) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high and low voltage motor rails.

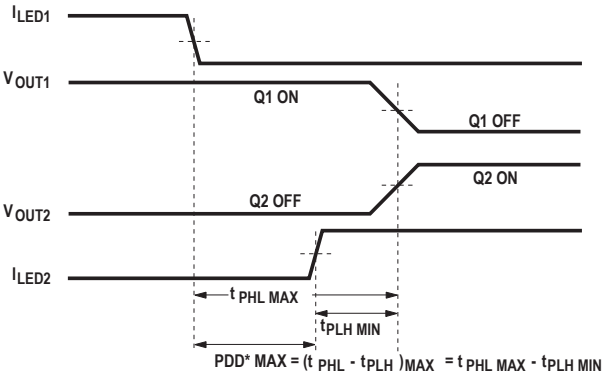
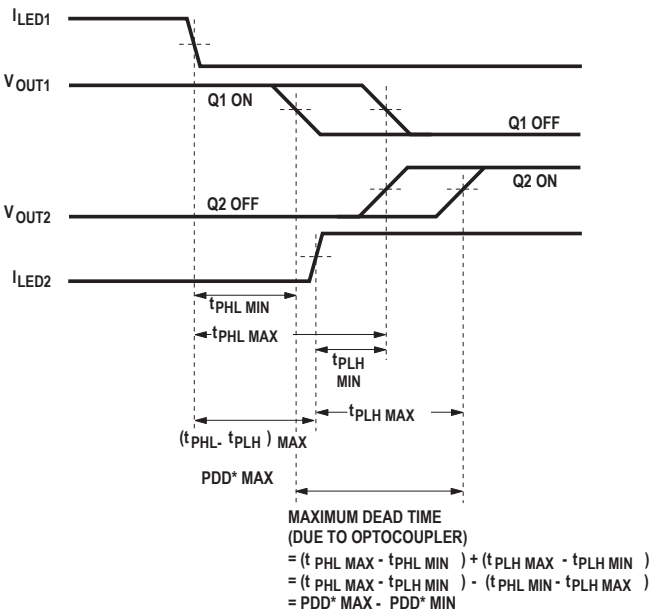


Figure 39. Minimum LED Skew for Zero Dead Time.

To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 35. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDD_{MAX}, which is specified to be 350 ns over the operating temperature range of -40°C to 100°C.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specifications as shown in Figure 40. The maximum dead time for the ACPL-3130 is 700 ns (= 350 ns - (-350 ns)) over an operating temperature range of - 40°C to 100°C.

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.



*PDD = PROPAGATION DELAY DIFFERENCE
NOTE: FOR DEAD TIME AND PDD CALCULATIONS ALL PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

Figure 40. Waveforms for Dead Time.

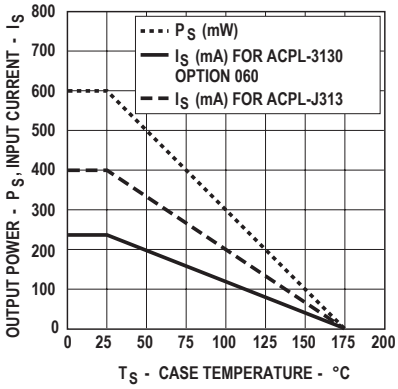


Figure 41. Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per IEC/EN/DIN EN 60747-5-5 for ACPL-3130 (option 060) and ACPL-J313.

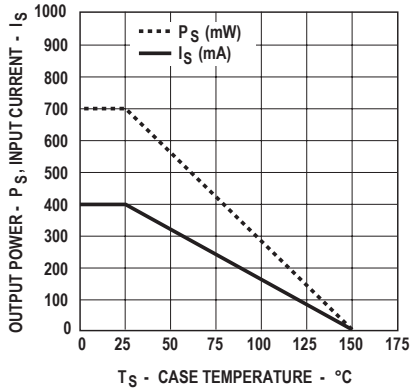


Figure 42. Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per IEC/EN/DIN EN 60747-5-5 for ACNW3130.

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