ACPL-K43T, ACPL-K44T

Automotive R²Coupler™ Wide Operating Temperature 1MBd Digital Optocoupler in a Stretched 8-Pin Surface Mount Plastic Package

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

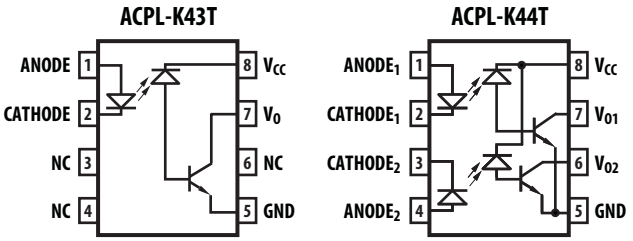
Description

The ACPL-K43T is a single channel, high temperature, high CMR, high speed digital optocoupler in an eight lead miniature footprint specifically used in the automotive applications. The ACPL-K44T is a dual channel equivalent of the ACPL-K43T. Both products are available in the stretched SO-8 package outline, designed to be compatible with standard surface mount processes.

This digital optocoupler uses an insulating layer between the light emitting diode and an integrated photo detector to provide electrical insulation between input and output. Separate connections for the photodiode bias and output transistor collector increase the speed up to a hundred times over that of a conventional photo-transistor coupler by reducing the base-collector capacitance.

Avago R²Coupler isolation products provide with reinforced insulation and reliability that delivers safe signal isolation critical in automotive and high temperature industrial applications.

Functional Diagram



Truth Table

LED	Vo
ON	LOW
OFF	HIGH

Note: The connection of a 0.1 µF bypass capacitor between pins 5 and 8 is recommended.

Features

- High Temperature and Reliability low speed digital interface for Automotive Application
- Ultra low drive for status feedback at I_F = 0.8 mA or 1.5 mA
- 30 kV/µs (Typ) High Common-Mode Rejection at V_{CM} = 1500 V
- Compact, Auto-Insertable Stretched SO8 Packages
- Qualified to AEC Q100 Grade 1 Test Guidelines
- Wide Operating Temperature Range: -40° C to +125° C
- High Speed: 1 MBd
- Low Propagation Delay: 1 µs max. at I_F = 10 mA
- Worldwide Safety Approval:
  - UL 1577 approval, 5 kV_{RMS}/1 min.
  - CSA Approval
  - IEC/EN/DIN EN 60747-5-5

Applications

- Automotive IPM Driver for DC-DC converters and motor inverters
- Status Feedback and Wake-Up Signal Isolation
- CANBus and SPI Communications Interface
- High Temperature Digital/Analog Signal Isolation

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Ordering Information

Specify part number followed by option number (if desired).

Part number	Option (RoHS Compliant)	Package	Surface Mount	Tape & Reel	UL 5000 V_{rms} / 1 Minute rating	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-K43T	-000E	Stretched SO-8	X		X		80 per tube
	-060E		X		X	X	80 per tube
	-500E		X	X	X		1000 per reel
	-560E		X	X	X	X	1000 per reel
ACPL-K44T	-000E	Stretched SO-8	X		X		80 per tube
	-060E		X		X	X	80 per tube
	-500E		X	X	X		1000 per reel
	-560E		X	X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

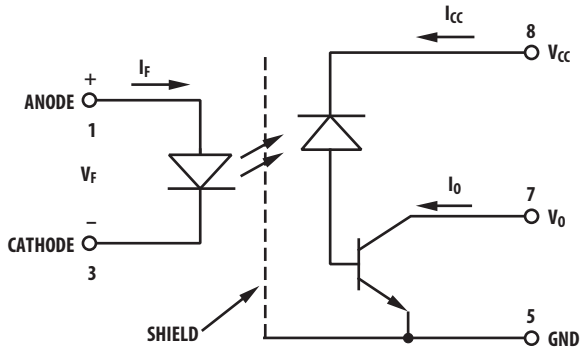
Example 1:

ACPL-K43T-560E to order product of SSO-8 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

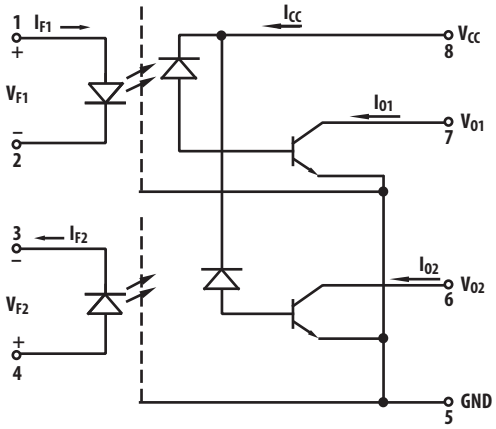
Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Schematic

ACPL-K43T

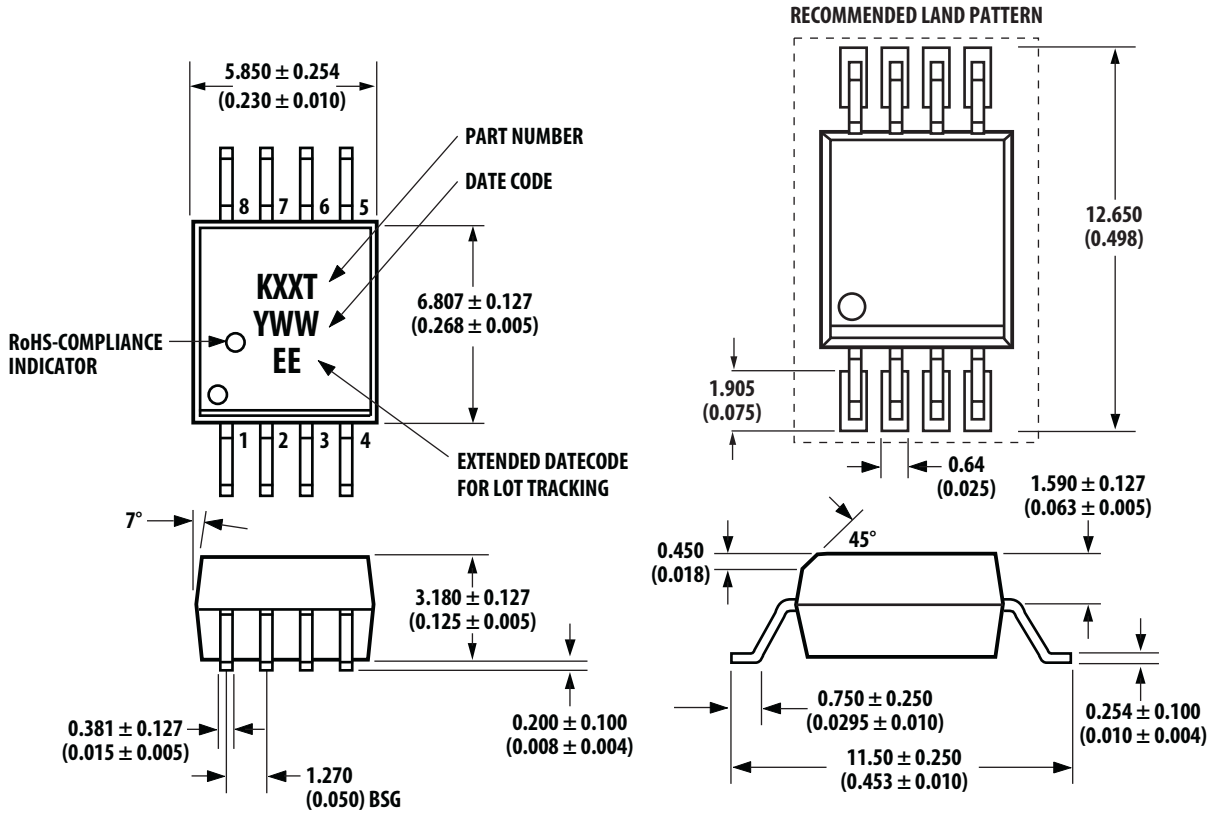


ACPL-K44T



USE OF 0.1 μF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS RECOMMENDED.

Package Outline Dimensions (Stretched SO8)



Dimensions in millimeters and (inches).

Note:
Lead coplanarity = 0.1 mm (0.004 inches).
Floating lead protrusion = 0.25mm (10mils) max.

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).
Note: Non-halide flux should be used.

Regulatory Information

The ACPL-K43T and ACPL-K44T are approved by the following organizations:

UL

UL 1577, component recognition program up to V_{ISO} = 5 kV_{RMS}.

CSA

CSA Component Acceptance Notice #5.

IEC/EN/DIN EN 60747-5-5

IEC 60747-5-5
EN 60747-5-5
DIN EN 60747-5-5

Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-K43T ACPL-K44T	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group (DIN VDE0109)		IIIa		Material Group (DIN VDE 0109)

IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristic (Option 060E and 560E)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 150 V_{rms}		I – IV	
for rated mains voltage ≤ 300 V_{rms}		I – IV	
for rated mains voltage ≤ 450 V_{rms}		I – IV	
for rated mains voltage ≤ 600 V_{rms}		I – IV	
for rated mains voltage ≤ 1000 V_{rms}		I – III	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1140	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial discharge < 5 pC	V_{PR}	2137	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, t_m = 10 sec, Partial discharge < 5 pC	V_{PR}	1824	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	8000	V_{peak}
Safety Limiting Values (Maximum values allowed in the event of a failure)			
Case Temperature	T_S	175	°C
Input Current	$I_{S, INPUT}$	230	mA
Output Power	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Note
Storage Temperature		T_{STG}	-55	150	°C	
Operating Ambient Temperature		T_A	-40	125	°C	
Average Forward Input Current		$I_{F(avg)}$		20	mA	
Peak Forward Input Current (50% duty cycle, 1 ms pulse width)		$I_{F(peak)}$		40	mA	
Peak Transient Input Current (≤ 1 µs pulse width, 300 ps)		$I_{F(trans)}$		100	mA	
Reversed Input Voltage		V_R		5	V	
Input Power Dissipation (per channel)		P_{IN}		30	mW	
Output Power Dissipation		P_O		100	mW	
Average Output Current		I_O		8	mA	
Peak Output Current		$I_{O(pk)}$		16	mA	
Supply Voltag		V_{CC}	-0.5	30	V	
Output Voltage		V_O	-0.5	20	V	
Lead Soldering Cycle	Temperature			260	°C	
	Time			10	s	

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Supply Voltage	V_{CC}		20	V	
Operating Temperature	T_A	-40	125	°C	

Electrical Specifications (DC)

Over recommended operating T_A = -40° C to 125° C, unless otherwise specified

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	32	65	100	%	T_A = 25° C, V_{CC} = 4.5 V, V_O = 0.4 V, I_F = 10 mA	1, 2, 4	1
		24	65					
		33	160			V_{CC} = 4.5 V, V_O = 0.4 V, I_F = 1.5 mA		
		25	165			V_{CC} = 4.5 V, V_O = 0.4 V, I_F = 0.8 mA		
Logic Low Output Voltage	V_{OL}		0.1	0.5	V	V_{CC} = 4.5 V, I_O = 2.4 mA, I_F = 10 mA		
			0.1			V_{CC} = 4.5 V, I_O = 0.5 mA, I_F = 1.5 mA		
			0.1			V_{CC} = 4.5 V, I_O = 0.2 mA, I_F = 0.8 mA		
Logic High Output Current	I_{OH}		$3x10^{-5}$	0.5	µA	T_A = 25° C, V_O = V_{CC} = 5.5 V, I_F = 0 mA	11, 12	
			$8x10^{-5}$	5		V_O = V_{CC} = 20 V		
Logic Low Supply Current (per Channel)	I_{CCL}		85	200	µA	I_F = 10 mA, V_O = open, V_{CC} = 20 V		
			15			I_F = 1.5 mA, V_O = open, V_{CC} = 20 V		
Logic High Supply Current (per Channel)	I_{CCH}		0.02	1	µA	T_A = 25° C, I_F = 10 mA, V_O = open, V_{CC} = 20 V		
				2.5				
Input Forward Voltage	V_F	1.45	1.55	1.75	V	T_A = 25° C, I_F = 10 mA	3	
		1.25	1.55	1.85				
Input Reversed Breakdown Voltage	BV_R	5			V	I_R = 10 µA		
Temperature Coefficient of Forward Voltage	$\Delta V_F / \Delta T_A$		-1.5		mV/°C	I_F =10 mA		
			-1.8			I_F =1.5 mA		
Input Capacitance	C_{IN}		90		pF	F = 1 MHz, V_F = 0		

Switching Specifications (AC)

Over recommended operating (T_A = -40° C to 125° C), V_{CC} = 5.0 V unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions			Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	0.07	0.15	0.8	µs	T_A = 25° C	I_F = 10 mA, R_L = 1.9 kΩ	Pulse: f = 10 kHz, Duty cycle = 50%, V_{CC} = 5.0 V, C_L = 15 pF, V_{THHL} = 1.5 V	5, 6, 7, 8, 9, 10, 13	2, 3
		0.06		1.0						
			0.7	5			I_F = 1.5 mA, R_L = 10 kΩ			
			1	10			I_F = 0.8 mA, R_L = 27 kΩ			
Propagation Delay Time to Logic High at Output	t_{PLH}	0.15	0.5	0.8	µs	T_A = 25° C	I_F = 10 mA, R_L = 1.9 kΩ	Pulse: f = 10 kHz, Duty cycle = 50%, V_{CC} = 5.0 V, C_L = 15 pF, V_{THHL} = 2.0 V	5, 6, 7, 8, 9, 10, 13	2, 3
		0.03		1.0						
			0.9	5			I_F = 1.5 mA, R_L = 10 kΩ			
			2	10			I_F = 0.8 mA, R_L = 27 kΩ			
Pulse Width Distortion	PWD		0.35	0.45	µs	T_A = 25° C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F = 10 mA, V_{CC} = 5.0 V, R_L = 1.9 kΩ, C_L = 15 pF, V_{THHL} = 1.5 V, V_{THLH} = 2.0 V			2, 3, 4
				0.85						
Propagation Delay Difference Between Any 2 Parts	PDD		0.35	0.5	µs	T_A = 25° C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F = 10 mA, V_{CC} = 5.0 V, R_L = 1.9 kΩ, C_L = 15 pF, V_{THHL} = 1.5 V, V_{THLH} = 2.0 V			2, 3, 5
				0.9						
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$	15	30		kV/µs	I_F = 0 mA	V_{CM} = 1500 V_{p-p}, R_L = 1.9 kΩ, V_{CC} = 5 V, T_A = 25° C		14	6
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	15	30		kV/µs	I_F = 10 mA				
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$		5		kV/µs	I_F = 0 mA	V_{CM} = 1500 V_{p-p}, R_L = 10 kΩ, V_{CC} = 5 V, T_A = 25° C		14	6
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$		5		kV/µs	I_F = 1.5 mA				

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	5000			V_{RMS}	RH ≤ 50%, t = 1 min., T_A = 25° C		7, 8
Input-Output Resistance	R_{I-O}		10^{14}		Ω	V_{I-O} = 500 Vdc		7
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 Vdc		7

* The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating.

Notes:

1. Current Transfer Ratio in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100.
2. Use of a 0.1 µF bypass capacitor connected between pins 5 and 8 is recommended.
3. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
4. Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given device.
5. The difference between t_{PLH} and t_{PHL} between any two parts under the same test condition.
6. Common transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the rising edge of the common mode pulse, V_{CM}, to assure that the ouput will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the falling edge of the common mode pulse signal, V_{CM} to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
7. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
8. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{RMS} for 1 second.

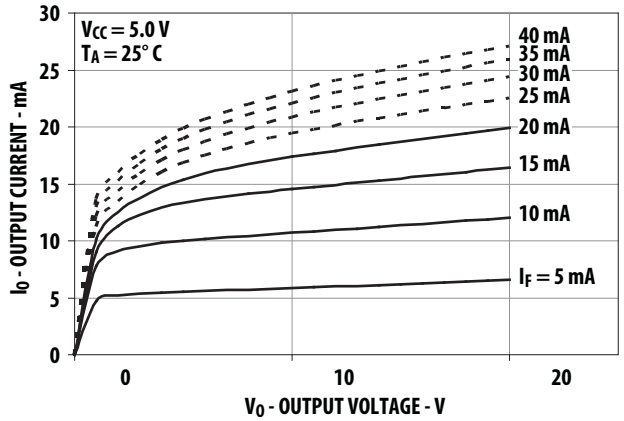


Figure 1. DC and Pulsed Transfer Characteristics

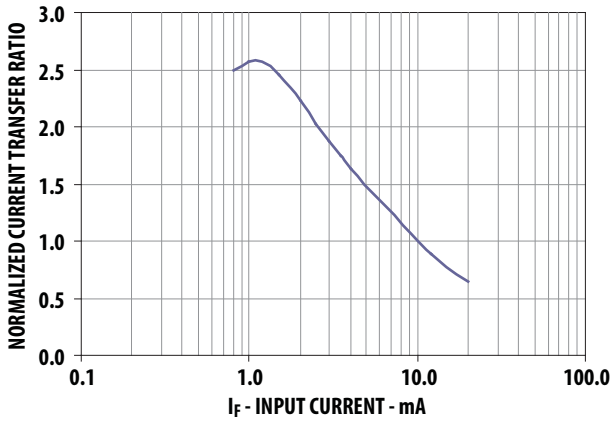


Figure 2. Current Transfer Ratio vs. Input Current V_O = 0.4 V, V_{CC} = 5 V, T_A = 25° C

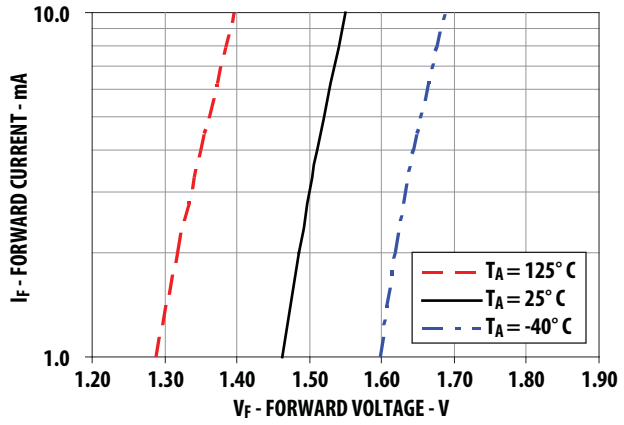


Figure 3. Input Current vs. Forward Voltage

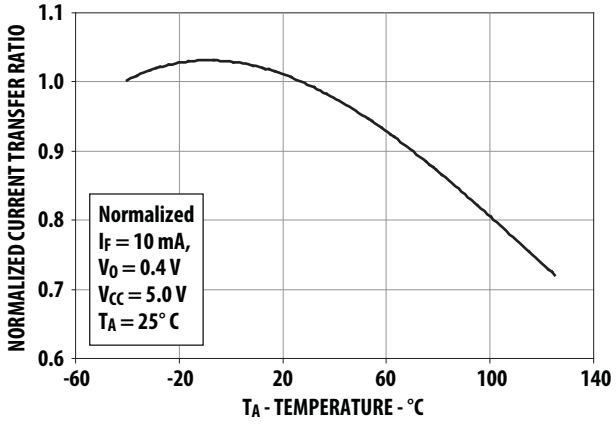


Figure 4. Current Transfer Ratio vs. Temperature

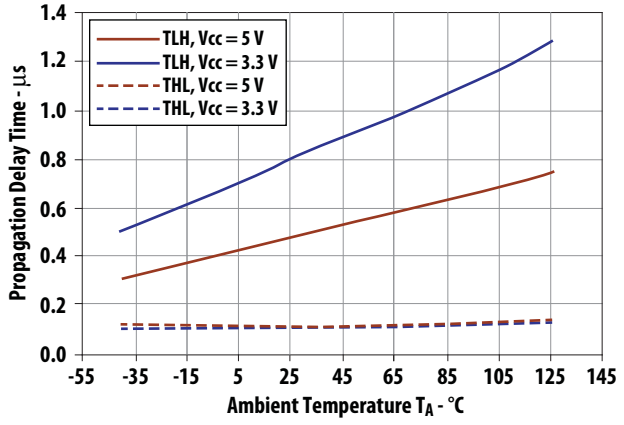


Figure 5, Propagation Delay Time vs. Temperature
I_F = 10 mA, R_L = 1.9 kΩ, C_L = 15 pF

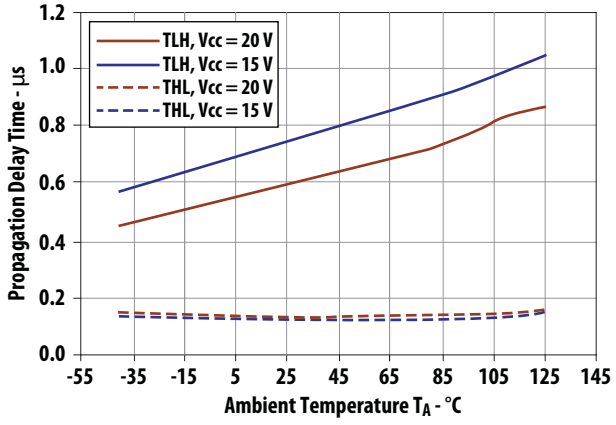


Figure 6. Propagation Delay Time vs. Temperature
I_F = 10 mA, R_L = 20 kΩ, C_L = 100 pF

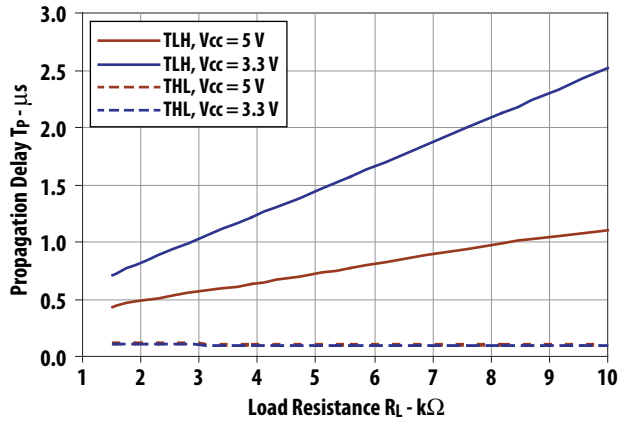


Figure 7. Propagation Delay Time vs. Load Resistance

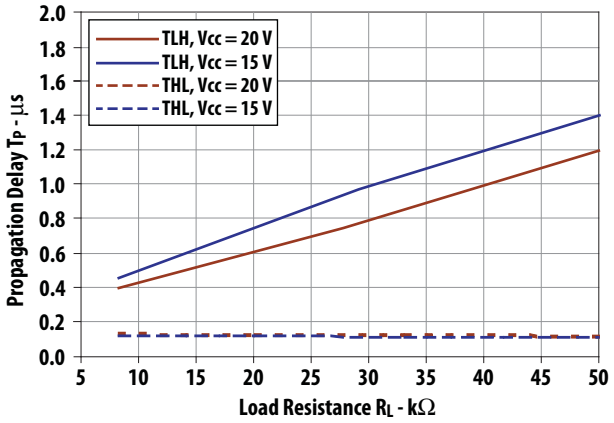


Figure 8. Propagation Delay Time vs. Load Resistance

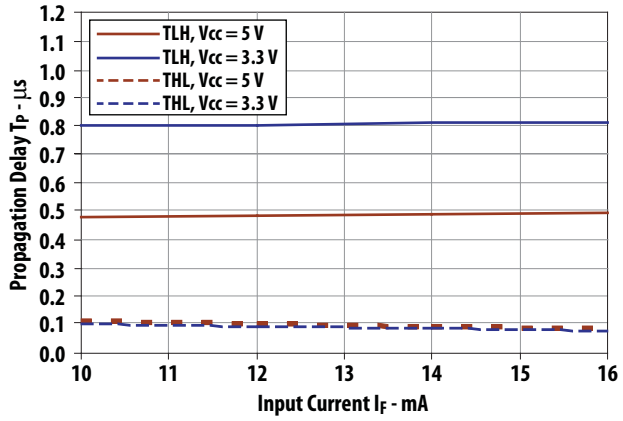


Figure 9. Propagation Delay Time vs. Input Current
$R_L = 1.9\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°\ C$

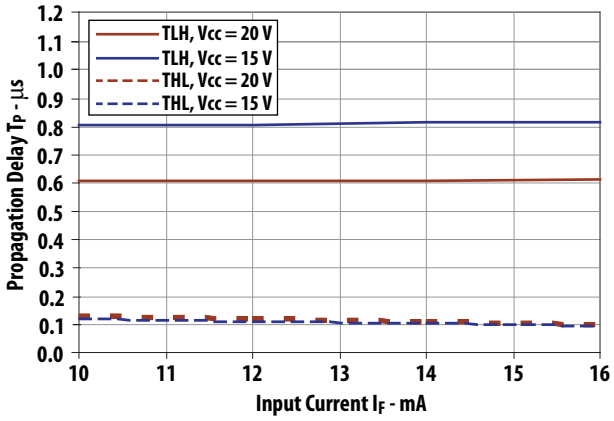


Figure 10. Propagation Delay Time vs. Input Current
$R_L = 20\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°\ C$

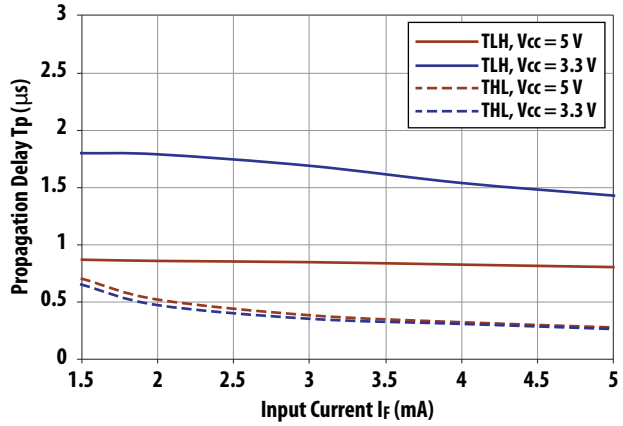


Figure 10a. Propagation Delay Time vs. Input Current
$R_L = 10\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°\ C$

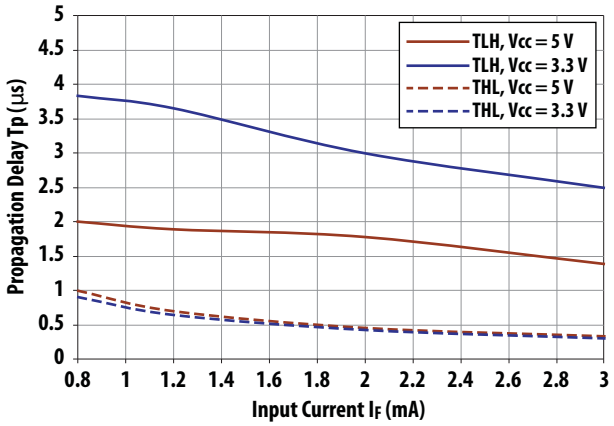


Figure 10b. Propagation Delay Time vs. Input Current
$R_L = 27\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°\ C$

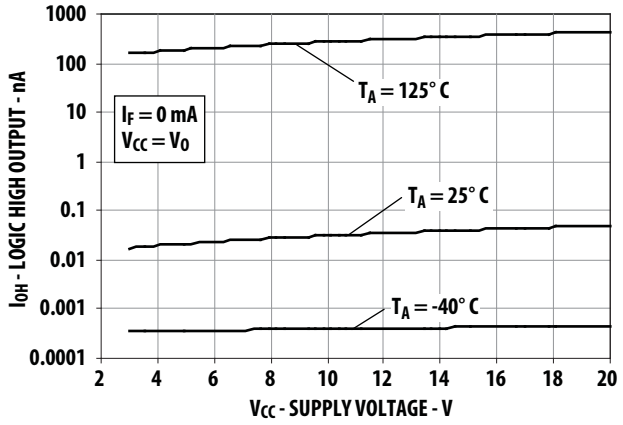


Figure 11. Logic High Output Current vs Supply Voltage

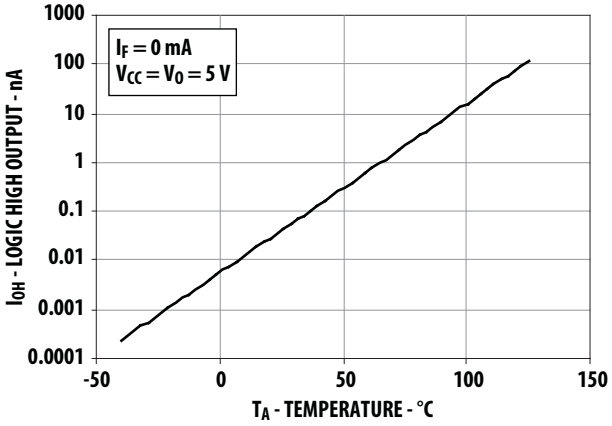


Figure 12. Logic High Output Current vs Temperature

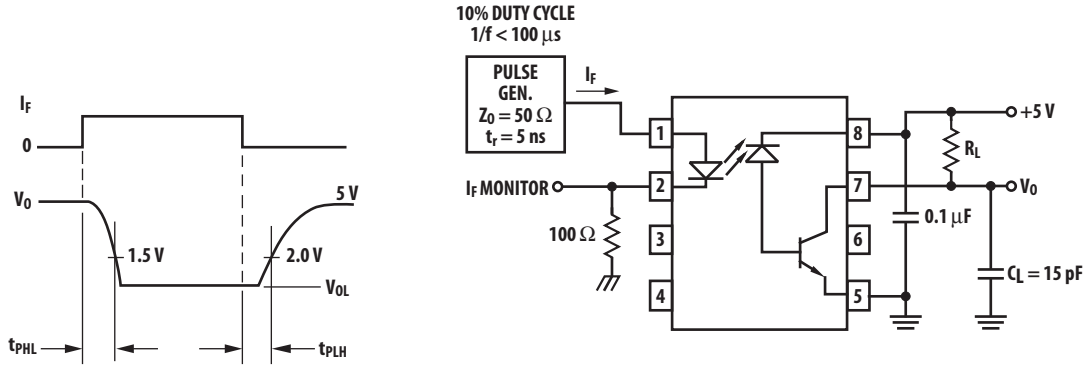


Figure 13. Switching Test Circuit

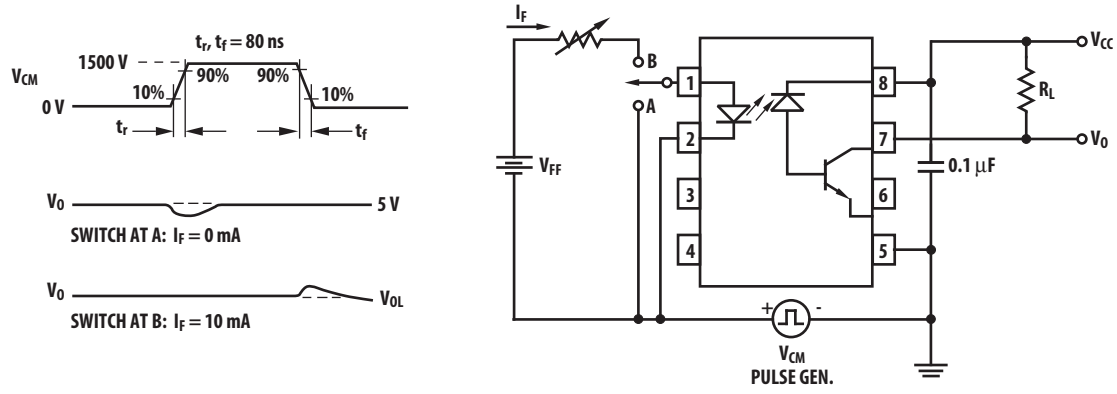


Figure 14. Test Circuit for Transient Immunity and Typical Waveforms

Thermal Resistance Model for ACPL-K43T

The diagram of ACPL-K43T for measurement is shown in Figure 15. Here, one die is heated first and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the 2nd die is heated and all the dice temperatures are recorded. With the known ambient temperature, the die junction temperature and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in matrix form. This yields a 2 by 2 matrix for our case of two heat sources.

$$\begin{vmatrix} R_{11} & R_{12} \\ R_{21} & R_{22} \end{vmatrix} \times \begin{vmatrix} P_1 \\ P_2 \end{vmatrix} = \begin{vmatrix} \Delta T_1 \\ \Delta T_2 \end{vmatrix}$$

R_{11} : Thermal Resistance of Die1 due to heating of Die1 (˚C/W)

R_{12} : Thermal Resistance of Die1 due to heating of Die2 (˚C/W)

R_{21} : Thermal Resistance of Die2 due to heating of Die1 (˚C/W)

R_{22} : Thermal Resistance of Die2 due to heating of Die2 (˚C/W)

P_1 : Power dissipation of Die1 (W)

P_2 : Power dissipation of Die2 (W)

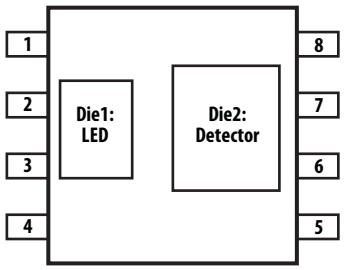


Figure 15. Diagram of ACPL-K43T for measurement

T_1 : Junction temperature of Die1 due to heat from all dice (˚C)

T_2 : Junction temperature of Die2 due to heat from all dice (˚C)

T_a : Ambient temperature (˚C)

ΔT_1 : Temperature difference between Die1 junction and ambient (˚C)

ΔT_2 : Temperature deference between Die2 junction and ambient (˚C)

$T_1 = (R_{11} \times P_1 + R_{12} \times P_2) + T_a$

$T_2 = (R_{21} \times P_1 + R_{22} \times P_2) + T_a$

Measurement data on a low K board:

R_{11} = 160 ˚C/W, R_{12}= R_{21} = 74 ˚C/W, R_{22} = 115 ˚C/W

Thermal Resistance Model for ACPL-K44T

The diagram of ACPL-K44T for measurement is shown in Figure 16. Here, one die is heated first and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the 2nd ,3rd and 4th die is heated and all the dice temperatures are recorded. With the known ambient temperature, the die junction temperature and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in matrix form. This yields a 4 by 4 matrix for our case of two heat sources.

$$\begin{vmatrix} R_{11} & R_{12} & R_{13} & R_{14} \\ R_{21} & R_{22} & R_{23} & R_{24} \\ R_{31} & R_{32} & R_{33} & R_{34} \\ R_{41} & R_{42} & R_{43} & R_{44} \end{vmatrix} \times \begin{vmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \end{vmatrix} = \begin{vmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \Delta T_4 \end{vmatrix}$$

R_{11} : Thermal Resistance of Die1 due to heating of Die1 (˚C/W)

R_{12} : Thermal Resistance of Die1 due to heating of Die2 (˚C/W)

R_{13} : Thermal Resistance of Die1 due to heating of Die3 (˚C/W)

R_{14} : Thermal Resistance of Die1 due to heating of Die4 (˚C/W)

R_{21} : Thermal Resistance of Die2 due to heating of Die1 (˚C/W)

R_{22} : Thermal Resistance of Die2 due to heating of Die2 (˚C/W)

R_{23} : Thermal Resistance of Die2 due to heating of Die3 (˚C/W)

R_{24} : Thermal Resistance of Die2 due to heating of Die4 (˚C/W)

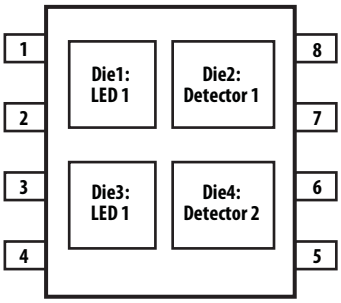


Figure 16. Diagram of ACPL-K44T for measurement

R_{31} : Thermal Resistance of Die3 due to heating of Die1 (˚C/W)
R_{32} : Thermal Resistance of Die3 due to heating of Die2 (˚C/W)
R_{33} : Thermal Resistance of Die3 due to heating of Die3 (˚C/W)
R_{34} : Thermal Resistance of Die3 due to heating of Die4 (˚C/W)
R_{41} : Thermal Resistance of Die4 due to heating of Die1 (˚C/W)
R_{42} : Thermal Resistance of Die4 due to heating of Die2 (˚C/W)
R_{43} : Thermal Resistance of Die4 due to heating of Die3 (˚C/W)
R_{44} : Thermal Resistance of Die4 due to heating of Die4 (˚C/W)
P_1 : Power dissipation of Die1 (W)
P_2 : Power dissipation of Die2.
P_3 : Power dissipation of Die3 (W)
P_4 : Power dissipation of Die4.
T_1 : Junction temperature of Die1 due to heat from all dice (˚C)
T_2 : Junction temperature of Die2 due to heat from all dice (˚C)
T_3 : Junction temperature of Die3 due to heat from all dice (˚C)
T_4 : Junction temperature of Die4 due to heat from all dice (˚C)
T_a : Ambient temperature (˚C)
ΔT_1 : Temperature difference between Die1 junction and ambient (˚C)
ΔT_2 : Temperature deference between Die2 junction and ambient (˚C)
ΔT_3 : Temperature difference between Die3 junction and ambient (˚C)
ΔT_4 : Temperature deference between Die4 junction and ambient (˚C)

$$T_1 = (R11 \times P1 + R12 \times P2 + R13 \times P3 + R14 \times P4) + Ta \text{ -- (1)}$$

$$T_2 = (R21 \times P1 + R22 \times P2 + R23 \times P3 + R24 \times P4) + Ta \text{ -- (2)}$$

$$T_3 = (R31 \times P1 + R32 \times P2 + R33 \times P3 + R34 \times P4) + Ta \text{ -- (3)}$$

$$T_4 = (R41 \times P1 + R42 \times P2 + R43 \times P3 + R44 \times P4) + Ta \text{ -- (4)}$$

Measurement data on a low K board:

R_{11}	R_{12}	R_{13}	R_{14}	R_{21}	R_{22}	R_{23}	R_{24}	R_{31}	R_{32}	R_{33}	R_{34}	R_{41}	R_{42}	R_{43}	R_{44}
160	76	76	76	76	115	76	76	76	76	160	76	76	76	76	115

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