ACM100 Automotive Camera Module

Features

- Complete camera solution for automotive camera applications
  - Monochrome, wide dynamic range camera (>120 dB intrascene)
  - Excellent visible and near IR sensitivity
  - 640 by 480 resolution
  - Choice of M-12 lens
  - Noise correction and image enhancement processing
  - NTSC interface
- Fully programmable and configurable
  - Multiple output options: interlaced or progressive scan
  - Multiple lens options
  - I2C port for camera control
  - Fully parameterized processing and camera control
  - Region of interest Autobrite® and exposure control
- Fully qualified automotive component
  - Normal Operating Temperature: – 40 to +85 °C
  - Degraded Operating Temperature: – 40 to +115 °C
  - Meets interior/in-cabin environmental requirements
  - Contact factory for complete qualification plans and reports
- Other features
  - Low power (1200 mW @ 4.0V& 30 fps)
  - Single supply with voltage protection
  - Built-in temperature measurement

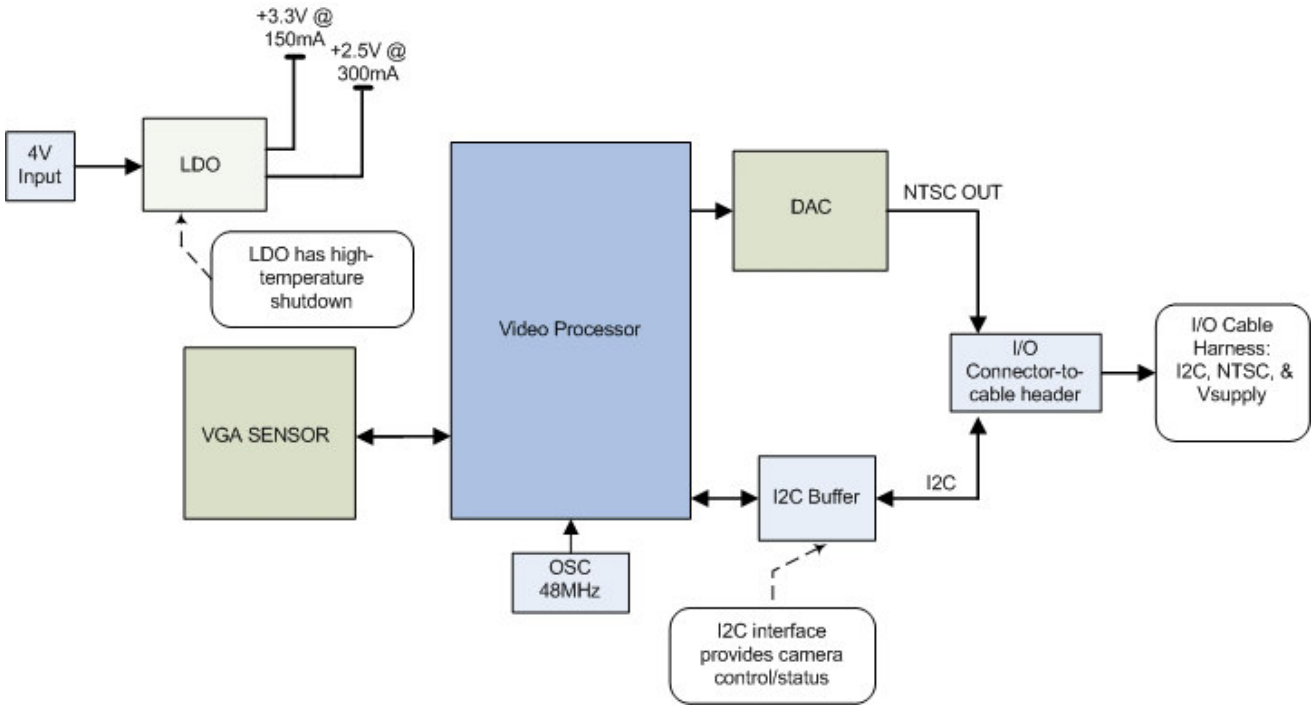
Functional Description

Cypress ACM100 Automotive Camera Module is the first fully-integrated imaging solution designed specifically for automotive vision systems. Built with Cypress CMOS imager, Autobrite® technology and video processing, the module produces crisp, clear video in any range (up to 120 dB) and excellent visible and near-IR sensitivity ensures detail rich scene information regardless of lighting conditions. This highly accurate image reproduction is required for automotive applications such as lane departure warning, night vision, adaptive cruise control, driver monitoring and intelligent airbag deployment.

System Block Diagram

The figure below shows a block diagram of the ACM100 module. The module includes an imager, with focusing optics, a processing chip and a NTSC video interface.

Figure 1. System Block Diagram



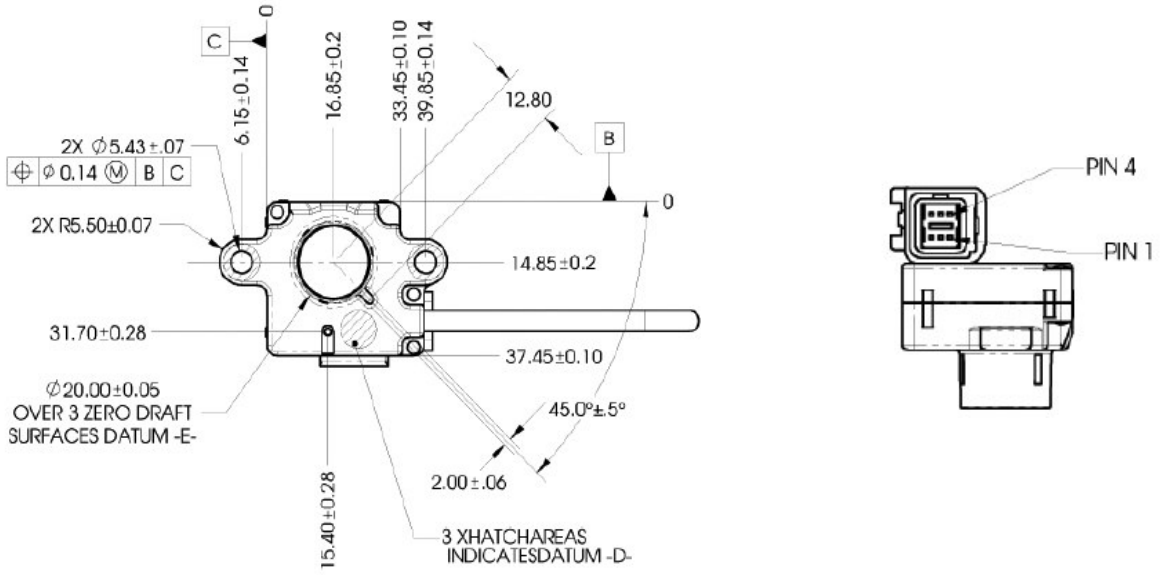
Interface Description

The ACM100 module is intended to support a variety of automotive applications, so the module has been designed with flexible mechanical and electrical interfaces. Each of the interfaces is described in one of the following sections.

Mechanical Interface

The ACM100 module provides a flexible, fastener based mounting feature. The mounting holes on the ACM100 are sized for M5 screws. In addition, a variety of planar surfaces are provided to facilitate the alignment of the camera to the desired orientation in the vehicle. *Figure 2* below defines the mechanical interfaces and envelope.

Figure 2. Preliminary Envelope Drawing



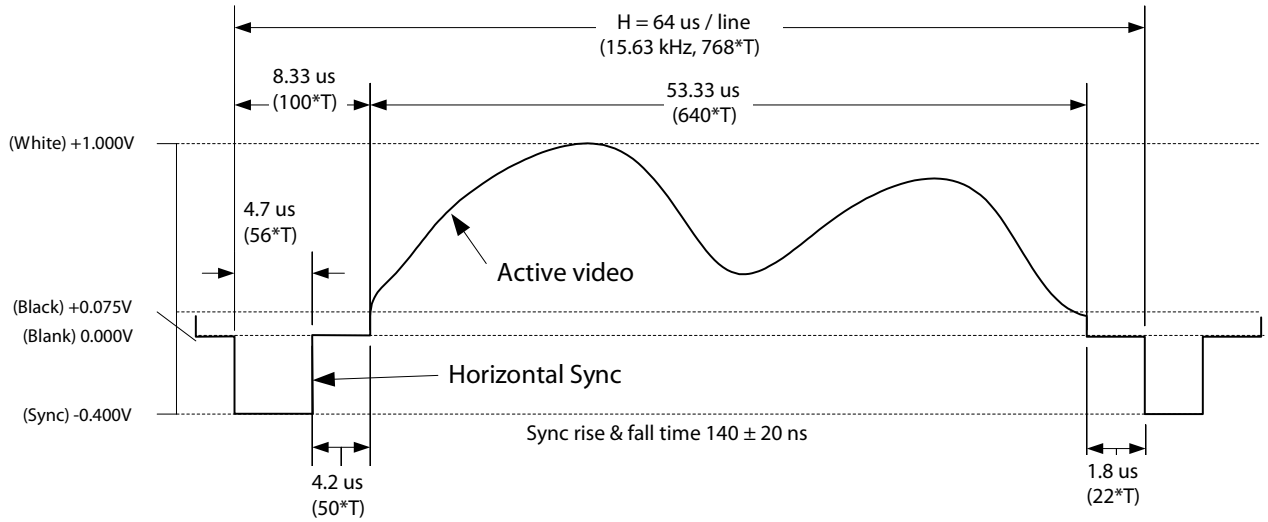
Analog Video Interface

The ACM100 module offers an analog video interface. The camera supports both progressive scan and interlaced modes as described in the following sections.

Interlaced Video Output Option

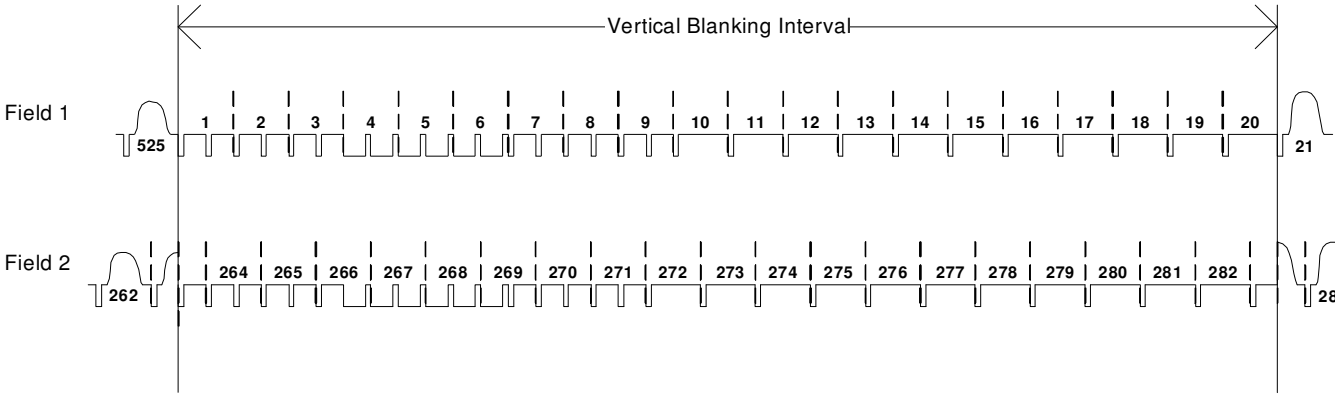
It uses a 60 fps imager scan and the pseudo-interlace scanning option (defined in a later section) to generate 30 frame per second, or 60 field per second video. *Figure 3* defines the timing of the video output and the voltage levels for the 1.4 Vpp waveform.

Figure 3. Horizontal Line Timing



Progressive Scan Output Option

Figure 4. Progressive Scan Output Option



Serial Control Interface

The ACM100 utilizes the I2C bus to control and provide status from an application. The I2C bus is a standard two wire serial bus with data rates up to 400,000 bits per second.

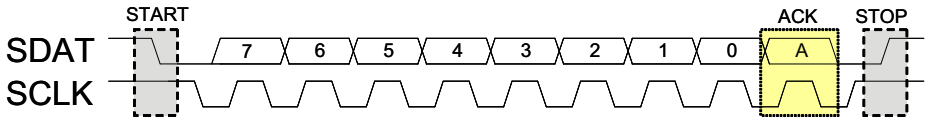
The two interface signals are called SCLK and SDAT. SCLK provides a clock for asserting and sampling the SDAT signal. SCLK is unidirectional from the bus master, typically an image processing chip, to the ACM100. SDAT is the data bus and is bi-directional. Both signals are open-drain and require a pullup resistor of 1.5K Ohms.

Data is always transmitted with the Most-Significant-Bit (MSB) first. Eight bits of data are always transferred and are followed by a single ACKnowledge bit which is driven by the receiver of the previous 8 data bits.

Data transfer is initiated with a START condition. The START condition is indicated when the SDAT signal goes low while SCLK remains high. The START condition may be initiated at anytime during a transfer and the ACM100 will restart the transfer to begin accepting the DEVICE ADDRESS which must immediately follow the START.

The SDAT line must only transition when SCLK is low when data is being transferred. If SDAT transitions while SCLK is high, then it will be interpreted as either a START or a STOP condition. Sufficient timing margins must be provided around the rising and falling edges of SCLK to insure that a START or STOP condition is not mistakenly recognized.

Figure 5

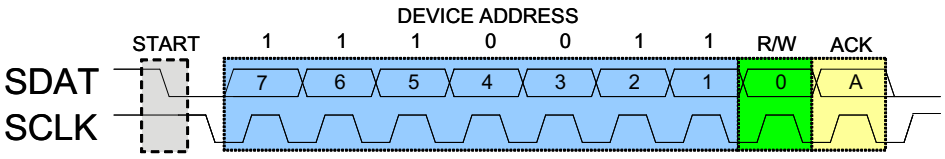


The DEVICE ADDRESS is a sequence of 7 bits, a READ/WRITE bit and an ACKnowledge bit. Data is always transmitted MSB first and LSB last as shown in *Figure 6*. The DEVICE ADDRESS is 7 bits long and must be 1110_011 (0xE6). The LSB of the first byte is the READ/WRITE bit where a high (1) indicates that a READ cycle will follow and a low (0) indicates that a write cycle will follow. After the READ/WRITE bit, the ACM100 will assert SDAT low shortly after SCLK goes low to acknowledge that the DEVICE ADDRESS has been recognized and the ACM100 is ready to process the command that follows. If the I2C bus master does not receive an acknowledge bit, it should restart the transaction as the ACM100 did not recognize its DEVICE ADDRESS

If a read transaction has been requested (READ/WRITE is high), then the ACM100 will begin driving SDAT with the register data at the current address. If a write transaction has been requested then the bus master should send the REG ADDRESS byte. The REG ADDRESS byte specifies which register in the ACM100 is to be accessed.

The next two bytes of data are the write data where the MSB is sent first and the LSB second. Upon completion of all data being transferred, the master should issue a STOP command to place the I2C interface in an idle state. A STOP command is initiated by first driving SDAT low and SCLK high, then bringing SDAT high while SCLK remains high.

Figure 6



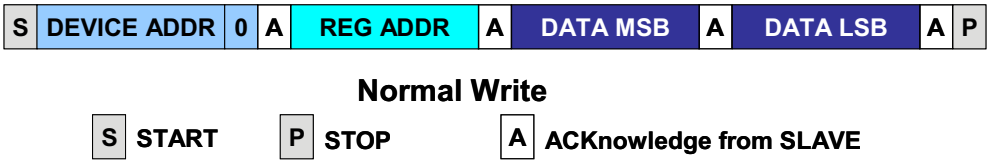
Normal Write Cycle

A normal write cycle is shown in *Figure 7* below. The transaction begins with a START condition and then the DEVICE ADDRESS and then the READ/WRITE bit which must be 0. The ACM100 will acknowledge that it is ready for the transaction by asserting ACK low shortly after the falling edge of SCLK during the READ/WRITE bit. The ACM100 will tristate SDAT so the pullup can bring SDAT high shortly after the next falling edge of SCLK.

The 2nd byte of a transaction is the REGISTER ADDRESS byte which is the address of the register within the ACM100 that is being written to. The ACM100 will assert ACK indicating that the address has been accepted. The 3rd byte of the transaction are the most significant bits (MSB) of the register being written to (bits 15:8). The 4th byte is the least significant bits (LSBs) of the register being written to (bits 7:0).

The command is terminated with a STOP condition. Alternatively, another START command can be initiated at this point. Note that the register is updated when the STOP (or another START) condition is recognized. All 16 bits of the register are updated at the same time

Figure 7. Normal Write Cycle



Noise Immune Write

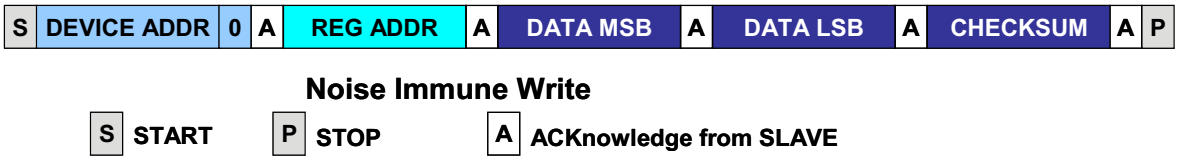
The I2C bus is susceptible to noise when run on a cable or even across a long distance on a PCB. To protect the camera operation in potentially noisy environments, the ACM100 has a feature that insures that I2C writes are only performed if the data is correct. A normal write cycle is performed as in the previous section but an additional byte of data is transferred which is a checksum of the REGISTER ADDRESS and the two data bytes. The checksum is easily computed on a microcontroller using the following formula:

CHECKSUM = 0xFF + REGISTER_ADDRESS + DATA_MSB + DATA_LSB

T*Figure 8* below shows the sequence of bytes to insure a valid register write in the presence of noise on the I2C bus. Note that register REG9 bit 0 will enable the mode that requires the checksum byte be included for all write transactions. This mode is off by default which makes I2C writes compatible with previous versions of the ACM100. The register is updated during the ACK bit of the CHECKSUM byte if the checksum is correct. The ACM100 will not acknowledge the CHECKSUM byte if the transaction has been corrupted and the checksum does not match the computed checksum. The lack of the ACK in this case can be used as an indicator by the I2C bus master that the transaction has been corrupted and should be retried.

When the checksum mode is enabled (REG9[0]=1) then the checksum is required and writes will no longer be compatible with previous versions of the ACM100. This mode insures that all writes have a good checksum. When the backwards compatible mode is disabled, the checksum byte is optional.

Figure 8. Noise Immune Write

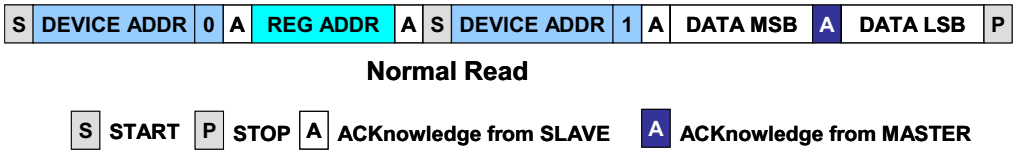


Normal Read Cycle

A normal read cycle begins with a write cycle which is terminated after the REG_ADDR byte. This partial transaction is required to properly set the REGISTER ADDRESS to the register being read. Following the new START command and the DEVICE ADDRESS, the ACM100 will drive the MSBs of the register onto the SDA line. The I2C bus master must then provide an ACK bit for that byte. If the I2C master does not provide ACK the readback data, then the ACM100 I2C interface will return to the IDLE state and wait for a new START. The ACM100 will then drive the LSBs onto the SDA line and then the I2C bus master can either issue a STOP command or just not ACK the byte to end the transaction. The REGISTER ADDRESS is not automatically incremented after each byte so only one register can be read during each transaction. The register being read is sampled during the ACK bit of the DEVICE ADDRESS where the R/W bit is a 1. This insures that the two halves of the register being read are consistent as many registers are volatile and can update at any time - including the time between when the MSBs are being read out onto the I2C bus and when the LSBs are being read.

The REGISTER ADDRESS remains loaded with whatever the last value was sent. Thus, a write followed by a read of the same register does not require reloading the REGISTER ADDRESS. Instead, a START and the DEVICE ADDRESS with R/W set 1 can immediately follow the DATA LSB of the write transaction. Note that there is no noise immunity protection on setting the REGISTER ADDRESS.

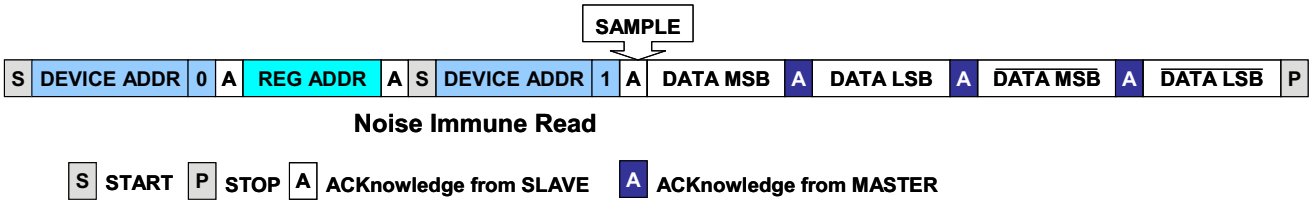
Figure 9. Normal Read Cycle



Noise Immune Reads

Noise immune reads are supported by reading the data bytes multiple times within the same I2C transaction. *Figure 10* shows that the data in the register is sampled during the ACK bit of the DEVICE ADDRESS. The data is then read out during the DATA MSB and DATA LSB cycles. If additional bytes are read out, the ones-complement of the data can be read in sequence. The data can be compared by the I2C bus master to insure that the data is correct and that noise has not corrupted the I2C transaction. Note that the register data is always consistent as long as the bytes are read out without initiating a new I2C transaction (IE: a new START/STOP). If the bytes have been corrupted, the DATA MSB and DATA LSB fields can simply be read again as the register is not re-read unless a new DEVICE ADDRESS is issued. Note that this mode is backwards compatible with older versions of the ACM100 as reading the ones-complement of the register data is optional.

Figure 10. Noise Immune Reads



Connector Definition

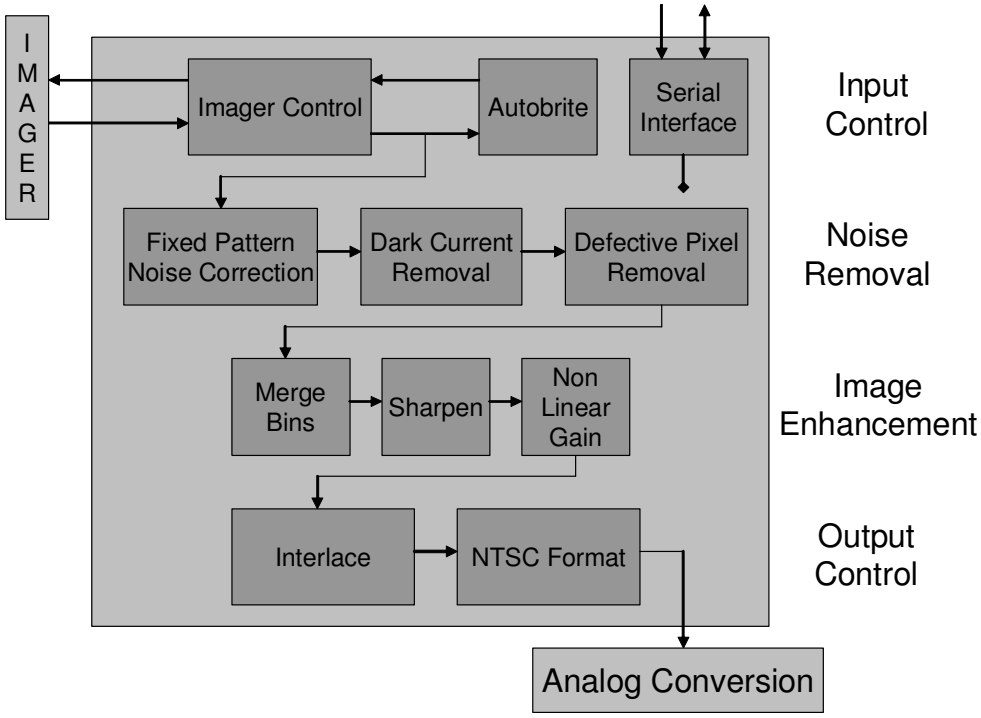
The standard camera comes with a pigtail connector terminated with a Hirose GT17VSN-6DP-HU. Please inquire as to the availability of other connectors should your application require a different connector. The following table defines the connector pins for the Hirose connector.

Number	Signal	Pins Required	Wire Color
1	I2C_SDAT	1	Green
2	PWR_IN_A	1	Red
3	GND	1	Blue
4	I2C_SCLK	1	Gray
5	GND	1	Yellow
6	NTSC_OUT	1	White

Functional Specification

The *Figure 11* below illustrates the processing contained in the ACM100 camera. Some of the key features of the processing are described in the following sections

Figure 11. Processing Block Diagram

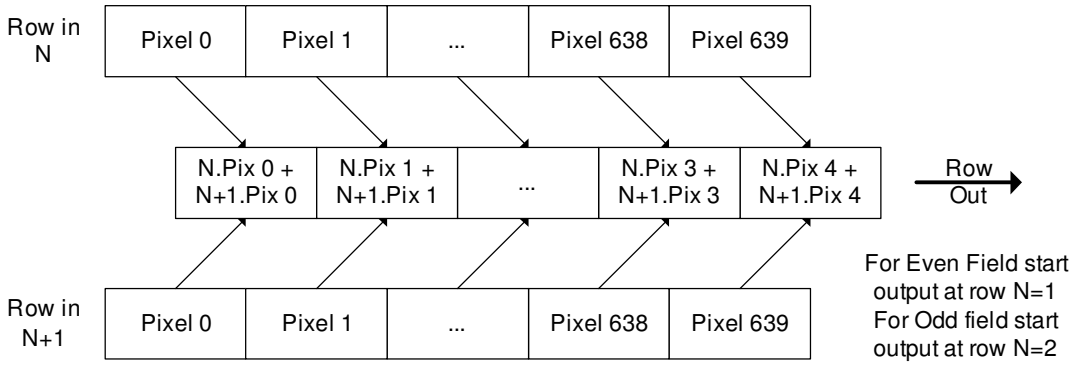


Pseudo Interlace

In the progressive scan mode, the imager is scanned at 30 Hz and fed directly to the pipeline and video output. In the interlaced version, the camera employes a technique referred to as Pseudo Interlacing.

Pseudo interlace provides a data stream capable of RS-170 (NTSC) compatibility. Pseudo interlace provides a benefit over standard interlacing by reducing motion artifacts. The way pseudo-interlace is generated in this system is that the sensor is read at 60fps. Each frame read out of the sensor is used to generate one field of the output image. When frame N is used to generate field 0, frame N+1 is used to generate field 1. Adjacent pairs of rows are averaged and output as a single row in order to not lose any sensitivity even though the sensor is integrating for only half as long (60 fps vs 30 fps). For field 0 the rows are summed in pairs starting with row 0 of the sensor. For field 1 the rows are summed in pairs starting with row 1 of the sensor. *Figure 12* illustrates the generation of one field; the generation of the other field is essentially the same, with an offset of 1 input row at the beginning.

Figure 12. Progressive Row Generation Diagram



Autobrite ®

The ACM100 module includes both automatic and manual control of both the integration period and the dynamic range. The automatic control may be based on the entire contents of the image, or on a user specified region of interest. The following sections describe the control in more detail.

Region of Interest

The camera includes a region of interest feature that can be used to influence the automatic control of the dynamic range and the integration period. The user designates a region of interest (of programmable size and position) within the full frame. The camera automatically optimizes the exposure and dynamic range for this region (alternatively, the region can be ignored for exposure and dynamic range setting). The region is defined by specifying the upper left and lower right corners of a rectangle using pixel row and column numbers.

Tint Control

The camera provides for both automatic and manual control of the integration period (exposure time). This can be specified independently of the gamma control – that is either can be fixed or set automatically. The Tint control algorithm attempts to set the camera to an integration period that places the average pixel value at a default or user specified level.

In addition to setting the desired image average, the user may bound the integration period that is available to the automatic control. This can prevent the integration from exceeding motion blur limits in dark environments.

Gamma Control

The camera provides for both automatic and manual control of the dynamic range by selecting one of 29 response, or gamma, curves. This can be specified independently of the Tint control – that is either can be fixed or set automatically.

Autobrite tracks two parameters to control the selection of a gamma code: the number of saturated pixels (those at the maximum digital value) and the number of pixels in the top histogram bin of the image. These parameters are tracked on a per image basis using binary counters.

The algorithm can be tuned by setting the number of bits active in each counter. The logic responds to the overflow of the counter. Therefore the maximum number of saturated pixels and minimum number of top bin pixels desired are both set as a power of two.

The algorithm works by increasing the dynamic range when the number of saturated pixels (max gray level) exceeds the saturation setting. The dynamic range is reduced when the number of pixels in the top bin of a histogram (of programmable size) falls below the specified value.

In addition to setting the target values, the user may limit the maximum gamma setting available to the algorithm. This may be useful to applications that respond poorly to extremely high gamma values.

Transition Control

The camera includes features that allow the user to influence the response of the camera to dynamic lighting conditions. Human vision applications may desire a slow, smooth response to changes in lighting for aesthetic reasons. Machine vision application, not being influenced by aesthetic concerns, may desire a faster response. The camera includes features to allow the user to adjust the dynamic response of the camera to suit the application.

Image Processing Fetaures

The camera includes a number of features that improve or remove artifacts from the image. These features are described in the following sections.

Dark Current Removal

The camera automatically senses the dark current using inactive, or dark, columns in the sensor. The current is measured for each row and subtracted from the image. This feature may be disabled by the user.

Column Fixed Pattern Noise Correction

During the vertical retrace period of scanning the imager, a fixed voltage is applied to all of the columns of the imager. This voltage is sampled by the ADC and used to calculate offset errors on a column basis. These errors are then removed from the next frame. This feature may be disabled by the user.

Defective Pixel Correction

The camera includes a feature to compensate for defective pixels. A 3x3 non-linear filter is used to screen out defective pixels. The center pixel is compared against the average of its neighbors and if it is too high or low, the average is substituted for the defective pixel. This feature may be disabled by the user.

Sharpening Filter

The camera includes a 3X3 sharpening filter. The user may disable or specify the strength of the filter.

Detailed Specifications

The following sections outline some of the detailed specifications of the module.

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Storage Temperature ..... –40°C to +125°C

Operating Temperature ..... –40°C to +115°C

Electrical Characteristics

(The following specifications apply for TA = –40ºC to +85ºC.)

Input Voltage..... –0.3V to VCC +0.3V

ESD Susceptibility 2000V

Operating Conditions

Supply Voltage .....4.0V +/-5%

Operating Temperature ..... –40°C to +85°C

Reduced Performance..... +85°C to +115°C

Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
VCC	Supply Voltage		3.8	4.0	4.2	V
PACT	Active power consumption	300 mA @ 4V Full frame 30 fps		1200		mW
I2C Levels						
VOH	Output Level [high]	IOH = –4.0 mA	2.0		VCC	V
VOL	Output Level [low]	IOL = 4.0 mA	GND		0.8	V
VIH	Input Level [high]		2.3		5.5	V
VIL	Input Level [low]		-0.5	8	10	V
ILOAD	Input Leakage Current	VI = 0V to 3.3V		0.01	10	mA
CIN	Input Capacitance	VIN = 0V, f=1.0 MHz		8	10	pF
COUT	Output Capacitance	VIN = 0V, f=1.0 MHz		10	12	pF
tr,tf	Rise/Fall Time				5	ns

Composite Video Signals

Drive Impedance	75 Ohm
Video Signal	1.4 V p-p into a 75 - ohm load
White Level	1.000 V + 5%
Black Level	0.075 V + 5%
Blank Level	0.000 V
Sync Level	–0.400 V + 5%
Vertical Frequency	59.93 Hz + 5%
Horizontal Frequency	15.75 kHz + 5%
Data Format	Interlaced/Progressive
Pixel Output Rate	12 Mhz

Register Description

0x00 User Tint

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	0	1	0	0	0	0	0	1	1	0	0
AB_K			TINT_EN	TINT											

The User Tint register is used when manual control of the integration period is required by the application. The bits are defined as follows:

[15:13] AB_K : This bit field can be used to slow down the response of the automatic Tint control to changes in the scene. This may be desirable if smooth changes between camera settings are preferable to rapid response. New Tint values are calculated based on the assumption that the image average will scale linearly with the Tint setting. The algorithm works by calculating the difference between the current and target image average and then based on that difference calculating what change in Tint is required to attain the desired image average. The algorithm then multiplies the change in Tint by the AB_K value and then adds the result to the current Tint value. Therefore, smaller values of AB_K will cause the Tint value to adjust in smaller increments, although the size of the steps will remain proportional to the lighting change for a fixed AB_K.

The following table shows some examples of how AB_K affects the Tint calculations for a desired image average of 128. (Calculated Tint = Tint(128/Image Average))

Image Average	Tint	Calculated Tint	Tint Difference	AB_K	New Tint
50	100	256	156	1	256
50	100	256	156	0.5	178
50	100	256	156	0.25	139
150	250	213	-37	1	213
150	250	213	-37	0.5	231
150	250	213	-37	0.25	241

The operation of this field is defined by the following table. Other values are not defined and should not be used

AB_K	Description
4	Normal Response
3	75% of Normal Speed
2	50% of Normal Speed
1	25% of Normal Speed

[12] TINT_EN: Writing a '1' to this bit will enable manual control of the integration period. When enabled, the TINT value specified in this register will be used and automatic control of the integration period is disabled. Writing a '0' to this location will disable manual control and enable the automatic control of the integration period. Changes to this bit will take affect on the next full frame of video.

[11:0] TINT: This field specifies the integration period as a number of rows. The maximum integration is 525 rows. At a frame rate of 30 fps, writing a value of 0X20D would result in a 33 msec integration period. Changes to this parameter will take affect on the next full frame of video.

0x01 Min Tint

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
TINT_SKIP				MIN_TINT											

The Min Tint register is used to specify the minimum integration period available to the algorithm controlling Autobrite as well as controlling several other features. The bits are defined as follows:

[15:12] TINT_SKIP: This field specifies the frequency at which Tint updates made when automatic control of Tint is enabled. This field is set to a 2 frames by default to accommodate the one frame latency between calculation of a new Tint value and its taking effect. Note that the Tint will settle in the same number and size of steps, but will take longer to settle. To change the size of steps that Tint will use to adjust, use the AB_K parameter.

[11:0] MIN_TINT: This field is used to specify the minimum integration period that the Autobrite algorithm will use to control the camera. It is only valid when manual control of the integration period is disabled. It is specified as the number of row periods you wish to have the sensor integrate. The maximum integration is 525 rows. Changes to this parameter will take affect on the next full frame of video.

0x02 Max Tint

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	0	1	0	0	0	0	0	1	1	0	0
Reserved	Reserved			MAX_TINT											

The Max Tint register is used to specify the maximum integration period available to the algorithm controlling Autobrite as well as controlling several other features. The bits are defined as follows:

[15:12] Reserved: These bits are reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of this bit.

[11:0] MAX_TINT: This field is used to specify the maximum integration period that the Autobrite algorithm will use to control the camera. It is only valid when manual control of the integration period is disabled. It is specified as the number of row periods you wish to have the sensor integrate. Changes to this parameter will take affect on the next full frame of video.

0x03 Merge Bins Control 1

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
Reserved	Q_Slope			Max_Q											

The Merge Bins Control register is used to enable and control the behavior of the merge bins contrast enhancement algorithm. The merge bins algorithm can be controlled by specifying a Q function that indicates how strongly gray levels should be affected by the algorithm. The Q function can be specified in one of two methods. The first method assumes that a maximum Q is specified for gray level zero and that this value is reduced for increasing gray levels at a specified slope until a minimum Q value is reached. The alternative is to manually load a table which will specify a unique Q value for each gray level.

The bits are defined as follows:

[15] Reserved: This bit is reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of this bit.

[14:12] Q_Slope: The Q Slope field specifies the rate at which the Q value is reduced for increasing gray shades. This field is cumulatively subtracted from the initial, maximum value

[11:0] Max_Q: The Max Q field specifies the Q value for gray level zero. This forms the starting point for the Q function. Note: if the Min_Q value is set to be higher than the Max_Q value, the result will be a flat threshold at the Min_Q value.

0x04 Gain/Gamma Control

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	1	1	1	1	0	0	0	1	1	0
Reserved	GAMMA_SKIP				MAX_GAMMA					GAMMA					GAMMA_EN

The Gain/Gamma Control register is used to specify parameters that affect the gamma control of the camera as well as the digital gain. The bits are defined as follows:

[15] Reserved: This bit is reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of this bit.

[14:11]GAMMA_SKIP: This field specifies the frequency at which gamma may be updated by the automatic control algorithm (when enabled.) The default is set to 2 to account for a one frame latency between the calculation of a new value and its effect. Lower values may result in an overshoot in the response to a step change in image lighting.

[10:6]MAX_GAMMA: These bits define the maximum gamma code that will be available to the algorithm controlling the dynamic range of the sensor. Changes to this parameter will take affect on the next full frame of video.

[5:1] GAMMA: These bits specify the value of gamma to be used when user gamma is enabled. Increasing values of gamma represent increasing amounts of signal compression – resulting in increased dynamic range. Values of 3 and below are linear and the maximum value of 31 represents the maximum dynamic range of the sensor. Changes to this field take affect immediately – even in the middle of a frame. This may result in a frame with the top and bottom portions of the image being taken with different gamma settings.

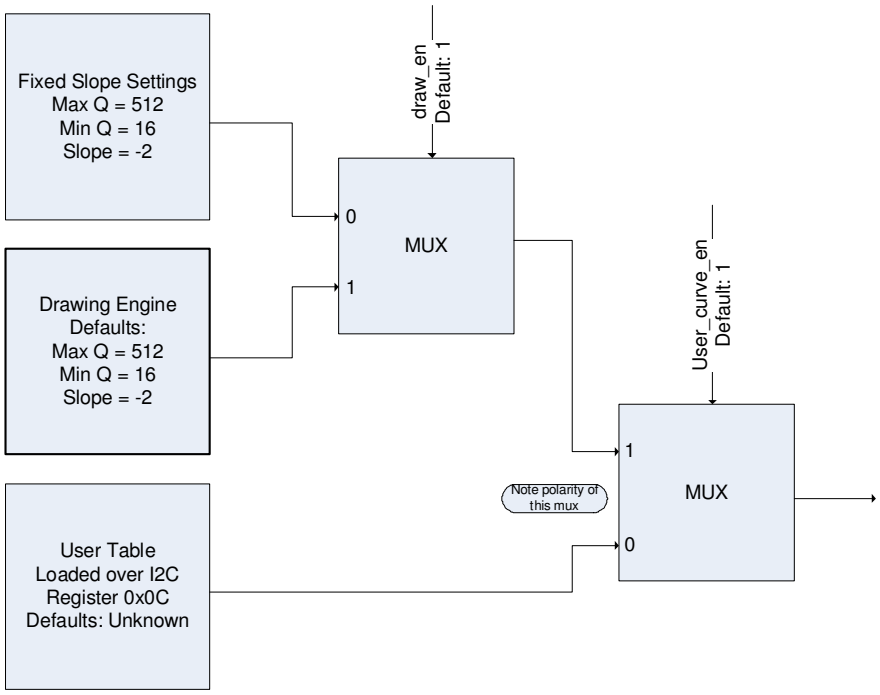
[0] GAMMA_EN: Writing a '1' to this bit will enable the use of the gamma value specified in the GAMMA field of this register to be used in place of the value calculated by the Autobrite algorithm. This may result in a frame with the top and bottom portions of the image being taken with different gamma settings

0x05 Merge Bins Control 2

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0
Reserved		User_Curve_En	Draw_Enable	Min_Q											

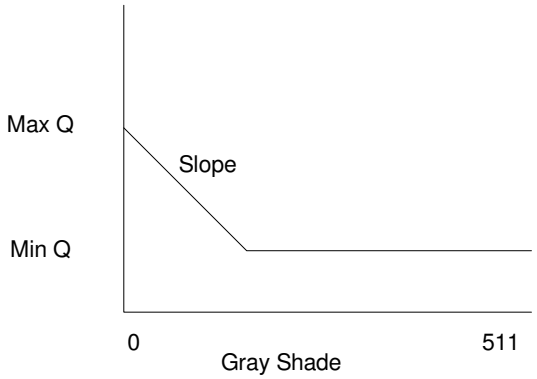
The Merge Bins Control register is used to enable and control the behavior of the merge bins contrast enhancement algorithm. The merge bins algorithm can be controlled by specifying a Q function that indicates how strongly gray levels should be affected by the algorithm. The Q function can be specified in one of several methods as shown in *Figure 13*.

Figure 13. Q Threshold Selection



The first two methods assume that the Q function has a specific shape defined by Max Q, Min Q and Slope parameters resulting in a Q function as shown in *Figure 14*.

Figure 14. Standard Threshold Shape



The alternative is to manually load a table which will specify a unique Q value for each gray level. The bits are defined as follows:

[15:14] Reserved: These bits are reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of these bits.

[13]User_Curve_En: Writing a '0' to this bit will enable the use of a user loaded curve. This must be loaded via register 0x15 prior to enabling this function. [12] Draw_En Writing a '1' to this bit will enable a Q function based on the parameters programmed in registers 0x3 and 0x5.

[11:0] Min_Q The Min Q field specifies the Q value at which the function will level off. The Q value for gray shade zero is set to the max Q value and then decremented by the Q Slope until this value is reached. Note: if the Min_Q value is set to be higher than the Max_Q value, the result will be a flat threshold at the Min_Q value.

0x06 ROI 1

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
ROI_XOFF[15:8]								ROI_XON[7:0]							

The ROI 1 register is used to specify the size and location of the region of interest box in the x axis (imager columns). The bits are defined as follows:

[15:8] ROI_XOFF: This field specifies the 8 most significant bits of the ending X coordinate. The least significant bits are fixed at “000”. Therefore, the resolution of this coordinate is limited to multiples of 8.

[7:0] ROI_XON : This field specifies the 8 most significant bits of the starting X coordinate. The least significant bits are fixed at “000”. Therefore, the resolution of this coordinate is limited to multiples of 8.

0x07 ROI 2

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	1	1	1	1	0	0	1	0	1	1	1	0
ROI_YOFF[15:8]								ROI_YON[7:0]							

The ROI 2 register is used to specify the size and location of the region of interest box in the x axis (imager rows). The bits are defined as follows:

[15:8] ROI_YOFF: This field specifies the 8 most significant bits of the ending Y coordinate. The least significant bits are fixed at “00”. Therefore, the resolution of this coordinate is limited to multiples of 4.

[7:0] ROI_XON : This field specifies the 8 most significant bits of the starting Y coordinate. The least significant bits are fixed at “00”. Therefore, the resolution of this coordinate is limited to multiples of 4.

0x08 Video Control

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	1	1	0	1	1	0	1	0	0	1
Reserved	TINT_HYST_EN	Reserved	DARK_OFFSET_EN	SHARP_STRENGTH	SHARP_EN	Rseserved	FPN_OFFSET_EN	FULL_FRAME_FPN	AGC_MODE	MB_EN	MB_ROI_EN	SK_EN	Reserved	NTSC_TEST_ENABLE	NTSC__EN

The Video control register is used to enable various features that affect the output video signal.

[15] Reserved: This bit is reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of this bit.

[14] TINT_HYST: Writing a ‘1’ to this bit will cause the automatic control of the Tint settings to have additional hysteresis. This added hysteresis will cause changes of less than two lines to be suppressed. This is useful in eliminating the appearance of flickering in very bright scenes where a change of one line of integration time represents a significant change in image brightness.

[13] Reserved:	This bit is reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of this bit.
[12] DARK_OFFSET_EN:	Writing a ‘1’ to this location will enable dark current correction. Writing a ‘0’ will disable dark current correction.
[11] SHARP_STRENGTH:	Writing a ‘1’ to this bit will cause the sharpening filter to be at the stronger setting. Writing a ‘0’ to this bit will cause the sharpening filter to be at a weaker setting.
[10] SHARP_EN:	Writing a ‘1’ to this bit will enable the 3X3 FIR, sharpening filter. This filter has two default strengths.
[9] Reserved:	This bit is reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of this bit.
[8] FPN_OFFSET_EN:	Writing a ‘1’ to this location will enable the automatic correction of column fixed pattern offset errors in the hardware. FPN coefficients are calculated by placing known voltages on the columns when imager data is not being read. Writing a ‘0’ to this location will disable FPN offset correction. Note that on power up or after a system reset, this may require as much as two minutes to reach full performance. This is a result of filtering on the correction values to remove the affects of non-fixed pattern noise.
[7] FULL_FRAME_FPN:	Writing a ‘1’ to this location will cause FPN data to be collected over the entire frame. This is a test feature and it will cause the video to be overwritten. Writing a ‘0’ to this bit will enable normal operation.
[6] AGC_MODE:	Writing a ‘0’ to this bit will disable all gain stages in the processing pipeline including merge bins. This mode is intended to be used to measure the SNR of the imager. Writing a ‘1’ to this bit will enable normal operation of the processing pipeline.
[5] MB_EN:	Writing a ’1’ to this bit will enable Merge Bins contrast enhancement block in the processing pipeline. This block applies an adjustable non-linear function to ensure the video is mapped efficiently to 8 bits
[4] MB_ROI_EN:	Writing a ’1’ to this bit will enable the ROI feature for the merge bins algorithm. Enabling this feature causes the algorithm to generate a non-linear transform that optimizes the portion of the image in the region of interest. The same transform is applied to the entire image, but the transform is calculated to optimize the region of interest.
[3] SK_EN:	Writing a ‘1’ to this location will enable the starkiller, non-linear filter. This filter detects and corrects for single pixel defects in the imager.
[2] Reserved:	This bit is reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of this bit.
[1] NTSC_TEST_ENABLE:	Writing a ‘1’ to this bit will cause the camera to generate a test pattern on the NTSC output. Writing a ‘0’ will enable normal operation.
[0]NTSC_EN:	Writing a ‘0’ to this bit will turn off the NTSC output of the camera. Writing a ‘1’ to this bit will enable the NTSC output.

0x09 Video Control 2

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PIX_RPLC		NLG_EN	NLG_Strength	Reserved							Data format	Reserved			CHKSUM

The Video control register is used to enable various features that affect the output video signal. The bits are defined as follows:

[15:14] PIX_RPLC: This field can be used to replace the active video with either all white or all black pixels. This is a feature that can be used to test/troubleshoot the camera. The field is defined by the following table:

PIX_RPLC	PIX_RPLC
00	**Normal Video**
01	**Video is all black**
10	**Video is all white**
11	**Video is a counting value**

[13] NLG_EN: Writing a '1' to this field will enable a non-linear gain to be applied which will boos the signal strength of darker regions of the image without saturating the bright images.

[12] NLG_Strength: Writing a '1'to this field will enable the stronger setting of the non-linear gain function. Writing a '0' will enable the weaker setting.

[11:5] Reserved: These bits are reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of these bits.

[4] Data Format When this bit is set to 0 it sets to Interlaced mode and when this bit is set to 1 it sets to Progressive mode

[3:0] Reserved These bits are reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of these bits.

[0] CHKSUM Writing a 1 to this bit puts the I2C bus interface into a mode where the CHECKSUM byte is required for all I2C register writes. The default for this bit is 0 which enables I2C writes to be terminated at the end of the 2nd data byte which is compatible with older versions of the ACM100. For more details See "Noise Immune Write" on page 4.

0x0A Autobrite Control

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1	1	0	1	0	0	1	1	1
Reserved	Reserved	SHOW_ROI_BOX	ROI_EN	ROI_Polarity	Reserved										

The Autobrite Control register is used to specify parameters that influence the automatic selection of a gamma code (dynamic range control.) The bits are defined as follows:

[15] Reserved: This bit is reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of this bit.

[14] Reserved: This bit is reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of this bit.

[13] SHOW_ROI_BOX: Writing a '1' to this location will enable the generation of a line around the region of interest that has been defined using registers 6 and 7. This is useful for checking to ensure the region of interest has been set correctly. Writing a '0' to this location will disable this feature.

[12] ROI_EN: Writing a '1' to this location will enable the ROI feature. Writing a '0' to this location will disable the feature and cause the entire frame to be used for automated control of the Tint and Gamma

[11] ROI_POLARITY: Writing a '1' to this location will cause the area inside the region of interest to be used to calculate Gamma, Tint and linear remap settings. Writing a '0' to this location will cause the area outside the region of interest to be used.

[10:0] Reserved: These bits are reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of these bits.

0x0B FOD Control

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0
Reserved															

The FOD Control register is used to specify the frame on demand mode desired for the application. Please refer to *ECK100 Detailed Product Specification* for detailed information on the operation of Frame on Demand and Strobe control features.

[15:0] Reserved: These bits are reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of these bits.

0x0C Dark Current (Read Only)

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				DARK_CURRENT											

The Dark Current register can be used to read back the average dark current correction value. This value is related to temperature. The bits are defined as follows:

[15:12] Reserved: These bits are reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of these bits.

[11:0] DARK_CURRENT: This field reads back the dark current correction factor which can be used to determine to current temperature of the sensor.

0x0C Merge Bins Table Load (Write Only)

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				Q											

The Table load register is used to load an arbitrary Q function. The merge bins algorithm can be controlled by specifying a Q function that indicates how strongly gray levels should be affected by the algorithm. The Q function can be specified in one of two methods. The first method assumes that a maximum Q is specified for gray level zero and that this value is reduced for increasing gray levels at a specified slope until a minimum Q value is reached. The alternative is to manually load a table which will specify a unique Q value for each gray level.

The bits are defined as follows:

[15:12] Reserved: Reserved for future use

[11:0] Q: The first time this field is written after a power on or reset (including a soft reset initiated by writing to register 0xF) the Q value will be stored in the table at the location for gray code 0. The second write will store the Q value into location 1 and subsequent writes will continue to increment the storage location. The algorithm uses 512 locations.

0x0D Video Status (Read Only)

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			CUR_GAMMA					IMAG_AV							

The Video Status register is a read only register that provides the status of the current image to the user.

The bits are defined as follows:

[15:13] Reserved: These bits are reserved for future use and should not be set. To ensure compatibility with future releases, we recommend using a read/modify/write operation to preserve the status of these bits.

[12:8] CUR_GAMMA: This bit field represents the current gamma code most recently calculated by the Autobrite algorithm. This value is updated as soon as the new value is calculated and there is a two frame latency before they take effect.

[7:0] IMAG_AV: This bit field represents the current image average most recently calculated by the Autobrite algorithm.

0x0F Firmware Version/Soft Reset

Bit Definition															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Definition When Read															
PCB_Ver				HW_Ver				RTL_Maj_Ver				RTL_Min_Ver			
Definition When Written															
Reserved															

When read, the Firmware Version/Soft Reset register is used to determine the revision status of the camera. When written, the register is used to reset the camera. The following defines the fields of this register:

Read

[15:12] PCB_Ver: This field reads back the revision level of the PCB. It is incremented each time the artwork is changed on the PCB in the camera.

[11:8] HW_Ver: This field reads back the hardware version of the camera. It starts at zero with each PCB version and is incremented as changes are made to the hardware that do not affect the PCB artwork.

[7:4] RTL_Maj_Ver: This field reads back the major revision code for the firmware in the FPGA. This field is independent of the PCB and HW versions and is incremented each time a major change to the functionality of the FPGA is implemented.

[3:0] RTL_Min_Ver: This field is reset each time the RTL_Maj_Ver field changes and is incremented each time the firmware is changed.

Write

[15:1] Reserved: These bits are reserved for future use and should not be set. Write ‘0’s to this field.

[0] RST: Writing a ‘1’ to this bit will return all registers to the power on state.

Environmental Specifications

Specification	Value	Comment
Normal Operating Temperature	– 40℃ to +85℃	See General Specifications for sensitivity de-rating over temperature. Video performance guaranteed from –40℃ to +85 ℃
Degraded Operating Temperature	– 40℃ to +115 ℃	
Storage Temperature	– 40℃ to +130 ℃	
Humidity	100% relative humidity	
Salt Mist Atmosphere	Passenger compartment compliant	
Dust	Passenger compartment compliant	100 mg/m^3
Chemical Resistance	Passenger compartment compliant	Leather wax, anti-mist spray, cleaning soap, deodorizer spray, coffee, tea, soft drinks

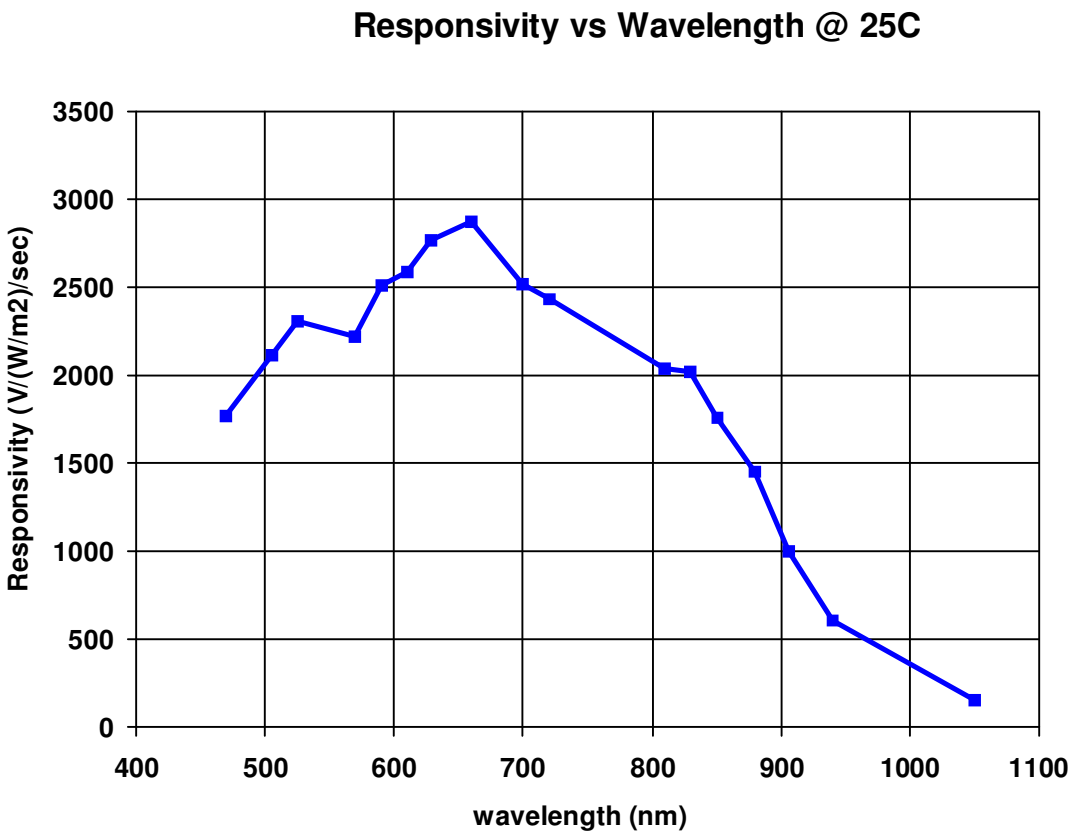
Performance Specifications

The ACM100 module is intended to support a variety of applications, many with differing optical field of view requirements. To facilitate the differences, the ACM100 module is available with a selection of lenses. The following table summarizes the general performance of the camera and at 25^{o}C. Data are for imager (IM103) performance. Performance specifications will vary based on lens selection. Specifications of available lenses are described in later sections.

Parameter	Value	Notes
Resolution	640H X 480V	Additional columns/rows for image processing
FPN	<0.1% of full signal rms	Excluding temporal noise sources
Response nonuniformity	<1.0% rms	Standard deviation from the mean photo response from 10 to 90% of full signal
Minimum illumination	1 mW/m2	850nm faceplate power SNR>10 required @ 30fps and 85 C (Signal over temporal noise)
Responsivity	>10 V/lux-sec	
Noise Equivalent Irradiation	1.5 nW/cm2 @ 525 nm 3 nW/cm2 @ 850 nm 6 nW/cm2 @ 940 nm	irradiance required to achieve an SNR of 1
Pixel pitch	8 microns square	
Defective Pixels	<80 0 clusters	Configurable defect correction available
Online temperature estimate	Mean dark signal register	
Dynamic Range	120 dB captured	

Electro-Optical Performance

Figure 15. Responsivity



18° FOV Lens Specifications

The following specifications apply to the 18 degree field of view lens

Specifications	Value
HFOV	18°
F/#	2.0
efl	16.0 mm
Lens element	All Glass, AR Coated

30° FOV Lens Specifications

Specifications	Value
HFOV	30o
F/#	<2.0
efl	9.55 mm
Lens element	All Glass, AR Coated

50° FOV Lens Specifications

The following specifications apply to the nominal 50 degree FOV lens.

Specifications	Value
HFOV	50°
F/#	≤2.0
efl	5.5 mm
Lens element	All Glass, AR Coated

90° FOV Lens Specifications

Specifications	Value
HFOV	90°
F/#	<2.0
efl	2.56 mm
Lens element	All Glass, AR Coated

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REV.	**ECN.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	499837	See ECN	QGS	New Data Sheet