ACE5372

Low Power Real-Time Clock (RTC)

Description

The ACE5372 is a CMOS type real-time clock, which is connected to the CPU via two wires and capable of serial transmission of clock to the CPU. The ACE5372 can generate various periodic interrupt clock pulses lasting for long period (one month), and alarm interrupt can be made by two incorporated systems. Since an oscillation circuit is driven at a constant voltage, it undergoes fluctuations of few voltage and consequently offers low current consumption (TYP. 400nA @ 5V)

It also provides an oscillator halt sensing function applicable for data validation at power-on and other occasions. The product also incorporates a time trimming circuit that adjusts the clock with higher precision by adjusting any errors in crystal oscillator frequencies based on signals from the CPU. The crystal oscillator may be selected from 32KHz or 32.768KHz types.

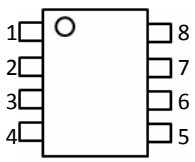
It adopts 8-pin SOP or TSSOP package.

Features

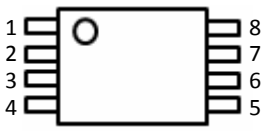
- Lowest supply current: 400nA TYP.@5V
- Connected to the CPU via only 2-wires (MAX. 100KHz)
- A clock counter (counting hours. Minutes. and seconds) and a calendar counter (counting leap years, years, months, days, and days of the week) in BCD codes.
- Two system output of alarm functions
- Oscillation halt sensing to judge internal data validity
- Clock output of 32.768KHz (32KHz) (output controllable via a register)
- Second digit adjustment by ±30 seconds
- Automatic leap year recognition up to the year 2099
- 12-hour or 24-hour time display selectable
- High precision time trimming circuit
- Oscillator of 32.768KHz or 32KHz may be used
- CMOS logic
- Package: 8pin SOP or TSSOP

Packaging Type

SOP-8



TSSOP-8



Pin	Symbol	Definition	Value	In/Out
1	INTRB	Interrupt Output B	0~12V	Out
2	SCL	Serial Clock Line	0~5.5V	In
3	SDA	Serial Data Line	0~5.5V	In/Out
4	GND	Ground Power	0V	Power
5	INTRA	Interrupt Output A	0~12V	Out
6	OSCOUT	Oscillator Circuit Output	0~1.5V	Out
7	OSCIN	Oscillator Circuit Input	0~1.5V	IN
8	VDD	Supply Voltage	1.8~5.5V	Power

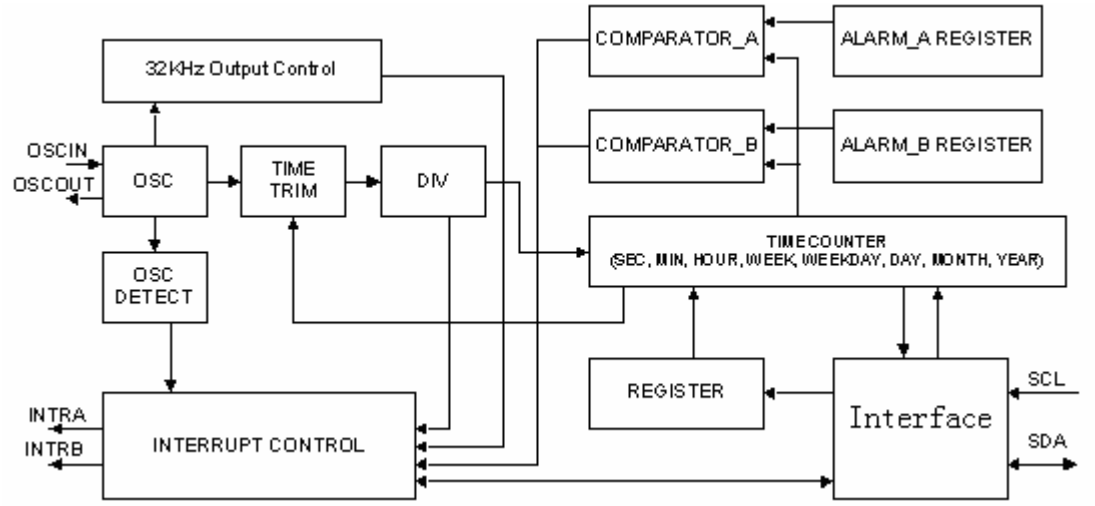
Ordering information

Selection Guide

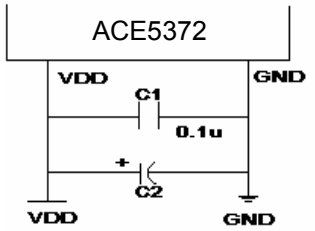
ACE5372 XX + H

- H: Halogen - free
- Pb - free
- XX: FM : SOP-8, TM: TSSOP-8

Block Diagram



VDD and GND

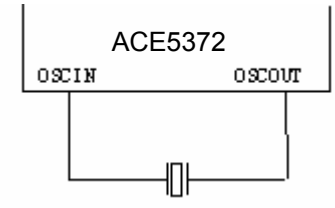


The VDD pin is connected to the positive power supply and GND to the ground. To prevent the possibility of noise, when rapidly changing signal took place on ACE5372 pin, we have to place a capacitance beside the ACE5372. One possibility is to place a bypass capacitance as close as to the ACE5372. The capacitance capacity of C2 could be determined per user's demand, which provides large current passing ability between the pin and the ground.

Bypass Capacitance

OSCIN and OSCOUT

These pins configure an oscillator circuit by connecting a crystal oscillator between the OSCIN-OSCOUT pins. The diagram beside shows the connection method of such crystal oscillator circuit. It's recommended to choose the right crystal oscillator parameter referring to the supplier's suggestion, since it does determine the start-up reliability and oscillation stability provided by external devices. The influence of the distributing capacitance should be considered when choosing capacitance capacity in an oscillator circuit. To minimize output distortion, both crystal oscillator and capacitance should be installed as close to ACE5372 pin as possible.



Crystal Oscillator Connection with External Capacitance

SCL and SDA

SCL and SDA are Serial Clock Line and Serial Data Line, relatively. SCL is used to input shift clock pulses to synchronize data input/output to and from the SDA pin with this clock. SDA inputs and outputs written or read data in synchronization with shift clock pulses from the SCL pin. Depend on different level of current, separate pull-up resistance can be added to SCL and SDA on exterior circuit board.

INTRA and INTRB

INTRA and INTRB are two interrupt output ports and are both open drain outputs. When using ACE5372 a pull-up resistance must be connected with pins of INTRA and INTRB. INTRA could output periodic interrupt pulses and alarm interrupt (ALARM-A, ALARM-B); INTRB could output 32.768KHz clock pulses (when 32.768KHz crystal is used), periodic interrupt pulses, alarm interrupt (ALARM-B). When power is activated from 0V, it could output 32.768kHz clock pulses (when 32.768KHz crystal is used).

Functional Descriptions

Allocation of Internal Addresses

Internal Address	Contents	Function
0H	Second Counter	Counting and storing seconds in BCD codes
1H	Minute Counter	Counting and storing minutes in BCD codes
2H	Hour Counter	Counting and storing hours in BCD codes
3H	Day of the Week Counter	Counting and storing days of the week in BCD codes
4H	Day Counter	Counting and storing days in BCD codes
5H	Month Counter	Counting and storing months in BCD codes
6H	Year Counter	Counting and storing years in BCD codes
7H	Time Trimming Register	Storing adjusting parameter and external select control of crystal oscillator
8H	Alarm_A (Minute Register)	Storing minutes in Timer A
9H	Alarm_A (Hour Register)	Storing hours in Timer A
AH	Alarm_A (Day of the Week Register)	Storing days of the week in Timer A
BH	Alarm_B (Minute Register)	Storing minutes in Timer B
CH	Alarm_B (Hour Register)	Storing hours in Timer B
DH	Alarm_B (Day of the Week Register)	Storing days of the week in Timer B
EH	Control Register 1	Storing ring enable, interrupt output port select, and periodic interrupt cycle select information
FH	Control Register 2	Storing time display select, interrupt and alarm signal, oscillator halt sensing information

Calendar Counter

The ACE5372 can exchange from year to second (lower two bits) with CPU. When the lower two bits of the year could be divided by 4, that year is leap year. It could automatically recognize the year between 2000 and 2099 and these data are stored separately in registers from 0H to 6H.

High Precision time Trimming function

The ACE5372 has an internal oscillation circuit capacitance CGND and CVDD so that an oscillation circuit may be configured simply by externally connecting a crystal. The ACE5372 incorporates a time trimming circuit (at internal address 7H) that adjusts gain or loss of the clock from the CPU up to approx.±189ppm(±194ppm when 32.000KHz crystal is used) by approximately 3ppm steps to correct discrepancy in oscillation frequency.

*Clock display is possible at much higher precision than conventional real-time clock while using a crystal with broader fluctuation in precision.

* Even seasonal frequency fluctuation may be corrected by adjusting seasonal clock error.

For those systems that have temperature detection precision of clock, function may be increased by correcting clock error according to temperature fluctuations.

Alarm function and Periodic Interrupt

Alarm Function:

The ACE5372 has an alarm function that outputs an interrupt signal from $\overline{\text{INTRA}}$ or $\overline{\text{INTRB}}$ output pins to the CPU when the day of the week, hour or minute corresponds to the setting. These two systems of alarms (ALARM-A, ALARM-B), each may output interrupt signal separately at a specific time. The alarm may be selectable between on and off for each day of the week, thus allowing outputting alarm everyday or on a specific day of the week. The ALARM-A is output from the $\overline{\text{INTRA}}$ pin while the ALARM-B is output from either the $\overline{\text{INTRA}}$ or the $\overline{\text{INTRB}}$ pins. Polling is possible separately for each alarm function.

Periodic Interrupt:

The ACE5372 can output periodic interrupt pulses in addition to alarm function from the $\overline{\text{INTRA}}$ and $\overline{\text{INTRB}}$ pins. This frequency may be selected from 2Hz, 1Hz, 1/60Hz, 1/3600Hz and monthly by controlling register (at lower 3 bits of internal address EH) output selectively.

Output waveform for periodic interrupt may be selected from regular pulse waveform (2Hz and 1Hz) and waveforms (every second, every minute, every hour and every month) that are appropriate for CPU level

Oscillation Halt Sensing

The oscillation halt sending function uses a register (XSTP bit at internal address FH) to store oscillation halt information. This function may be used to determine if the ACE 5372 supply power has been booted from 0V and if it has been backed up. This function is useful for determining if clock data is valid or invalid.

Clock Output

The ACE5372 may output oscillation frequency from INTRB pin. This clock output is set for output by default, which is set to on or off by setting the register (internal address FH bit CLEN). It can also choose different crystal oscillator (32.768KHz or 32.000KHz) by setting the register (internal address 7H at bit XSL), and output clock pulses with two different frequencies.

Registers

1. Clock Counter (at internal address 0-2H)

*Time digit display (in BCD code)

Second digits: Range from 00 to 59 and carried to minute digits when incremented from 59 to 00.

Minute digits: Range from 00 to 59 and carried to hour digits when incremented from 59 to 00.

Hour digits: See descriptions on the $\overline{12}$/24 bit (Section 7). Carried to day and day-of-the week digits when incremented from 11 p.m. to 12 a.m. or 23 to 00.

Any registered imaginary time should be replaced with correct time as carrying to such registered imaginary time digits from lower-order ones cause the clock counter malfunction.

Second digit register (at internal address 0H)

D7	D6	D5	D4	D3	D2	D1	D0	Operation
-	S40	S20	S10	S8	S4	S2	S1	Write
0	S40	S20	S10	S8	S4	S2	S1	Read
0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Default

Minute digit register (at internal address 1H)

D7	D6	D5	D4	D3	D2	D1	D0	Operation
-	M40	M20	M10	M8	M4	M2	M1	Write
0	M40	M20	M10	M8	M4	M2	M1	Read
0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Default

Hour digit register (at internal address 2H)

D7	D6	D5	D4	D3	D2	D1	D0	Operation
-	-	H20 or P/ $\bar{A}$	H10	H8	H4	H2	H1	Write
0	0	H20 or P/ $\bar{A}$	H10	H8	H4	H2	H1	Read
0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Default

* Default means read value when XSTP bit is set to “I” by starting up from 0V, or supply voltage drop etc.

2. Day-of-the-week Counter (at internal address 3H)

*Day-of-the-week digits are incremented by 1 when carried to 1-day digits.

*Day-of-the-week digits display (incremented in septimal notation):

(W4,W2,W1) = (0,0,0)→(0,0,1)→……→(1,1,0)→(0,0,0)

*The relation between days of the week and day-of-the-week digits is defined as:

Sunday=(0,0,0); Monday=(0,0,1); …… ; Saturday=(1,1,0)

(W4, W2, W1) should not be set to (1,1,1).

D7	D6	D5	D4	D3	D2	D1	D0	Operation
-	-	-	-	-	W4	W2	W1	Write
0	0	0	0	0	W4	W2	W1	Read
0	0	0	0	0	Undefined	Undefined	Undefined	Default

*The default means read value when XSTP bit is set to “1” by starting up from 0V, or supply voltage drop, etc.

3. Calendar Counter (at internal address4-6H)

* The automatic calendar function provides the following calendar digit displays in BCD code and could recognize the leap year.

Day digits: Range from 1 to 31 (for January, March, May, July, August, October, and December).

Range from 1 to 30 (for April, June, September, and November)

Range from 1 to 29 (for February in leap years)

Range from 1 to 28 (for February in ordinary years)

Month DIGITS:

Range from 1 to 12 and carried to year digits when cycled to 1. Carried to year digits when cycled from 12 to 1.

Year digits:

Range from 00 to 99 and 00,04,08, …….,92, and 96 are counted as leap years.

Any registered imaginary time should be replaced with correct time as carrying to such registered imaginary time digits from lower-order ones cause the clock counter malfunction.

Day digit register (at internal address 4H)

D7	D6	D5	D4	D3	D2	D1	D0	Operation
-	-	D20	D10	D8	D4	D2	D1	Write
0	0	D20	D10	D8	D4	D2	D1	Read
0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Default

*Default means read value when XSTP bit is set to “1” by starting up from 0V, or supply voltage drop, etc.

Mouth digit register (at internal address 5H)

D7	D6	D5	D4	D3	D2	D1	D0	Operation
-	-	-	MO10	MO8	MO4	MO2	MO1	Write
0	0	0	MO10	MO8	MO4	MO4	MO1	Read
0	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Default

*Default means read value when XSTP bit is set to “1” by starting up from 0V, or supply voltage drop, etc.

Year digit register (at internal address 6H)

D7	D6	D5	D4	D3	D2	D1	D0	Operation
Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1	Write
Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1	Read
Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Default

*Default means read value when XSTP bit is set to “1” by starting up from 0V, or supply voltage drop, etc.

4. Time Trimming Register (at internal address 7H)

D7	D6	D5	D4	D3	D2	D1	D0	Operation
XSL_	F6	F5	F4	F3	F2	F1	F0	Write
XSL_	F6	F5	F4	F3	F2	F1	F0	Read
0	0	0	0	0	0	0	0	Default

*Default means read value when XSTP bit is set to “1” by starting up from 0V, or supply voltage drop, etc.

XSL bit

The $\overline{\text{XSL}}$ bit is used to select a crystal oscillator.Set the $\overline{\text{XSL}}$ to“0”(default) to use 32.768KHz；Set $\overline{\text{XSL}}$ to“1”to use 32KHz.

F6 to F0

The time trimming circuit adjust one second count based on this readings when second digit is 00,20, or 40 seconds. Normally, counting up to seconds is made once per 32,768 of clock pulse (or 32,000 when 32.000KHz crystal is used) generated by the oscillator. Setting data to this register activates the time trimming circuit. Register counts will be incremented as ((F5,F4,F3,F2,F1,F0)-1) x2 when F6 is set to “0”. Register counts will be incremented as ((F5, F4, F3, F2, F1, F0)-1) x2 when F6 is set to “0”.

Register counts will be decremented as (($\overline{\text{F5}}$, $\overline{\text{F4}}$, $\overline{\text{F3}}$, $\overline{\text{F2}}$, $\overline{\text{F1}}$, $\overline{\text{F0}}$)+1) x2 when F6 is set to “1”.

Counts will not change when (F6, F5, F4, F3, F2, F1, F0) are set to (*, 0, 0, 0, 0, 0, *).

For example, when 32.768KHz crystal is used. When (F6, F5, F4, F3, F2, F1, F0) are set to (0,1, 0, 1, 0, 0,1), counts will change as: 32768+(29-1)*2=32824 (clock will be delayed) when second digit is 00, 20, or 40.When (F6, F5, F4, F3, F2, F1, F0) are set to (0, 0, 0, 0, 0, 0, 1), counts will remain 32,768 without changing when second digit is 00, 20, or 40. When (F6, F5, F4, F3, F2, F1, F0) are set to (1,1,0,1,0,0,1), counts will change as: 32768+（-17+1）*2=32736 (clock will be advanced) when second digit is 00, 20, or 40.

Adding 2 clock pulses every 20 seconds: 2/（32768*20）=3.051ppm (or 3.125ppm when 32.000KHZcrystal is used), delays the clock by approx. 3ppm. Likewise, decrementing 2 clock pulses advances the clock by 3ppm. Thus the clock may be adjusted to the precision of±1.5ppm. Note that the time trimming function only adjusts clock timing and oscillation frequency but 32.768KHz clock output is not adjusted.

5. Alarm Register (Alarm-A : internal address 8-AH; Alarm-B : internal address B-DH)

Alarm-A minute register (at internal address 8H)

D7	D6	D5	D4	D3	D2	D1	D0	Operation
-	AM40	AM20	AM10	AM8	AM4	AM2	AM1	Write
0	AM40	AM20	AM10	AM8	AM4	AM2	AM1	Read
0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Default

Alarm-B minute register (at internal address BH)

D7	D6	D5	D4	D3	D2	D1	D0	Operation
-	BM40	BM20	BM10	BM8	BM4	BM2	BM1	Write
0	BM40	BM10	BM10	BM8	BM4	BM2	BM1	Read
0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Default

Alarm-A hour register (at internal address 9H)

D7	D6	D5	D4	D3	D2	D1	D0	Operation
-	-	AH20,AP/ $\bar{A}$	AH10	AH8	AH4	AH2	AH1	Write
0	-	AH20,AP/ $\bar{A}$	AH10	AH8	AH4	AH2	AH1	Read
0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Default

Alarm-B hour register (at internal address CH)

D7	D6	D5	D4	D3	D2	D1	D0	Operation
-	-	BH20,BP/ $\bar{A}$	BH10	BH8	BH4	BH2	BH1	Write
0	0	BH20,BP/ $\bar{A}$	BH10	BH8	BH4	BH2	BH1	Read
0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Default

Alarm-A day-of-week register (at internal address AH)

D7	D6	D5	D4	D3	D2	D1	D0	Operation
-	AW6	AW5	AW4	AW3	AW2	AW1	AW0	Write
0	AW6	AW5	AW4	AW3	AW2	AW1	AW0	Read
0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Default

Alarm-B day-of-the-week register (at internal address DH)

D7	D6	D5	D4	D3	D2	D1	D0	Operation
-	BW6	BW5	BW4	BW3	BW2	BW1	BW0	Write
0	BW6	BW5	BW4	BW3	BW2	BW1	BW0	Read
0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Default

*Default means read value when XSTP bit is set to “1” by starting up from 0V, or supply voltage drop, etc.

* ALARM-A, ALARM-B hour register D5 is set to “0” for AM and “1” for PM in the 12-hour display system.
The register D5 indicates 10 digit of hour digit in 24-hour display system.

* To activate alarm operation, any imaginary alarm time setting should not be left to avoid un-matching.

* In hour digit display midnight is et to “12”, noon is set to “32” in 12-hour display system.

* AW0 to AW6 (BW0 to BW6) correspond to the day-of-the-week counter being set at (0,0,0) to (1,1,0).
No alarm pulses are output when all of AW0 to AW6 (BW0 to BW6) are set to “0”

Example of Alarm Time Settings

Alarm Time Settings	Day-of-the-week							12-hour system				24-hour system			
	Sun	Mon	Tue	Wed	Thu	Fri	Sat	10H	1H	10M	1M	10H	1H	10M	1M
00:00AM every day	1	1	1	1	1	1	1	1	2	0	0	0	0	0	0
05:27AM every day	1	1	1	1	1	1	1	0	5	2	7	0	5	2	7
11:59AM every day	1	1	1	1	1	1	1	1	1	5	9	1	1	5	9
00:00PM on Mon thru Fri	0	1	1	1	1	1	0	3	2	0	0	1	2	0	0
05:56PM on Wed	0	0	0	1	0	0	0	2	5	5	6	1	7	5	6
11:59PM on Tue, Thu, and Sat	0	0	1	0	1	0	1	3	1	5	9	2	3	5	9

6. CONTROL Register 1 (at internal address EH)

D7	D6	D5	D4	D3	D2	D1	D0	Operation
AALE	BALE	SL2	SL1	TEST	CT2	CT1	CT0	Write
AALE	BALE	SL2	SL1	TEST	CT2	CT1	CT0	Read
0	0	0	0	0	0	0	0	Default

*The default means read value when XSTP bit is set to “1” by starting up from 0V, or supply voltage drop, etc.

AALE , BALE
ALARM-A, ALARM-B enable bits

AALE，BALE	Description	Operation
0	ALARM-A，ALARM-B correspondence action invalid	Default
1	ALARM-A，ALARM-B correspondence action valid	

L2, SL1
Interrupt output select bits

SL2	SL1	Description	Operation
0	0	Outputs ALARM-A, ALARM-B, INT to the INTRA. Outputs 32K clock pulses to the INTRB.	Default
0	1	Outputs ALARM-A, INT to the INTRA. Outputs 32K clock pulses, ALARM-B to the INTRB.	
1	0	Outputs ALARM-A, ALARM-B to the INTRA. Outputs 32K clock pulses, INT to the INTRB.	
1	1	Outputs ALARM-A to the INTRA. Outputs 32K clock pulses, ALARM-B, INT to the INTRB.	

By setting SL1 and SL2 bits, two alarm pulses (ALARM-A, ALARM-B), periodic interrupt output (INT), 32K clock pulses may be output to the INTRA or INTRB pins selectively.

TEST
ACE5372 Test bit

TEST	Description	Operation
0	Ordinary operation mode	Default
1	Test mode	

CT2, CT1, CT0
Periodic interrupt cycle select bit

CT2	CT1	CT0	Description	
			Wave Form Mode	Cycle and INTRA（INTRB）Falling Timing
0	0	0	-	INTRA（INTRB）at high level
0	0	1	-	INTRA（INTRB）at low level
0	1	0	Pulse Mode	2Hz（Duty 50%）
0	1	1	Pulse Mode	1Hz（Duty 50%）
1	0	0	Level Mode	Every second（synchronized with second count up）
1	0	1	Level Mode	Every minute（00 second of every minute）
1	1	0	Level Mode	Every hour（00 minute 00 second of every hour）
1	1	1	Level Mode	Every month（the 1st day 00 A.M. 00 minute 00 second of every month）

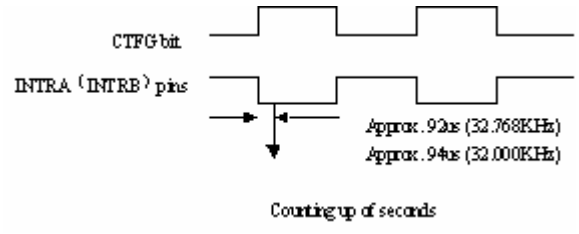
1) Pulse mode: Outputs 2Hz, 1Hz clock pulses. For relationships with counting up of seconds see the diagram below.

In the 2Hz clock pulse mode, 0.496s clock pulses and 0.504s clock pulses are output alternatively. Duty cycle for 1Hz clock pulses becomes 50.4%.

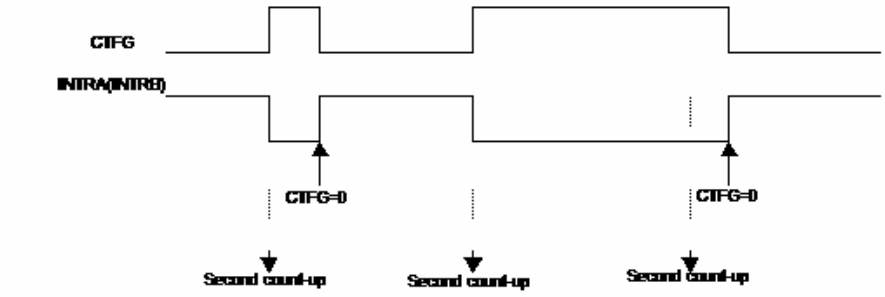
2) Level mode: One second, one minute or one month may be selected for an interrupt cycle. Counting up of seconds is matched with falling edge of interrupt output.

3) When the time trimming circuit is used, periodic interrupt cycle changes every 20 seconds.
Pulse mode:"L" duration of output pulses may change in the maximum range of ±3.784ms (±3.875ms when 32KHz crystal is used).
For example, Duty will be 50±0.3784% (or 50±0.3875% when 32KHz crystal is used) at 1Hz.
Level Mode: Frequency is one second may change in the maximum range of ±3.784ms (±3.875ms when 32KHz crystal is used).
Relation Between Mode Waveforms and CRFG Bit

◆ Pulse mode



◆ Level mode



7. Control Register 2 (at internal address FH)

D7	D6	D5	D4	D3	D2	D1	D0	Operation
-	-	12_/24	ADJ	CLEN_	CTFG	AAFG	BAFG	Write
0	0	12_/24	XSTP	CLEN_	CTFG	AAFG	BAFG	Read
0	0	Undefined	1	0	0	0	0	Default

*The default means read value when XSTP bit is set to "1" by starting up from 0V, or supply voltage drop, etc.

$\overline{1}$2/24

$\overline{1}$2/24-hour Time Display System Selection bit

$\overline{1}$2/24	Description
0	12-hour time display system
1	24-hour time display system

Being set this bit at "0" indicates 12-hour display system while "1" indicates 24-hour system.

Time Display Digit Table

24-hour time display system	12-hour time display system	24-hour time display system	12-hour time display system
00	12(AM12)	12	32(PM12)
01	01(AM1)	13	21(PM1)
02	02(AM2)	14	22(PM2)
03	03(AM3)	15	23(PM3)
04	04(AM4)	16	24(PM4)
05	05(AM5)	17	25(PM5)
06	06(AM6)	18	26(PM6)
07	07(AM7)	19	27(PM7)
08	08(AM8)	20	28(PM8)
09	09(AM9)	21	29(PM9)
10	10(AM10)	22	30(PM10)
11	11(AM11)	23	31(PM11)

Either the 12-hour or 24-hour time display system should be selected before writing time data.

ADJ

±30 Second Adjust Bit

ADJ	Description
0	Ordinary operation
1	Second digit adjustment

* The following operations are performed by setting the second ADJ bit to 1

1) For second digits ranging from “00” to “29” seconds：Time counters smaller than seconds are reset and second digits are set to “00”.
2) For second digits ranging from “30” to “59” seconds: Time counters smaller than seconds are reset and second digits are set to “00”. Minute digits are incremented by 1.

* Second digits are adjusted within 122us(within 125us: when 32KHz crystal is used) from writing operation to ADJ.

The ADJ bit is for write only and allows no read operation.

XSTP

Oscillator Halt Sending Bit

XSTP	Description	Operation
0	Ordinary oscillation	
1	Oscillator halt sensing	default

The XSTP bit senses the oscillator halt.

* When oscillation is halted after initial power on from 0V or drop in supply voltage the bit is set to “1” and which remains to be “1” after it is restarted. This bit may be used to judge validity of clock and calendar count data after power on or supply voltage drop.

* When this bit is set to “1”, $\overline{X}$SL，F6 to F0，CT2，CT1，CT0，AALE，BALE，SL2，SL1， $\overline{C}$LEN and TEST bits are reset to “0”. $\overline{I}$NTRA will stop output and the $\overline{I}$NTRB will output 32KHz clock pulses.

The XSTP bit is set to “0” by setting the control register 2 (address FH) during ordinary oscillation.

CLEN

32KHz Clock Output Bit

$\overline{C}$LEN	Description	Operation
0	32KHz clock output enabled	Default
1	32KHz clock output disabled	

By setting this bit to “0”, output of clock pulses of the same frequency as the crystal oscillator is enabled.

CTFG

Periodic Interrupt Flag Bit

CTFG	Description	Operation
0	Periodic interrupt output=OFF	Default
1	Periodic interrupt output=ON	

This bit is set to “1” when periodic interrupt pulses are output ($\overline{I}$NTRA or $\overline{I}$NTRB= “L”).

The CTFG bit may be set only to “0” in the interrupt level mode. Setting this bit to “0” sets either the $\overline{I}$NTRA or the $\overline{I}$NTRB to OFF (“H”). When this bit is set to “1” nothing happens.

AAFG, BAFG

ALARM-A, ALARM-B Flag Bit

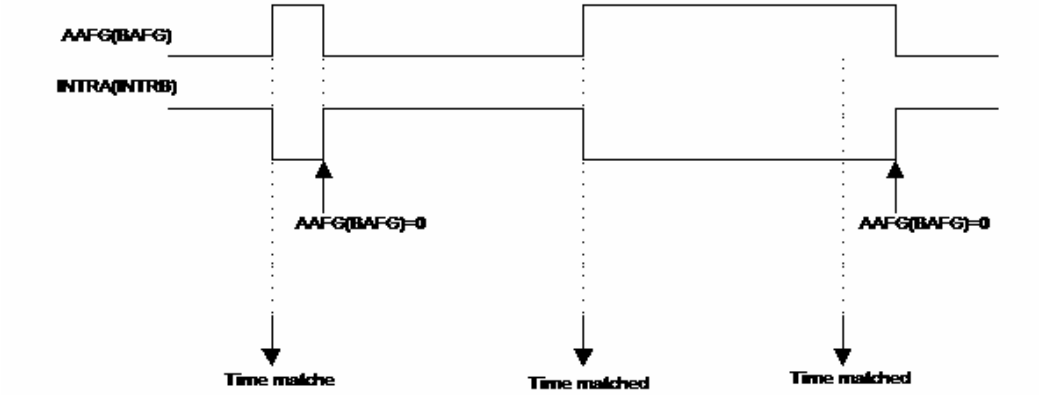
ALARM-A，ALARM-B	Description	Operation
0	Unmatched alarm register with clock counter	Default
1	Matched alarm register with clock counter	

* The alarm interruption is enabled only when the AALE, BALE bits are set to “1”. This bit turns to “1” when matched time is sensed for each alarm.

* The AAFG, BAFG bit may be set only to “0”. Setting this bit to “0” sets either the $\overline{I}$NTRA or the $\overline{I}$NTRB to the OFF “H”. When this bit is set to “1” nothing happens.

When the AALE, BALE bit is set to “0”, alarm operation is disabled and “0” is read from the AAFG, BAFG bit.

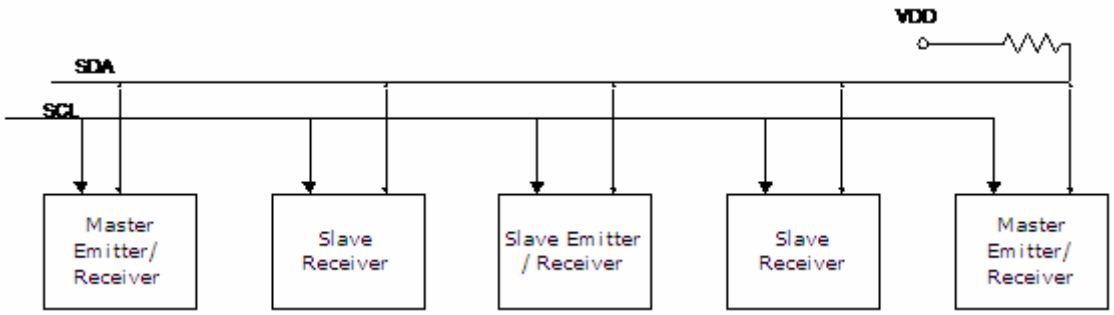
Output Relationships Between AAFG（BAFG）Bit and $\overline{I}$NTRA（ $\overline{I}$NTRB）



Transmission System of Interface

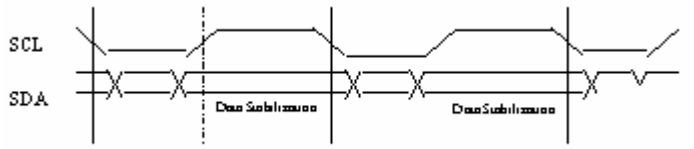
Communication protocol determines: circuits in the equipment which sends data through SDA bus are regarded as emitters, contrarily, circuits in the equipment which receives data through SDA bus are regarded as receivers. Master equipment and master circuit control data transmission; Slave circuit is controlled.

Typical System Bus Structure



Data Validity Protocol

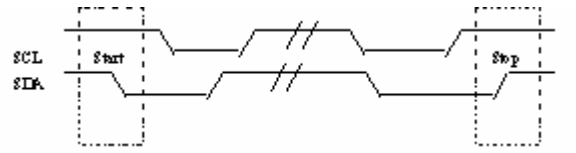
Data transmission protocol determines: Transmit one bit data in every clock cycle. SDA must be kept at a certain state while SCL is at the “H” state as shown below during data transmission.



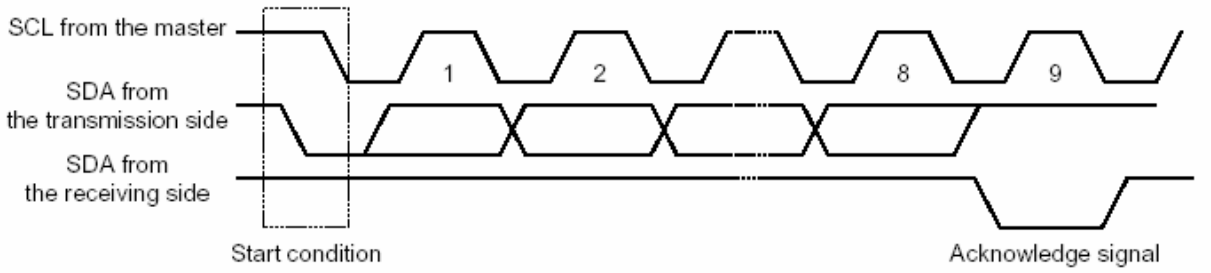
Start and stop conditions

The SCL and SDA pins are at the “H” level when no data transmission is made. Changing the SDA from “H” to “L” when the SCL and the SDA are “H” activates the start condition and access is started. Changing the SDA from “L” to “H” when the SCL is “H” activates stop condition and accessing stopped.

Start and stop conditions



As the arrival of the start condition, master emitter must send out an address command bit, which includes slave address and R/W model; When a certain receiver in bus is chosen, it will send ACK signal and SDA changes into low voltage. ACK signal indicates the success of data transmission. When SCL clock drops, emitter sends continuously 8 bits and releases the data bus (SDA changes into high voltage).



The slave address

The high effective 7 bits (bit7---bit1) in the address byte are defined as device type id. In ACE5372, these 7 bits are 0110010. The lowest bit0 is defined as R/W model. When this bit is "1", it is read model, while "0" is write model.

The slave address

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	1	1	0	0	1	0	R/W

BIT7-BIT1 : The slave address of the ACE5372 is defined as 0110010

BIT0 : R/W definition

"1" is read model

"0" is write model

Data transmission format in the Interface Communication

Interface generates no Chip Enable signals. In place of it each device has a 7bit slave address allocated. The first 1byte is allocated to this 7bit of slave address and to the command (R/ $\overline{W}$) for which data transmission direction is designated b the data transmission thereafter.

The slave address of the ACE5372 is specified at (0110010).

At the end of data transmission/receiving stop condition is generated to complete transmission. However, if start condition is generated without generating stop condition, repeated start condition is met and transmission/receiving data may be continued by setting the slave address again. Use this procedures when the transmission direction needs t be changed during one transmission.

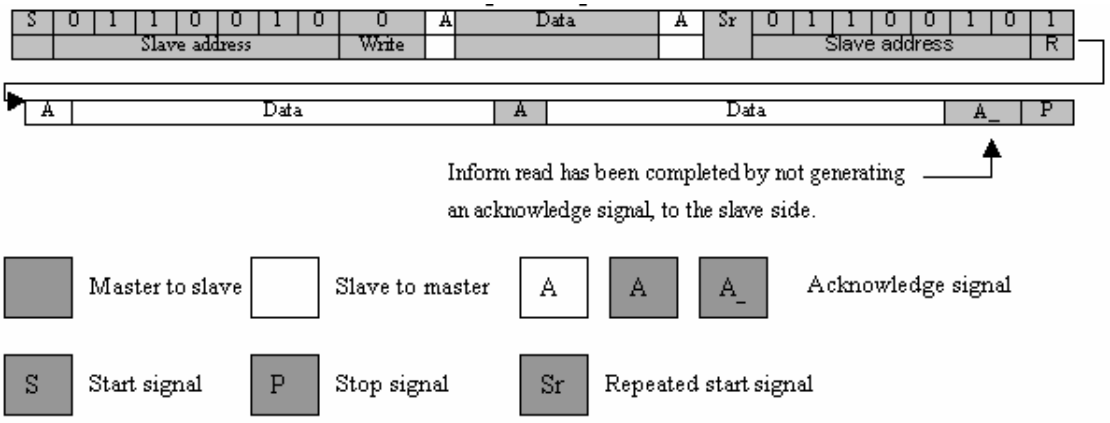
Data is written into the slave from the master

S	0	1	1	0	0	1	0	0	A	Data	A	Data	A	P
	Slave address							Write						

When data is read from the slave immediately after 7bit addressing from the master

S	0	1	1	0	0	1	0	1	A	Data	A	Data	A_	P
	Slave address							Read						

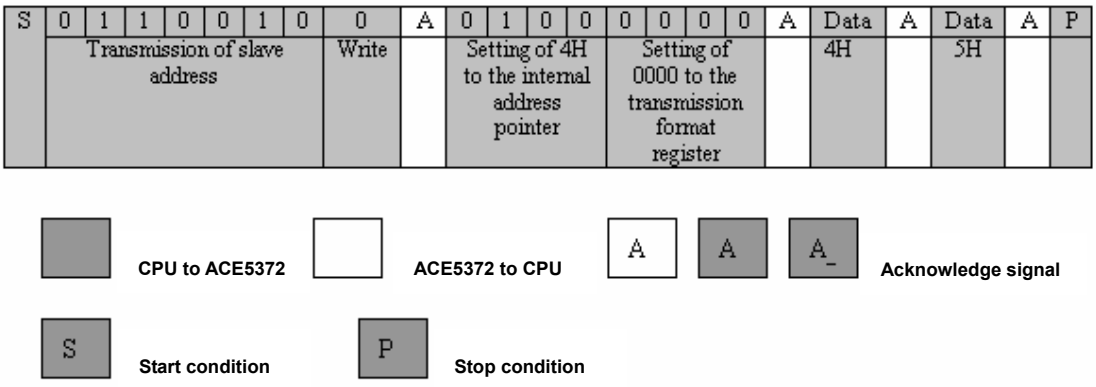
When the transmission direction is to be changed during transmission



Data Transmission Write Format in the ACE5372

A) First send 7 address bit(0110010), the eighth bit is write command “0”.
B) When the ninth bit is ACK signal, ACE5372 is under writing condition.
C)In the following byte, the high 4 bits are determined as internal address in ACE5372(0H-FH), the low 4 bits are transmission model.
D)After another bit’s ACK signal, it starts writing data normally.
E)After writing 1 byte data, there will be 1 bit ACK signal and then writing data in next 1 byte starts. Only when there is a stop signal in the bit after ACK signal, can the writing operation be stopped.

Example of data writing (When writing to internal address 4H to 5H)

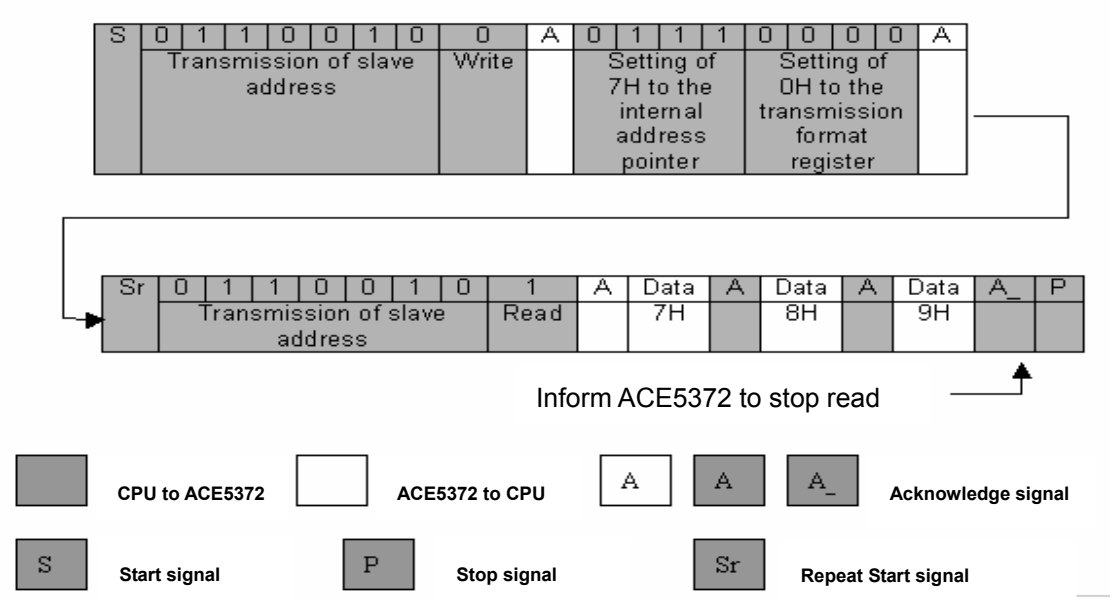


Data Transmission Read Format in the ACE5372

The ACE5372 allows the following three readout methods of data from an internal register.
I) The first method to reading data from the named internal address
A)The first three steps are the same as write model
B)After one bit ACK signal, a new start signal will be produced to change the direction of data transmission in INTERFACE connection.
C)Then send 7 address bit(0110010), the eighth bit command is “1”, ACE5372 is under data reading condition.
D) After another bit’s ACK signal, it starts reading data normally.

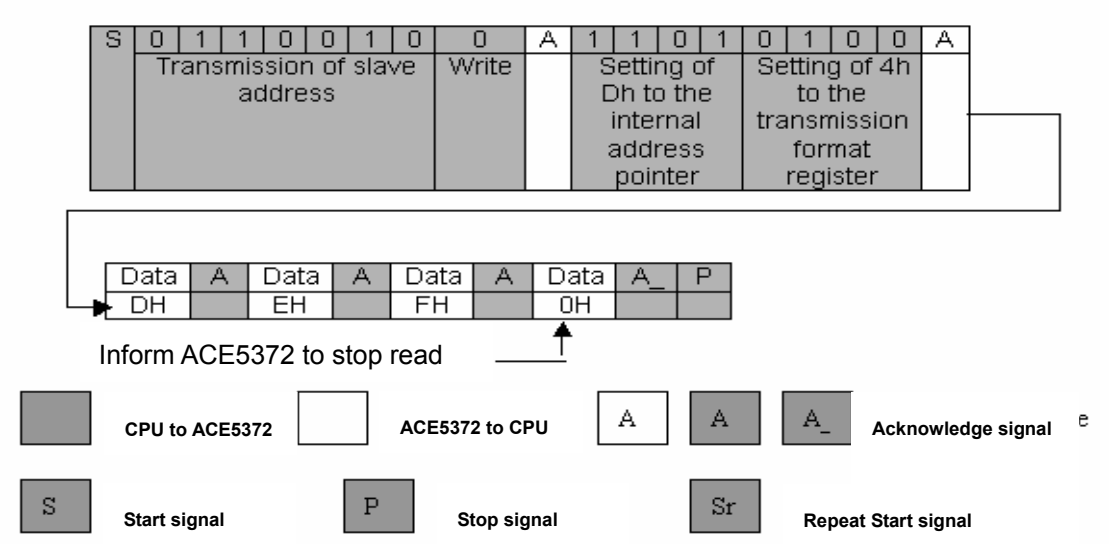
E)When a byte data is read and CPU sends 1 bit ACK signal, a next byte data can be read. Only when the 1 bit ACK signal which is sent by CPU is high voltage, can the reading operation be stopped and then CPU sends stop signals.

Example 1 of data read (when data is read from 7H to 9H)



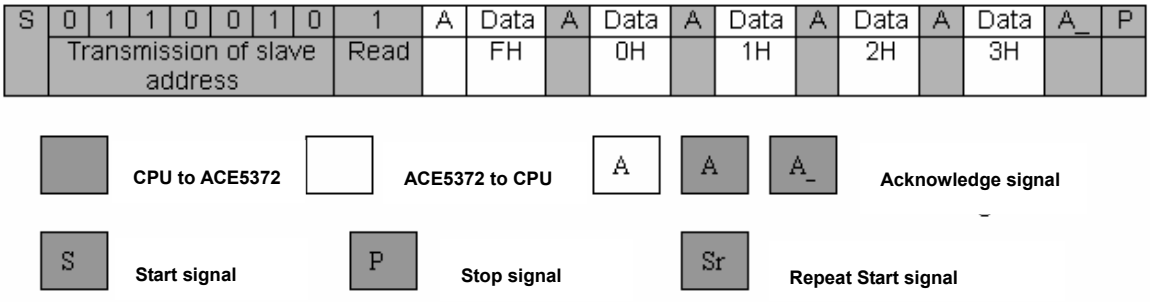
II) The second method to reading data from the internal register is to start immediately after writing to the internal address pointer and the transmission format register. Set 4h to the transmission format register when this method is used.

Example 2 of data read (when data is read from internal address Dh to 0h)



III) The third method to reading data from the internal register is to start reading immediately after writing to the slave address(0110010) and the (R/ $\overline{W}$) bit. Since the internal address pointer is set to Fh by default , this method is only effective when reading is started from the internal address Fh.

Example 3 of data read (when data is read from internal address Fh to 3h).



Data Transmission Under Special Condition

The ACE5372 hold the clock tentatively for duration from start condition to stop condition to avoid invalid read or write clock on carrying clock. To prevent invalid read or write clock shall be made during one transmission operation. When 0.5 to 1.0 seconds elapses after start condition any access to the ACE5372 is automatically released to release tentative hold of the clock and access from the CPU is forced to be terminated (automatic resume function from the interface).

Also a second start condition after the first condition and before the stop condition is regarded as the “repeated start condition”. Therefore, when 0.5 to 1.0 seconds passed after the first start condition, access to the ACE5372 is automatically released.

The user shall always be able to access the real-time clock as long as the following two conditions are met.

1) No stop condition shall be generated until clock read/write is started and completed.
2) One cycle read/write operation shall be completed within 0.5 seconds.

Bad example of reading from seconds to hours (invalid read)

(Start condition) → (Read of seconds) → (Read of minutes) → (Stop condition) → (Start condition) → (Read of hour) → (Stop condition)

Assuming read was started at 09:59:59PM, and while reading seconds and minutes the time advanced to 10:00:00 PM. At this time second digit is hold so the read as 59:59. ACE5372 confirms (Stop condition) and carry second digit being hold and the time changes to 10:00:00 PM. Then, when the hour digit is read, it changes to 10. The wrong results of 10:59:59 will be read.

Configuration of Oscillating Circuit and Time Trimming Circuit

a)In general crystal oscillators are classified by their central frequency of CL (load capacitance) and available further grouped in several ranks as ±10，±20 and ±50ppm of fluctuations in precision.

b)The fluctuation of IC circuit frequency is ±5~10ppm at room temperature.

c)Here, the clock accuracy at room temperature varies along with the variation of the characteristic of crystal oscillator.

Configuration of Oscillating Circuit

Because the adjustment of crystal oscillator frequency is also the adjustment of clock frequency, so the former adjustment can be done through C_{IN} & C_{OUT} on the both sides of crystal.

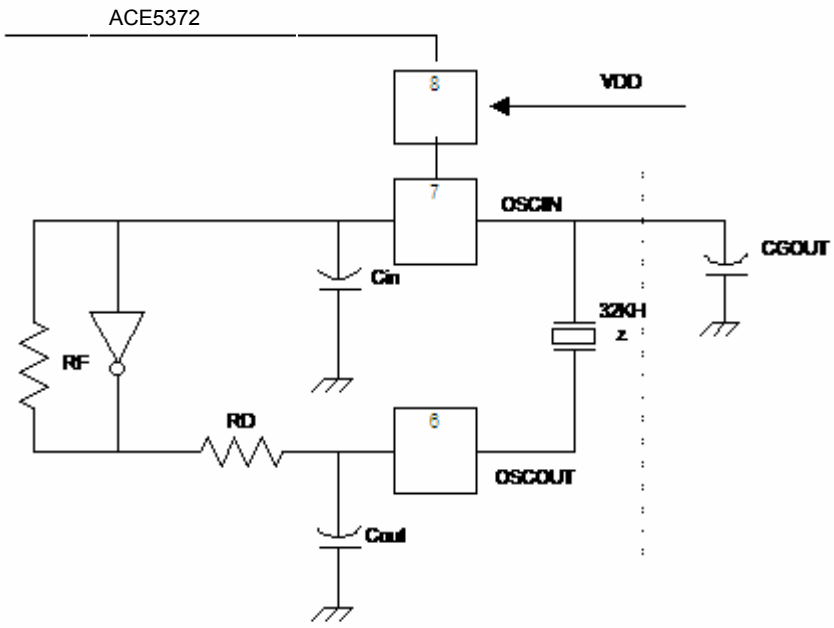
ACE5372 clock cooperates with C_{IN} & C_{OUT}, so oscillator frequency can be referred to crystal C_L. General, relation between C_L and C_{IN} or C_{OUT} is as follows：

$$Cl = \frac{Cin * Cout}{Cin + Cout} + Cs$$

C_S：Board floating capacitance

If crystal oscillator frequency is on the higher side, the CL should be decreased, contrarily, the CL should be increased.

According to this standard, the best CL is chosen to adjust frequency and clock frequency. For example: if the frequency is on the higher side, it can be lowed by attaching a C_{GOUT} capacitor.



*C_{GOUT}＝0~15pF

Time Trimming Circuit

Using the time trimming circuit gain or lose of clock may be adjusted with high precision by changing clock pulses for one second every 20 seconds.

1.When oscillation frequency[*1] > target frequency[*2]（clock gain）

$$\text{Adjustment amount}^{*3} = \frac{(OscilationFrequency - T\arg etFrequency + 0.1)}{OscillationFrequency * 2 / (T\arg etFrequency * 20)}$$

= (Oscillation frequency – Target frequency) x 10 +1

*1) Oscillation frequency: Clock frequency output from the $\overline{\text{INTRB}}$ pin

*2) Target frequency: TYP. 32.768KHz to 32.000KHz

*3) Adjustment amount: A value to be set finally to F6 to F0 bits. This value is expressed in 7 bit binary digits with sign bit (two's compliment).

2.When oscillation frequency = target frequency (no clock gain or loss)
Set the adjustment value to 0 or +1, or –64, or –63 to disable adjustment.
3.When oscillation frequency < target frequency (clock losses)

Adjustment amount = $\frac{(OscilationFrequency - T\arg etFrequency)}{OscillationFrequency * 2 / (T\arg etFrequency * 20)}$

= (Oscillation frequency – Target frequency) x 10

Example of Calculations
1) When oscillation frequency = 32770kHz; target frequency = 32768kHz
Adjustment value = （32770-32768+0.1）/(32770*2/(32768*20))
=(32770-32768)*10+1=21
Set （F6，F5，F4，F3，F2，F1，F0）=（0，0，1，0，1，0，1）
2) When oscillation frequency =32762kHz; target frequency = 32768kHz
Adjustment value =（32762-32768）/(32762*2/(32768*20))
= (32762-32768)*10=-60
To express –60 in 7bi binary digits with sign bit (two's compliment)
Subtract 60(3Ch) from 128(80h) in the above case, 80h-3Ch=44h
Thus set （F6，F5，F4，F3，F2，F1，F0）=（1，0，0，0，1，0，0）
After adjustment, adjustment error against the target frequency will the approx. ±1.5ppm at a room temperature.

Notice:

1) Clock frequency output from the $\overline{\text{INTRB}}$ pin will change after adjustment by the clock adjustment circuit.

2) Adjustment range:

A)When oscillation frequency is higher than target frequency, the range of adjustment values is （F6，F5，F4，F3，F2，F1，F0）=（0，0，0，0，0，0，1）to (0，1，1，1，1，1，1) and actual adjustable amount shall be -3.05ppm to –189.2ppm (-3.125ppm to 193.7ppm for 32000Hz crystal).

B) When oscillation frequency is lower than target frequency, the range of adjustment values is （F6，F5，F4，F3，F2，F1，F0）=（1，1，1，1，1，1，1）to（1，0，0，0，0，1，0）and actual adjustable amount shall be 3.05ppm to 189.2ppm (3.125ppm to 193.7ppm for 32000Hz crystal)

Output Waveforms

The following three output waveforms can be output from the $\overline{\text{INTRA}}$ ($\overline{\text{INTRB}}$) pin.

1）Alarm interrupt

When a registered time for alarm (such as day-of-the-week, hour or minute) coincide with calendar counter (such as day-of-the-week, hour or minute) interrupt to the CPU are requested with the output pin being on "L". Alarm interrupt consists of Alarm_A and Alarm_B, both have equivalent functions.

2）Periodic interrupt

Outputs an output waveform selected by setting the periodic interrupt frequency select bit. Waveforms include pulse mode and level mode.

3）32KHz clock output

Clock pulses generated in the oscillation circuit are output as they are.

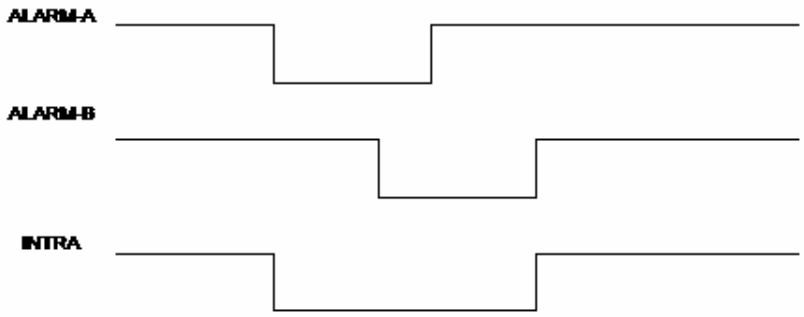
Control of the $\overline{INTRA}$ ($\overline{INTRB}$) Output (flag bit, enable bit, interrupt output select bit)

Of the three output wave forms listed above, interrupt output conditions may be set by setting the flag bit that monitors output state on the register, the enable bit that enables an output wave form and the output select bit that selects either $\overline{INTRA}$ or $\overline{INTRB}$ to be output.

	Flag bit	Enable bit	Interrupt output select bit （SL2，SL1） (D5，D4 at EH)			
			（0，0）	（0，1）	（1，0）	（1，1）
Alarm_A	AAFG (D1 at FH)	AALE (D7 at EH)	$\overline{INTRA}$	$\overline{INTRA}$	$\overline{INTRA}$	$\overline{INTRA}$
Alarm_B	BAFG (D0 at FH)	BALE (D6 at EH)	$\overline{INTRA}$	$\overline{INTRB}$	$\overline{INTRA}$	$\overline{INTRB}$
Periodic interrupt	CTFG (D2 at FH)	Disabled at CT2=CT1=CT0=0 (D2 to D0 at EH)	$\overline{INTRA}$	$\overline{INTRA}$	$\overline{INTRB}$	$\overline{INTRB}$
32KHz clock output	NO	$\overline{CLEN}$ (D3 at FH)	$\overline{INTRB}$	$\overline{INTRB}$	$\overline{INTRB}$	$\overline{INTRB}$

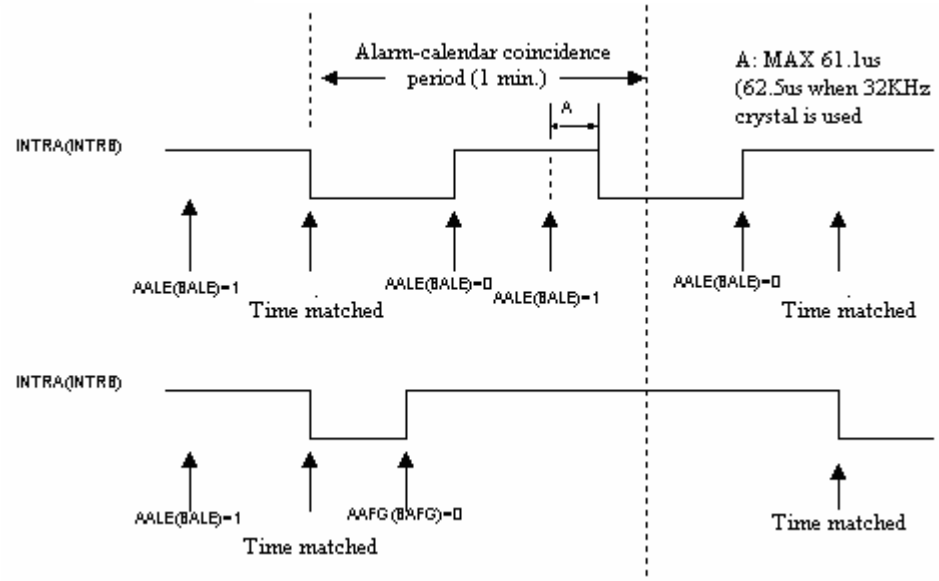
* When power ON (XSTP=1) since AALE=BALE=CT2=CT1=CT0= $\overline{CLEN}$=SL2=SL1=0, $\overline{INTRA}$=OFF ("H") and 32KHz clock pulses are output from the $\overline{INTRB}$ pin.

When more than one output waveforms are output from a single output pin, the output will have OR wave form of negative logic of both.



Alarm Interrupt

For setting an alarm time, designated time such as day-of-the-week, hour or minute should be set to the alarm registers being AALE（BALE）bit to 0. After that set the AALE（BALE） bit to 1, from this moment onward when such registered alarm time coincide the value of calendar counter the $\overline{INTRA}$ ($\overline{INTRB}$) comes down to "L" (ON). The $\overline{INTRA}$ ($\overline{INTRB}$) output can be controlled by operating to the AALE (BALE) and AAFG (BAFG) bits.



Periodic (Clock) Interrupt

The $\overline{\text{INTRA}}$ ($\overline{\text{INTRB}}$) pin output, the periodic interrupt cycle select bits (CT2, CT1, CT0) and the interrupt output select bits (SL2, SL1) can be used to interrupt the CPU in a certain cycle. The periodic interrupt cycle select bits can be used to select either one of two interrupt output modes: the pulse mode and the level mode.

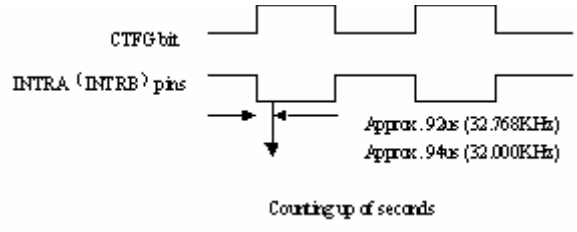
CT2	CT1	CT0	Description	
			Wave Form Mode	Cycle and INTRA(INTRB) Falling Timing
0	0	0	-	INTRA（INTRB）OFF (Default)
0	0	1	-	INTRA（INTRB）fixed at “L”
0	1	0	Pulse Mode	2Hz (Duty 50%)
0	1	1	Pulse Mode	1Hz (Duty 50%)
1	0	0	Level Mode	Every second (coincident with second count-up)
1	0	1	Level Mode	Every minute (00 second of every minute)
1	1	0	Level Mode	Every hour (00minute 00second of every hour)
1	1	1	Level Mode	Every month (1st day, 00:00:00 a.m.of every month)

1) Pulse mode: Output 2Hz, 1Hz clock pulses. For relationships with counting up of seconds see the diagram below.
   In the 2Hz clock pulse mode, 0.496s clock pulses and 0.504s clock pulse are output alternatively.
   Duty cycle for 1Hz clock pulses becomes 50.4%.
2) Level mode: One second, one minute one month may be selected for an interrupt cycle.
   Counting up of seconds is matched with falling edge of interrupt output.
3) When the time trimming circuit is used, periodic interrupt cycle changes every 20 seconds.
   Pulse mode: “L” duration of output pulses may change in the maximum range of ±3.784ms
   (±3.875ms when 32KHz crystal is used)
   For example, Duty will be 50±0.3784% (or 50±0.3875% when 32KHz crystal is used)at 1Hz.

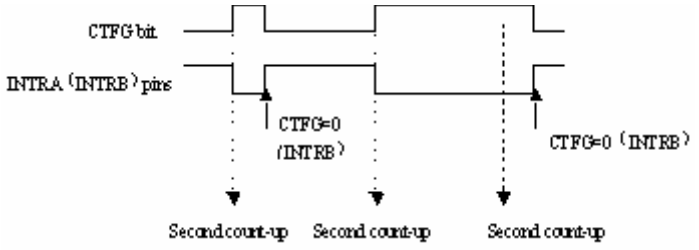
Level mode: Frequency in one second may change in the maximum range of ±3.784ms (±3.875ms when 32KHz crystal is used).

Relation Between Mode Waveforms and CRFG Bit

◆ **Pulse mode**



◆ **Level mode**



32Khz Clock Output

The crystal oscillator can generate clock pulses of 32KHz from the $\overline{\text{I}}$NTRB pin. The pin is changed to "H" by setting the $\overline{\text{C}}$LEN bit to "1".

* 32KHz clock pulse output will not be affected from settings in the clock adjustment register.

When power ON (XSTP=1), 32KHz clock pulses are output from the $\overline{\text{I}}$NTRB pin.

Oscillator Halt Sensing

Oscillation halt can be sensed through monitoring the XSTP bit with preceding setting of the XSTP bit to "0" by writing data to the control register 2.Upon oscillator halt sending, the XSTP bit is switched from 0 to 1. This function can be applied to judge clock data validity. When the XSTP bit is "1", $\overline{\text{X}}$SL, F6 to F0, CT2, CT1, CT0, AALE, BALE, SL2, SL1, $\overline{\text{C}}$LEN and TEST bits are reset to "0".

*1）The XSTP bit is set to "1" upon power-on from 0V. Note that any instantaneous power disconnection may cause operation failure.

*2）Once oscillation halt has been sensed, the XSTP bit is held at "1" even if oscillation is restarted.

Ensure error-free oscillation half sensing by preventing the following events:

1) Instantaneous disconnection of VDD
2) Condensation on the crystal oscillator
3) Generation of noise on the PCB in the crystal oscillator
4) Application of voltage exceeding prescribed maximum ratings to the individual pins of the IC

DC Characteristics

T_{OPT}=-40℃ to +85℃, GND=0V, VDD=3.6V, f_{OSC}=32,768Hz or 32,000Hz

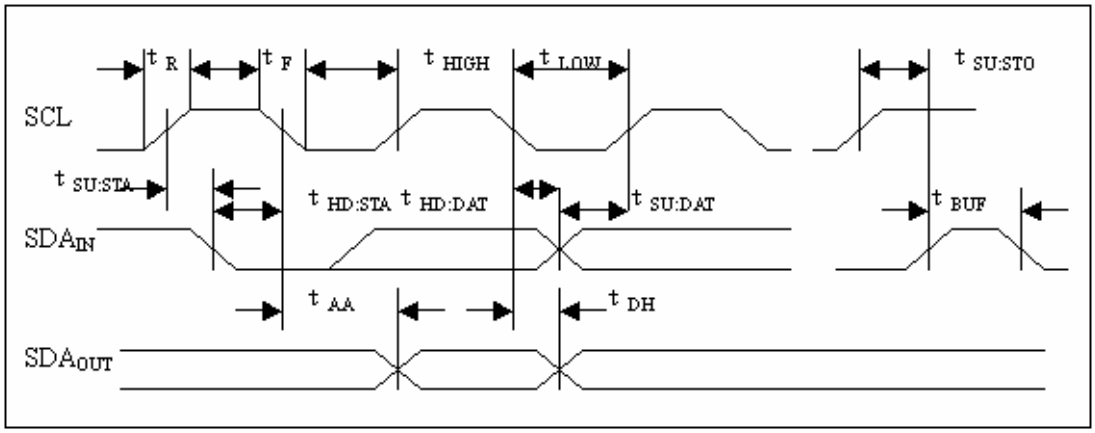
Symbol	Item	Pin name	Conditions	Min.	Typ.	Max.	Unit
VIH	"H" Input Voltage	SCL, SDA		0.8VDD		6.0	V
VIL	"L" Input Voltage	SCL, SDA		-0.3		0.3VDD	V
IOL1	"L" Output Current	INTRA, INTRB	VOL1=0.4V	1			mA
IOL2		SDA	VOL2=0.6V	7			mA
IILK	Input Leakage Current	SCL	VI=6VorGND VDD=6V	-1		1	uA
VDD	Operating Voltage	VDD		1.8		5.5	V
	Counting Voltage	GND		1.2		5.5	V
IOZ	Output Off State Leakage Current	SDA, INTRA, INTRB	VO=6VorGND VDD=6V	-1		1	uA
IDD	Standby Current	VDD	VDD=5V, TOPT=25℃ SCL,SDA=5V		0.4		uA

AC Characteristics

Characteristics Parameter

T_A= -40℃ to +85℃ , V_{DD} =4.5V to 5.5V

Symbol	Item	Conditions	Min.	Max.	Unit
f_{SCL}	SCL Clock Frequency		0	100	KHz
t_{LOW}	SCL Clock "L" Time		4.7		us
t_{HIGH}	SCL Clock "H" Time		5		us
t_{BUF}	Bus release Time	before next data is transmitted	4.7		us
$t_{SU:STA}$	Start Condition Setup Time		4.7		us
$t_{SU:STO}$	Stop Condition Setup Time		4.7		us
$t_{HD:STA}$	Start Condition Hold Time		4		us
$t_{HD:STO}$	Stop Condition Hold Time		4		us
$t_{SU:DAT}$	Data Setup Time		250		ns
$t_{HD:DAT}$	Data input Hold Time		0		ns
T_{HD}	Data output Hold Time	SCL negedge to SDA data changes	0		ns
t_{AA}	clock output	SCL negedge to SDA data availed	0.3	3.5	us
t_R	Rising Time of SCL and SDA (Input)			1	us
t_F	Falling Time of SCL and SDA (Input)			300	ns
t_I	Spike width that can be removed with input filter			100	ns

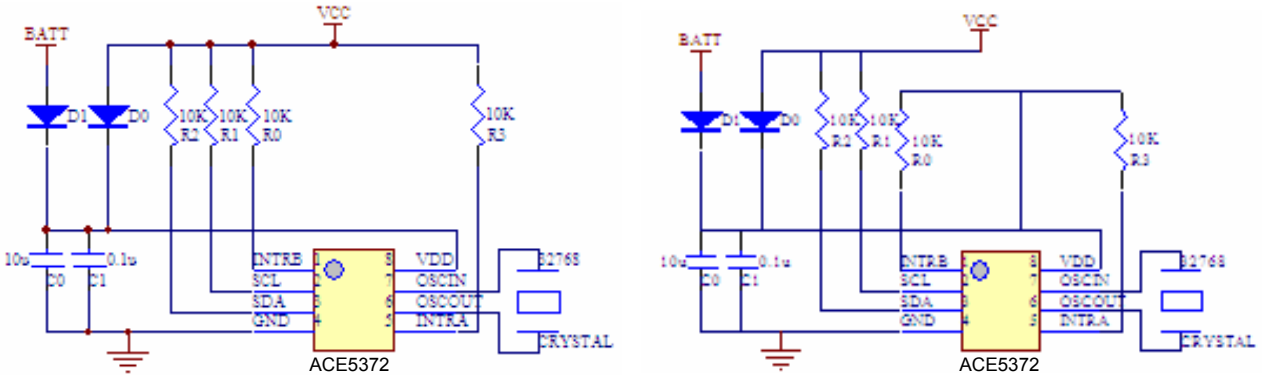


Absolute Maximum Ratings

Symbol	Item	Conditions	Ratings	Unit
VDD	Supply Voltage		-0.3 to +7.0	V
VI	Input Voltage	SCL，SDA	-0.3 to +7.0	V
VO1	Output Voltage 1	SDA	-0.3 to +7.0	V
VO2	Output Voltage 2	INTRA, INTRB	-0.3 to +12.0	V
TOPT	Operating Temperature		-40 to +85	℃
TSTG	Storage Temperature		-55 to +125	℃

Typical Applications

Example of Circuit



1.Mount the high-and low-frequency by-pass capacitors C0 and C1 (TYP. C1=10uF, C2=0.1uF)

2.The typical volume of pull-up resistance R0~R3 is 10KΩ

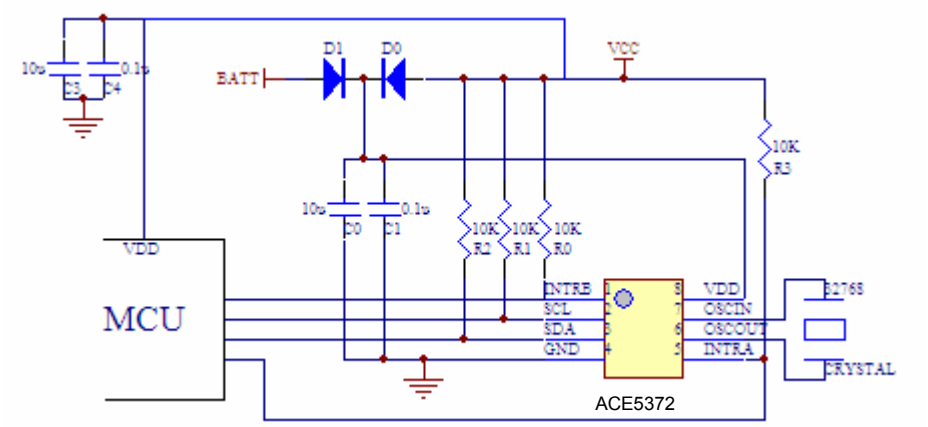
3.BATT and VCC's Voltage: $V_{BATT} \leq V_{VCC}$

4.Connect the pull-up resistor of the INTRA pin or the INTRB pin to two different positions depending battery back-up:

A. when the spare battery supplies power, INTRA (B) is not used.

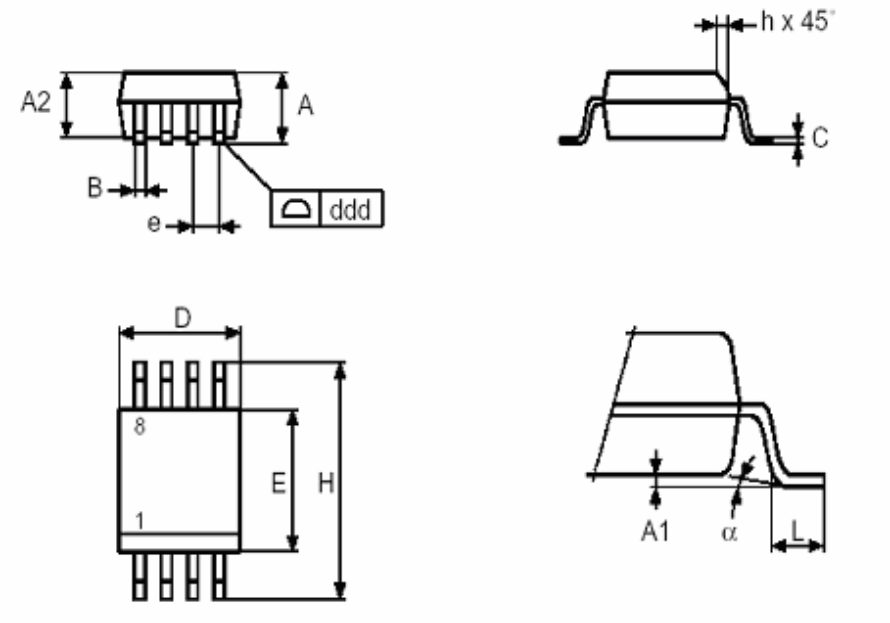
B. when the spare battery supplies power, INTRA (B) is used.

Example of Interface Circuit to the CPU



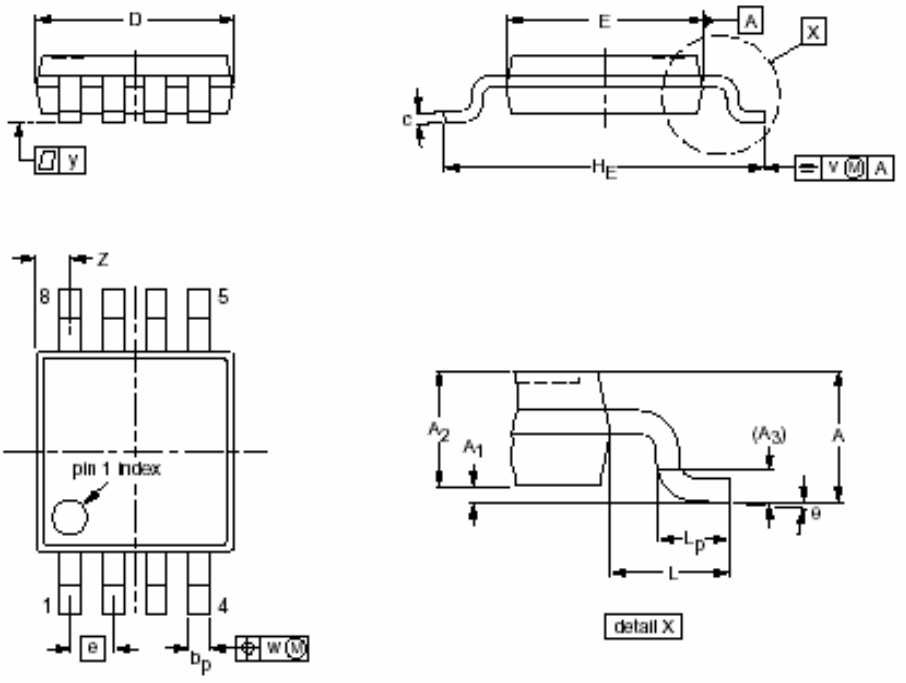
Package Information

SOP-8



Symbol	mm			Inches		
	Min	Typ.	Max	Min	Typ.	Max
A	1.35	-	1.75	0.053	-	0.069
A1	0.10	-	0.25	0.004	-	0.010
B	0.33	-	0.51	0.013	-	0.020
C	0.19	-	0.25	0.007	-	0.010
D	4.80	-	5.00	0.189	-	0.197
ddd	-	-	0.10	-	-	0.004
E	3.80	-	4.00	0.150	-	0.157
e	-	1.27	-	-	0.050	-
H	5.80	-	6.20	0.228	-	0.244
h	0.25	-	0.50	0.010	-	0.020
L	0.40	-	0.90	0.016	-	0.035
α	0°	-	8°	0°	-	8°

Tssop-8



Dimensions (mm are the original dimensions)

Unit	A max.	A1	A2	A3	Bp	C	D(1)	E(2)	e
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.32 0.12	0.25 0.10	3.10 2.90	4.60 4.20	0.65

Unit	H_E	L	Lp	v	w	y	Z(1)	θ
mm	6.70 6.10	0.94	0.80 0.20	0.1	0.1	0.1	0.70 0.35	10^0 0^0

Notes

1.Plastic or metal protrusions of 0.15mm maximum per side are not included

2.Plastic or metal protrusions of 0.25mm maximum per side are not included

Notes

ACE does not assume any responsibility for use as critical components in life support devices or systems without the express written approval of the president and general counsel of ACE Electronics Co., LTD. As sued herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and shoes failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.